V85X3 Datasheet

Specifications are subject to change without notice.

Revision History

Date	Version	Description
2020.08.06	V1.0	Initial Release.

General Description

The V85X3 series is a highly integrated 32bit MCU which is suitable for varies kind of applications. It is integrated with Cortex-M0 MCU, 256KB FLASH, 32KB SRAM, UART/SPI/I2C, LCD, WDT and Timer. The V85X3 series also have varies kind of power mode which can realize ultra-low power IoT products with powerful computing power.

Features

- Working voltage (V8503/V8533/V8513): 2.2V ~ 5.5V.
- Working Current:
  - Normal mode: 1.633 mA @6.5536MHz
  - Idle mode: 0.379 mA @6.5536MHz
  - Sleep mode (LCD active, RTC_PSCA=0, VDD=3.3V, AVCCLDO power down): 9.3μA
  - Sleep mode (LCD inactive, RTC_PSCA=0, VDD=3.3V, AVCCLDO power down): 3.1μA
  - Deep Sleep mode (RTC_PSCA=0, VDD=3.3V, AVCCLDO power down): 2.9μA
  - RTC only mode (RTC_PSCA=0, BATRTC=3.3V): 1.3μA
- Package:
  - LQFP100 (V8503)
  - LQFP80 (V8533)
  - LQFP64 (V8513)
- Operation Temperature: -40~+105℃
- Storage Temperature: -55~+150℃
- MCU
  - 32 bits Cortex-M0 with maximum 26.2144 MHz operation speed.
  - Single cycle multiplier.
  - Standard 2-wires SWD debug interface.
  - 256KB FLASH with write protect, support both IAP and ISP (V8513 only support 128KB FLASH).
  - 32K bytes SRAM with parity check and data retention under sleep mode.
  - 256 bytes SRAM with data retention under deep-sleep mode.
  - Support abort exception detection including FLASH check-sum error, SRAM parity error, memory address error and memory align error.
- Interface Controller
  - Maximum 6 UART controllers with parity check.
  - Each UART TX channel can be coupled with IR carrier for IR transmission.
  - Maximum 2 ISO7816 controllers.
  - Maximum 2 SPI master/slave controllers.
  - Maximum 1 I2C master/slave controller.
  - 4 32 bits timers.
  - 4 16 bits PWM timers.
  - 4 channels DMA controller.
  - 128/192/256 bits AES CODEC.

- ECC encrypt/decrypt accelerated engine.
- Dual frame buffer LCD controller
  - ✓ 4COM/6COM/8COM.
  - ✓ 1/3 or 1/4 bias.
  - ✓ Support multi-kinds of scan frequency.
  - ✓ LCD voltage: The default output is about 3.3V. Adjustment range: 2.7~3.6V, 0.06V per step.
- Watch dog timers with programmable period.
- Support multiple wake-up sources under each mode.
- Maximum 82 GPIOs.
- Maximum 16 GPIOs can be external interrupt and wakeup sources under all modes.

- ● Analog Controller
  - 16bits ADC with 10Ksps.
  - Maximum 8 external input.
  - ADC supports manual sample mode or auto sample mode.
  - Maximum 2 comparators with single end input or differential input.
  - Embedded 32 KHz and 6.5 MHz RCO.
  - Embedded 2 PLLs.
  - Support external 32.768 KHz crystal or 6.5536MHz crystal (optional).
  - Support crystal absent detect for both 32.768 KHz and 6.5536 MHz crystal.
  - Each clock can be selected to be system clock.
  - Support digital clock divider up-to 1/256.
  - Support low voltage detection with programmable level.
  - Support power-on reset for both AVCC and DVCC.
  - Support two DC input with auto-switch function and voltage detection for each input.
  - Support standalone RTC battery input.
  - Support 1ppm RTC auto-calibration under all modes.

V85X3 series product

	V8503	V8533	V8513
ADC channel	8	7	4
Tiny ADC channel	2	2	0
UART	6	6	5
UART32K	2	2	2
ISO7816	2	2	2
SPI	2	2	2
I2C	1	1	1
Comparator	2	2	2
GPIO	82	69	53
External interrupt IO	16	15	15
32-bit Timer	4	4	4
16-bit PWM Timer	4	4	4
PWM out	4	4	4
DMA channel	4	4	4
LCD	76x4, 74x6, 72x8	63x4, 61x6, 59x8	49x4, 47x6, 45x8
FLASH	256KB	256KB	128KB
SRAM	32KB	32KB	32KB
Package type	100-LQFP	80-LQFP	64-LQFP

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Figure List

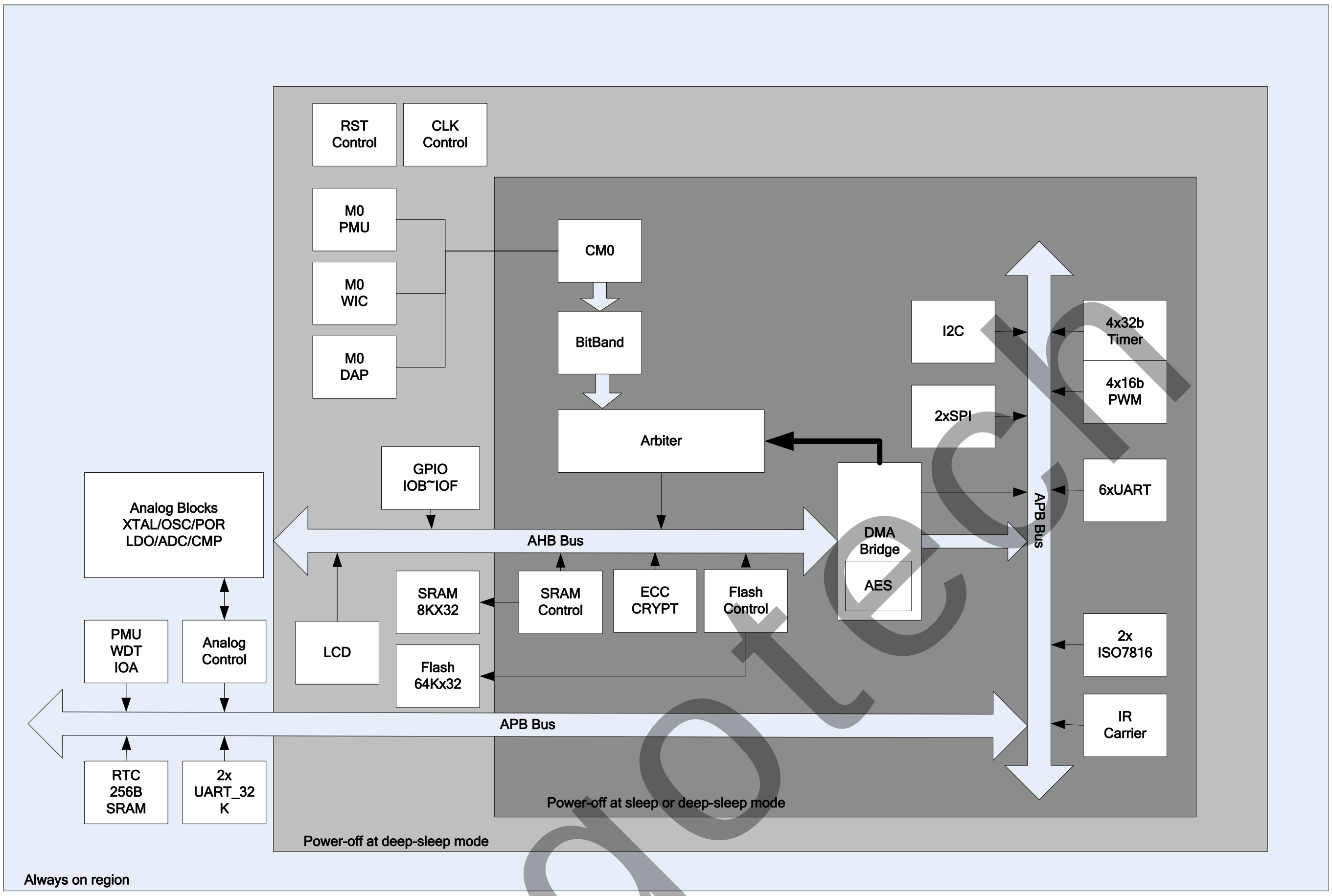

RST Control
CLK Control
M0 PMU
M0 WIC
M0 DAP
CM0
BitBand
Arbiter
I2C
2xSPI
4x32b Timer
4x16b PWM
6xUART
GPIO IOB~IOF
Analog Blocks XTAL/OSC/POR LDO/ADC/CMP
AHB Bus
DMA Bridge
AES
APB Bus
SRAM 8KX32
SRAM Control
ECC CRYPT
Flash Control
Flash 64Kx32
LCD
PMU WDT IOA
Analog Control
2x ISO7816
IR Carrier
APB Bus
RTC 256B SRAM
2x UART_32K
Power-off at sleep or deep-sleep mode
Power-off at deep-sleep mode
Always on region

Table List

1.Electrical Characteristics

1.1. Absolute Maximum Ratings

Stresses above those listed as "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 1-1 Absolute Maximum Ratings

Symbol	Ratings	Min	Max	Unit
V_{VDD}-V_{SS}	External supply voltage	-0.3	+5.8	V
V_{IN}-V_{SS}	External signal input to GPIO pins.	-0.3	+5.8	V
S_{VDD}	IO power-on slope	5V/sec	1V/usec	--
I_{INJ_PAD}	Single pin input injection current	-10	+10	mA
I_{INJ_SUM}	Sum of all input injected current	-50	+40	mA
T_W	Working temperature range	-40	+105	℃
T_S	Storage temperature	-55	+150	℃
T_J	PN junction temperature	-40	+125	℃

1.2. Normal Operating Voltage

Table 1-2 Operating Voltage

Symbol	Parameter	Conditions(-40~+105℃)	Min	Typ	Max	Unit
$V_{IN,VDD}$	Input voltage range of VDD	V8503/V8533/V8513	2.2	3.3/5	5.5	V
$V_{IN,BATRTC}$	Input voltage range of BATRTC		2.2	3.3/5	5.5	V

1.3. Driving Capability Characteristics

Table 1-3 Driving Condition of Power PINs

Symbol	Parameter	Conditions(-40~+105℃)	Min	Typ	Max	Unit
$I_{DRV,VDD}$	Driving Capability of VDD				40*[1]	mA
$I_{DRV,AVCC}$	Driving Capability of AVCC				30	mA
$I_{DRV,DVCC}$	Driving Capability of DVCC				35	mA
$I_{DRV,AVCCOUT}$	Driving Capability of AVCC_OUT				20*[2]	mA

*[1]: Driving current of VDD include peripheral loads and loads at AVCC, DVCC and AVCC_OUT.

*[2]: The sum of the driving capability of AVCC pin and AVCC_OUT pin cannot exceed 30mA.

1.4. Switching resistance of Power PIN

Table 1-4 Switching Resistance of Power PIN

Symbol	Parameter	Conditions(-40~+105℃)		Min	Typ	Max	Unit
$R_{on,\ BATRTC2RTC}$	Switch-on Resistance between BATRTC and RTC module	RTC module powered by BATRTC IL=10 μA	3.3V	325	500	675	ohm
			5V	250	400	475	ohm
$R_{on,\ VDD2RTC}$	Switch-on Resistance between VDD and RTC module	RTC module powered by VDD IL=10 μA	3.3V	325	500	675	ohm
			5V	250	400	475	ohm
$R_{on,\ VDD2AVCC}$	Switch-on Resistance between VDD and AVCC when power down AVCCLDO	VDD=3.3V, IL*<30 mA		6.5	7.3	9.0	ohm

*: Load current on AVCC.

1.5. Power consumption

Table 1-5 General Operating Conditions

Symbol	Parameter	Conditions (25℃, VDD=3.3V, AVCCLDO power off)	Min	Typ	Max	Unit
I_{ACTIVE}	Active current.	26.2144 MHz system		5082		μA

		clock				
		13.1072 MHz system clock		2792		
		6.5536 MHz system clock		1633		
		3.2768 MHz system clock		1016		
		1.6384 MHz system clock		713		
		819.2 kHz system clock		548		
		409.6 kHz system clock		461		
		204.8 kHz system clock		418		
		32K RC system clock(FLASH deep-standby)		10.0		
		32K RC system clock(power on FLASH)		75.0		
I_{IDLE}	Idle current.	26.2144MHz system clock		1114		µA
		13.1072MHz system clock		625		
		6.5536MHz system clock		379		
		3.2768MHz system clock		256		
		1.6384MHz system clock		195		
		819.2kHz system clock		164		
		409.6kHz system clock		149		
		204.8kHz system clock		141		
		32K RC system clock		5.1		
I_{SLP1}	Sleep current at LCD off.	RTCCLK no frequency division		3.1 6.3@80℃		µA
		RTCCLK 4 frequency division		2.8		
I_{SLP2}	Sleep current at LCD on.	RTCCLK no frequency division		9.3		µA
		RTCCLK 4 frequency division		9.0		
I_{DSLP}	Deep-sleep current,	RTCCLK no frequency		2.9		µA

		division				
		RTCCLK 4 frequency division		2.6		
$I_{RTCONLY}$	RTC only mode current, BATRTC = 3.3V VDD=0V	RTCCLK no frequency division		1.3		μA
		RTCCLK 4 frequency division		1.1		

Table 1-6 Power Consumption of Each Module

module	Power consumption(μA)	State (25℃, VDD=3.3V)
CMP 1/2	0.08	IT_CMP=00(Bias current=20nA)
	0.4	IT_CMP=01(Bias current=100nA)
	2	IT_CMP=1*(Bias current=500nA)
BGP	108	
ADC	230	
TinyADC	0.7	
Temp sensor	370	
LCD	5	LCD driving res=600k
	9.9	LCD driving res=300k
	14.5	LCD driving res=200k
	19	LCD driving res=150k
32768 XTAL	0.6	
32K RC	0.2	
6.5M RC	80	
6.5M XTAL	120	
PLL_L	20	
PLL_H	40	
AVCCLDO	1	

1.6. Embedded Reset and Power Control Block Characteristics

Table 1-7 Embedded Reset and Power Control Block Characteristics

Symbol	Parameter	Conditions (25℃)	Min	Typ	Max	Unit
t_{RST}	Reset de-bounce time.			20		μS
V_{PORH}	PORH detect voltage (AVCCLDO).		1.955	2.08	2.163	V
V_{PORL}	PORL detect voltage (DVCCLDO).		1.222	1.3	1.352	V
V_{VDCIN}	VDCIN detect level.		1.222	1.3	1.352	V
V_{AVCCLV}	AVCCLV detect level.		2.35	2.5	2.6	V
$V_{VDDALRAM}$	VDD supervisor voltage threshold	V_{TH} configurable, V_{TH}=2.9V;	2.726	2.9	3.016	V
AVCC	AVCC voltage		3.2	3.3	3.4	V
V_{AVCC_Drop}	AVCC voltage drop	I_{OUT}=30mA			200	mV
LCDLDO	LCDLDO voltage		3.2	3.3	3.4	V
V_{LCDLDO_Drop}	LCDLDO voltage drop				20	mV

Table 1-8 Hysteresis Voltage Characteristics

Symbol	Parameter	Conditions (25℃)	Min	Typ	Max	Unit
V_{PORH_HTRES}	PORH detect hysteresis voltage.		53.2	66.5	79.8	mV
V_{PORL_HTRES}	PORL detect hysteresis voltage.		33.6	42.0	50.4	mV
V_{VDCIN_HTRES}	VDCIN detect hysteresis voltage.		33.6	42.0	50.4	mV
V_{AVCCLV_HTRES}	AVCCLV detect hysteresis voltage.		33.6	42.0	50.4	mV
$V_{VDDALRAM\_HTRES}$	VDD supervisor hysteresis voltage.	$V_{TH\_VDDALARM}$ = 4.5 V	114.0	142.5	171.0	mV
		$V_{TH\_VDDALARM}$ = 4.2V	106.4	133.0	159.6	mV
		$V_{TH\_VDDALARM}$ = 3.9 V	98.8	123.5	148.2	mV

		$V_{TH\_VDDALARM}$ = 3.6V	91.2	114.0	136.8	mV
		$V_{TH\_VDDALARM}$ = 3.2 V	81.1	101.4	121.6	mV
		$V_{TH\_VDDALARM}$ = 2.9 V	73.5	91.9	110.2	mV
		$V_{TH\_VDDALARM}$ = 2.6 V	65.9	82.4	98.8	mV
		$V_{TH\_VDDALARM}$ = 2.3 V	58.3	72.9	87.4	mV

1.7. GPIO Characteristics

Table 1-9 GPIO Characteristics

Symbol	Parameter	V_{VDDIO}	Conditions (-40~105℃)	Min	Max	Unit
V_{IH}	Input high voltage	5V		0.7*V_{VDD}		V
		3.3V		2		
V_{IL}	Input low voltage	5V			0.3*V_{VDD}	V
		3.3V			0.3*V_{VDD}	V
V_{HSYS}	Schmitt trigger hysteresis	5V		0.1*V_{VDD}		V
		3.3V				
I_{IH}	Input high current	5V			+1	μA
		3.3V				
I_{IL}	Input low current	5V		-1		μA
		3.3V				
V_{OH}	Output high voltage	5V	11.2mA	V_{VDD} -0.8	V_{VDD}	V
		3.3V	5.6mA	2.4	V_{VDD}	V
V_{OL}	Output low voltage	5V	11.2mA		0.5	V
		3.3V	5.6mA		0.4	V
C_{IN}	Input capacitance	5V			10	pF
		3.3V				

1.8. ADC Characteristics

Table 1-10 ADC Characteristics

Symbol	Parameter	Conditions (25℃)	Min	Typ	Max	Unit
BGPREF	BGP Voltage		1.18	1.2	1.22	V
PSRR	Power Supply Rejection Ratio of BGP			-55		dB
V_{ADC}	ADC operation voltage		2.7	3.3	3.6	V
I_{ADC}	ADC operation current.		170	230	350	µA
f_{ADCLK}	ADC sampling clock.			1.6384		MHz
C_{ADC}	Internal sample and hold capacitance.			1		pF
INL	Integrated non linearity.			2		LSB
DNL	Differential non linearity.			1		LSB
Offset	Offset error			5		mV
$V_{WITHSTAND}$	Withstand voltage (input of ADC Channel)		-0.7		VDD	V

1.9. Comparator Characteristics

Table 1-11 Comparator Characteristics

Symbol	Parameter	Conditions (25℃)	Min	Typ	Max	Unit
V_{CMP}	Comparator operation voltage(AVCC)		2.2	3.3	3.6	V
I_{CMP}	Comparator operation current.	Input bias current 20nA, input 50kHz square wave.		0.08		µA
		Input bias current 100nA, input 50kHz square wave.		0.4		µA
		Input bias current 500nA, input 50kHz square wave.		2		µA
td	Propagation delay	Input bias current 20nA, input 50kHz		1.6		µS

		square wave.				
		Input bias current 100nA, input 50kHz square wave.		0.63		μS
		Input bias current 500nA, input 50kHz square wave.		0.27		μS
V_{CMPIN}	Comparator input voltage range.		0.8		VDD-0.3	V
V_{CMPREF}	Comparator reference voltage	Reference voltage is VREF	1.222	1.3	1.352	V
		Reference voltage is BGPREF	1.18	1.2	1.22	V
V_{HTRES}	Comparator hysteresis voltage		20.0	25.0	30.0	mV

1.10. Clock and PLL Characteristics

Table 1-12 Clock and PLL Characteristics

Symbol	Parameter	Conditions (-40~105℃)	Min	Typ	Max	Unit
V_{DDPLLL}	PLLL operating voltage (DVCC)		1.35	1.5	1.65	V
$I_{VDDPLLL}$	PLLL operating current			30		μA
V_{DDPLLH}	PLLH operating voltage (DVCC)		1.35	1.5	1.65	V
$I_{VDDPLLH}$	PLLH operating current			40		μA
V_{DDRCL}	RCL operating voltage (AVCC)		2.2	3.3	3.6	V
I_{VDDRCL}	RCL operating current			0.2		μA
f_{RCL}	RCL frequency.		29.7	32	35.5	kHz
V_{DDRCH}	RCH operating voltage (AVCC)		2.2	3.3	3.6	V
I_{VDDRCH}	RCH operating current			45		μA
f_{RCH}	RCH frequency.		6.357	6.5	6.75	MHz
V_{DDXOH}	XOH operating voltage (AVCC)		2.2	3.3	3.6	V
I_{VDDXOH}	XOH operating current			150		μA
f_{XOH}	XOH frequency.			6.5536		MHz

1.11. FLASH and SRAM Characteristics

Table 1-13 FLASH and SRAM Characteristics

Parameter	Conditions	Min	Typ	Max	Unit
FLASH word read access time.		38			ns
FLASH program time	-40~105℃	20000			time
FLASH data retention time	-40~105℃	20			year
FLASH byte program time		6		7.5	μS
FLASH page erase time (512 bytes)		4		5	ms
FLASH chip erase time		30		40	ms
FLASH active read current	26MHz access.		2.5	3.5	mA
FLASH active program current				3.5	mA
FLASH active erase current				2	mA
FLASH standby current			80	150	μA
FLASH deep standby current			0.1	6	μA
SRAM data retention voltage (DVCC)	-40~105℃	1.35	1.5	1.65	V

1.12. ESR Characteristics of Crystal Oscillator

Table 1-14 ESR Characteristics of Crystal Oscillator

Parameter	Conditions (-40~105℃)	Min	Typ	Max	Unit
ESR of 6.5536M crystal oscillator				40	Ω
ESR of 32768K crystal oscillator				50	KΩ

*: ESR (Equivalent series resistance)

1.13. Stabilization Time of Clock and Wake up Time

Table 1-15 Stabilization Time of Clock and Wake-up Time

Parameter	Conditions (-40~105℃)	Min	Typ	Max	Unit
PLLL lock time				1	ms
PLLH lock time				15	μS
Stabilization time of RCL				200	μS
Stabilization time of RCH				5	μS
Stabilization time of BGP				10	μS
Wake up time from sleep mode when RCH as system clock			18.4		μS
Wake up time from sleep mode when PLLL as system clock			1.03		mS
Wake up time from sleep mode when PLLH as system clock			22.8		μS
Interrupt response time in IDLE mode when RCH as system clock			6		μS
Interrupt response time in IDLE mode when PLLL as system clock			1.6		μS
Interrupt response time in IDLE mode when PLLH as system clock			1.6		μS

1.14. ADC Conversion Time

ADC clock frequency, CIC down sampling rate and CIC output skip point number influence the ADC conversion time. Please refer the following tables for the details:

Table 1-16 ADC Conversion Time (ADC clock frequency and CIC down sampling rate are variable)

ADCLK/MHz CIC down Sample rate ADC Conversion time/ms	6.5536	3.2768	1.6384	0.8192	0.4096
1/512	0.937	0.937	1.875	3.750	7.500
1/256	0.468	0.468	0.937	1.875	3.750
1/128	0.234	0.234	0.468	0.937	1.875
1/64	0.117	0.117	0.234	0.468	0.937
Other parameter configuration: CICSKIP=6, CIC output skip first two points.					

Note1: CIC is 3 order filter in this file, the data is stable when the first two sampling points is ignored.

Note2: $T_{ADC\_CONVER\ SION} = \frac{1}{\left(R_{CIC\_DownSa\ mple} * \frac{f_{ADC}}{2}\right)} * N_{Sample\_Poi\ nt}$ (except ADC clock equal 6.5536MHz). Example, CIC down sample is 1/512, ADCLK is 3.2768MHz, and skip first two points, then $T_{ADC\_CONVER\ SION} = \frac{1}{\left(\frac{1}{512} * \frac{3.2768MHz}{2}\right)} * 3 = 0.937ms$

Table 1-17 ADC Conversion Time (CIC output skip point number is variable)

Parameter	CIC output skip point number	ADC Conversion time	Unit
MADC conversion time	2	1.875	mS
	3	2.520	mS
	4	3.150	mS
	5	3.780	mS
	6	4.410	mS
	7	5.040	mS
Other parameter configuration: CIC down sample is 1/512, ADCLK is 1.6384MHz			

1.15. TinyADC Conversion Time

Table 1-18 TinyADC Conversion Time

Parameter	Conditions	Min	Typ	Max	Unit
TinyADC conversion time			40		μS

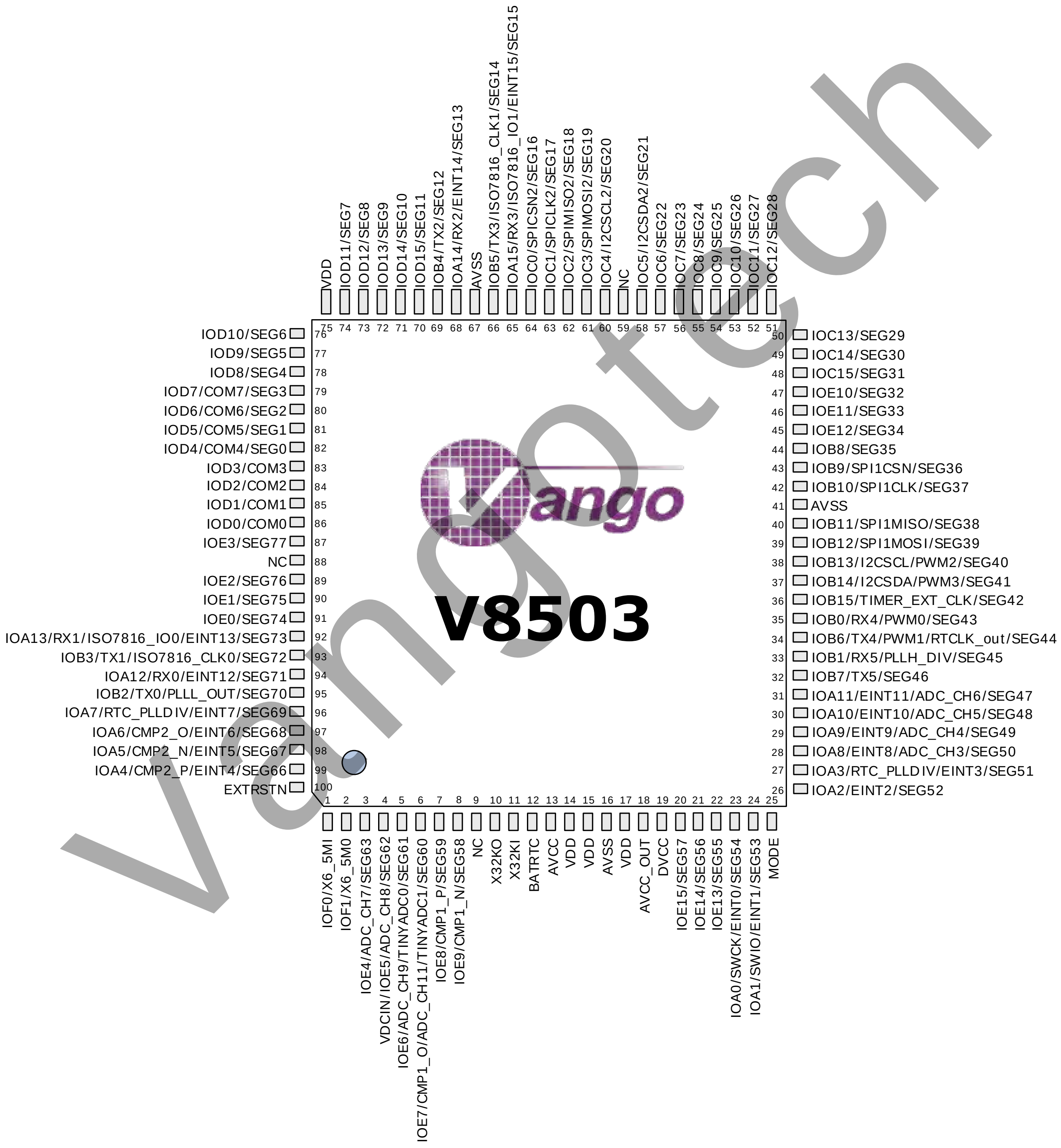
1.16. ESD handling ratings

Table 1-19 ESD handling ratings

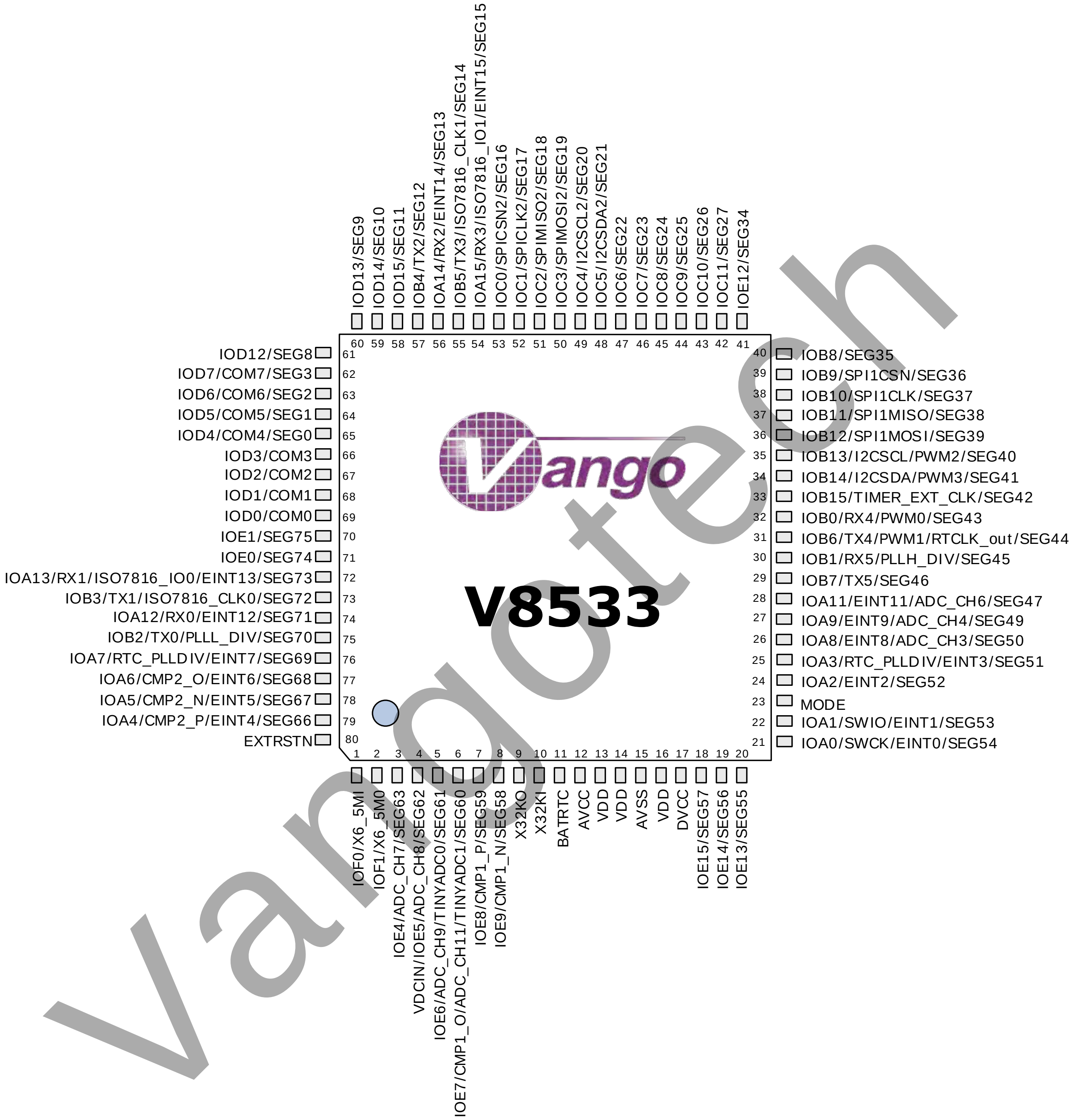
Parameter	Conditions	Min	Max
HBM	Mil-Std-883J Method 3015.9	-4KV	+4KV
MM	EDEC EIA/JESD22-A115	-300V	+300V
LATCH-UP	JEDEC EIA/JESD78E	-200mA	+200mA

2.Pin Assignments

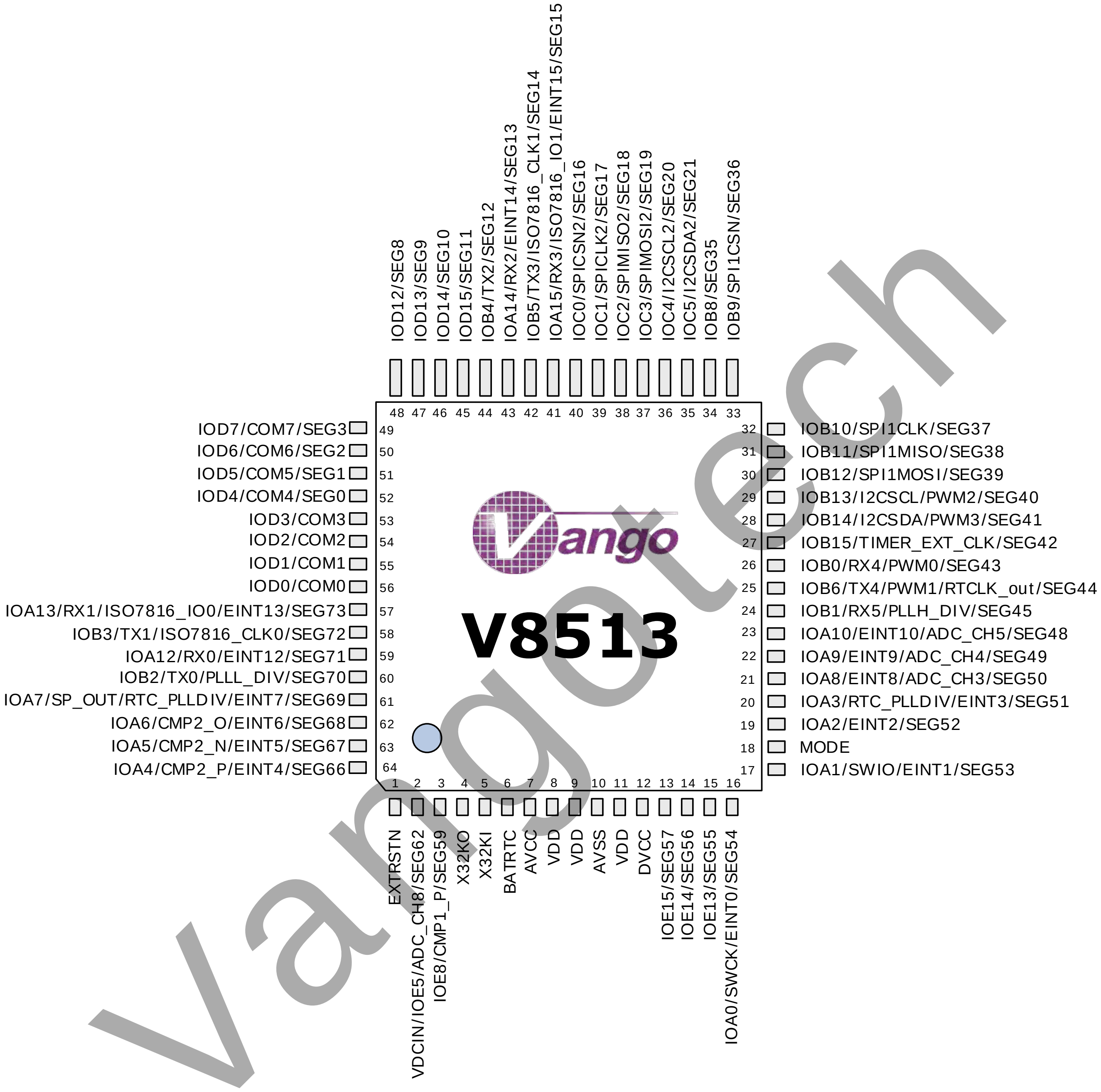
2.1. V8503 Pin Assignments



2.2. V8533 Pin Assignments



2.3. V8513 Pin Assignments



2.4. V85X3 Pin Descriptions

Table 2-1 V85X3 Pin Descriptions

Pin Number			Pin Name	Type	Description
V8503	V8533	V8513			
1	1		IOF0	I/O	Default: IOF0 Function 1: 6.5536M crystal input
2	2		IOF1	I/O	Default: IOF1 Function 1: 6.5536M crystal output
3	3		IOE4	I/O	Default: IOE4 Function 1: ADC_CH7 input Function 2: SEG63
4	4	2	IOE5	I/O	Default: VDCIN input. Function 1: ADC_CH8 input Function 2: IOE5 Function 3: SEG62
5	5		IOE6	I/O	Default: IOE6 Function 1: ADC_CH9 input and tiny ADC channel 0 input Function 2: SEG61
6	6		IOE7	I/O	Default: IOE7 Function 1: Comparator 1 output Function 2: ADC_CH11 input and tiny ADC channel 1 input Function 3: SEG60
7	7	3	IOE8	I/O	Default: IOE8 Function 1: Comparator 1 P input Function 2: SEG59
8	8		IOE9	I/O	Default: IOE9 Function 1: Comparator 1 N input Function 2: SEG58
9			NC		No connected.
10	9	4	X32KO	O	32768 Hz crystal output pin. The internal matching capacitance is 12 pF.
11	10	5	X32KI	I	32768 Hz crystal input pin
12	11	6	BATRTC	P	RTC Battery input pin
13	12	7	AVCC	O/P	AVCC output pin, user should connect a 0.1 uF and 10uF de-couple capacitor at this pin.
14	13	8	VDD	P	Main VDD power input. User should connect a 0.1uF de-couple capacitor at this pin.
15	14	9	VDD	P	Main VDD power input
16	15	10	AVSS	G	Analog ground
17	16	11	VDD	P	Main VDD power input

18			AVCC_OUT	O	AVCC voltage output pin. This pin has the same electrical level as AVCC, user can be used to drive small power modules.
19	17	12	DVCC	O/P	DVCC output pin, user should connect a 0.1 uF and 10uF de-couple capacitor at this pin.
20	18	13	IOE15	I/O	Default: IOE15 Function 2: SEG57
21	19	14	IOE14	I/O	Default: IOE14 Function 2: SEG56
22	20	15	IOE13	I/O	Default: IOE13 Function 2: SEG55
23	21	16	IOA0	I/O	Default: IOA0 (MODE=1), SWCLK(MODE=0) Function 1: EINT0 Function 2: SEG54
24	22	17	IOA1	I/O	Default: IOA1 (MODE=1), SWDIO(MODE=0) Function 1: EINT1 Function 2: SEG53
25	23	18	MODE	I	Debug mode or normal mode selection. 0: Debug mode 1: Normal mode The signal level of this pin should be the same as VDD, and the state of this IO should not change during normal or debug operation.
26	24	19	IOA2	I/O	Default: IOA2 Function 1: EINT2 Function 2: SEG52
27	25	20	IOA3	I/O	Default: IOA3 Function 1: Second pulse output (RTC_PLLDIV output) Function 2: EINT3 Function 3: SEG51
28	26	21	IOA8	I/O	Default: IOA8 Function 1: EINT8 Function 2: ADC_CH3 input Function 3: SEG50
29	27	22	IOA9	I/O	Default: IOA9 Function 1: EINT9 Function 2: ADC_CH4 input Function 3: SEG49
30		23	IOA10	I/O	Default: IOA10 Function 1: EINT10 Function 2: ADC_CH5 input Function 3: SEG48

31	28		IOA11	I/O	Default: IOA11 Function 1: EINT11 Function 2: ADC_CH6 input Function 3: SEG47
32	29		IOB7	I/O	Default: IOB7 Function 1: UART TXD 5 Function 2: SEG46
33	30	24	IOB1	I/O	Default: IOB1 Function 1: UART RXD 5 Function 3: PLLH divider output Function 4: SEG45
34	31	25	IOB6	I/O	Default: IOB6 Function 1: UART TXD 4 Function 2: PWM1 In/Out line Function 3: RTCCLK output Function 4: SEG44
35	32	26	IOB0	I/O	Default: IOB0 Function 1: UART RXD4 Function 2: PWM0 In/Out line Function 3: SEG43
36	33	27	IOB15	I/O	Default: IOB15 Function 1: Timer external clock input Function 2: SEG42
37	34	28	IOB14	I/O	Default: IOB14 Function 1: I2C SDA Function 2: PWM3 In/Out line Function 3: SEG41
38	35	29	IOB13	I/O	Default: IOB13 Function 1: I2C SCL Function 2: PWM2 In/Out line Function 3: SEG40
39	36	30	IOB12	I/O	Default: IOB12 Function 1: SPI1 MOSI Function 2: SEG39
40	37	31	IOB11	I/O	Default: IOB11 Function 1: SPI1 MISO Function 2: SEG38
41			AVSS	G	Analog ground
42	38	32	IOB10	I/O	Default: IOB10 Function 1: SPI1 CLK Function 2: SEG37
43	39	33	IOB9	I/O	Default: IOB9 Function 1: SPI1 CSN Function 2: SEG36
44	40	34	IOB8	I/O	Default: IOB8 Function 2: SEG35

45	41		IOE12	I/O	Default: IOE12 Function 1: SEG34
46			IOE11	I/O	Default: IOE11 Function 1: SEG33
47			IOE10	I/O	Default: IOE10 Function 1: SEG32
48			IOC15	I/O	Default: IOC15 Function 1: SEG31
49			IOC14	I/O	Default: IOC14 Function 1: SEG30
50			IOC13	I/O	Default: IOC13 Function 1: SEG29
51			IOC12	I/O	Default: IOC12 Function 1: SEG28
52	42		IOC11	I/O	Default: IOC11 Function 1: SEG27
53	43		IOC10	I/O	Default: IOC10 Function 1: SEG26
54	44		IOC9	I/O	Default: IOC9 Function 1: SEG25
55	45		IOC8	I/O	Default: IOC8 Function 1: SEG24
56	46		IOC7	I/O	Default: IOC7 Function 1: SEG23
57	47		IOC6	I/O	Default: IOC6 Function 1: SEG22
58	48	35	IOC5	I/O	Default: IOC5 Function 1: I2C SDA (2) Function 2: SEG21
59			NC		No connected.
60	49	36	IOC4	I/O	Default: IOC4 Function 1: I2C SCL (2) Function 2: SEG20
61	50	37	IOC3	I/O	Default: IOC3 Function 1: SPI2 MOSI Function 2: SEG19
62	51	38	IOC2	I/O	Default: IOC2 Function 1: SPI2 MISO Function 2: SEG18
63	52	39	IOC1	I/O	Default: IOC1 Function 1: SPI2 CLK Function 2: SEG17
64	53	40	IOC0	I/O	Default: IOC0 Function 1: SPI2 CSN Function 2: SEG16

65	54	41	IOA15	I/O	Default: IOA15 Function 1: UART RXD 3 Function 2: ISO7816 I/O1 Function 3: EINT15 Function 4: SEG15
66	55	42	IOB5	I/O	Default: IOB5 Function 1: UART TXD 3 Function 2: ISO7816 CLK1 Function 3: SEG14
67			AVSS	G	Analog ground.
68	56	43	IOA14	I/O	Default: IOA14 Function 1: UART RXD 2 Function 2: EINT14 Function 3: SEG13
69	57	44	IOB4	I/O	Default: IOB4 Function 1: UART TXD 2 Function 2: SEG12
70	58	45	IOD15	I/O	Default: IOD15 Function 1: SEG11
71	59	46	IOD14	I/O	Default: IOD14 Function 1: SEG10
72	60	47	IOD13	I/O	Default: IOD13 Function 1: SEG9
73	61	48	IOD12	I/O	Default: IOD12 Function 1: SEG8
74			IOD11	I/O	Default: IOD11 Function 1: SEG7
75			VDD	P	Main VDD power input
76			IOD10	I/O	Default: IOD10 Function 1: SEG6
77			IOD9	I/O	Default: IOD9 Function 1: SEG5
78			IOD8	I/O	Default: IOD8 Function 1: SEG4
79	62	49	IOD7	I/O	Default: IOD7 Function 1: COM7/SEG3
80	63	50	IOD6	I/O	Default: IOD6 Function 1: COM6/SEG2
81	64	51	IOD5	I/O	Default: IOD5 Function 1: COM5/SEG1
82	65	52	IOD4	I/O	Default: IOD4 Function 1: COM4/SEG0
83	66	53	IOD3	I/O	Default: IOD3 Function 1: COM3
84	67	54	IOD2	I/O	Default: IOD2 Function 1: COM2

85	68	55	IOD1	I/O	Default: IOD1 Function 1: COM1
86	69	56	IOD0	I/O	Default: IOD0 Function 1: COM0
87			IOE3	I/O	Default: IOE3 Function 1: SEG77
88			NC		No connected.
89			IOE2	I/O	Default: IOE2 Function 1: SEG76
90	70		IOE1	I/O	Default: IOE1 Function 1: SEG75
91	71		IOE0	I/O	Default: IOE0 Function 1: SEG74
92	72	57	IOA13	I/O	Default: IOA13 Function 1: UART RXD 1 Function 2: ISO7816 I/O 0 Function 3: EINT13 Function 4: SEG73
93	73	58	IOB3	I/O	Default: IOB3 Function 1: UART TXD 1 Function 2: ISO7816 CLK 0 Function 3: SEG72
94	74	59	IOA12	I/O	Default: IOA12 Function 1: UART RXD 0 Function 2: EINT12 Function 3: SEG71
95	75	60	IOB2	I/O	Default: IOB2 Function 1: UART TXD 0 Function 2: PLLL output Function 3: SEG70
96	76	61	IOA7	I/O	Default: IOA7 Function 1: Second pulse output (RTC_PLLDIV output) Function 2: EINT7 Function 3: SEG69
97	77	62	IOA6	I/O	Default: IOA6 Function 1: Comparator 2 output Function 2: EINT6 Function 3: SEG68
98	78	63	IOA5	I/O	Default: IOA5 Function 1: Comparator 2 N input Function 2: EINT5 Function 3: SEG67

99	79	64	IOA4	I/O	Default: IOA4 Function 1: Comparator 2 P input Function 2: EINT4 Function 3: SEG66
100	80	1	EXTRSTN	I	External reset pin, low active

3.Functional Block Diagram

3.1. Functional Block Diagram

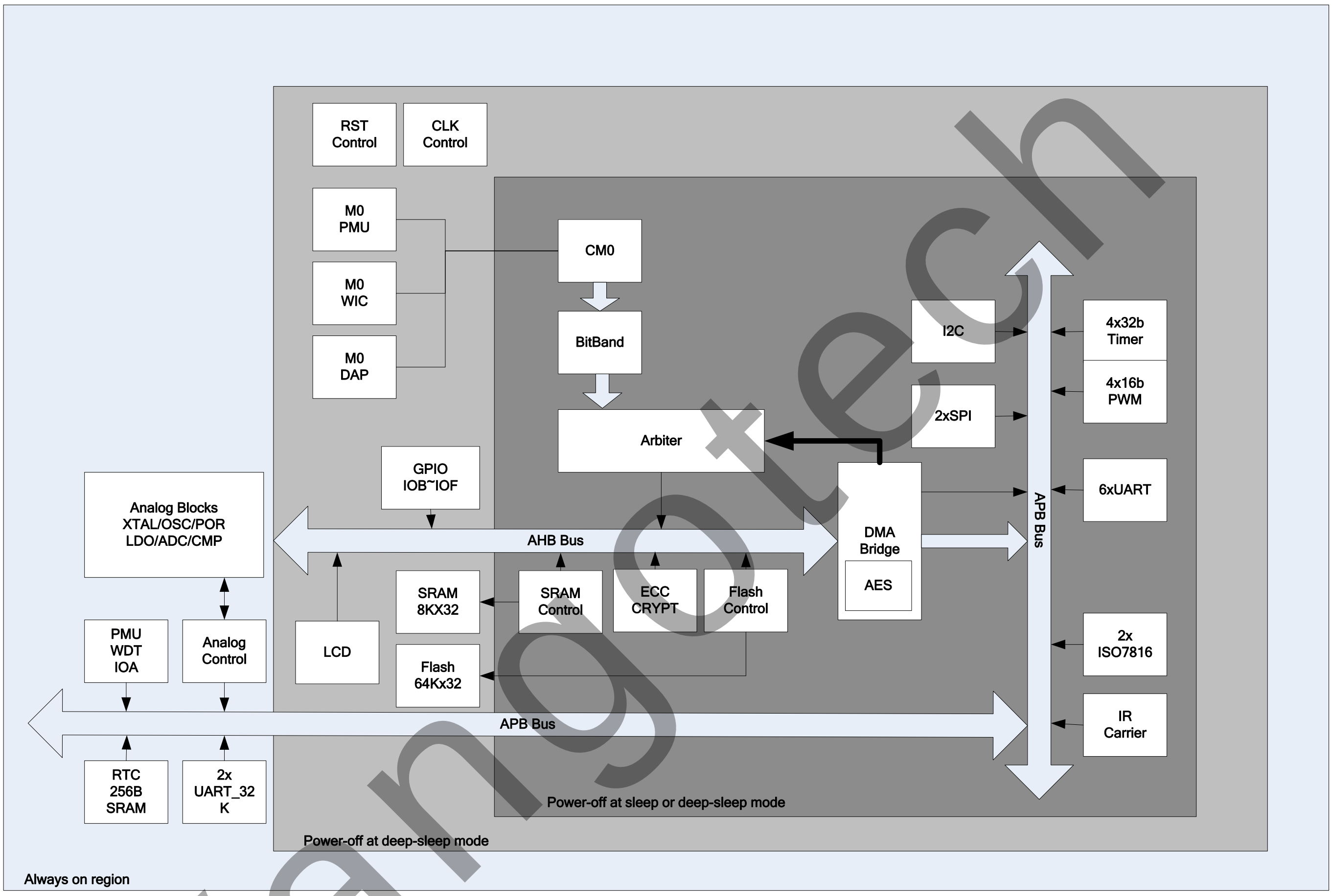


Figure 3-1 V85X3 Functional Block Diagram

3.2. Power System Block Diagram

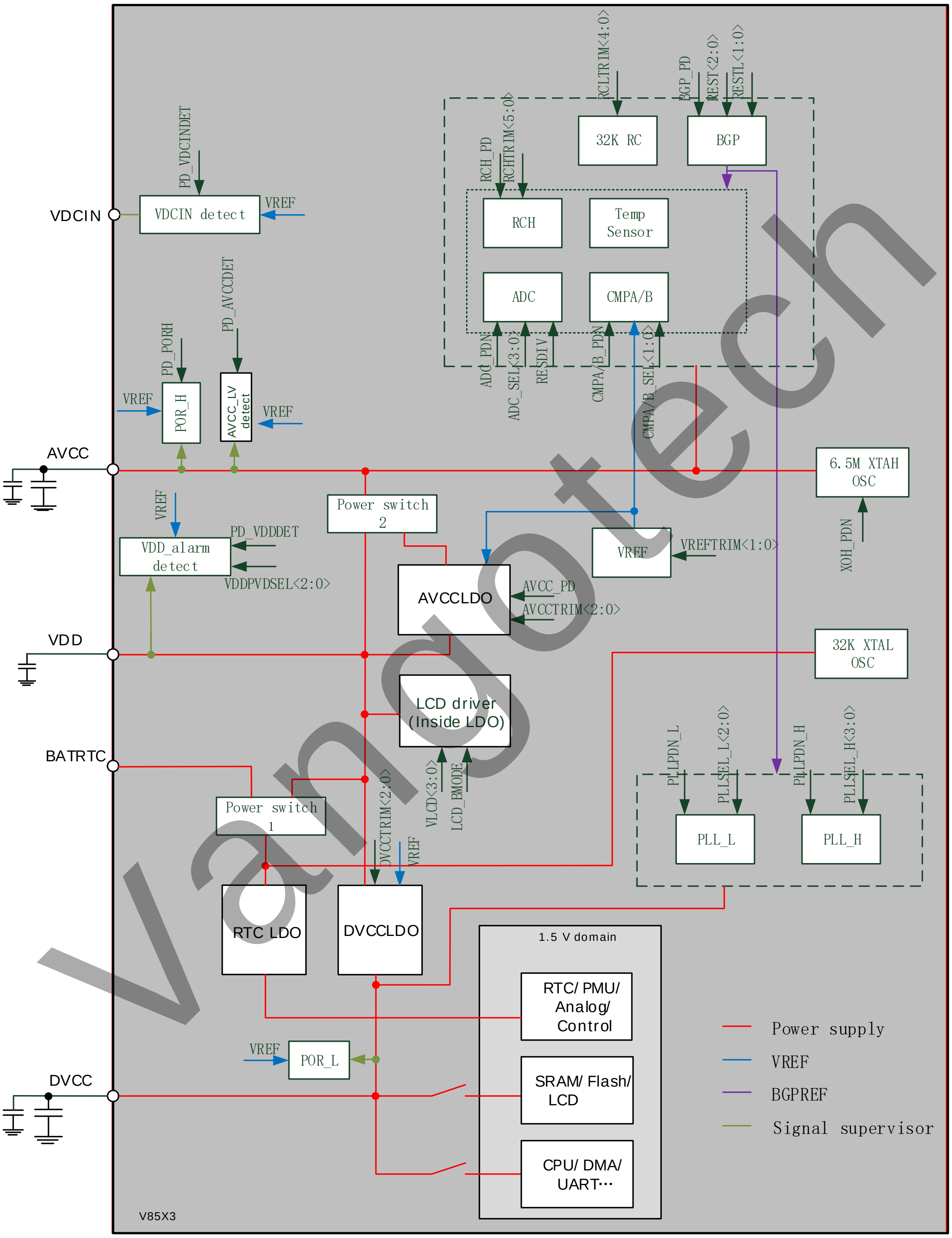
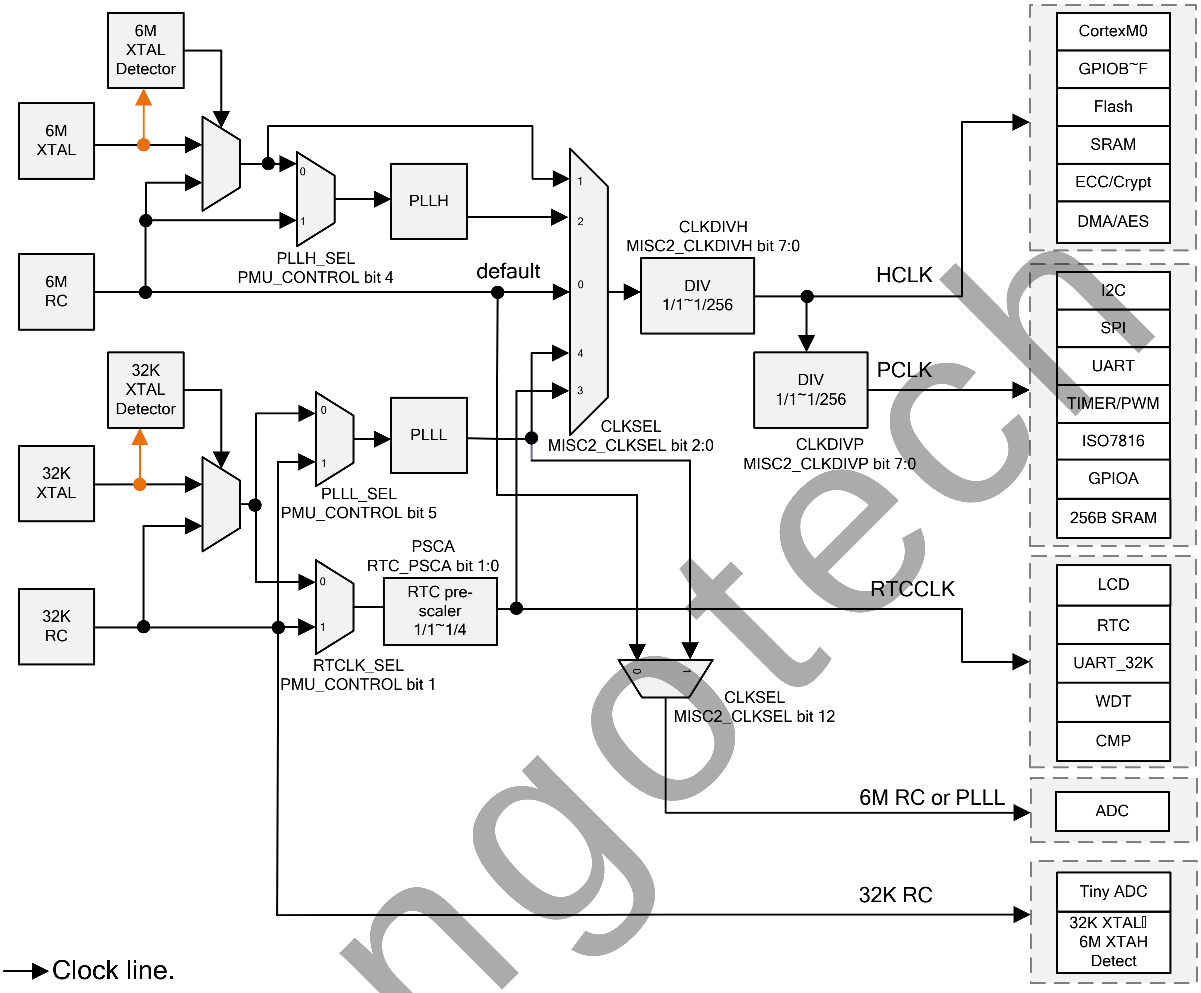


Figure 3-2 V85X3 Power System Block Diagram

3.3. Clock Block Diagram



→Clock line.

→ Oscillator circuit detect signal line. 6M XTAL detector and 32K XTAL detector is sourced by 32K RC clock. When this oscillator circuit stops running, 6M RC clock will replace 6M XTAL clock, 32K RC clock will replace 32K XTAL clock, and the monitoring circuit will stimulate the crystal oscillator circuit until it runs again.

Figure 3-3 V85X3 Clock Block Diagram

4.Memory Maps

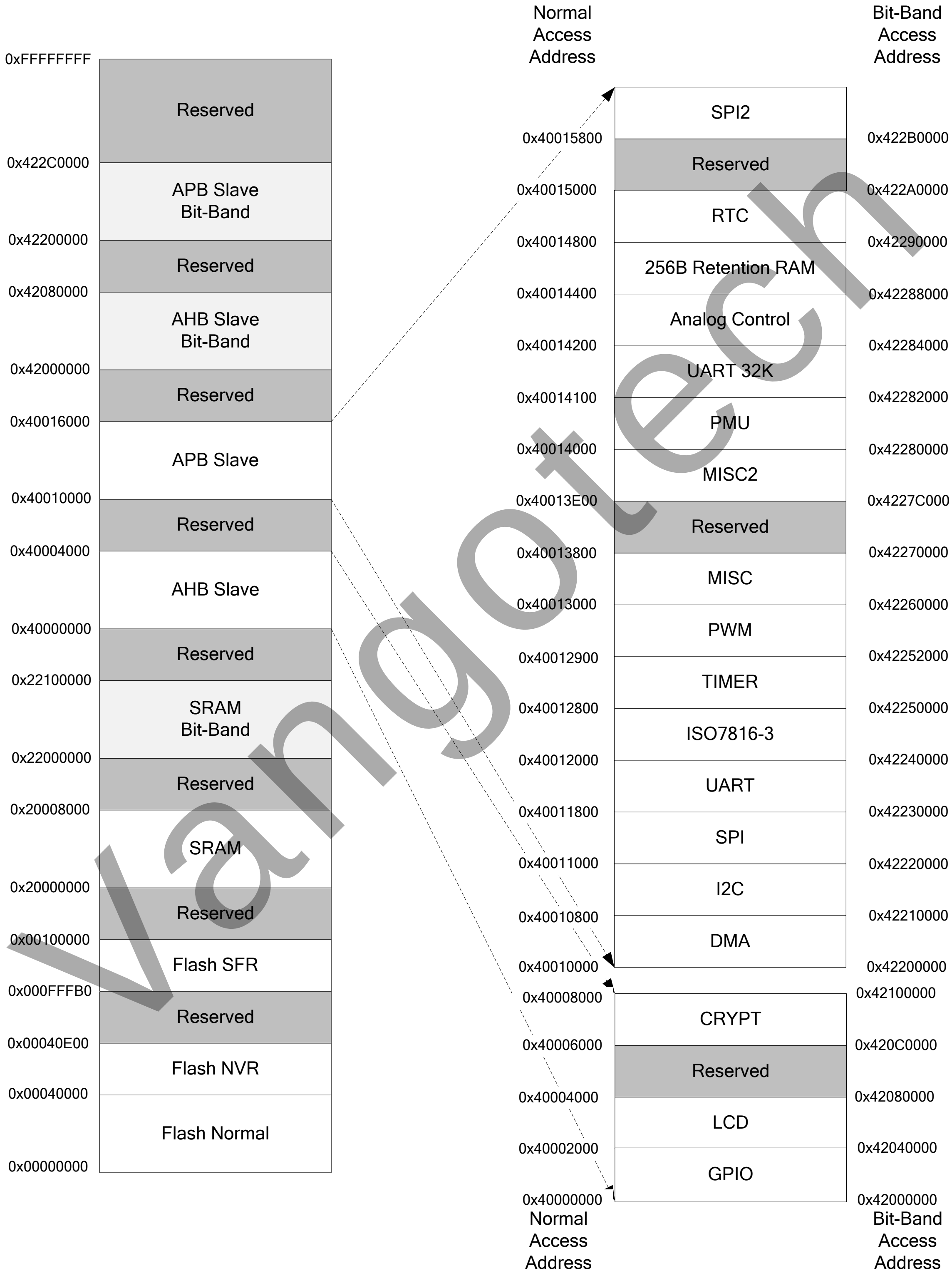


Figure 4-1 V85X3 Memory Maps

The bit-band region can only be accessed by Cortex-M0. The DMA controller can't access these regions. For all other regions, they can be accessed by both Cortex-M0 and DMA controller.

4.1. Register Location

4.1.1. PMU Register Location

Table 4-1 Register Location of the PMU Controller (PMU Base: 0x40014000)

Name	Type	Address	Description	Default
PMU_DSLEEPEN	R/W	0x0000	PMU deep sleep enable register	0x00000000
PMU_DSLEEPPASS	R/W	0x0004	PMU deep sleep password register	0x00000000
PMU_CONTROL	R/W	0x0008	PMU control register	0x0000
PMU_STS	R/C	0x000C	PMU Status register	0x0000074
PMU_IOAOEN	R/W	0x0010	IOA output enable register	0xFFFF
PMU_IOAIE	R/W	0x0014	IOA input enable register	0xFFFF
PMU_IOADAT	R/W	0x0018	IOA data register	0x0000
PMU_IOAATT	R/W	0x001C	IOA attribute register	0x0000
PMU_IOAWKUEN	R/W	0x0020	IOA wake-up enable register	0x00000000
PMU_IOASTS	R	0x0024	IOA input status register	--
PMU_IOAINTSTS	R/C	0x0028	IOA interrupt status register	0x0000
PMU_IOASEL	R/W	0x0038	IOA special function select register	0x0000
VERSIONID	R	0x003C	Version ID of V85X3	--
PMU_WDTPASS	R/W	0x0040	Watch dog timing unlock register	0x00000000
PMU_WDTEN	R/W	0x0044	Watch dog timer enable register	0x1
PMU_WDTCLR	W	0x0048	Watch dog timer clear register	0x0000
PMU_IOANODEG	R/W	0x0050	IOA no-deglitch control register.	0x0000

Table 4-2 Register Location of the PMU Controller (PMU Retention RAM Base: 0x40014400)

Name	Type	Address	Description	Default
PMU_RAM0	R/W	0x0000	PMU 32 bits Retention RAM 0	--
PMU_RAM1	R/W	0x0004	PMU 32 bits Retention RAM 1	--
PMU_RAM2	R/W	0x0008	PMU 32 bits Retention RAM 2	--
			…..	

PMU_RAM63	R/W	0x00FC	PMU 32 bits Retention RAM 63	--

4.1.2. ANA Register Location

Table 4-3 Register Location of ANA Controller (ANA Base: 0x40014200)

Name	Type	Address	Description	Default
ANA_REG0	R/W	0x0000	Analog register 0	0x00
ANA_REG1	R/W	0x0004	Analog register 1	0x00
ANA_REG2	R/W	0x0008	Analog register 2	0x00
ANA_REG3	R/W	0x000C	Analog register 3	0x00
ANA_REG4	R/W	0x0010	Analog register 4	0x00
ANA_REG5	R/W	0x0014	Analog register 5	0x00
ANA_REG6	R/W	0x0018	Analog register 6	0x00
ANA_REG7	R/W	0x001C	Analog register 7	0x00
ANA_REG8	R/W	0x0020	Analog register 8	0x00
ANA_REG9	R/W	0x0024	Analog register 9	0x00
ANA_REGA	R/W	0x0028	Analog register 10	0x00
ANA_REGB	R/W	0x002C	Analog register 11	From FLASH
ANA_REGC	R/W	0x0030	Analog register 12	From FLASH
ANA_REGD	R/W	0x0034	Analog register 13	From FLASH
ANA_REGE	R/W	0x0038	Analog register 14	From FLASH
ANA_REGF	R/W	0x003C	Analog register 15	0x00
ANA_CTRL	R/W	0x0050	Analog control register	0x0000000
ANA_CMPOUT	R	0x0054	Comparator result register	0x0030
ANA_INTSTS	R/C	0x0060	Analog interrupt status register	0x0000
ANA_INTEN	R/W	0x0064	Analog interrupt enable register	0x0000
ANA_ADCCTRL	R/W	0x0068	ADC control register	0x00000000
ANA_ADCDATA0	R	0x0070	ADC channel 0 data register	--
ANA_ADCDATA1	R	0x0074	ADC channel 1 data register	--
ANA_ADCDATA2	R	0x0078	ADC channel 2 data register	--
ANA_ADCDATA3	R	0x007C	ADC channel 3 data register	--

ANA_ADCDATA4	R	0x0080	ADC channel 4 data register	--
ANA_ADCDATA5	R	0x0084	ADC channel 5 data register	--
ANA_ADCDATA6	R	0x0088	ADC channel 6 data register	--
ANA_ADCDATA7	R	0x008C	ADC channel 7 data register	--
ANA_ADCDATA8	R	0x0090	ADC channel 8 data register	--
ANA_ADCDATA9	R	0x0094	ADC channel 9 data register	--
ANA_ADCDATAA	R	0x0098	ADC channel 10 data register	--
ANA_ADCDATAB	R	0x009C	ADC channel 11 data register	--
ANA_CMPCNT1	R/C	0x00B0	Comparator 1 counter	0x00000000
ANA_CMPCNT2	R/C	0x00B4	Comparator 2 counter	0x00000000
ANA_MISC	R/W	0x00B8	Analog misc. control register	0x00

4.1.3. RTC Register Location

Table 4-4 Register Location of RTC Controller (RTC Base: 0x40014800)

Name	Type	Address	Description	Default	Write Protect	Read Protect
RTC_SEC	R/W	0x0000	RTC second register	--	V	V
RTC_MIN	R/W	0x0004	RTC minute register	--	V	V
RTC_HOUR	R/W	0x0008	RTC hour register	--	V	V
RTC_DAY	R/W	0x000C	RTC day register	--	V	V
RTC_WEEK	R/W	0x0010	RTC week-day register	--	V	V
RTC_MON	R/W	0x0014	RTC month register	--	V	V
RTC_YEAR	R/W	0x0018	RTC year register	--	V	V
RTC_WKUSEC	R/W	0x0020	RTC wake-up second register	0x00	V	
RTC_WKUMIN	R/W	0x0024	RTC wake-up minute register	0x00	V	
RTC_WKUHOUR	R/W	0x0028	RTC wake-up hour register	0x00	V	
RTC_WKUCNT	R/W	0x002C	RTC wake-up counter register	0x0000000	V	
RTC_CAL	R/W	0x0030	RTC calibration register	--	V	
RTC_DIV	R/W	0x0034	RTC PLL divider register	0x0000000		
RTC_CTL	R/W	0x0038	RTC PLL divider control register	0x0		

RTC_PWD	R/W	0x0044	RTC password control register	0x00000000		
RTC_CE	R/W	0x0048	RTC write enable control register	0x0		
RTC_LOAD	R/W	0x004C	RTC read enable control register	--		
RTC_INTSTS	R/W	0x0050	RTC interrupt status control register	0x000		
RTC_INTEN	R/W	0x0054	RTC interrupt enable control register	0x000		
RTC_PSCA	R/W	0x0058	RTC clock pre-scaler control register	0x0	V	
RTC_ACCTRL	R/W	0x0080	RTC auto-calibration control register	0x0000	V	
RTC_ACTI	R/W	0x0084	RTC auto-calibration center temperature control register	0x1800	V	
RTC_ACF200	R/W	0x0088	RTC auto-calibration 200*frequency control register	0x640000	V	
RTC_ACADCW	R/W	0x008C	RTC auto-calibration manual ADC value control register	0x0000	V	
RTC_ACP0	R/W	0x0090	RTC auto-calibration parameter 0 control register	0x0000	V	
RTC_ACP1	R/W	0x0094	RTC auto-calibration parameter 1 control register	0x0000	V	
RTC_ACP2	R/W	0x0098	RTC auto-calibration parameter 2 control register	0x0000	V	
RTC_ACP3	R	0x009C	RTC auto-calibration parameter 3 control register	0x0000		
RTC_ACP4	R/W	0x00A0	RTC auto-calibration parameter 4 control register	0x0000	V	
RTC_ACP5	R/W	0x00A4	RTC auto-calibration parameter 5 control register	0x0000	V	
RTC_ACP6	R/W	0x00A8	RTC auto-calibration parameter 6 control register	0x0000	V	
RTC_ACP7	R/W	0x00AC	RTC auto-calibration parameter 7 control register	0x0000	V	
RTC_ACK1	R/W	0x00B0	RTC auto-calibration parameter k1 control register	0x0000	V	
RTC_ACK2	R/W	0x00B4	RTC auto-calibration parameter	0x0000	V	

			k2 control register			
RTC_ACK3	R/W	0x00B8	RTC auto-calibration parameter k3 control register	0x0000	V	
RTC_ACK4	R/W	0x00BC	RTC auto-calibration parameter k4 control register	0x0000	V	
RTC_ACK5	R/W	0x00C0	RTC auto-calibration parameter k5 control register	0x0000	V	
RTC_ACTEMP	R	0x00C4	RTC auto-calibration calculated temperature register	0x0000	V	
RTC_ACPPM	R	0x00C8	RTC auto-calibration calculated PPM register	0x0000	V	
RTC_WKUCNTR	R	0x00CC	This register is used to represent the current WKUCNT value	0x000000	V	
RTC_ACKTEMP	R/W	0x00D0	RTC auto-calibration k temperature section control register	0x3C2800EC	V	

4.1.4. FLASH Register Location

Table 4-5 Register Location of FLASH Controller (FLASH Controller Base: 0x00000000)

Name	Type	Address	Description	Default
FLASH_STS	R	0xFFFBC	FLASH programming status register	0x00
FLASH_INT	R/C	0xFFFCC	FLASH Checksum interrupt status	0x0
FLASH_CSSADDR	R/W	0xFFFD0	FLASH Checksum start address	0x00000
FLASH_CSEADDR	R/W	0xFFFD4	FLASH Checksum end address	0xFFFFF
FLASH_CSVALUE	R	0xFFFD8	FLASH Checksum value register	--
FLASH_CSCVALUE	R/W	0xFFFDC	FLASH Checksum compare value register	0x00000000
FLASH_PASS	R/W	0xFFFE0	FLASH password register	0x00000000
FLASH_CTRL	R/W	0xFFFE4	FLASH control register	0x0
FLASH_PGADDR	R/W	0xFFFE8	FLASH program address register	0x00000
FLASH_PGDATA	R/W	0xFFFEC	FLASH program word data register	--
FLASH_PGB0	R/W	0xFFFEC	FLASH program byte data register 0	--
FLASH_PGB1	R/W	0xFFFED	FLASH program byte data register 1	--
FLASH_PGB2	R/W	0xFFFEE	FLASH program byte data register 2	--

FLASH_PGB3	R/W	0xFFFEF	FLASH program byte data register 3	--
FLASH_PGHW0	R/W	0xFFFEC	FLASH program half-word data register 0	--
FLASH_PGHW1	R/W	0xFFFEE	FLASH program half-word data register 1	--
FLASH_SERASE	R/W	0xFFFF4	FLASH sector erase control register	0x00000000
FLASH_CERASE	R/W	0xFFFF8	FLASH chip erase control register	0x00000000
FLASH_DSTB	R/W	0xFFFFC	FLASH deep standby control register	0x00000000

4.1.5. GPIO Register Location

Table 4-6 Register Location of GPIO Controller (GPIO Base: 0x40000000)

Name	Type	Address	Description	Default
IOB_OEN	R/W	0x0020	IOB output enable register	0xFFFF
IOB_IE	R/W	0x0024	IOB input enable register	0xFFFF
IOB_DAT	R/W	0x0028	IOB data register	0x0000
IOB_ATT	R/W	0x002C	IOB attribute register	0x0000
IOB_STS	R	0x0030	IOB input status register	--
IOC_OEN	R/W	0x0040	IOC output enable register	0xFFFF
IOC_IE	R/W	0x0044	IOC input enable register	0xFFFF
IOC_DAT	R/W	0x0048	IOC data register	0x0000
IOC_ATT	R/W	0x004C	IOC attribute register	0x0000
IOC_STS	R	0x0050	IOC input status register	--
IOD_OEN	R/W	0x0060	IOD output enable register	0xFFFF
IOD_IE	R/W	0x0064	IOD input enable register	0xFFFF
IOD_DAT	R/W	0x0068	IOD data register	0x0000
IOD_ATT	R/W	0x006C	IOD attribute register	0x0000
IOD_STS	R	0x0070	IOD input status register	--
IOE_OEN	R/W	0x0080	IOE output enable register	0xFFFF
IOE_IE	R/W	0x0084	IOE input enable register	0xFFFF
IOE_DAT	R/W	0x0088	IOE data register	0x0000
IOE_ATT	R/W	0x008C	IOE attribute register	0x0000
IOE_STS	R	0x0090	IOE input status register	--

IOF_OEN	R/W	0x00A0	IOF output enable register	0x3
IOF_IE	R/W	0x00A4	IOF input enable register	0x3
IOF_DAT	R/W	0x00A8	IOF data register	0x0
IOF_ATT	R/W	0x00AC	IOF attribute register	0x0
IOF_STS	R	0x00B0	IOF input status register	--
IOB_SEL	R/W	0x00C0	IOB special function select register	0x00
IOE_SEL	R/W	0x00CC	IOE special function select register	0x00
IO_MISC	R/W	0x00E0	IO misc. control register	0x00

4.1.6. DMA Register Location

Table 4-7 Register Location of DMA Controller (DMA Base: 0x40010000)

Name	Type	Address	Description	Default
DMA_IE	R/W	0x0000	DMA interrupt enable register	0x000
DMA_STS	R/W	0x0004	DMA status register	0x0000
DMA_C0CTL	R/W	0x0010	DMA channel 0 control register	0x00000000
DMA_C0SRC	R/W	0x0014	DMA channel 0 source register	0x00000000
DMA_C0DST	R/W	0x0018	DMA channel 0 destination register	0x00000000
DMA_C0LEN	R	0x001C	DMA channel 0 transfer length register	0x0000
DMA_C1CTL	R/W	0x0020	DMA channel 1 control register	0x00000000
DMA_C1SRC	R/W	0x0024	DMA channel 1 source register	0x00000000
DMA_C1DST	R/W	0x0028	DMA channel 1 destination register	0x00000000
DMA_C1LEN	R	0x002C	DMA channel 1 transfer length register	0x0000
DMA_C2CTL	R/W	0x0030	DMA channel 2 control register	0x00000000
DMA_C2SRC	R/W	0x0034	DMA channel 2 source register	0x00000000
DMA_C2DST	R/W	0x0038	DMA channel 2 destination register	0x00000000
DMA_C2LEN	R	0x003C	DMA channel 2 transfer length register	0x0000
DMA_C3CTL	R/W	0x0040	DMA channel 3 control register	0x00000000
DMA_C3SRC	R/W	0x0044	DMA channel 3 source register	0x00000000
DMA_C3DST	R/W	0x0048	DMA channel 3 destination register	0x00000000
DMA_C3LEN	R	0x004C	DMA channel 3 transfer length register	0x0000

DMA_AESCTL	R/W	0x0050	DMA AES control register	0x00000000
DMA_AESKEY0	R/W	0x0060	DMA AES key 0 register	0x00000000
DMA_AESKEY1	R/W	0x0064	DMA AES key 1 register	0x00000000
DMA_AESKEY2	R/W	0x0068	DMA AES key 2 register	0x00000000
DMA_AESKEY3	R/W	0x006C	DMA AES key 3 register	0x00000000
DMA_AESKEY4	R/W	0x0070	DMA AES key 4 register	0x00000000
DMA_AESKEY5	R/W	0x0074	DMA AES key 5 register	0x00000000
DMA_AESKEY6	R/W	0x0078	DMA AES key 6 register	0x00000000
DMA_AESKEY7	R/W	0x007C	DMA AES key 7 register	0x00000000

4.1.7. UART Register Location

Table 4-8 Register Location of UART Controller (UART Base: 0x40011800)

Name	Type	Address	Description	Default
UART0_DATA	R/W	0x0000	UART0 data register	0x00
UART0_STATE	R/C	0x0004	UART0 status register	0x00
UART0_CTRL	R/W	0x0008	UART0 control register	0x000
UART0_INTSTS	R/C	0x000C	UART0 interrupt status register	0x00
UART0_BAUDDIV	R/W	0x0010	UART0 baud rate divide register	0x00000
UART0_CTRL2	R/W	0x0014	UART0 control register 2	0x0
UART1_DATA	R/W	0x0020	UART1 data register	0x00
UART1_STATE	R/C	0x0024	UART1 status register	0x00
UART1_CTRL	R/W	0x0028	UART1 control register	0x000
UART1_INTSTS	R/C	0x002C	UART1 interrupt status register	0x00
UART1_BAUDDIV	R/W	0x0030	UART1 baud rate divide register	0x00000
UART1_CTRL2	R/W	0x0034	UART1 control register 2	0x0
UART2_DATA	R/W	0x0040	UART2 data register	0x00
UART2_STATE	R/C	0x0044	UART2 status register	0x00
UART2_CTRL	R/W	0x0048	UART2 control register	0x000
UART2_INTSTS	R/C	0x004C	UART2 interrupt status register	0x00
UART2_BAUDDIV	R/W	0x0050	UART2 baud rate divide register	0x00000

UART2_CTRL2	R/W	0x0054	UART2 control register 2	0x0
UART3_DATA	R/W	0x0060	UART3 data register	0x00
UART3_STATE	R/C	0x0064	UART3 status register	0x00
UART3_CTRL	R/W	0x0068	UART3 control register	0x000
UART3_INTSTS	R/C	0x006C	UART3 interrupt status register	0x00
UART3_BAUDDIV	R/W	0x0070	UART3 baud rate divide register	0x00000
UART3_CTRL2	R/W	0x0074	UART3 control register 2	0x0
UART4_DATA	R/W	0x0080	UART4 data register	0x00
UART4_STATE	R/C	0x0084	UART4 status register	0x00
UART4_CTRL	R/W	0x0088	UART4 control register	0x000
UART4_INTSTS	R/C	0x008C	UART4 interrupt status register	0x00
UART4_BAUDDIV	R/W	0x0090	UART4 baud rate divide register	0x00000
UART4_CTRL2	R/W	0x0094	UART4 control register 2	0x0
UART5_DATA	R/W	0x00A0	UART5 data register	0x00
UART5_STATE	R/C	0x00A4	UART5 status register	0x00
UART5_CTRL	R/W	0x00A8	UART5 control register	0x000
UART5_INTSTS	R/C	0x00AC	UART5 interrupt status register	0x00
UART5_BAUDDIV	R/W	0x00B0	UART5 baud rate divide register	0x00000
UART5_CTRL2	R/W	0x00B4	UART5 control register 2	0x0

4.1.8. UART 32K Register Location

Table 4-9 Register Location of UART 32K Controller (UART 32K 0 Base: 0x40014100)

Name	Type	Address	Description	Default
U32K0_CTRL0	R/W	0x0000	UART 32K 0 control register 0	0x00
U32K0_CTRL1	R/W	0x0004	UART 32K 0 control register 1	0x00
U32K0_PHASE	R/W	0x0008	UART 32K 0 baud rate control register	0x4B00
U32K0_DATA	R	0x000C	UART 32K 0 receive data buffer	--
U32K0_STS	R/C	0x0010	UART 32K 0 interrupt status register	0x00
U32K1_CTRL0	R/W	0x0080	UART 32K 1 control register 0	0x00
U32K1_CTRL1	R/W	0x0084	UART 32K 1 control register 1	0x00

U32K1_PHASE	R/W	0x0088	UART 32K 1 baud rate control register	0x4B00
U32K1_DATA	R	0x008C	UART 32K 1 receive data buffer	--
U32K1_STS	R/C	0x0090	UART 32K 1 interrupt status register	0x00

4.1.9. ISO7816 Register Location

Table 4-10 Register Location of ISO7816 Controller (ISO7816 Base: 0x40012000)

Name	Type	Address	Description	Default
ISO78160_BAUDDIVL	R/W	0x0004	ISO78160 baud-rate low byte register	0x00
ISO78160_BAUDDIVH	R/W	0x0008	ISO78160 baud-rate high byte register	0x00
ISO78160_DATA	R/W	0x000C	ISO78160 data register	0x00
ISO78160_INFO	R/C	0x0010	ISO78160 information register	0x00
ISO78160_CFG	R/W	0x0014	ISO78160 control register	0x00
ISO78160_CLK	R/W	0x0018	ISO78160 clock divider control register	0x00
ISO78161_BAUDDIVL	R/W	0x0044	ISO78161 baud-rate low byte register	0x00
ISO78161_BAUDDIVH	R/W	0x0048	ISO78161 baud-rate high byte register	0x00
ISO78161_DATA	R/W	0x004C	ISO78161 data register	0x00
ISO78161_INFO	R/C	0x0050	ISO78161 information register	0x00
ISO78161_CFG	R/W	0x0054	ISO78161 control register	0x00
ISO78161_CLK	R/W	0x0058	ISO78161 clock divider control register	0x00

4.1.10. TIMER/PWM Register Location

Table 4-11 Register Location of 32b TIMER Controller (32b TIMER Base: 0x40012800)

Name	Type	Address	Description	Default
TMR0_CTRL	R/W	0x0000	Timer 0’s control register	0x0
TMR0_VALUE	R/W	0x0004	Timer 0’s current count register	0x00000000
TMR0_RELOAD	R/W	0x0008	Timer 0’s reload register	0x00000000
TMR0_INT	R/C	0x000C	Timer 0’s interrupt status register	0x0
TMR1_CTRL	R/W	0x0020	Timer 1’s control register	0x0
TMR1_VALUE	R/W	0x0024	Timer 1’s current count register	0x00000000

TMR1_RELOAD	R/W	0x0028	Timer 1's reload register	0x00000000
TMR1_INT	R/C	0x002C	Timer 1's interrupt status register	0x0
TMR2_CTRL	R/W	0x0040	Timer 2's control register	0x0
TMR2_VALUE	R/W	0x0044	Timer 2's current count register	0x00000000
TMR2_RELOAD	R/W	0x0048	Timer 2's reload register	0x00000000
TMR2_INT	R/C	0x004C	Timer 2's interrupt status register	0x0
TMR3_CTRL	R/W	0x0060	Timer 3's control register	0x0
TMR3_VALUE	R/W	0x0064	Timer 3's current count register	0x00000000
TMR3_RELOAD	R/W	0x0068	Timer 3's reload register	0x00000000
TMR3_INT	R/C	0x006C	Timer 3's interrupt status register	0x0

Table 4-12 Register Location of 16b PWM TIMER Controller (16-bit PWM TIMER Base: 0x40012900)

Name	Type	Address	Description	Default
PWM0_CTL	R/W	0x0000	PWM Timer 0's control register	0x00
PWM0_TAR	R	0x0004	PWM Timer 0's current count register	0x0000
PWM0_CCTL0	R/W	0x0008	PWM Timer 0's compare control register 0	0x000
PWM0_CCTL1	R/W	0x000C	PWM Timer 0's compare control register 1	0x000
PWM0_CCTL2	R/W	0x0010	PWM Timer 0's compare control register 2	0x000
PWM0_CCR0	R/W	0x0014	PWM Timer 0's compare data register 0	0x0000
PWM0_CCR1	R/W	0x0018	PWM Timer 0's compare data register 1	0x0000
PWM0_CCR2	R/W	0x001C	PWM Timer 0's compare data register 2	0x0000
PWM1_CTL	R/W	0x0020	PWM Timer 1's control register	0x00
PWM1_TAR	R	0x0024	PWM Timer 1's current count register	0x0000
PWM1_CCTL0	R/W	0x0028	PWM Timer 1's compare control register 0.	0x000
PWM1_CCTL1	R/W	0x002C	PWM Timer 1's compare control register 1	0x000
PWM1_CCTL2	R/W	0x0030	PWM Timer 1's compare control register 2	0x000
PWM1_CCR0	R/W	0x0034	PWM Timer 1's compare data register 0	0x0000
PWM1_CCR1	R/W	0x0038	PWM Timer 1's compare data register 1	0x0000
PWM1_CCR2	R/W	0x003C	PWM Timer 1's compare data register 2	0x0000
PWM2_CTL	R/W	0x0040	PWM Timer 2's control register	0x00

PWM2_TAR	R	0x0044	PWM Timer 2's current count register	0x0000
PWM2_CCTL0	R/W	0x0048	PWM Timer 2's compare control register 0	0x000
PWM2_CCTL1	R/W	0x004C	PWM Timer 2's compare control register 1	0x000
PWM2_CCTL2	R/W	0x0050	PWM Timer 2's compare control register 2	0x000
PWM2_CCR0	R/W	0x0054	PWM Timer 2's compare data register 0	0x0000
PWM2_CCR1	R/W	0x0058	PWM Timer 2's compare data register 1	0x0000
PWM2_CCR2	R/W	0x005C	PWM Timer 2's compare data register 2	0x0000
PWM3_CTL	R/W	0x0060	PWM Timer 3's control register	0x00
PWM3_TAR	R	0x0064	PWM Timer 3's current count register	0x0000
PWM3_CCTL0	R/W	0x0068	PWM Timer 3's compare control register 0	0x000
PWM3_CCTL1	R/W	0x006C	PWM Timer 3's compare control register 1	0x000
PWM3_CCTL2	R/W	0x0070	PWM Timer 3's compare control register 2	0x000
PWM3_CCR0	R/W	0x0074	PWM Timer 3's compare data register 0	0x0000
PWM3_CCR1	R/W	0x0078	PWM Timer 3's compare data register 1	0x0000
PWM3_CCR2	R/W	0x007C	PWM Timer 3's compare data register 2	0x0000
PWM_O_SEL	R/W	0x00F0	PWM output selection register	0xDB51

4.1.11. LCD Register Location

Table 4-13 Register Location of LCD Controller (LCD Base: 0x40002000)

Name	Type	Address	Description	Default
LCD_FB00	R/W	0x0000	LCD Frame buffer 0 register	--
LCD_FB01	R/W	0x0004	LCD Frame buffer 1 register	--
LCD_FB02	R/W	0x0008	LCD Frame buffer 2 register	--
LCD_FB03	R/W	0x000C	LCD Frame buffer 3 register	--
LCD_FB04	R/W	0x0010	LCD Frame buffer 4 register	--
LCD_FB05	R/W	0x0014	LCD Frame buffer 5 register	--
LCD_FB06	R/W	0x0018	LCD Frame buffer 6 register	--
LCD_FB07	R/W	0x001C	LCD Frame buffer 7 register	--
LCD_FB08	R/W	0x0020	LCD Frame buffer 8 register	--
LCD_FB09	R/W	0x0024	LCD Frame buffer 9 register	--

LCD_FB0A	R/W	0x0028	LCD Frame buffer 10 register	--
LCD_FB0B	R/W	0x002C	LCD Frame buffer 11 register	--
LCD_FB0C	R/W	0x0030	LCD Frame buffer 12 register	--
LCD_FB0D	R/W	0x0034	LCD Frame buffer 13 register	--
LCD_FB0E	R/W	0x0038	LCD Frame buffer 14 register	--
LCD_FB0F	R/W	0x003C	LCD Frame buffer 15 register	--
LCD_FB10	R/W	0x0040	LCD Frame buffer 16 register	--
LCD_FB11	R/W	0x0044	LCD Frame buffer 17 register	--
LCD_FB12	R/W	0x0048	LCD Frame buffer 18 register	--
LCD_FB13	R/W	0x004C	LCD Frame buffer 19 register	--
LCD_FB14	R/W	0x0050	LCD Frame buffer 20 register	--
LCD_FB15	R/W	0x0054	LCD Frame buffer 21 register	--
LCD_FB16	R/W	0x0058	LCD Frame buffer 22 register	--
LCD_FB17	R/W	0x005C	LCD Frame buffer 23 register	--
LCD_FB18	R/W	0x0060	LCD Frame buffer 24 register	--
LCD_FB19	R/W	0x0064	LCD Frame buffer 25 register	--
LCD_FB1A	R/W	0x0068	LCD Frame buffer 26 register	--
LCD_FB1B	R/W	0x006C	LCD Frame buffer 27 register	--
LCD_FB1C	R/W	0x0070	LCD Frame buffer 28 register	--
LCD_FB1D	R/W	0x0074	LCD Frame buffer 29 register	--
LCD_FB1E	R/W	0x0078	LCD Frame buffer 30 register	--
LCD_FB1F	R/W	0x007C	LCD Frame buffer 31 register	--
LCD_FB20	R/W	0x0080	LCD Frame buffer 32 register	--
LCD_FB21	R/W	0x0084	LCD Frame buffer 33 register	--
LCD_FB22	R/W	0x0088	LCD Frame buffer 34 register	--
LCD_FB23	R/W	0x008C	LCD Frame buffer 35 register	--
LCD_FB24	R/W	0x0090	LCD Frame buffer 36 register	--
LCD_FB25	R/W	0x0094	LCD Frame buffer 37 register	--
LCD_FB26	R/W	0x0098	LCD Frame buffer 38 register	--
LCD_FB27	R/W	0x009C	LCD Frame buffer 39 register	--

LCD_CTRL	R/W	0x0100	LCD control register	0x00
LCD_CTRL2	R/W	0x0104	LCD control register 2	0x0000
LCD_SEGCTRL0	R/W	0x0108	LCD segment enable control register 0	0x00000000
LCD_SEGCTRL1	R/W	0x010C	LCD segment enable control register 1	0x00000000
LCD_SEGCTRL2	R/W	0x0110	LCD segment enable control register 2	0x00000000

4.1.12. SPI Register Location

Table 4-14 Register Location of SPI1 Controller (SPI1 Base: 0x40011000)

Name	Type	Address	Description	Default
SPI1_CTRL	R/W	0x0000	SPI1 Control Register	0x0000
SPI1_TXSTS	R/W	0x0004	SPI1 Transmit Status Register	0x8200
SPI1_TXDAT	R/W	0x0008	SPI1 Transmit FIFO register	--
SPI1_RXSTS	R/W	0x000C	SPI1 Receive Status Register	0x0000
SPI1_RXDAT	R	0x0010	SPI1 Receive FIFO Register	--
SPI1_MISC	R/W	0x0014	SPI1 Misc. Control Register	0x0003

Table 4-15 Register Location ofSPI2 Controller (SPI2 Base: 0x40015800)

Name	Type	Address	Description	Default
SPI2_CTRL	R/W	0x0000	SPI2 Control Register	0x0000
SPI2_TXSTS	R/W	0x0004	SPI2 Transmit Status Register	0x8200
SPI2_TXDAT	R/W	0x0008	SPI2 Transmit FIFO register	--
SPI2_RXSTS	R/W	0x000C	SPI2 Receive Status Register	0x0000
SPI2_RXDAT	R	0x0010	SPI2 Receive FIFO Register	--
SPI2_MISC	R/W	0x0014	SPI2 Misc. Control Register	0x0003

4.1.13. I2C Register Location

Table 4-16 Register Location of I2C Controller (I2C Base: 0x40010800)

Name	Type	Address	Description	Default
I2C_DATA	R/W	0x0000	I2C data register	0x00
I2C_ADDR	R/W	0x0004	I2C address register	0x00

I2C_CTRL	R/W	0x0008	I2C control/status register	0x00
I2C_STS	R/W	0x000c	I2C status register	0xF8
I2C_CTRL2	R/W	0x0018	I2C interrupt enable register	0x0

4.1.14. MISC Register Location

Table 4-17 Register Location of MISC Controller (MISC Base: 0x40013000)

Name	Type	Address	Description	Default
MISC_SRAMINT	R/C	0x0000	SRAM parity error Interrupt	0x00
MISC_SRAMINIT	R/W	0x0004	SRAM initialize register	0x01
MISC_PARERR	R	0x0008	SRAM parity error address register	0x0000
MISC_IREN	R/W	0x000C	IR enable control register	0x00
MISC_DUTYL	R/W	0x0010	IR duty low pulse control register	0x0000
MISC_DUTYH	R/W	0x0014	IR Duty high pulse control register	0x0000
MISC_IRQLAT	R/W	0x0018	Cortex-M0 IRQ latency control register	0x00
MISC_HIADDR	R	0x0020	AHB invalid access address	--
MISC_PIADDR	R	0x0024	APB invalid access address	--

Table 4-18 Register Location of MISC2 Controller (MISC2 Base: 0x40013E00)

Name	Type	Address	Description	Default
MISC2_FLASHWC	R/W	0x0000	FLASH wait cycle register	0x2100
MISC2_CLKSEL	R/W	0x0004	Clock selection register	0x0
MISC2_CLKDIVH	R/W	0x0008	AHB clock divider control register	0x00
MISC2_CLKDIVP	R/W	0x000C	APB clock divider control register	0x01
MISC2_HCLKEN	R/W	0x0010	AHB clock enable control register	0x1FF
MISC2_PCLKEN	R/W	0x0014	APB clock enable control register	0xFFFFFFFF

4.1.15. CRYPT Register Location

Table 4-19 Register Location of CRYPT Controller (MISC Base: 0x40006000)

Name	Type	Address	Description	Default
CRYPT_CTRL	R/W	0x0000	CRYPT control register	0x0000

CRYPT_PTRA	R/W	0x0004	CRYPT pointer A	0x0000
CRYPT_PTRB	R/W	0x0008	CRYPT pointer B	0x0000
CRYPT_PTRO	R/W	0x000C	CRYPT pointer O	0x0000
CRYPT_CARRY	R	0x0010	CRYPT carry/borrow bit register	0x0

4.1.16. Info Information Register

The analog trim data and boot option is stored in Info Sector 6 (0x40C00); the RTC calibration data is stored in Info Sector 4 (0x40800). The address 0x40800 ~ 0x409FF data is written by SP606 tool (offline download and RTC calibration). Other data is written before leaving factory. The following table shows the details of this information.

Info Sector data can only be read and cannot be written. All information has a backup. The first data in the form is expressed in 1, and second copies in 2. Each data has a checksum data. Checksum algorithm: add up each data, and reverse the result.

Table 4-20 Info Information Register

Address	Sign	Data	Description
0x00040800	P4	RTC normal temperature offset 1	Load low 16 bits to RTC_ACP4 register, such as 0. (Unit: 0.1ppm).
0x00040804		Check sum 1	INV (SUM (0x40800, 0x40800))
0x00040808	P4	RTC normal temperature offset 2	Load low 16 bits to RTC_ACP4 register, such as 0. (Unit: 0.1ppm).
0x0004080C		Check sum 2	INV (SUM (0x40808, 0x40808))
0x00040810	K1	Crystal secondary calibration coefficient K1 1	Load to RTC_ACK1 register. K1 is calculated as follows: K1=B1/1000000*65536, B1 is the segment factor of crystal oscillator' quadratic curve. For example, the value of K1 is 20827.
0x00040814	K2	Crystal secondary calibration coefficient K2 1	Load to RTC_ACK2 register. K2 is calculated as follows: K2=B2/1000000*65536, B2 is the segment factor of crystal oscillator' quadratic curve. For example, the value of K2 is 21496.
0x00040818	K3	Crystal secondary calibration coefficient K3 1	Load to RTC_ACK3 register. K3 is calculated as follows: K3=B3/1000000*65536, B3 is the segment factor of crystal oscillator' quadratic curve. For example, the value of K3 is 22020.
0x0004081C	K4	Crystal secondary calibration coefficient K4 1	Load to RTC_ACK4 register. K4 is calculated as follows: K4=B4/1000000*65536, B4 is the segment factor of crystal oscillator' quadratic curve. For example, the

			value of K4 is 24517.
0x00040820	K5	Crystal secondary calibration coefficient K5 1	Load to RTC_ACK5 register. K5 is calculated as follows: K5=B5/1000000*65536, B5 is the segment factor of crystal oscillator' quadratic curve. For example, the value of K5 is 25257.
0x00040824		Check sum 1	INV (SUM (0x40810, 0x40820))
0x00040828	K1	Crystal secondary calibration coefficient K1 2	Load to RTC_ACK1 register. K1 is calculated as follows: K1=B1/1000000*65536, B1 is the segment factor of crystal oscillator' quadratic curve. For example, the value of K1 is 20827.
0x0004082C	K2	Crystal secondary calibration coefficient K2 2	Load to RTC_ACK2 register. K2 is calculated as follows: K2=B2/1000000*65536, B2 is the segment factor of crystal oscillator' quadratic curve. For example, the value of K2 is 21496.
0x00040830	K3	Crystal secondary calibration coefficient K3 2	Load to RTC_ACK3 register. K3 is calculated as follows: K3=B3/1000000*65536, B3 is the segment factor of crystal oscillator' quadratic curve. For example, the value of K3 is 22020.
0x00040834	K4	Crystal secondary calibration coefficient K4 2	Load to RTC_ACK4 register. K4 is calculated as follows: K4=B4/1000000*65536, B4 is the segment factor of crystal oscillator' quadratic curve. For example, the value of K4 is 24517.
0x00040838	K5	Crystal secondary calibration coefficient K5 2	Load to RTC_ACK5 register. K5 is calculated as follows: K5=B5/1000000*65536, B5 is the segment factor of crystal oscillator' quadratic curve. For example, the value of K5 is 25257.
0x0004083C		Check sum 2	INV (SUM (0x40828, 0x40838))
0x00040840	ACTI	Fixed point temperature of crystal 1	Load to RTC_ACTI register, such as 0x1800
0x00040844		Check sum 1	INV (SUM (0x40840, 0x40840))
0x00040848	ACTI	Fixed point temperature of crystal 2	Load to RTC_ACTI register, such as 0x1800
0x0004084C		Check sum 2	INV (SUM (0x40848, 0x40848))
0x00040850	KTEMP x(x=4 ~1)	Temperature section division settings 1	Load to RTC_ACKTEMP register, such as 0x3C2800EC
0x00040854		Check sum 1	INV (SUM (0x40850, 0x40850))

0x00040858	KTEMP x(x=4 ~1)	Temperature section division settings 2	Load to RTC_ACKTEMP register, such as 0x3C2800EC
0x0004085C		Check sum 2	INV (SUM (0x40858, 0x40858))
…			Reserved.
0x00040CE0		BAT_R offset 1	(3.6-BAT measure result) * 1000, resister division
0x00040CE4		BAT_C offset 1	(3.6-BAT measure result) * 1000, cap division
0x00040CE8		Check sum 1	INV (SUM (0x40CE0, 0x40CE4))
0x00040CEC			Reserved.
0x00040CF0		BAT_R offset 2	(3.6-BAT measure result) * 1000, resister division
0x00040CF4		BAT_C offset 2	(3.6-BAT measure result) * 1000, cap division
0x00040CF8		Check sum 2	INV (SUM (0x40CF0, 0x40CF4))
0x00040CFC			Reserved.
0x00040D00	P1/P0	RTC_ACP1/0 set 1	Load the high 16 bits to RTC_ACP1 register, such as 1060; Load the low 16 bits to RTC_ACP0, such as -214.
0x00040D04	P2′	RTC_ACP2 set 1	The value in this register is recorded as P2′, such as -19746971. According to the formula P2=P2′+(Tr-Tm)*256 to calculate P2, and load P2 to RTC_ACP2 register.
0x00040D08	P5	RTC_ACP5 set 1	Load the high 16 bits to RTC_ACP5 register, such as 6444 and the low 16 bits are abandoned.
0x00040D0C	P7/P6′	RTC_ACP 7/6 set 1	Load the high 16 bits to RTC_ACP7 register, such as 0. Load the low 16 bits to P6′ register, such as 1342. According to the formula: P6=a*P6′ to calculate P6, where a=PCLK/6553600.
0x00040D10		Check Sum set 1	INV (SUM (0x40DE0, 0x40DEC))
0x00040D14	P1/P0	RTC_ACP1/0 set 2	Load the high 16 bits to RTC_ACP1 register, such as 1060; Load the low 16 bits to RTC_ACP0, such as -214.
0x00040D18	P2′	RTC_ACP2 set 2	The value in this register is recorded as P2′, such as -19746971. According to the formula P2=P2′+(Tr-Tm)*256 to calculate P2, and load P2 to RTC_ACP2 register.
0x00040D1C	P5	RTC_ACP5 set 2	Load the high 16 bits to RTC_ACP5 register, such as

			6444 and the low 16 bits are abandoned.
0x00040D20	P7/P6′	RTC_ACP 7/6 set 2	Load the high 16 bits to RTC_ACP7 register, such as 0; Load the low 16 bits to P6′ register, such as 1342. According to the formula: P6=a*P6′ to calculate P6, where a=PCLK/6553600.
0x00040D24		Check Sum set 2	INV (SUM (0x40DF4, 0x40E00))
0x00040D28		AVCC gain 1	Pre-trim result/3.3 * 10000
0x00040D2C		DVCC gain 1	Pre-trim result/3.3 * 10000
0x00040D30		BGP gain 1	Pre-trim result/1.2 * 10000
0x00040D34		RCL gain 1	Pre-trim result/32768 * 10000
0x00040D38		RCH gain 1	Pre-trim result/6553600 * 10000
0x00040D3C		Check sum 1	INV(SUM(0x40D28, 0x40D38))
0x00040D40		AVCC gain 2	Pre-trim result/3.3 * 10000
0x00040D44		DVCC gain 2	Pre-trim result/3.3 * 10000
0x00040D48		BGP gain 2	Pre-trim result/1.2 * 10000
0x00040D4C		RCL gain 2	Pre-trim result/32768 * 10000
0x00040D50		RCH gain 2	Pre-trim result/6553600 * 10000
0x00040D54		Check sum 2	INV(SUM(0x40D40, 0x40D50))
0x00040D58		ID word 0, Backup 1	
0x00040D5C		ID word 1, Backup 1	
0x00040D60		ID Check sum 1	INV (SUM (0x40D58, 0x40D5C))
0x00040D64		ID word 0, Backup 2	
0x00040D68		ID word 1, Backup 2	
0x00040D6C		ID Check sum 2	INV (SUM (0x40D64, 0x40D68))
0x00040D70	Tr	Real Temperature 1 (from tmp275)	According to the formula P2=P2′+(Tr-Tm)*256 to calculate P2, and load P2 to RTC_ACP2 register.
0x00040D74	Tm	Measure Temperature 1 (from ADC)	
0x00040D78		Temp Check sum 1	INV(SUM(0x40D70, 0x40D74))
0x00040D7C	Tr	Real Temperature 2 (from tmp275)	According to the formula P2=P2′+(Tr-Tm)*256 to calculate P2, and load P2 to RTC_ACP2 register.
0x00040D80	Tm	Measure Temperature 2 (from ADC)	

0x00040D84		Temp Check sum 2	INV (SUM (0x40D7C, 0x40D80))
0x00040D88			Reserved.
0x00040D8C			Reserved.
0x00040D90		Measure LCD LDO gain 1	Pre-trim result/3.3 * 10000
0x00040D94		VLCD setting 1	
0x00040D98		LCD LDO Check sum 1	INV (SUM (0x40D90, 0x40D94))
0x00040D9C		Measure LCD LDO gain 2	Pre-trim result/3.3 * 10000
0x00040DA0		VLCD setting 2	
0x00040DA4		LCD LDO Check sum 2	INV (SUM (0x40D9C, 0x40DA0))
0x00040DC0		Analog trim data1	Program during CP flow for analog parameter
0x00040DC4		0xFFFFFFFF	
0x00040DC8		0xFFFFFFFF	
0x00040DCC		Checksum1	INV (SUM (0x40DC0, 0x40DC8)), the data of 0x00040DC8 address is replaced by 0xFFFFFFFF.
0x00040DD0		Analog trim data2.	Program during CP flow for analog parameter
0x00040DD4		0xFFFFFFFF	
0x00040DD8		0xFFFFFFFF	
0x00040DDC		Checksum2	INV (SUM (0x40DD0, 0x40DD8)), the data of 0x00040DD8 address is replaced by 0xFFFFFFFF.
…			
0x00040400	a1	ADC coefficient 1 of ADC_CHx channel in 3.3V system under no divider mode condition	Vdc=a1/100000000*X+b1/100000000 (32 bits complement)
0x00040404	b1		
0x00040408	a2	ADC coefficient 1 of ADC_CHx channel in 3.3V system under resistive divider mode condition	Vdc=a2/100000000*X+b2/100000000 (32 bits complement)
0x0004040C	b2		
0x00040410	a3	ADC coefficient 1 of ADC_CHx channel in 3.3V system under	Vdc=a3/100000000*X+b3/100000000 (32 bits complement)
0x00040414	b3		

		capacitive divider mode condition	
0x00040418	a4	ADC coefficient 1 of VDD channel in 3.3V system under resistive divider mode condition	Vdc=a4/100000000*X+b4/100000000 (32 bits complement)
0x0004041C	b4		
0x00040420	a5	ADC coefficient 1 of VDD channel in 3.3V system under capacitive divider mode condition	Vdc=a5/100000000*X+b5/100000000 (32 bits complement)
0x00040424	b5		
0x00040428	a6	ADC coefficient 1 of BATRTC channel in 3.3V system under resistive divider mode condition	Vdc=a6/100000000*X+b6/100000000 (32 bits complement)
0x0004042C	b6		
0x00040430	a7	ADC coefficient 1 of BATRTC channel in 3.3V system under capacitive divider mode condition	Vdc=a7/100000000*X+b7/100000000 (32 bits complement)
0x00040434	b7		
0x00040438		Checksum1	INV(SUM(0x00040400, 0x00040434))
0x0004043C			Reserved.
0x00040440	a1	ADC coefficient 2 of ADC_CHx channel in 3.3V system under no divider mode condition	Vdc=a1/100000000*X+b1/100000000 (32 bits complement)
0x00040444	b1		
0x00040448	a2	ADC coefficient 2 of ADC_CHx channel in 3.3V system under resistive divider mode condition	Vdc=a2/100000000*X+b2/100000000 (32 bits complement)
0x0004044C	b2		
0x00040450	a3	ADC coefficient 2 of ADC_CHx channel in 3.3V system under capacitive divider mode condition	Vdc=a3/100000000*X+b3/100000000 (32 bits complement)
0x00040454	b3		
0x00040458	a4	ADC coefficient 2 of VDD channel in 3.3V	Vdc=a4/100000000*X+b4/100000000 (32 bits complement)
0x0004045C	b4		

		system under resistive divider mode condition	
0x00040460	a5	ADC coefficient 2 of VDD channel in 3.3V system under capacitive divider mode condition	Vdc=a5/100000000*X+b5/100000000 (32 bits complement)
0x00040464	b5		
0x00040468	a6	ADC coefficient 2 of BATRTC channel in 3.3V system under resistive divider mode condition	Vdc=a6/100000000*X+b6/100000000 (32 bits complement)
0x0004046C	b6		
0x00040470	a7	ADC coefficient 2 of BATRTC channel in 3.3V system under capacitive divider mode condition	Vdc=a7/100000000*X+b7/100000000 (32 bits complement)
0x00040474	b7		
0x00040478		Checksum2	INV(SUM(0x00040440, 0x00040474))
0x0004047C			Reserved.
0x00040480	A1	ADC coefficient 1 of ADC_CHx channel in 5V system under no divider mode condition	Vdc=A1/100000000*X+B1/100000000 (32 bits complement)
0x00040484	B1		
0x00040488	A2	ADC coefficient 1 of ADC_CHx channel in 5V system under resistive divider mode condition	Vdc=A2/100000000*X+B2/100000000 (32 bits complement)
0x0004048C	B2		
0x00040490	A3	ADC coefficient 1 of ADC_CHx channel in 5V system under capacitive divider mode condition	Vdc=A3/100000000*X+B3/100000000 (32 bits complement)
0x00040494	B3		
0x00040498	A4	ADC coefficient 1 of VDD channel in 5V system under resistive divider mode condition	Vdc=A4/100000000*X+B4/100000000 (32 bits complement)
0x0004049C	B4		
0x000404A0	A5	ADC coefficient 1 of	Vdc=A5/100000000*X+B5/100000000 (32 bits

0x000404A4	B5	VDD channel in 5V system under capacitive divider mode condition	complement)
0x000404A8	A6	ADC coefficient 1 of BATRTC channel in 5V system under resistive divider mode condition	Vdc=A6/100000000*X+B6/100000000 (32 bits complement)
0x000404AC	B6		
0x000404B0	A7	ADC coefficient 1 of BATRTC channel in 5V system under capacitive divider mode condition	Vdc=A7/100000000*X+B7/100000000 (32 bits complement)
0x000404B4	B7		
0x000404B8		Checksum1	INV(SUM(0x00040480, 0x000404B4))
0x000404BC			Reserved.
0x000404C0	A1	ADC coefficient 2 of ADC_CHx channel in 5V system under no divider mode condition	Vdc=A1/100000000*X+B1/100000000 (32 bits complement)
0x000404C4	B1		
0x000404C8	A2	ADC coefficient 2 of ADC_CHx channel in 5V system under resistive divider mode condition	Vdc=A2/100000000*X+B2/100000000 (32 bits complement)
0x000404CC	B2		
0x000404D0	A3	ADC coefficient 2 of ADC_CHx channel in 5V system under capacitive divider mode condition	Vdc=A3/100000000*X+B3/100000000 (32 bits complement)
0x000404D4	B3		
0x000404D8	A4	ADC coefficient 2 of VDD channel in 5V system under resistive divider mode condition	Vdc=A4/100000000*X+B4/100000000 (32 bits complement)
0x000404DC	B4		
0x000404E0	A5	ADC coefficient 2 of VDD channel in 5V system under capacitive divider mode condition	Vdc=A5/100000000*X+B5/100000000 (32 bits complement)
0x000404E4	B5		

0x000404E8	A6	ADC coefficient 2 of BATRTC channel in 5V system under resistive divider mode condition	Vdc=A6/100000000*X+B6/100000000 (32 bits complement)
0x000404EC	B6		
0x000404F0	A7	ADC coefficient 2 of BATRTC channel in 5V system under capacitive divider mode condition	Vdc=A7/100000000*X+B7/100000000 (32 bits complement)
0x000404F4	B7		
0x000404F8		Checksum2	INV(SUM(0x000404C0, 0x000404F4))

5.Power system

V85X3 power supply has the following features:

- Supporting 5.5V and 3.3V power supply;
- Supporting RTC independent battery. When RTCBAT is out of the battery power, RTC will be supplied by the main power.
- The GPIO ports are powered by VDD.
- The analog circuitry inside the chip is powered by AVCC;
- The digital circuitry inside the chip and PLL circuitry are powered by DVCC;
- Supporting low voltage monitoring and real-time monitoring battery voltage.

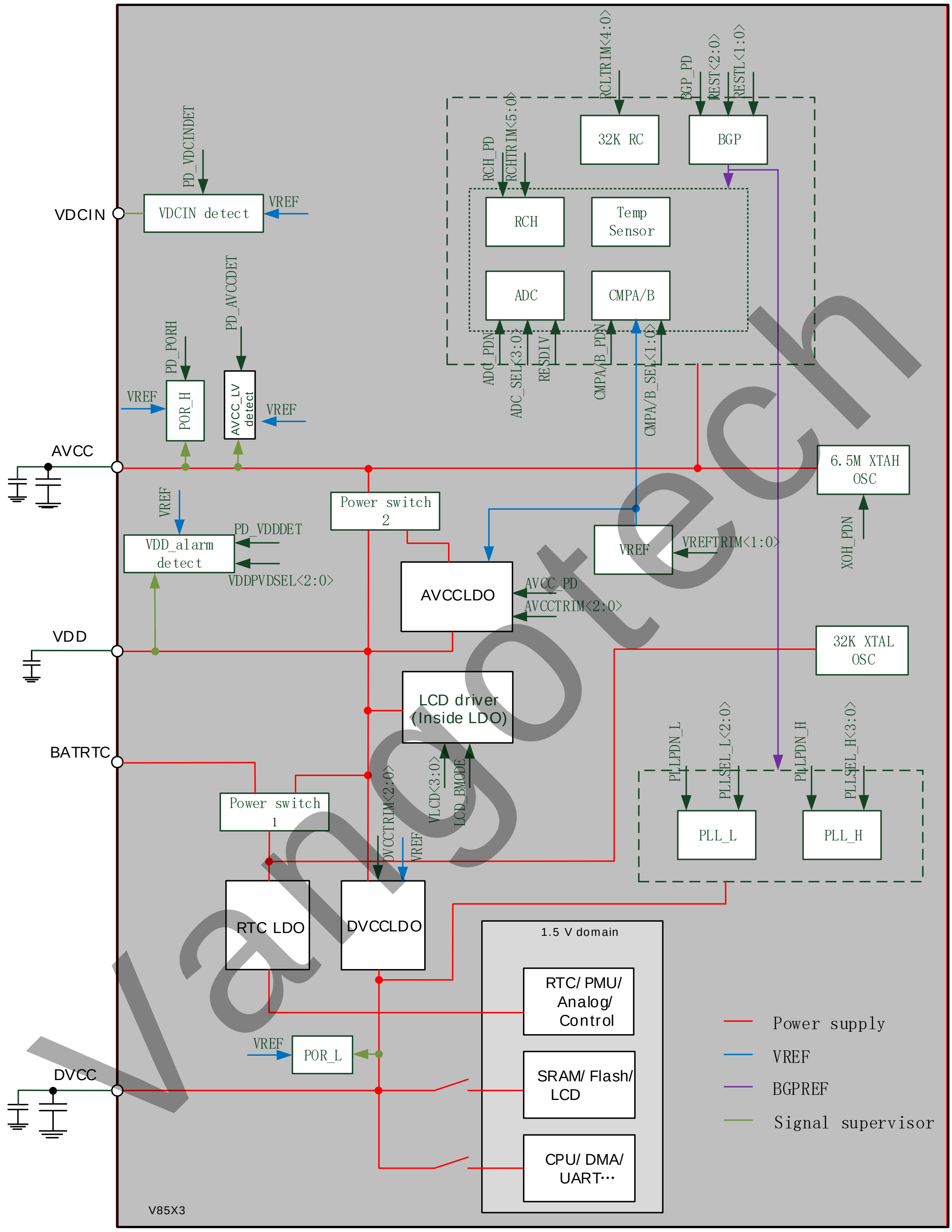


Figure 5-1 V85X3 Power System Block Diagram

5.1. Register Location

Table 5-1 Register Location of ANA Controller for Power (ANA Base: 0x40014200)

Name	Type	Address	Description	Default
ANA_REG5	R/W	0x0014	Analog register 5	0x00
ANA_REG6	R/W	0x0018	Analog register 6	0x00
ANA_REG7	R/W	0x001C	Analog register 7	0x00
ANA_REG8	R/W	0x0020	Analog register 8	0x00
ANA_REGA	R/W	0x0028	Analog register 10	0x00
ANA_REGF	R/W	0x003C	Analog register 15	0x00
ANA_CTRL	R/W	0x0050	Analog control register	0x0000000
ANA_CMPOUT	R	0x0054	Comparator result register	0x0030
ANA_INTSTS	R/C	0x0060	Analog interrupt status register	0x0000
ANA_INTEN	R/W	0x0064	Analog interrupt enable register	0x0000

5.2. Register Definition

5.2.1. ANA_REG5 Register

Table 5-2 Description of Each Bit in ANA_REG5 for Power

Bit	Name	Function	Notes
6	PD_AVCCDET	Power down AVCC low voltage detector for AVCC.	0: Power-up AVCCLV detector. 1: Power-down detector.

5.2.2. ANA_REG6 Register

Table 5-3 Description of Each Bit in ANA_REG6 for Power

Bit	Name	Function	Notes
7	BATRTCDISC	Discharge the BATRTC battery. Discharge resistance is 1.7k, and the discharge current is Vbatrtc/1.7k.	0: Disable 1.7k resistor from BATRTC to GND. 1: Enable 1.7k resistor from BATRTC to GND.

5.2.3. ANA_REG7 Register

Table 5-4 Description of Each Bit in ANA_REG7 for Power

Bit	Name	Function	Notes
7:0		Reserved.	0

5.2.4. ANA_REG8 Register

Table 5-5 Description of Each Bit in ANA_REG8 for Power

Bit	Name	Function	Notes
3:0	-	Reserved.	0
6:4	VDDPVDSEL[2:0]	Voltage selection of VDD power detector, the setting in this register will affect the status of VDDALARM.	000: 4.5V 001: 4.2V 010: 3.9V 011: 3.6V 100: 3.2V 101: 2.9V 110: 2.6V 111: 2.3V
7	PD_AVCCLDO	AVCCLDO control register, and control power-down or power-up of LDO.	0: Power up LDO, Voltage of AVCC pin is 3.3V. 1: Power down LDO, AVCC connect to VDD through a switch, and the switch resistor refer to table 1-4. AVCCLDO can be power down only when power supply less than 3.6V.

5.2.5. ANA_REG9 Register

Table 5-6 Description of Each Bit in ANA_REG9 for Power

Bit	Name	Function	Notes

7	PD_VDDDET	Power down VDD input VDDALARM detector. This module powered by VDD.	0: Power up. 1: Power down.

5.2.6. ANA_REGA Register

Table 5-7 Description of Each Bit in ANA_REGA for Power

Bit	Name	Function	Notes
6:0	-	Reserved.	Default value is 0x00, and must be set to 0x0A.
7	PD_VDCINDET	Power down VDCIN detector.	0: Power up. 1: Power down.

5.2.7. ANA_REGF Register

Table 5-8 Description of Each Bit in ANA_REGF for Power

Bit	Name	Function	Notes
1:0	-	Reserved.	0
2	AVCCO_EN	Enable AVCC_OUT pin to output AVCC level.	0: High resistance. 1: AVCC_OUT pin output AVCC level, and it can be used to drive small power module.

5.2.8. ANA_CTRL Register

Table 5-9 Description of ANA_CTRL Register for Power

Bit	Name	Type	Description	Default
26	PDNS2	R/W	This register is used to set the deep sleep behavior when VDDALARM is 0. (Still need to consider the PDNS setting). 0: Can’t enter deep-sleep mode when VDDALARM is 0. When VDDALARM is 1, the system can enter deep-sleep mode. The system will wake-up from deep-sleep mode automatically as long as VDDALARM is 0. 1: Can enter deep-sleep mode no-matter which state	0x0

			VDDALARM is.	
17:16	-	-	Reserved.	0
6	PDNS	R/W	This register is used to set the deep sleep behavior when VDCINDROP is 0. (Still need to consider the PDNS setting) 0: Can't enter deep-sleep mode when VDCINDROP is 0. When VDCINDROP is 1, the system can enter deep-sleep mode. The system will wake-up from deep-sleep mode automatically as long as VDCINDROP became 0. 1: Can enter deep-sleep mode no-matter which state VDCINDROP is.	0x0
5:4	-	-	Reserved.	0

5.2.9. ANA_CMPOUT Register

Table 5-10 Description of ANA_CMPOUT Register for Power

Bit	Name	Type	Description	Default
10	AVCCLV	R	AVCC low power status. And hysteresis voltage of AVCCLV is 20mV~30mV. 0: AVCC is higher than 2.5V. 1: AVCC is lower than 2.5V.	0x0
8	VDCINDROP	R	VDCIN drop status. 0: VDCIN is not drop (VDCIN higher than threshold). 1: VDCIN is drop (VDCIN lower than threshold).	0x0
7	VDDALARM	R	This bit shows the output of VDDALARM. 0: Voltage of VDD is higher than voltage setting by VDDPVDSEL. 1: Voltage of VDD is lower than voltage setting by VDDPVDSEL.	0x0
6:0	-	R	Reserved.	0

5.2.10. ANA_INSTS Register

Table 5-11 Description of ANA_INTSTS Register for Power

Bit	Name	Type	Description	Default
11	INTSTS11	R/C	Interrupt flag of sleep mode entry under VDCINDROP is 0(i.e. VDCIN higher than threshold), this interrupt will be generated when VDCINDROP is 0 and the entry of sleep or deep-sleep modes are detected. Programmer can enable this interrupt to force CPU awake from sleep or deep-sleep mode when VDCINDROP is 0 and the entry of sleep or deep-sleep modes are detected. Read 0: No Sleep mode entry interrupt. Read 1: Sleep mode entry interrupt is happened. Write 0: No effect. Write 1: clear this bit.	0x0
10	INTSTS10	R/C	Interrupt flag of AVCCLV (AVCC low power status), this interrupt will be generated when AVCCLV rising or falling. Read 0: No AVCCLV interrupt. Read 1: AVCCLV interrupt is happened. Write 0: No effect. Write 1: clear this bit.	0x0
8	INTSTS8	R/C	Interrupt flag of VDCINDROP (VDCIN status), this interrupt will be generated when VDCINDROP rising or falling. Read 0: No VDCIN interrupt. Read 1: VDCIN interrupt is happened. Write 0: No effect. Write 1: clear this bit.	0x0
7	INTSTS7	R/C	Interrupt flag of VDDALARM (VDD status), this interrupt will be generated when VDDALARM rising or falling. Read 0: No VDDALARM interrupt. Read 1: VDDALARM interrupt is happened. Write 0: No effect. Write 1: clear this bit.	0x0
6:0	-	-	Reserved.	0

5.2.11. ANA_INTEN Register

Table 5-12 Description of ANA_INTEN Register for Power

Bit	Name	Type	Description	Default
11	INTEN11	R/W	Interrupt and wake-up enable control of sleep mode entry, when VDCINDROP is 0 (i.e. VDCIN higher than threshold). Programmer can enable this interrupt to force CPU to wake from sleep or deep-sleep mode when VDCINDROP is 0 and the entry of sleep or deep-sleep modes are detected. 0: Disable Sleep mode entry interrupt and wake-up. 1: Enable Sleep mode entry interrupt and wake-up.	0x0
10	INTEN10	R/W	Interrupt and wake-up enable control of AVCCLV rising or falling. 0: Disable AVCCLV interrupt and wake-up. 1: Enable AVCCLV interrupt and wake-up.	0x0
9	-	-	Reserved.	0
8	INTEN8	R/W	Interrupt and wake-up enable control of VDCINDROP rising or falling. 0: Disable VDCIN interrupt and wake-up. 1: Enable VDCIN interrupt and wake-up.	0x0
7	INTEN7	R/W	Interrupt and wake-up enable control of VDDALARM rising or falling. 0: Disable VDDALARM interrupt and wake-up. 1: Enable VDDALARM interrupt and wake-up.	0x0
6:0	-	-	Reserved.	0

5.3. 3.3V Regulator Circuit (AVCC)

In V85X3, the analog circuit is powered by the 3.3V regulator circuit (AVCC). AVCC is controlled via the bit 'PD_AVCCLDO' (bit [7] of ANA_REG8). AVCCLDO can be power down only when power supply less than 3.6V.

AVCC has a driving capability of 30 mA.

AVCC can output from AVCC_OUT, and is controlled by the bit 'AVCCO_EN' (bit [2] of ANA_REGF). When AVCCO_EN=1, AVCC_OUT will output AVCC level. Otherwise, it will be in high-z state. AVCC_OUT has a driving capability of 20mA. The sum of the driving capability of AVCC pin and AVCC_OUT pin cannot exceed 30mA.

It is recommended to externally decouple the pin 'AVCC' with a 10uF capacitor in parallel with a 0.1-uF capacitor.

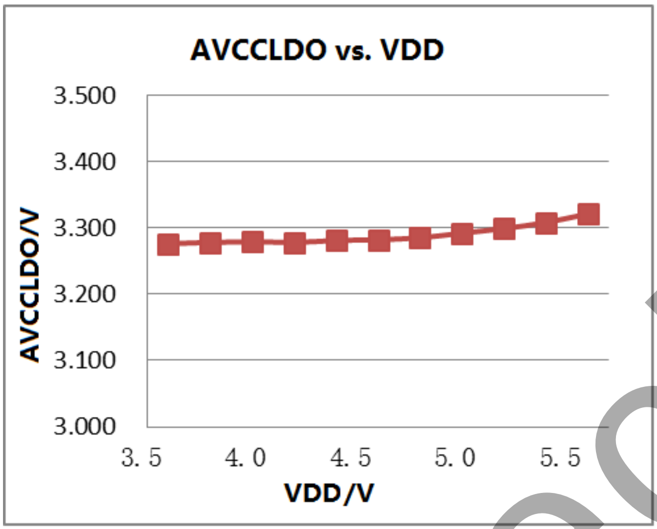


Figure 5-2 AVCCLDO Output and VDD Power Input

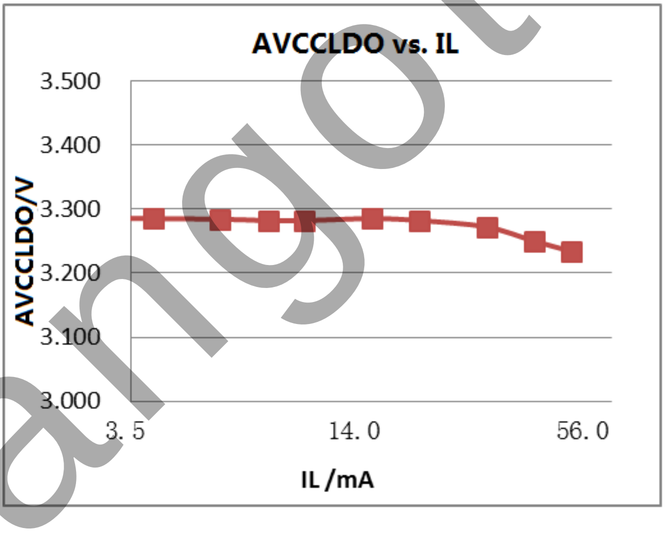


Figure 5-3 AVCCLDO Output and The Load Current

5.4. Digital Power Supply (DVCC)

In V85X3, PLL clock generation circuit and core digital blocks are powered by the digital power supply circuit. This circuit will output a stable voltage (DVCC, i.e. 1.5V) when power input (AVCC) is higher than 1.7V.

The digital power supply circuit has a driving capability of 35mA. When the load current through the circuits is less than 35mA, the digital power supply will be stable; when the load current is higher than 35mA, the higher the load current is, the lower the digital power supply will be.

This power supply circuit will not stop working until the system is powered off.

It is recommended to externally decouple the pin 'DVCC' with a 10uF capacitor in parallel with a 0.1-uF capacitor.

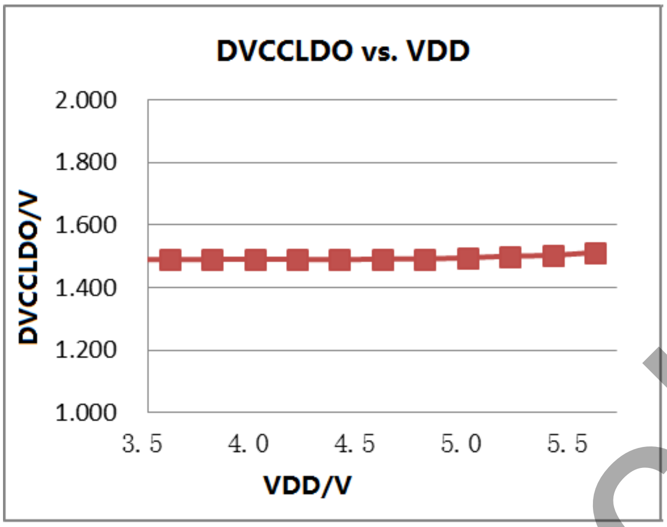


Figure 5-4 DVCCLDO Output and VDD Power Input

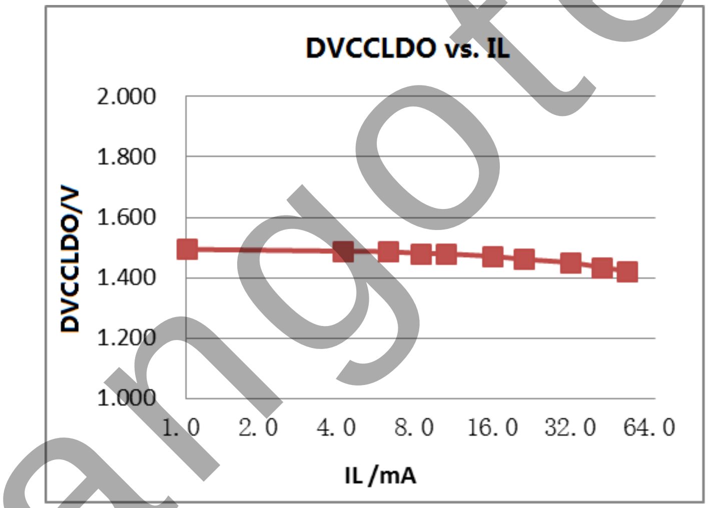


Figure 5-5 DVCCLDO Output and The Load Current

Power Supply Supervisor

5.5. Power Supervisor

5.5.1. VDCIN Supervisor

In V85X3, the main power is input into the pin 'VDCIN' after a resistive divider. The input voltage on the pin 'VDCIN' is monitored continuously by the power supply supervisor.

When the input voltage on the pin 'VDCIN' is lower than 1.3V(typical), a power-down event will occur, the bit 'VDCINDROP'('bit 8' of 'ANACMP_OUT') will be set to '1', and a power-down interrupt will be generated to MCU.

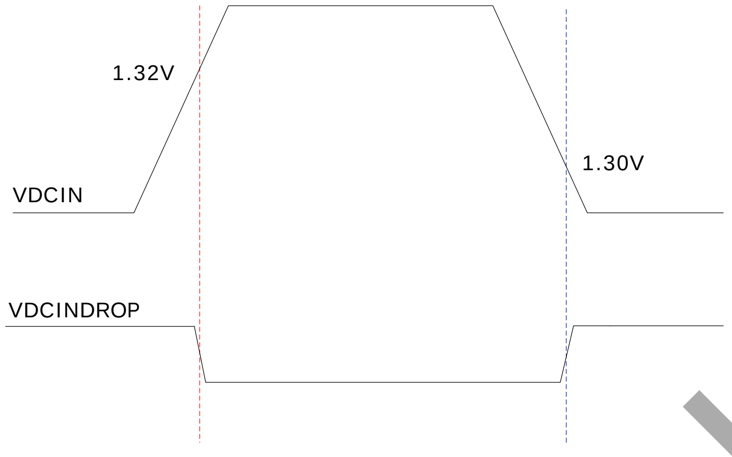


Figure 5-6 Relation Between VDCIN Input Signal and States of Flag Bits VDCINDROP

5.5.2. VDD Supervisor

Power alarm detector is designed to supervise the power state of VDD. When VDD is lower than the specified voltage threshold defined by VDDPVDSEL<2:0> in ANA_REG8, the power alarm signal will inform MCU by interrupt.

VDDPVDSEL<2:0>	Voltage selection of power detector	000: 4.5V;
		001:4.2V;
		010: 3.9V;
		011: 3.6V;
		100: 3.2V;
		101: 2.9V;
		110: 2.6V;
		111: 2.3V;

5.5.3. AVCC Supervisor

AVCCLV module is designed to supervise the power state of AVCC. When AVCC is lower than 2.5V, an LV signal will inform MCU by interrupt, in this situation, the ADC precision will be degraded much, so do not use ADC to measure any signal.

5.6. Power Switch

5.6.1. Power Switch 1

Power switch 1 is designed to switch RTC power between VDD and BATRTC. When VDD is higher than BATRTC, the switch will select VDD to be the power of RTC domain. Otherwise BATRTC will be the power of RTC.

5.6.2. Power Switch 2

Power switch 3 is designed to select AVCC voltage input source. When PD_AVCCLDO (ANA_REG8 bit 7) is set to 0, Voltage of AVCC pin is 3.3V. When PD_AVCCLDO (ANA_REG8 bit 7) is set to 1, AVCC connect to VDD through a switch, and the switch resistor refer to table 1-4. AVCCLDO can be power down only when power supply less than 3.6V.

5.7. Application Note

Two power supply: VDD is powered by one power source. BATRTC is powered by another power source. When VDD is powered down, and only BATRTC pin is powered up, the user should disable automatic temperature compensation. In applications, if user adopted BATRTC power supply independent, and automatic temperature compensation function is enabled when VDD is powered up, user should disable automatic temperature function when VDD is powered down.

One power supply: VDD and BATRTC are connected together, and powered by one power source. RTC auto-calibration can be enabled all the time.

6.Working Model

6.1. Introduction

The PMU controller is used to control the sleep and deep sleep mode of V85X3. There are 16 IOs integrated inside the PMU controller which can wake-up the chip from sleep or deep-sleep mode. The deep sleep mode will power off CPU and all peripherals including system SRAM, LCD controller and other GPIOs not included in PMU controller. Only RTC, analog controller and UART 32K module will be alive under this mode.

6.2. Features

--Deep mode entry/exit control, and corresponding module be reset when MCU wake up from deep sleep mode, the program starts to run from 0 address.

--Password protection to avoid entry deep-sleep mode in un-expected event.

--16 GPIOs with wake-up and interrupt function.

--Interrupt generation.

--When entry sleep and deep sleep mode, system clock will power down. When MCU wake up from sleep mode, hardware will switch the system clock to the setting before entry sleep mode. When MCU wake up from deep sleep mode, the hardware will switch the system clock to RCH automatically.

-- When wake up from deep sleep mode, the program will start from beginning and reset some corresponding modules.

--Crystal absent detect and interrupt.

--Embedded 256 Bytes Retention SRAM which can keep necessary data under deep-sleep mode.

6.3. Functional Block Diagram

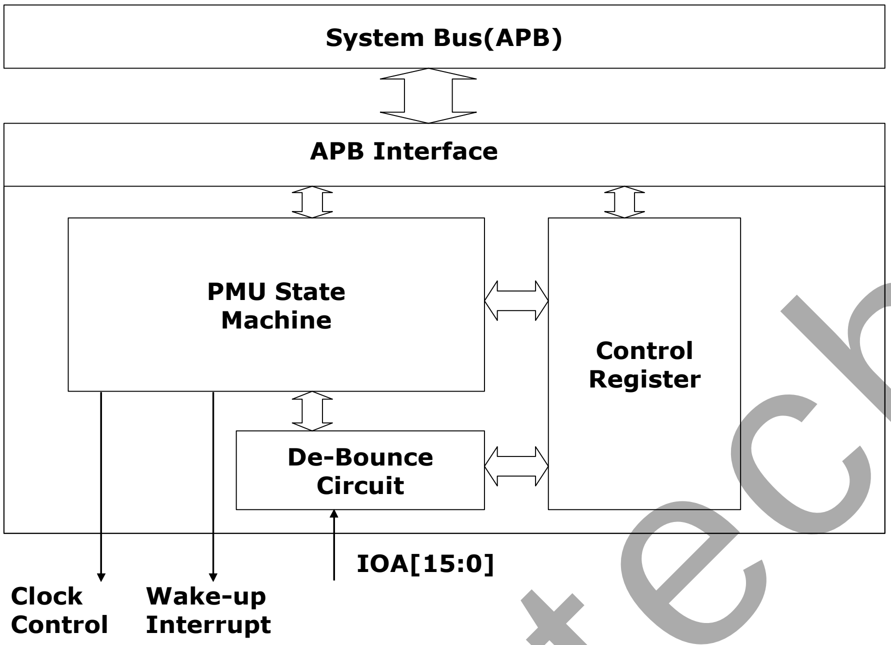


Figure 6-1 Functional Block Diagram of PMU Controller

6.4. Register Location

Table 6-1 Working model Register Location of the PMU Controller (PMU Base: 0x40014000)

Name	Type	Address	Description	Default
PMU_DSLEEPEN	R/W	0x0000	PMU deep sleep enable register	0x00
PMU_DSLEEPPASS	R/W	0x0004	PMU deep sleep password register	0x00
PMU_CONTROL	R/W	0x0008	PMU control register	0x0000
PMU_STS	R/C	0x000C	PMU Status register	0x0000074
VERSIONID	R	0x003C	Version ID of V85X3	--

Table 6-2 working model Register Location of the PMU Retention RAM (PMU Retention RAM Base: 0x40014400)

Name	Type	Address	Description	Default
PMU_RAM0	R/W	0x0000	PMU 32 bits Retention RAM 0	--
PMU_RAM1	R/W	0x0004	PMU 32 bits Retention RAM 1	--
PMU_RAM2	R/W	0x0008	PMU 32 bits Retention RAM 2	--

			…..	
PMU_RAM63	R/W	0x00FC	PMU 32 bits Retention RAM 63	--

Table 6-3 Register Location of ANA Controller for Working Mode (ANA Base: 0x40014200)

Name	Type	Address	Description	Default
ANA_CTRL	R/W	0x0050	Analog control register	0x0000000

6.5. Register Definitions

6.5.1. PMU_DSLEEPEN Register

To enable the deep sleep mode, programmer should write the correct password (0xAA5555AA) into PMU_DSLEEPPASS register first, and then write 0x55AAAA55 to PMU_DSLEEPEN register. Under debug mode (MODE is 0), it is not allowed to enter deep-sleep mode, and all writes to this register will be discarded. If the chip is in deep-sleep mode and MODE change from normal mode to debug mode, it will wake-up automatically to enable the access of ICE interface.

Table 6-4 Description of PMU_DSLEEPEN Register

Bit	Name	Type	Description	Default
31	WKU	R	Current wake-up signal status, this bit reflects the wake-up status received by PMU controller, programmer must make sure this bit is 0 before entering deep-sleep mode, otherwise the system will wake-up immediately because of non-clear WKU event.	0x0
30:0	-	-	Reserved.	0

6.5.2. PMU_DSLEEPPASS Register

Table 6-5 Description of PMU_DSLEEPPASS Register

Bit	Name	Type	Description	Default
31:1	-	-	Reserved.	0
0	UNLOCK	R	This bit indicates the entry of deep-sleep mode has been unlocked and is ready to entry deep-sleep mode. To unlock the deep sleep mode, programmer should write 0xAA5555AA to this register first. This bit will be cleared immediately after any register read or write to any PMU	0x0

			register, including ICE read/write. So programmer should set correct password to PMU_DSLEEPEN immediately.	

6.5.3. PMU_CONTROL Register

Table 6-6 Description of PMU_CONTROL Register

Bit	Name	Type	Description	Default
31:16	-	-	Reserved.	0
15:8	PWUPCYC	R/W	Power-up cycle count, this register controls the power-up wait time when a wake-up even is received. The unit is 32K clock period.	0x0
7:6	-	-	Reserved.	0
5	PLLL_SEL	R/W	Low speed PLL input clock selection. 0: 32K XTAL 1: 32K RC.	0x0
4	PLLH_SEL	R/W	High speed PLL input clock selection. 0: 6.5MHz RC 1: 6.5536MHz XTAL	0x0
3	INT_6M_EN	R/W	6.5536M XTAL absent interrupt enable register. This bit is used to control the interrupt signal output to CPU. When this bit is set to 1, if 6.5536M crystal is removed or broken, an interrupt will be issued to CPU. And if this event is happened during sleep or deep sleep, CPU will be waked up.	0x0
2	INT_32K_EN	R/W	32K XTAL absent interrupt enable register. This bit is used to control the interrupt signal output to CPU. When this bit is set to 1, if 32K crystal is removed or broken, an interrupt will be issued to CPU. And if this event is happened during sleep or deep sleep, CPU will be waked up.	0x0
1	RTCCLK_SEL	R/W	RTC Clock selection. 0: 32K XTAL 1: 32K RC	0x0
0	INT_IOA_EN	R/W	IOA0~15 interrupt enable register. This bit is used to control the interrupt signal output to CPU. User can set some of the IO pins as wake-up source during sleep or	0x0

			deep sleep.	

6.5.4. PMU_STS Register

Table 6-7 Description of PMU_STS Register

Bit	Name	Type	Description	Default
31:25	-	-	Reserved.	0
24	MODE	R	This register shows the current status of MODE pin. 0: Debug mode. 1: Normal mode.	--
23:7	-	-	Reserved.	0
6	DPORST	R/C	This bit indicated if the last reset is caused by internal digital power-on reset signal, and this bit is set to 1 only when the chip power supply first time (BATRTC will be discharged also). Write 1 to clear this bit.	0x1
5	PORST	R/C	This bit indicated if the last reset is caused by PORH reset or PORL reset. PORH reset is caused when AVCCLDO voltage is lower than 2.08V. PORL reset is caused when DVCCLDO voltage is lower than 1.3V. Write 1 to clear this bit.	0x1
4	EXTRST	R/C	This bit indicated if the last interrupt is cause by external reset signal. Write 1 to clear this bit.	0x1
3	EXIST_6M	R	6.5536M XTAL exist status register. This bit represents 6.5536M XTAL is existed or absent. After 6.5536MHz XTAL (BIT7 of ANA_REG3 is configured as 1) is turned on, the state bit will refresh, otherwise it will remain in its previous state. 0: 6.5536M crystal is absent. 1: 6.5536M crystal is existed.	0x0
2	EXIST_32K	R	32K XTAL exist status register. This bit represents 32K XTAL is existed or absent. 0: 32K crystal is absent. 1: 32K crystal is existed.	0x1
1	INT_6M	R/C	This bit represents the 6.5536M crystal absent interrupt status. When this bit is set to 1, it means the 6.5536M crystal is removed or broken.	0x0

			When the EXIST_6M state goes from 1 to 0, the state position is 1. Write 1 to this bit can clear this flag to 0.	
0	INT_32K	R/C	This bit represents the 32K crystal absent interrupt status. When this bit is set to 1, it means the 32K crystal is removed or broken. When the EXIST_32K state goes from 1 to 0, the state position is 1. Write 1 to this bit can clear this flag to 0.	0x0

6.5.5. ANA_CTRL Register

Table 6-8 Description of ANA_CTRL Register

Bit	Name	Type	Description	Default
26	PDNS2	R/W	This register is used to set the deep sleep behavior when VDDALARM is 0. (Still need to consider the PDNS setting). 0: Can’t enter deep-sleep mode when VDDALARM is 0. When VDDALARM is 1, the system can enter deep-sleep mode. The system will wake-up from deep-sleep mode automatically as long as VDDALARM became 0. 1: Can enter deep-sleep mode no-matter which state VDDALARM is.	0x0
6	PDNS	R/W	This register is used to set the deep sleep behavior when VDCINDROP is 0 (Still need to consider the PDNS setting). 0: Can’t enter deep-sleep mode when VDCINDROP is 0. When VDCINDROP is 1, the system can enter deep-sleep mode. The system will wake-up from deep-sleep mode automatically as long as VDCINDROP became 0. 1: Can enter deep-sleep mode no-matter which state VDCINDROP is.	0x0

6.6. Reset

After exit from each mode, some of the hardware module will be reset automatically, the following table shows the detail of reset of each module.

Table 6-9 Reset of Each Module under Different Events

Module	External Reset	Power-on Reset	Watch-dog Reset	M0-soft Reset	Exit RTC only mode	Wake up from		
						deep sleep	sleep	idle
Cortex-M0	V	V	V	V	V	V	-	-
System SRAM	-	-	-	-	Data lost	Data lost	-	-
Retention SRAM	-	-	-	-	Data lost	-	-	-
PMU (IOA)	V	V	V	-	V	-	-	-
WDT	V	V	V	-	V	-	-	-
RTC	V*	V*	V*	-	V*	-	-	-
UART 32K 0	V	V	V	-	V	-	-	-
UART 32K 1	V	V	V	-	V	-	-	-
Analog Controller	V	V	V	-	V	-	-	-
LCD	V	V	V	V	V	V	-	-
GPIO (IOB~IOF)	V	V	V	V	V	V	-	-
MISC2	V	V	V	V	V	V	-	-
MISC	V	V	V	V	V	V	V	-
I2C	V	V	V	V	V	V	V	-
SPI1/SPI2	V	V	V	V	V	V	V	-
UART	V	V	V	V	V	V	V	-
ISO7816	V	V	V	V	V	V	V	-
TIMER	V	V	V	V	V	V	V	-
PWM	V	V	V	V	V	V	V	-
DMA	V	V	V	V	V	V	V	-
SRAM Controller	V	V	V	V	V	V	V	-
FLASH Controller	V	V	V	V	V	V	V	-

Note (V*): RTC registers without write protection can be reset under external reset or power-on reset or watch-dog reset, other registers cannot be reset under one of reset external reset or power-on reset or watch-dog reset events.

For different mode, the enable or disable of clock generated module will be controlled by hardware or software, the following tables shows the detail of clock status under each mode.

Table 6-10 Clock Source Enable or Disable in Different Modes

Clock Source	Power modes				
	RTC only	Deep sleep	Sleep	IDLE	Active
6.5536M RC	OFF	OFF	OFF	Controlled by RCHPD	
6.5536M XTAL	OFF	OFF	OFF	Controlled by XOHPDN	
PLLH	OFF	OFF	OFF	Controlled by PLLHPDN	
PLLL	OFF	OFF	OFF	Controlled by PLLLPDN	
32K RC	ON	ON	ON	ON	
32K XTAL	ON	ON	ON	ON	

Clock Source	Exit RTC only mode	Wake up from different modes		
		Deep sleep	Sleep	IDLE
6.5536M RC	ON	ON	Controlled by RCHPD	
6.5536M XTAL	OFF	OFF	Controlled by XOHPDN	
PLLH	OFF	OFF	Controlled by PLLHPDN	
PLLL	OFF	OFF	Controlled by PLLLPDN	
32K RC	ON	ON	ON	
32K XTAL	ON	ON	ON	

6.6.1. External Reset

The external reset pin (EXTRSTN) can reset most of the modules inside V85X3. In order to prevent the external noise couple into this pin, a de-glitch circuit is embedded in V85X3. The following diagram shows an example of how this de-glitch circuit works. The de-glitch time will increase accordingly when the RTCCLK pre-scaler is set to a non-zero value. For example, when RTCCLK pre-scaler is set to 1/4, the de-glitch time will be increased to 91*4 = 364 μs.

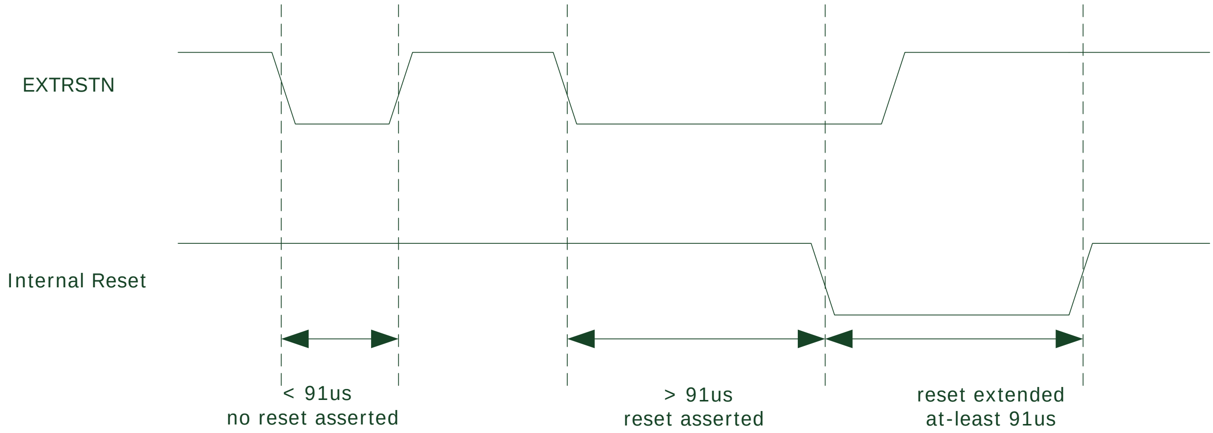


Figure 6-2 External Reset De-glitch Timing

6.6.2. WDT Reset

WDT's reset level is the same as POR.

6.6.3. POR Reset

The POR module can provide chip's internal reset, should work with external reset together.

6.6.4. M0-soft Reset

M0-soft reset instruction can reset the most modules in V85X3, details please refer to Figure 6-2.

6.6.5. Wake up from sleep /deep sleep/IDLE

Any interrupt can wake up the system from IDLE, some of them can wake up the system from sleep, and some of them can wake up the system from deep sleep.

Table 6-11 Interrupt Sources

Item	Vector address	Interrupt Nom.	Description	Enable bit of peripheral event	Flag of peripheral event	Wake-up source	
						Deep Sleep	Sleep
NMI	00000008h	-14	NMI				
HardFault	0000000Ch	-13	HardFault				

SVCall	0000002Ch	-5	SVCall				
PendSV	00000038h	-2	PendSV				
SysTick	0000003Ch	-1	SysTick				
PMU	00000040h	0	IOA0~15	PMU_CONTROL.0 and PMU_IOAWKUEN.0~15	PMU_IOAINTSTS.0~15	V	V
			32K crystal is removed or broken	PMU_CONTROL.2	PMU_STS.0	V	V
			6M crystal is removed or broken	PMU_CONTROL.3	PMU_STS.1		
RTC	00000044h	1	Reserved.	RTC_INTEN.0	RTC_INTSTS.0	V	V
			illegal time format	RTC_INTEN.1	RTC_INTSTS.1	V	V
			multi-second period is reach	RTC_INTEN.2	RTC_INTSTS.2	V	V
			multi-minute period is reach	RTC_INTEN.3	RTC_INTSTS.3	V	V
			multi-hour period is reach	RTC_INTEN.4	RTC_INTSTS.4	V	V
			mid-night (00:00) is reach	RTC_INTEN.5	RTC_INTSTS.5	V	V
			32K counter period is reach	RTC_INTEN.6	RTC_INTSTS.6	V	V
			auto calibration is done	RTC_INTEN.7	RTC_INTSTS.7	V	V
			illegal write to CE register	RTC_INTEN.8	RTC_INTSTS.8		
U32K0~1	00000048h	2\3	Receiver	U32Kx_CTRL1	U32Kx_ST	V	V

	0000004Ch		data input	.0	S.0		
			Receive parity error	U32Kx_CTRL1.1	U32Kx_STS.1	V	V
			Receive buffer overrun	U32Kx_CTRL1.2	U32Kx_STS.2	V	V
I2C	00000050h	4	Serial Interrupt	I2C_CTRL2.0	I2C_CTRL.3		
SPI1~2	00000054h 000000ACh	5\27	SPI Transmit	SPIx_TXSTS.14	SPIx_TXSTS.15		
			SPI Receive	SPIx_RXSTS.14	SPIx_RXSTS.15		
UART0~5	00000058h ~ 0000006Ch	6\7\8\9\10\11	Receive	UARTx_CTRL.3	UARTx_INTSTS.1		
			Transmit overrun	UARTx_CTRL.4	UARTx_INTSTS.2		
			Receive overrun	UARTx_CTRL.5	UARTx_INTSTS.3		
			Receive parity error	UARTx_CTRL.7	UARTx_INTSTS.4		
			Transmit done	UARTx_CTRL.8	UARTx_INTSTS.5		
ISO78160~1	00000070h ~ 00000074h	12\13	Receive	ISO7816x_CFG.5	ISO7816x_INFO.5		
			Transmit	ISO7816x_CFG.6	ISO7816x_INFO.6		
			Receive overrun	ISO7816x_CFG.7	ISO7816x_INFO.7		
Timer0~3	00000078h ~ 00000084h	14\15\16\17	Timer x overflow	TMRx_CTRL.3	TMRx_INT.0		
PWM0~3	00000088h ~ 000094h	18\19\20\21	PWM timer overflow	PWMx_CTL.1	PWMx_CTL.0		
			Compare 0	PWMx_CCTL0.4	PWMx_CCTL0.0		
			Compare 1	PWMx_CCTL1.4	PWMx_CCTL1.0		

			Compare 2	PWMx_CCTL2.4	PWMx_CCTL2.0		
DMA	00000098h	22	Channel 0 package end	DMA_IE.0	DMA_STS.0		
			Channel 1 package end	DMA_IE.1	DMA_STS.1		
			Channel 2 package end	DMA_IE.2	DMA_STS.2		
			Channel 3 package end	DMA_IE.3	DMA_STS.3		
			Channel 0 frame end	DMA_IE.4	DMA_STS.4		
			Channel 1 frame end	DMA_IE.5	DMA_STS.5		
			Channel 2 frame end	DMA_IE.6	DMA_STS.6		
			Channel 3 frame end	DMA_IE.7	DMA_STS.7		
			Channel 0 data abort	DMA_IE.8	DMA_STS.8		
			Channel 1 data abort	DMA_IE.9	DMA_STS.9		
			Channel 2 data abort	DMA_IE.10	DMA_STS.10		
			Channel 3 data abort	DMA_IE.11	DMA_STS.11		
FLASH	0000009Ch	23	checksum error	FLASH_CTRL.2	FLASH_INT.0		
ANA	000000A0h	24	manual ADC conversion done	ANA_INTEN.0	ANA_INTSTS.0		
			auto ADC conversion done	ANA_INTEN.1	ANA_INTSTS.1		
			COMP1 rising or falling	ANA_INTEN.2	ANA_INTSTS.2	V	V
			COMP2 rising	ANA_INTEN.3	ANA_INTS	V	V

			or falling		TS.3		
			VDDALARM rising or falling	ANA_INTEN.7	ANA_INTSTS.7	V	V
			VDCIN rising or falling	ANA_INTEN.8	ANA_INTSTS.8	V	V
			AVCCLV rising or falling	ANA_INTEN.10	ANA_INTSTS.10	V	V
			VDCINDROP is 0 and the entry of sleep or deep-sleep modes are detected	ANA_INTEN.11	ANA_INTSTS.11	V	V
			ANA_REGx error	ANA_INTEN.12	ANA_INTSTS.12	V	V
			TADC change over threshold	ANA_INTEN.13	ANA_INTSTS.13	V	V

6.7. Working Model

The following diagram shows the power state machine of V85X3.

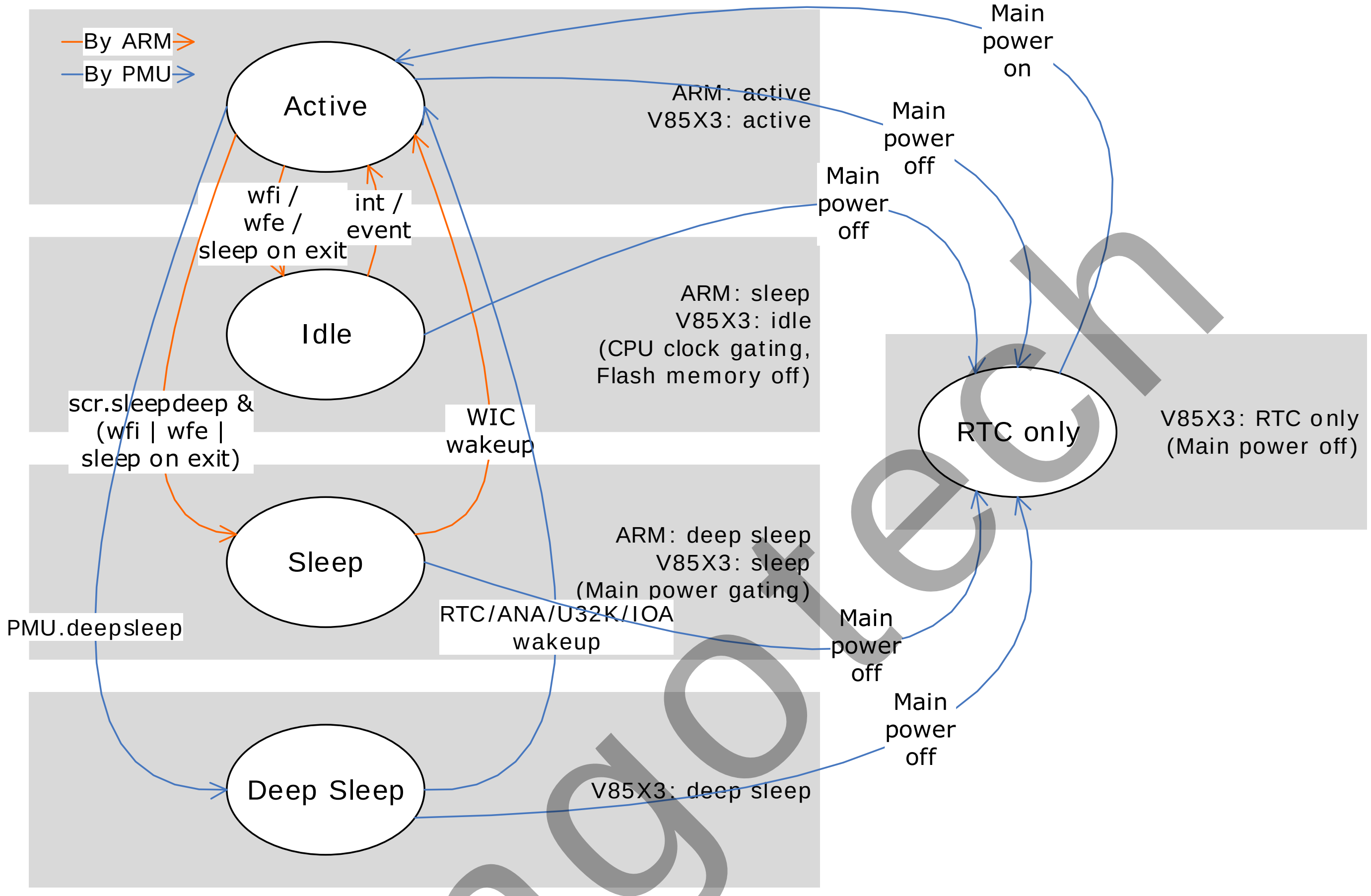


Figure 6-3 Power State Flow Chart of V85X3

According to the diagram above, idle mode or sleep is controlled by CPU directly, and the programmer only needs to execute corresponded instruction (WFI or WFE) to enter these two modes. For deep sleep mode, PMU controller will handle the entry and exit of this mode and it will always return to active mode after wake-up. Corresponded wake-up source must be set before entry deep sleep mode, this part should be taken care by software programmer. The following shows the wake-up source under each mode.

Note: (1) It should be noted that MCU could enter sleep mode or deep sleep mode only when MODE=1. If MCU execute instruction for entry sleep mode when MODE=0, MCU will enter idle mode. Before MCU enter deep sleep mode, programmer should configure PDNS (ANA_CTRL bit6) and PDNS2 (ANA_CTRL bit24) firstly, or judge the state of VDCINDROP and VDDALRAM. For details, please refer to ANA_CTRL register.

(2) Under RTCONLY mode (VDD power down, only BATRTC power supply), user should disable RTC automatic temperature compensation.

(3) When MCU wake up from sleep mode, hardware will switch the system clock to the setting before entry sleep mode. For example, the system clock is PLLL before entry sleep mode, the hardware will switch the system clock to PLLL when wake up from sleep mode. When MCU wake up from deep sleep

mode, the hardware will switch the system clock to RCH automatically. Before entry IDLE mode and wake up from IDLE mode, the hardware does not change the system clock automatically.

(4) If user enables RTC automatic temperature compensation, user can't select RCH as system clock before entry sleep mode. If user disables RTC automatic temperature compensation, user can select RCH as system clock before entry sleep mode. System clock source control by CLKSEL (MISC2_CTRL bit2:0).

(5) User can't select RTCCLK as system clock before entry sleep mode. System clock source control by CLKSEL (MISC2_CTRL bit2:0).

(6) When wake up from sleep mode, PLLL lock time is 1ms, and PLLH lock time is 15μs.

Table 6-12 Wake-up Source under Each Mode

INT Number	Source	Wake up from		
		deep sleep	sleep	idle
Event	-	-	-	-
NMI	SRAM Parity Error	-	-	V
0	PMU (Ext Int)	V	V	V
1	RTC	V	V	V
2	UART 32K 0	V	V	V
3	UART 32K 1	V	V	V
4	I2C	-	-	V
5	SPI1	-	-	V
6	UART0	-	-	V
7	UART1	-	-	V
8	UART2	-	-	V
9	UART3	-	-	V
10	UART4	-	-	V
11	UART5	-	-	V
12	ISO78160	-	-	V
13	ISO78161	-	-	V
14	TIMER0	-	-	V
15	TIMER1	-	-	V
16	TIMER2	-	-	V
17	TIMER3	-	-	V
18	PWM0	-	-	V

19	PWM1	-	-	V
20	PWM2	-	-	V
21	PWM3	-	-	V
22	DMA	-	-	V
23	FLASH	-	-	V
24	ANA	V	V	V
27	SPI2	-	-	V

6.8. Application Note

6.8.1. External IO Wake-up

All 16 IOAs can wake-up the system from sleep or deep-sleep mode. In order to prevent some glitches on these signal to unexpected wake-up the system, a de-glitch circuit is embedded in V85X3. The following diagram shows an example of how this de-glitch circuit works. The de-glitch time will increase accordingly when the RTCCLK pre-scaler is set to a non-zero value. For example, when RTCCLK pre-scaler is set to 1/4, the de-glitch time will be increased to122*4=488 μs. The de-glitch time only affects the wake-up signal under sleep and deep-sleep mode.

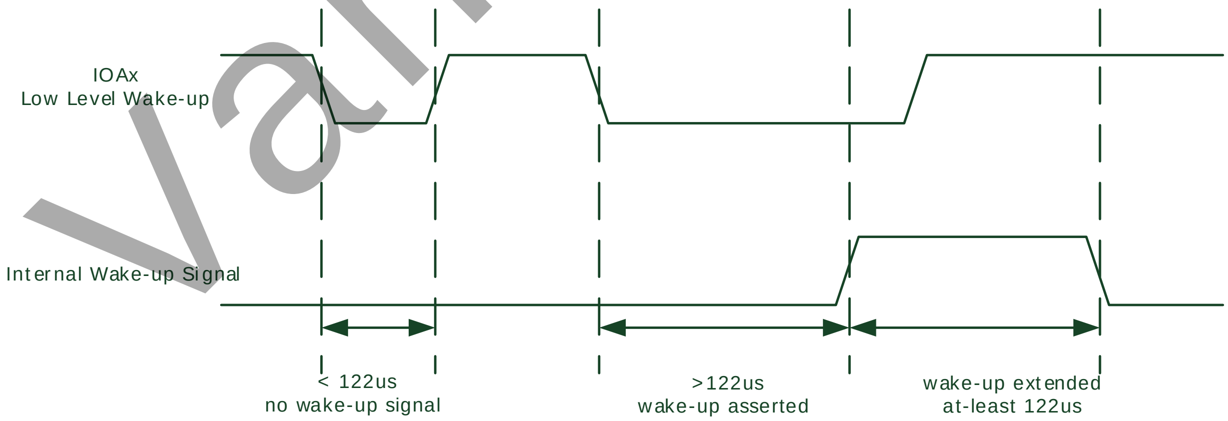
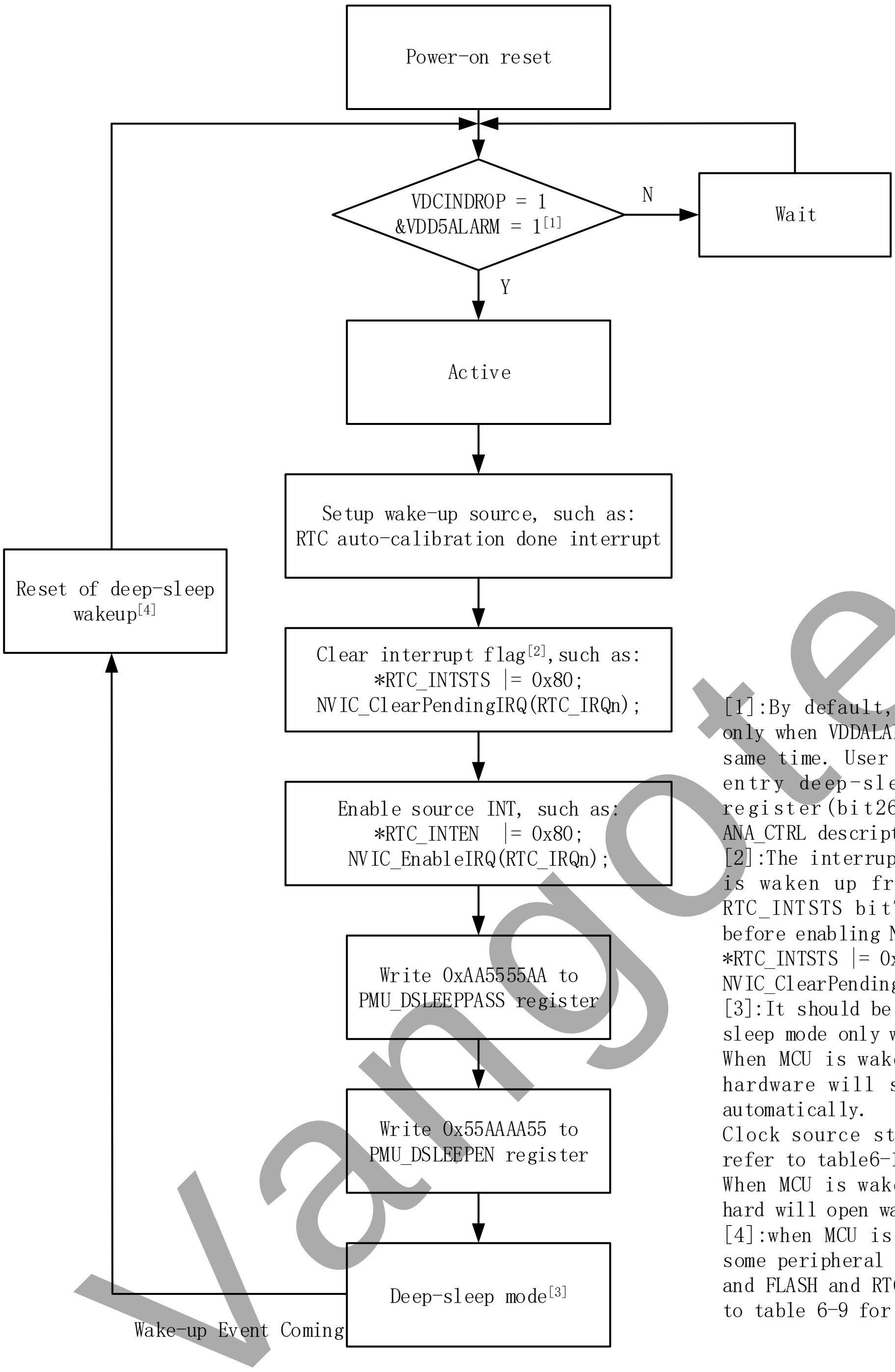


Figure 6-4 External Wake-up Example

6.8.2. Deep-sleep Entry Procedure

The following figure shows an example of deep-sleep mode entry procedure.



[1]:By default, MCU can entry deep-sleep mode only when VDDALARM and VDCINROP must be 1 at the same time. User can change the condition of MCU entry deep-sleep mode by setting ANA_CTRL register(bit26 and bit6). Please refer to ANA_CTRL description for details.

[2]:The interrupt flag will be set to 1 when MCU is waken up from deep-sleep mode, such as: RTC_INTSTS bit7. User should clear the flag before enabling NVIC interrupt again, such as:

*RTC_INTSTS |= 0x80;

NVIC_ClearPendingIRQ(RTC_IRQn);

[3]:It should be noted that MCU could enter deep-sleep mode only when MODE=1.

When MCU is waken up from deep sleep mode, the hardware will switch the system clock to RCH automatically.

Clock source state in different modes, please refer to table6-10 for details.

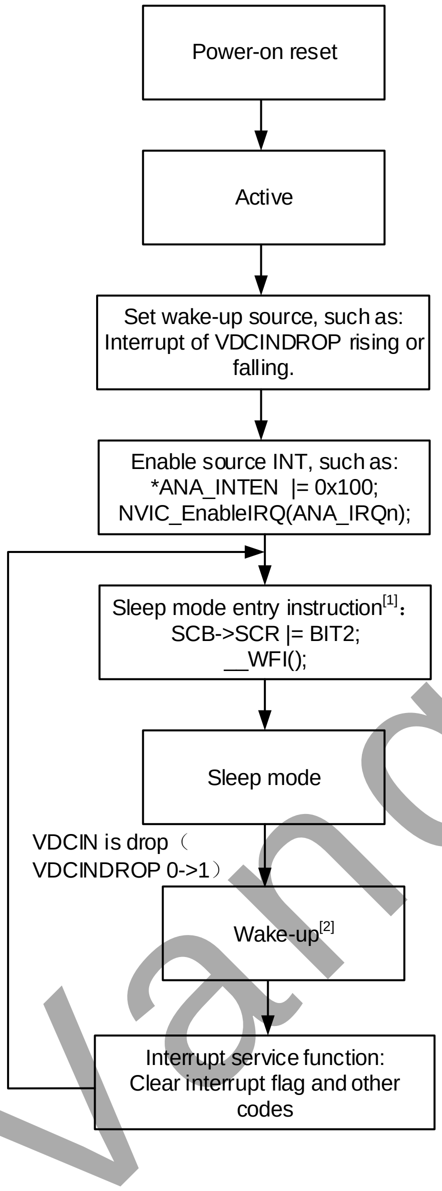
When MCU is waken up from deep-sleep mode, the hard will open watch dog automatically.

[4]:when MCU is waken up from deep-sleep mode, some peripheral will not be reset including SRAM and FLASH and RTC and WDT and so on, please refer to table 6-9 for details.

Figure 6-5 Deep-sleep Mode Entry Flow

6.8.3. Sleep Entry Procedure

The following figure shows an example of sleep mode entry procedure.


Power-on reset
Active
Set wake-up source, such as: Interrupt of VDCINDROP rising or falling.
Enable source INT, such as: *ANA_INTEN |= 0x100; NVIC_EnableIRQ(ANA_IRQn);
Sleep mode entry instruction[1]: SCB->SCR |= BIT2; __WFI();
Sleep mode
VDCIN is drop（VDCINDROP 0->1）
Wake-up[2]
Interrupt service function: Clear interrupt flag and other codes

[1]:It should be noted that MCU could enter sleep mode only when MODE=1. If MCU executes instruction for entry sleep mode when MODE=0, MCU will entry IDLE mode.

[2]:When MCU is waken up from deep-sleep mode, some peripheral will be reset including UART , SPI , I2C and so on, but LCD , GPIO , ANA and so on will not be reset, please refer to table 6-9 for details.

When MCU is waken up from sleep mode, hardware will switch the system clock to the state of entry sleep mode. For example, the system clock is PLLL before entering sleep mode, the hardware will switch the system clock to PLLL when waking up from sleep mode.

The sate of clock source in different modes , please refer to table 6-10 for details.

When MCU is waken up from deep-sleep mode, the hard will open watch dog automatically.

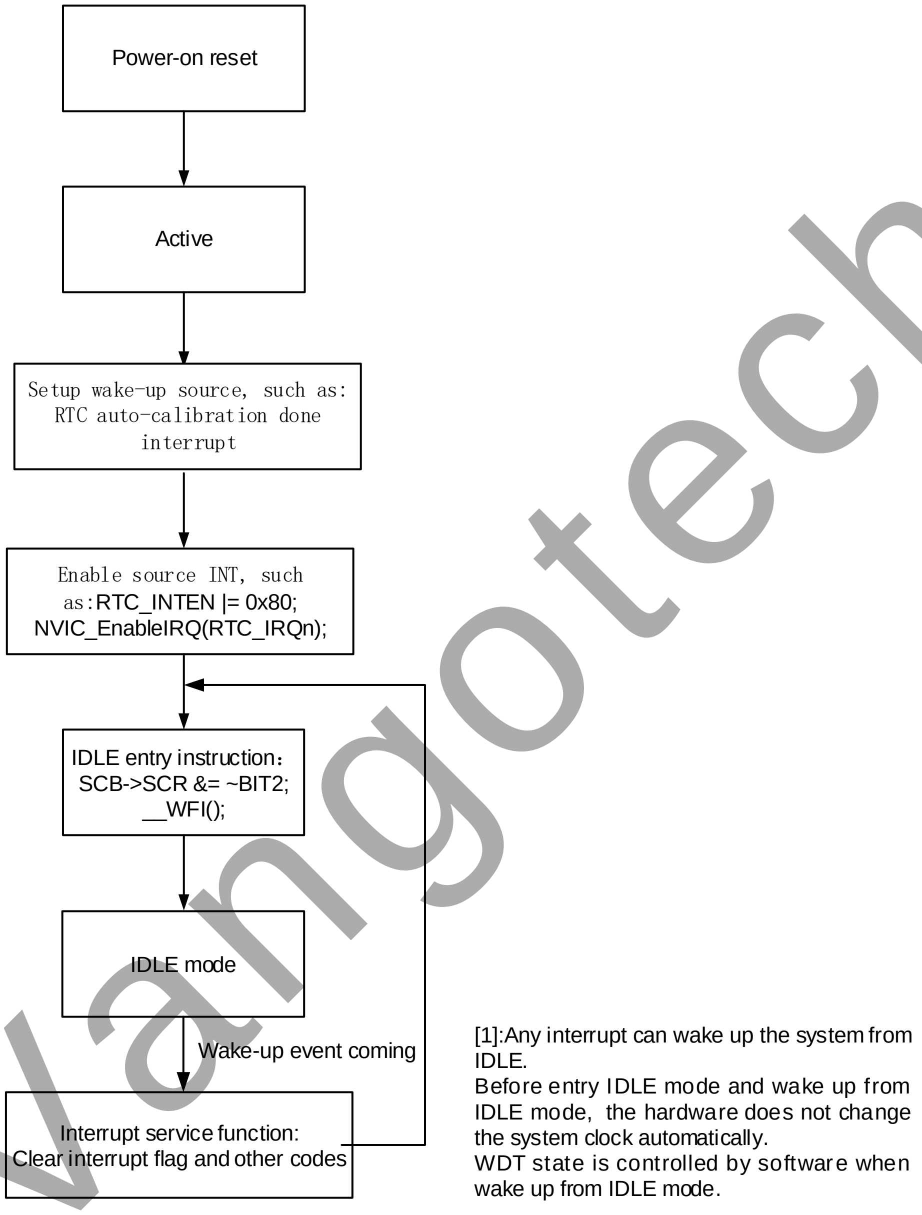
Note: (1)If user enables RTC automatic temperature compensation, user should not select RCH as system clock before entering sleep mode. If user does not enable RTC automatic temperature compensation, user can select RCH as system clock before entering sleep mode. System clock source is controlled by CLKSEL(MISC2_CTRL bit2:0).

(2)User should not select RTCCLK as system clock before entering sleep mode. System clock source is controlled by CLKSEL(MISC2_CTRL bit2:0).

Figure 6-6 Sleep Mode Entry Flow

6.8.4. IDLE Entry Procedure

The following figure shows an example of idle mode entry procedure.


Power-on reset
Active
Setup wake-up source, such as: RTC auto-calibration done interrupt
Enable source INT, such as:RTC_INTEN |= 0x80; NVIC_EnableIRQ(RTC_IRQn);
IDLE entry instruction: SCB->SCR &= ~BIT2; __WFI();
IDLE mode
Wake-up event coming
Interrupt service function: Clear interrupt flag and other codes

[1]:Any interrupt can wake up the system from IDLE.
Before entry IDLE mode and wake up from IDLE mode, the hardware does not change the system clock automatically.
WDT state is controlled by software when wake up from IDLE mode.

Figure 6-7 IDLE Mode Entry Flow

7.Clock Controller

7.1. Introduction

The settings in clock controller will be reset after wake-up from deep-sleep mode or system reset, programmer should restore the setting manually after wake-up from deep-sleep mode.

In the V85X3, there are four clock sources:

- The 32K RC oscillator circuit, to generate a 32.768K RC clock (32K RC). This circuit is running always. 32k RC can trimming from RCLTRIM [4:0] (ANA_REGB).
- The 32K crystal oscillator circuit, to generate a 32.768K XTAL clock (32K XTAL). This circuit is monitored by the 32K XTAL monitoring circuit that is sourced by 32K RC clock. When this oscillator circuit stops running, 32K RC clock will replace 32K XTAL, and the monitoring circuit will stimulate the crystal oscillator circuit until it runs again.
- The 6M RC oscillator circuit, to generate a 6.5536M RC clock (6M RC). This circuit can stop running by user register control. This circuit starts running from chip reset.
- The 6M XTAL oscillator circuit, to generate a 6.5536M XTAL clock (6M XTAL). This circuit can stop running by user register control.

In the V85X3, there are three clock domains:

- HCLK is generated by one of the 6.5536M XTAL\ 6.5536M RC\ 32.768K XTAL\ 32.768K RC or multiply of them. HCLK provides clock pulses for the CPU\FLASH\SRAM\DMA\GPIO\LCD\CRYPT.
- PCLK is divided from HCLK. PCLK provides clock pulses for the slow peripheral.
- RTCCLK provides clock pulses for the RTC\ WDT\ UART32K\ LCD.

For different mode, the enable or disable of clock generated module will be controlled by hardware or software, the following tables shows the detail of clock status under each mode.

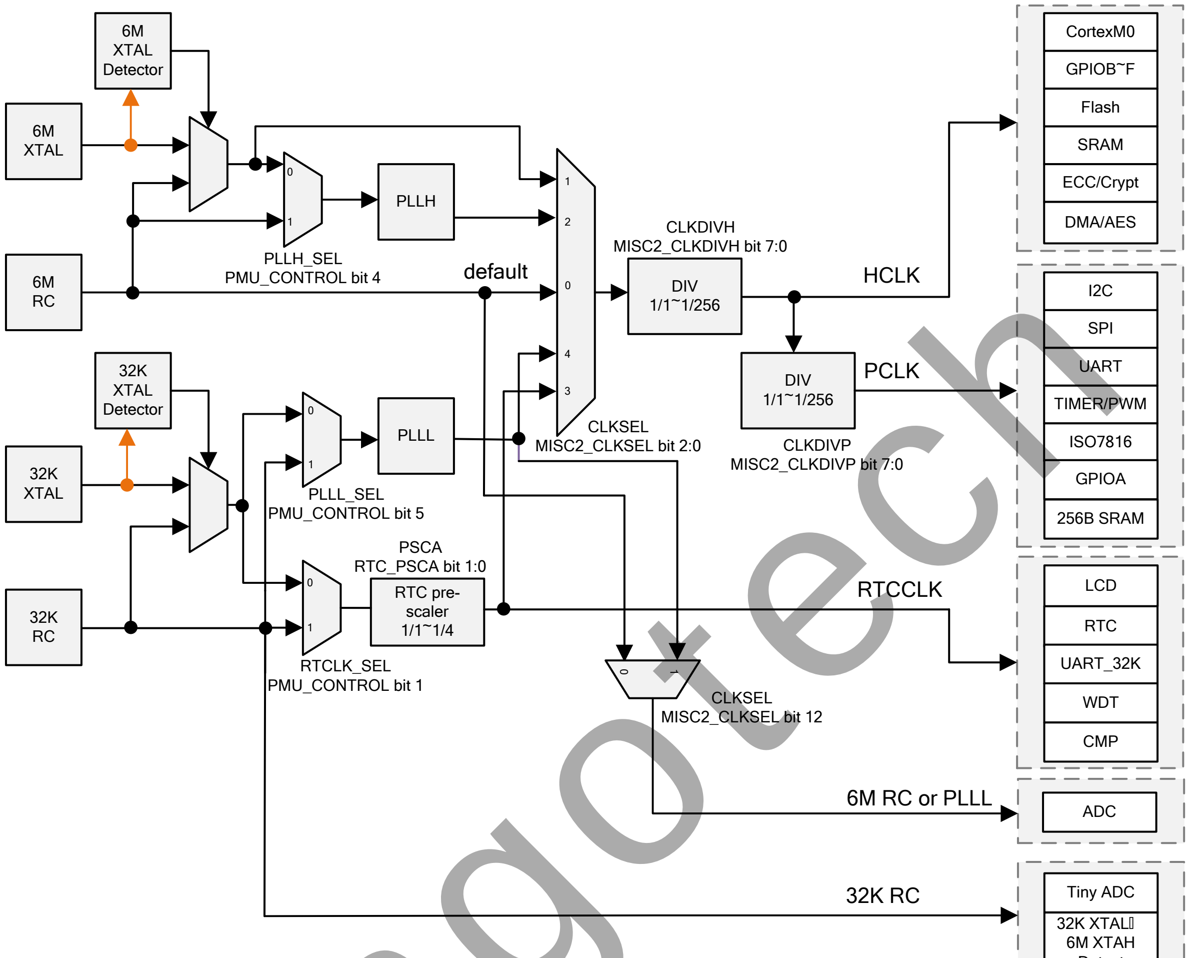
Table 7-1 Clock Source Enable or Disable in Different Modes

Clock Source	Power modes				
	RTC only	Deep sleep	Sleep	IDLE	Active
6.5536M RC	OFF	OFF	OFF	Controlled by RCHPD	
6.5536M XTAL	OFF	OFF	OFF	Controlled by XOHPDN	
PLLH	OFF	OFF	OFF	Controlled by PLLHPDN	
PLLL	OFF	OFF	OFF	Controlled by PLLLPDN	

32K RC	ON	ON	ON	ON
32K XTAL	ON	ON	ON	ON

Clock Source	Exit RTC only mode	Wake up from different modes		
		Deep sleep	**Sleep**	**IDLE**
6.5536M RC	ON	ON	Controlled by RCHPD	
6.5536M XTAL	OFF	OFF	Controlled by XOHPDN	
PLLH	OFF	OFF	Controlled by PLLHPDN	
PLLL	OFF	OFF	Controlled by PLLLPDN	
32K RC	ON	ON	ON	
32K XTAL	ON	ON	ON	

7.2. Block Diagram



→ Clock line.

→ Oscillator circuit detect signal line. 6M XTAL detector and 32K XTAL detector is sourced by 32K RC clock. When this oscillator circuit stops running, 6M RC clock will replace 6M XTAL clock, 32K RC clock will replace 32K XTAL clock, and the monitoring circuit will stimulate the crystal oscillator circuit until it runs again.

Figure 7-1 V85X3 Clock Block Diagram

7.3. Register Location

Table 7-2 Register Location of ANA Controller for CLOCK (ANA Base: 0x40014200)

Name	Type	Address	Description	Default
ANA_REG2	R/W	0x0008	Analog control register 2	0x00
ANA_REG3	R/W	0x000C	Analog control register 3	0x00
ANA_REG9	R/W	0x0024	Analog control register 9	0x00
ANA_REGB	R/W	0x002C	Analog control register 11	From FLASH
ANA_REGC	R/W	0x0030	Analog control register 12	From FLASH

ANA_CMPOUT	R	0x0054	Comparator result register	0x0030

Table 7-3 Register Location of the PMU Controller (PMU Base: 0x40014000)

Name	Type	Address	Description	Default
PMU_CONTROL	R/W	0x0008	PMU control register	0x0000
PMU_STS	R/C	0x000C	PMU Status register	0x0000074

Table 7-4 Register Location of MISC2 Controller (MISC2 Base: 0x40013E00)

Name	Type	Address	Description	Default
MISC2_CLKSEL	R/W	0x0004	Clock selection register	0x0
MISC2_CLKDIVH	R/W	0x0008	AHB clock divider control register	0x00
MISC2_CLKDIVP	R/W	0x000C	APB clock divider control register	0x01
MISC2_HCLKEN	R/W	0x0010	AHB clock enable control register	0x1FF
MISC2_PCLKEN	R/W	0x0014	APB clock enable control register	0xFFFFFFFF

7.4. Feature

--Clock control of each sub-module

--Clock divider of AHBCLK and APBCLK.

7.5. Register Definition

7.5.1. ANA_REG2 Register

Table 7-5 Description of ANA_REG2

Bit	Name	Function	Notes
7	XOLPD	32K crystal pad (XOL) power down control.	0: XOL power on. 1: XOL power down.

7.5.2. ANA_REG3 Register

Table 7-6 Description of ANA_REG3

Bit	Name	Function	Notes
3	BGPPD*	BGP power down control signal.	0: Power-up BGP. 1: Power-down BGP.
4	RCHPD	RCH (6.5536M RC) power down control signal.	0: Power-up RCH. 1: Power-down RCH.
5	PLLLPDN	PLLL (32768Hz input PLL) power up control signal.	0: Power-down PLLL. 1: Power-up PLLL.
6	PLLHPDN	PLLH (6.5536MHz input PLL) power up control signal.	0: Power-down PLLH. 1: Power-up PLLH.
7	XOHPDN	6.5536M crystal power up control signal.	0: Power-down XOH. 1: Power-up XOH.
Note*: RCH and PLL and ADC are related to BGP, must power-up BGP before power-up RCH or PLL or ADC. User can power down BGP by set BGPPD to 1 when BGP was not used in program. User could not power down BGP by set BGPPD to 1 when BGP was used in program, because the system has a protection function to ensure reliability. User can power down BGP in sleep mode and deep-sleep mode whether BGP is used or not.			

7.5.3. ANA_REG4 Register

Table 7-7 Description of ANA_REG2

Bit	Name	Function	Notes
7:0	-	Reserved.	Default: 0x00, must be set to 0x01 by user.

7.5.4. ANA_REG9 Register

Table 7-8 Description of ANA_REG9

Bit	Name	Function	Notes
2:0	PLLLSEL[2:0]	Frequency selection of PLLL.	000: 26.2144 MHz 001: 13.1072 MHz 010: 6.5536 MHz 011: 3.2768 MHz 100: 1.6384 MHz

			101: 0.8192MHz 110: 0.4096MHz 111: 0.2048MHz
6:3	PLLHSEL[3:0]	Frequency selection of PLLH. The PLLH’s frequency is the multiply of external XOH or internal RCH.	1000~1011: Reserved. 1100: 2 x Input clock 1101: 2.5 x Input clock 1110: 3 x Input clock 1111: 3.5 x Input clock 0000: 4 x Input clock 0001: 4.5 x Input clock 0010: 5 x Input clock 0011: 5.5 x Input clock 0100: 6 x Input clock 0101: 6.5 x Input clock 0110: 7 x Input clock 0111: 7.5 x Input clock

7.5.5. ANA_REGB Register

Table 7-9 Description of ANA_REGB

Bit	Name	Function	Notes

4:0	RCLTRIM[4:0]	Trimming of 32kHz RC.	00000~01111: increased by 4% for each step;
			10000~11111: decreased by 4% for each step;

Note: Users must not modify the configuration of ANA_REGx(x=B~E), it can be loaded from FLASH automatically.			

7.5.6. ANA_REGC Register

Table 7-10 Description of ANA_REGC

Bit	Name	Function	Notes

5:0	RCHTRIM[5:0]	Trimming of 6.5536MHz RC	000000~011111: increased by 1.25% for each step;
			100000~111111: decreased by 1.25% for each step;

Note: Users must not modify the configuration of ANA_REGx(x=B~E), it can be loaded from FLASH automatically.			

7.5.7. ANA_CMPOUT Register

Table 7-11 Description of ANA_CMPOUT Register

Bit	Name	Type	Description	Default
1	LOCKL	R	PLLL lock status. It takes about 1ms until PLLL locked. 0: PLLL is not lock. 1: PLLL is lock.	0x0
0	LOCKH	R	PLLH lock status. It takes about 15μs until PLLH locked. 0: PLLH is not lock. 1: PLLH is lock.	0x0

7.5.8. PMU_CONTROL Register

Table 7-12 Description of PMU_CONTROL Register

Bit	Name	Type	Description	Default
5	PLLL_SEL	R/W	Low speed PLL input clock selection. 0: 32KXTAL 1: 32K RC	0x0
4	PLLH_SEL	R/W	High speed PLL input clock selection. 0: 6.5MHz RC 1: 6.5536MHz XTAL	0x0
3	INT_6M_EN	R/W	6.5536M XTAL absent interrupt enable register. This bit is used to control the interrupt signal output to CPU. When this bit is set to 1, if 6.5536M crystal is removed or broken, an interrupt will be issued to CPU.	0x0

2	INT_32K_EN	R/W	32K XTAL absent interrupt enable register. This bit is used to control the interrupt signal output to CPU. When this bit is set to 1, if 32K crystal is removed or broken, an interrupt will be issued to CPU. And if this event is happened during sleep, CPU will be waked up.	0x0
1	RTCCLK_SEL	R/W	RTC Clock selection. 0: 32K XTAL 1: 32K RC	0x0

7.5.9. PMU_STS Register

Table 7-13 Description of PMU_STS Register

Bit	Name	Type	Description	Default
3	EXIST_6M	R	6.5536M XTAL exist status register. This bit represents 6.5536M XTAL is existed or absent. After 6.5536MHz XTAL (BIT7 of ANA_REG3 is configured as 1) is turned on, the state bit will refresh, otherwise it will remain in its previous state. 0: 6.5536M crystal is absent. 1: 6.5536M crystal is existed.	0x0
2	EXIST_32K	R	32K XTAL exist status register. This bit represents 32K XTAL is existed or absent. 0: 32K crystal is absent. 1: 32K crystal is existed.	0x1
1	INT_6M	R/C	This bit represents the 6.5536M crystal absent interrupt status. When this bit is set to 1, it means the 6.5536M crystal is removed or broken. When the EXIST_6M state goes from 1 to 0, the state position is 1. Write 1 to this bit can clear this flag to 0.	0x0
0	INT_32K	R/C	This bit represents the 32K crystal absent interrupt status. When this bit is set to 1, it means the 32K crystal is removed or broken. When the EXIST_32K state goes from 1 to 0, the state position is 1. Write 1 to this bit can clear this flag to 0.	0x0

7.5.10. MISC2_CLKSEL Register

Table 7-14 Description of MISC2_CLKSEL Register

Bit	Name	Type	Description	Default
31:3	-	-	Reserved.	0
2:0	CLKSEL	R/W	This register is used to control AHB clock source. 0: RCH (6.5MHz RC) 1: XOH (6.5536MHz XTAH). 2: PLLH. 3: RTCCLK (controlled by RTCCLK_SEL in PMU_CONTROL register). 4: PLLL. Before clock select to one of the clock source, programmer should enable the corresponded module first by setting PMU_CONTROL register.	0x0

7.5.11. MISC2_CLKDIVH Register

Table 7-15 Description of MISC2_CLKDIVH Register

Bit	Name	Type	Description	Default
31:8	-	-	Reserved.	0
7:0	CLKDIVH	R/W	This register is used to control AHB clock divider. 0: Clock source divide by 1 1: Clock source divide by 2. 2: Clock source divide by 3. …. 255: Clock source divide by 256.	0x00

7.5.12. MISC2_CLKDIVP Register

Table 7-16 Description of MISC2_CLKDIVP Register

Bit	Name	Type	Description	Default
31:8	-	-	Reserved.	0

7:0	CLKDIVP	R/W	This register is used to control APB clock divider. 0: AHB clock divide by 1. 1: AHB clock divide by 2. 2: AHB clock divide by 3. …. 255: AHB clock divide by 256.	0x01

7.5.13. MISC2_HCLKEN Register

Table 7-17 Description of MISC2_HCLKEN Register

Bit	Name	Type	Description	Default
31:9	-	-	Reserved.	0
8:0	HCLKEN	R/W	This register is used to control clock enable of each AHB module. The corresponded module can be turned-off only when its function is not been used. Refer to Table 7-18 for detail about each module. 0: Disable. 1: Enable.	0x1FF

Table 7-18 HCLK clock enable of each module

Bit	Module	Note
0	--	
1	Arbiter & Bus Matrix	Shouldn't off when CPU or DMA is active.
2	FLASH Controller	Shouldn't off.
3	SRAM Controller	Shouldn't off.
4	DMA Controller	
5	GPIO Controller	
6	LCD Controller	
7	--	
8	CRYPT Controller	

7.5.14. MISC2_PCLKEN Register

Table 7-19 Description of MISC2_PCLKEN Register

Bit	Name	Type	Description	Default
31:0	PCLKEN	R/W	This register is used to control clock enable of each APB module. The corresponded module can be turned-off only when its function is not been used. Refer to Table 7-20 for detail about each module. 0: Disable. 1: Enable.	0xFFFFFFFF

Table 7-20 PCLK Clock Enable of Each Module

Bit	Module	Note
0	AHB2APB Bridge	Shouldn't off.
1	DMA Controller	
2	I2C	
3	SPI1	
4	UART0	
5	UART1	
6	UART2	
7	UART3	
8	UART4	
9	UART5	
10	ISO78160	
11	ISO78161	
12	Timer	
13	MISC	
14	MISC2	
15	PMU	
16	RTC	
17	ANA	
18	U32K 0	

19	U32K 1	
20	Reserved.	
21	SPI2.	
31:22	Reserved.	

8.Analog Controller

8.1. Introduction

The Analog controller is used to control the analog function of V85X3. All the analog related control like ADC, comparator and other analog flag detection are controlled by this module. The analog controller is placed in always-on domain, so all the analog setting will be kept under deep-sleep mode.

8.2. Feature

-- Interrupt/wake-up signal generated for analog detect flag.

-- Comparator interrupt generation.

-- Comparator counter.

-- ADC manual and auto sample mode.

-- ADC interrupt generation.

8.3. Block Diagram

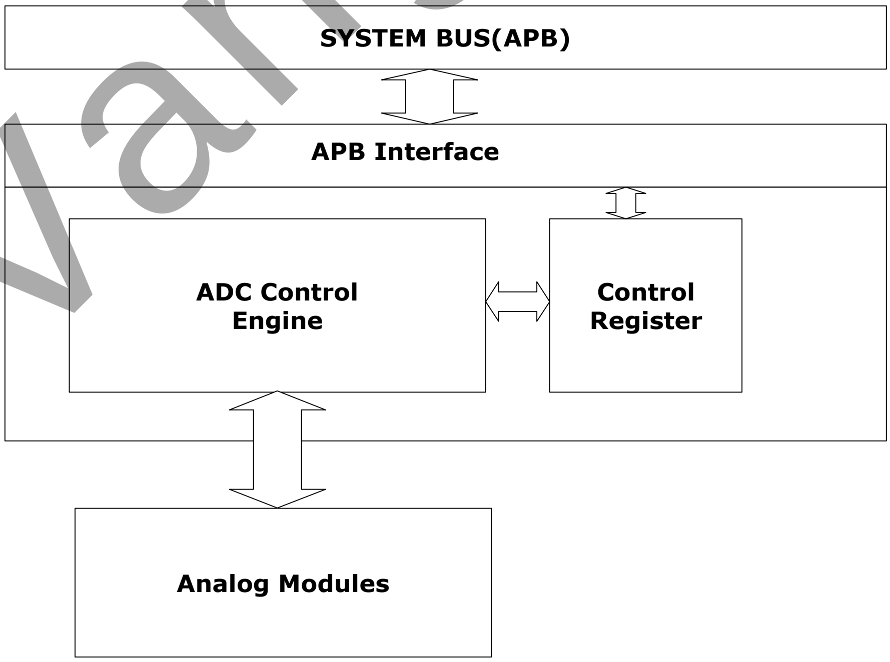


Figure 8-1 Functional Block Diagram of Analog Controller

8.4. Register Location

Table 8-1 Register Location of ANA Controller (ANA Base: 0x40014200)

Name	Type	Address	Description	Default
ANA_REG0	R/W	0x0000	Analog register 0	0x00
ANA_REG1	R/W	0x0004	Analog register 1	0x00
ANA_REG2	R/W	0x0008	Analog register 2	0x00
ANA_REG3	R/W	0x000C	Analog register 3	0x00
ANA_REG4	R/W	0x0010	Analog register 4	0x00
ANA_REG5	R/W	0x0014	Analog register 5	0x00
ANA_REG6	R/W	0x0018	Analog register 6	0x00
ANA_REG7	R/W	0x001C	Analog register 7	0x00
ANA_REG8	R/W	0x0020	Analog register 8	0x00
ANA_REG9	R/W	0x0024	Analog register 9	0x00
ANA_REGA	R/W	0x0028	Analog register 10	0x00
ANA_REGB	R/W	0x002C	Analog register 11	From FLASH
ANA_REGC	R/W	0x0030	Analog register 12	From FLASH
ANA_REGD	R/W	0x0034	Analog register 13	From FLASH
ANA_REGE	R/W	0x0038	Analog register 14	From FLASH
ANA_REGF	R/W	0x003C	Analog register 15	0x00
ANA_CTRL	R/W	0x0050	Analog control register	0x0000000
ANA_CMPOUT	R	0x0054	Comparator result register	0x0030
ANA_INTSTS	R/C	0x0060	Analog interrupt status register	0x0000
ANA_INTEN	R/W	0x0064	Analog interrupt enable register	0x0000
ANA_ADCCTRL	R/W	0x0068	ADC control register	0x00000000
ANA_ADCDATA0	R	0x0070	ADC channel 0 data register	--
ANA_ADCDATA1	R	0x0074	ADC channel 1 data register	--
ANA_ADCDATA2	R	0x0078	ADC channel 2 data register	--
ANA_ADCDATA3	R	0x007C	ADC channel 3 data register	--
ANA_ADCDATA4	R	0x0080	ADC channel 4 data register	--
ANA_ADCDATA5	R	0x0084	ADC channel 5 data register	--

ANA_ADCDATA6	R	0x0088	ADC channel 6 data register	--
ANA_ADCDATA7	R	0x008C	ADC channel 7 data register	--
ANA_ADCDATA8	R	0x0090	ADC channel 8 data register	--
ANA_ADCDATA9	R	0x0094	ADC channel 9 data register	--
ANA_ADCDATAA	R	0x0098	ADC channel 10 data register	--
ANA_ADCDATAB	R	0x009C	ADC channel 11 data register	--
ANA_CMPCNT1	R/C	0x00B0	Comparator 1 counter	0x00000000
ANA_CMPCNT2	R/C	0x00B4	Comparator 2 counter	0x00000000
ANA_MISC	R/W	0x00B8	Analog misc. control register	0x00

8.5. Register Definition

8.5.1. ANA_REGx Register

Table 8-2 Description of ANA_REGx

	Bit								
	7	6	5	4	3	2	1	0	Address
ANA_REG0	-	-	-		-		-		0x0000
ANA_REG1	-	-	GDE4	RESDIV	-				0x0004
ANA_REG2	-	-	REFSEL_CMP2	REFSEL_CMP1	CMP2_SEL[1:0]		CMP1_SEL[1:0]		0x0008
ANA_REG3	XOHPDN	PLLHPDN	PLLLPDN	RCHPD	BGPPD	CMP2PDN	CMP1PDN	ADCPDN	0x000C
ANA_REG4	-		-		-	-	-		0x0010
ANA_REG5	-	PD_AVCCDET	-	-	IT_CMP2[1:0]		IT_CMP1[1:0]		0x0014
ANA_REG6	BATRTCDISC	-	-	VLCD[3:0]				LCD_BMOD	0x0018
ANA_REG7	-	-	-	-	-	-	-	-	0x001C
ANA_REG8	PD_AVCCLDO	VDDPVDSEL[2:0]			-		-		0x0020
ANA_REG9	PD_VDDDET	PLLHSEL[3:0]				PLLLSEL[2:0]			0x0024
ANA_REGA	PD_VDCINDET	-	-	-	-	-	-	-	0x0028
ANA_REGB		-	-	RCLTRIM[4:0]					0x002C
ANA_REGC	-	-	RCHTRIM[5:0]						0x0030

ANA_REGD	-							0x0034
ANA_REGE	-							0x0038
ANA_REGF	ADTREF3_SEL	ADTREF2_SEL	ADTREF1_SEL	SEL_ADT	PDN_ADT	AVCCO_EN	-	0x003C

8.5.2. ANA_REG1 Register

Table 8-3 Description of each bit in ANA_REG1

Bit	Name	Function	Notes
3:0	-	Reserved.	0
4	RESDIV	Enable resistor division for M ADC's input signal	0: Disable 1: Enable 1/4 resistor division
5	GDE4	Enable cap division for M ADC's input signal	0: Disable 1: Enable 1/4 cap division
7:6	-	Reserved.	0

8.5.3. ANA_REG2 Register

Table 8-4 Description of each bit in ANA_REG2

Bit	Name	Function	Notes
1:0	CMP1_SEL[1:0]	Signal source selection of comparator A	00: CMP1_P to REF 01: CMP1_N to REF 1*: CMP1_P to CMP1_N
3:2	CMP2_SEL[1:0]	Signal source selection of comparator B	00: CMP2_P to REF 01: CMP2_N to REF 1*: CMP2_P to CMP2_N
4	REFSEL_CMP1	REF selection of CMP1	0: VREF 1: BGPREF.
5	REFSEL_CMP2	REF selection of CMP2	0: VREF 1: BGPREF.
7: 6		Reserved.	0

8.5.4. ANA_REG3 Register

Table 8-5 Description of each bit in ANA_REG3

Bit	Name	Function	Notes
0	ADCPDN	ADC power up control signal. ADC automatic conversion should be disabled before ADC is powered down.	0: Power-down ADC 1: Power-up ADC
1	CMP1PDN	CMP1 power up control signal	0: Power-down CMP1 1: Power-up CMP1
2	CMP2PDN	CMP2 power up control signal	0: Power-down CMP2 1: Power-up CMP2
3	BGPPD*	BGP power down control signal.	0: Power-up BGP 1: Power-down BGP
4	RCHPD	RCH (6.5536M RC) power down control signal	0: Power-up RCH 1: Power-down RCH
5	PLLLPDN	PLLL (32768Hz input PLL) power up control signal.	0: Power-down PLLL 1: Power-up PLLL
6	PLLHPDN	PLLH (6.5536MHz input PLL) power up control signal.	0: Power-down PLLH 1: Power-up PLLH
7	XOHPDN	6.5536M crystal power up control signal.	0: Power-down XOH 1: Power-up XOH
Note*: RCH and PLL and ADC are related to BGP, must power-up BGP before power-up RCH or PLL or ADC. User can power down BGP by set BGPPD to 1 when BGP was not used in program. User could not power down BGP by set BGPPD to 1 when BGP was used in program, because the system has a protection function to ensure reliability. User can power down BGP in sleep mode and deep-sleep mode whether BGP is used or not.			

8.5.5. ANA_REG4 Register

Table 8-6 Description of each bit in ANA_REG4

Bit	Name	Function	Notes
7:0	-	Reserved.	Default: 0x00, must be set to 0x01 by user.

8.5.6. ANA_REG5 Register

Table 8-7 Description of each bit in ANA_REG5

Bit	Name	Function	Notes

1:0	IT_CMP1[1:0]	Bias current selection of CMP1	00: 20nA;
			01: 100nA;
			1*: 500nA;

3:2	IT_CMP2[1:0]	Bias current selection of CMP2	00: 20nA;
			01: 100nA;
			1*: 500nA;

5:4	-	Reserved.	0
6	PD_AVCCDET	Power down AVCC low voltage detector.	0: Power-up AVCC LV detector. 1: Power-down detector.
7	-	Reserved.	0

8.5.7. ANA_REG6 Register

Table 8-8 Description of each bit in ANA_REG6

Bit	Name	Function	Notes
0	LCD_BMODE	LCD BIAS mode selection	0: 1/3 bias; 1: 1/4 bias.

4:1	VLCD[3:0]	LCD driving voltage	VLCD=0: default
			VLCD=0~5: adjust range =+60mV*VLCD
			VLCD=6~15: adjust range =-60mV*(VLCD-5)

6:5	-	Reserved.	0
7	BATRTCDISC	Discharge the BATRTC battery. Discharge resistance is 1.7k, and the discharge current is Vbatrtc / 1.7k.	1: enable 1.7k resistor from BATRTC to GND

8.5.8. ANA_REG7 Register

Table 8-9 Description of each bit in ANA_REG7

Bit	Name	Function	Notes
7:0	-	Reserved.	Default: 0x00, must be set to 0x00.

8.5.9. ANA_REG8 Register

Table 8-10 Description of each bit in ANA_REG8

Bit	Name	Function	Notes
3: 0	-	Reserved.	0
6:4	VDDPVDSEL[2:0]	Voltage selection of VDD power detector, the setting in this register will affect the status of VDDALARM.	000: 4.5V 001: 4.2V 010: 3.9V 011: 3.6V 100: 3.2V 101: 2.9V 110: 2.6V 111: 2.3V
7	PD_AVCCLDO	AVCCLDO control register, and control power-down or power-up of LDO.	0: Power up LDO, Voltage of AVCC pin is 3.3V. 1: Power down LDO, AVCC connect to VDD through a switch, and the switch resistor refer to table 1-4. AVCCLDO can be power down only when power supply less than 3.6V.

8.5.10. ANA_REG9 Register

Table 8-11 Description of each bit in ANA_REG9

Bit	Name	Function	Notes

2:0	PLLLSEL[2:0]	Frequency selection of PLLL	000: 26.2144MHz 001: 13.1072MHz 010: 6.5536MHz 011: 3.2768MHz 100: 1.6384MHz 101: 0.8192MHz 110: 0.4096MHz 111: 0.2048MHz
6:3	PLLHSEL[3:0]	Frequency selection of PLLH. The PLLH's frequency is the multiply of external XOH or internal RCH.	1000~1011: Reserved. 1100: 2 x Input clock 1101: 2.5 x Input clock 1110: 3 x Input clock 1111: 3.5 x Input clock 0000: 4 x Input clock 0001: 4.5 x Input clock 0010: 5 x Input clock 0011: 5.5 x Input clock 0100: 6 x Input clock 0101: 6.5 x Input clock 0110: 7 x Input clock 0111: 7.5 x Input clock
7	PD_VDDDET	Power down VDD input VDDALARM detector. This module powered by VDD.	0: Power up. 1: Power down.

8.5.11. ANA_REGA Register

Table 8-12 Description of each bit in ANA_REGA

Bit	Name	Function	Notes
6:0	-	Reserved.	Default: 0x00, must be set to 0x0A.
7	PD_VDCINDET	PD VDCIN detector	0: Power up

			1: Power down

8.5.12. ANA_REGB Register

Table 8-13 Description of each bit in ANA_REGB

Bit	Name	Function	Notes

4:0	RCLTRIM[4:0]	Trimming of 32kHz RC.	00000~01111: increased by 4% for each step;
			10000~11111: decreased by 4% for each step;

7:5	VREFTRIM[2:0]	Trimming of VREF, which will affect DVCC/AVCC's output by same ratio	011: +9%; 010: +6%; 001: +3%; 000: 0%; 100: -3%; 101: -6%; 110: -9%; 111: -12%;
Note: Users must not modify the configuration of ANA_REGx(x=B~E), it can be loaded from FLASH automatically.			

8.5.13. ANA_REGC Register

Table 8-14 Description of each bit in ANA_REGC

Bit	Name	Function	Notes

5:0	RCHTRIM[5:0]	Trimming of 6.5536MHz RC	000000~011111:increased by 1.25% for each step;
			100000~111111:decreased by 1.25% for each step;

7:6	-	Reserved.	0
Note: Users must not modify the configuration of ANA_REGx(x=B~E), it can be loaded from FLASH automatically.			

8.5.14. ANA_REGF Register

Table 8-15 Description of each bit in ANA_REGF

Bit	Name	Function	Notes
1:0	-	Reserved.	0
2	AVCCO_EN	Enable AVCC_OUT pin to output AVCC level.	0: High resistance. 1: AVCC_OUT pin output AVCC level, and it can be used to drive small power module.
3	PDN_ADT	Power up Tiny ADC	0: Power down. 1: Power up
4	SEL_ADT	Signal selection for ADT	0: Connect to IOE6 1: Connect to IOE7
5	ADTREF1_SEL	REF1 of ADT selection	0: 0.9V 1: 0.7V
6	ADTREF2_SEL	REF2 of ADT selection	0: 1.8V 1: 1.6V
7	ADTREF3_SEL	REF3 of ADT selection	0: 2.7V 1: 2.5V

8.5.15. ANA_CTRL Register

Table 8-16 Description of ANA_CTRL Register

Bit	Name	Type	Description	Default
31: 27	-	R/W	Reserved.	0
26	PDNS2	R/W	This register is used to set the deep sleep behavior when VDDALARM is 0 (Still need to consider the PDNS setting). 0: Can't enter deep-sleep mode when VDDALARM is 0. When VDDALARM is 1, The system can enter deep-sleep mode. And system will wake-up from deep-sleep mode automatically as long as VDDALARM became 0. 1: Can enter deep-sleep mode no-matter which state VDDALARM is.	0x0

25:24	VDCINDEB	R/W	VDCIN de-bounce control register. 0: No de-bounce. 1: 2 RTCCLK de-bounce. 2: 3 RTCCLK de-bounce. 3: 4 RTCCLK de-bounce. When de-bounce is enabled, the input signal is valid only when the signal isn’t change in multi-cycles of RTCCLK clock. And, the response time of the wake-up and interrupt will be delayed until the signal is valid. This circuit can work under all mode including sleep and deep-sleep mode.	0x0
23:22	CMP2DEB	R/W	Comparator 2 de-bounce control register. 0: No de-bounce. 1: 2 RTCCLK de-bounce. 2: 3 RTCCLK de-bounce. 3: 4 RTCCLK de-bounce. When de-bounce is enabled, the input signal is valid only when the signal isn’t change in multi-cycles of RTCCLK clock. And, the response time of the wake-up and interrupt will be delayed until the signal is valid. This circuit can work under all mode including sleep and deep-sleep mode.	0x0
21:20	CMP1DEB	R/W	Comparator 1 de-bounce control register. 0: No de-bounce. 1: 2 RTCCLK de-bounce. 2: 3 RTCCLK de-bounce. 3: 4 RTCCLK de-bounce. When de-bounce is enabled, the input signal is valid only when the signal isn’t change in multi-cycles of RTCCLK clock. And, the response time of the wake-up and interrupt will be delayed until the signal is valid. This circuit can work under all mode including sleep and deep-sleep mode.	0x0
19:16	-	-	Reserved.	0
15:8	RCHTGT	R/W	RCH auto calibration target register. This register is used to store the target value of RCH. When the target	0x0

			frequency is 6.5536MHz, user should fill 6553600/32768 = 200 to this register.	
7	-	-	Reserved.	0
6	PDNS	R/W	This register is used to set the deep sleep behavior when VDCINDROP is 0(Still need to consider the PDNS setting). 0: Can't enter deep-sleep mode when VDCINDROP is 0. When VDCINDROP is 1, The system can enter deep-sleep mode. And system will wake-up from deep-sleep mode automatically as long as VDCINDROP became 0. 1: Can enter deep-sleep mode no-matter which state VDCINDROP is.	0x0
5:4	-	-	Reserved.	0
3:2	COMP2_SEL	R/W	This register is used to control the interrupt and wake-up signal generation of COMP2. 0: Off. 1: Rising edge of COMP2. 2: Falling edge of COMP2. 3: Change of COMP2.	0x0
1:0	COMP1_SEL	R/W	This register is used to control the interrupt and wake-up signal generation of COMP1. 0: Off. 1: Rising edge of COMP1. 2: Falling edge of COMP1. 3: Change of COMP1.	0x0

8.5.16. ANA_CMPOUT Register

Table 8-17 Description of ANA_CMPOUT Register

Bit	Name	Type	Description	Default
31:16	-	-	Reserved.	0
15:14	TADCO	R	Tiny ADC output.	-
13:11	-	-	Reserved.	0
10	AVCCLV	R	AVCC low power status. And hysteresis voltage of	0x0

			AVCCLV is 20mV~30mV. 0: AVCC is higher than 2.5V. 1: AVCC is lower than 2.5V.	
9	-	-	Reserved.	0
8	VDCINDROP	R	VDCIN drop status 0: VDCIN is not drop (VDCIN higher than threshold). 1: VDCIN is drop (i.e. VDCIN lower than threshold).	0x0
7	VDDALARM	R	This bit shows the output of VDDALARM. 0: Voltage of VDD is higher than voltage setting by VDDPVDSEL. 1: Voltage of VDD is lower than voltage setting by VDDPVDSEL.	0x0
6:4	-	-	Reserved.	0
3	COMP2	R	This bit shows the output of comparator 2.	0x0
2	COMP1	R	This bit shows the output of comparator 1.	0x0
1	LOCKL	R	PLLL lock status. It takes about 1ms until PLLL locked. 0: PLLL is not lock. 1: PLLL is lock.	0x0
0	LOCKH	R	PLLH lock status. It takes about 15μs until PLLH locked. 0: PLLH is not lock. 1: PLLH is lock.	0x0

8.5.17. ANA_INSTS Register

Table 8-18 Description of ANA_INTSTS Register

Bit	Name	Type	Description	Default
31:14	-	-	Reserved.	0
13	INTSTS13	R/C	TADC change over-threshold interrupt. This interrupt will be set when the TADC is rising or falling and the change value compare to previous cycle is larger than	0x0

			the threshold setting in the TADCTH in ANA_MISC register, this interrupt flag will be set. Read 0: No TADC over threshold interrupt. Read 1: TADC over threshold is happened. Write 0: No effect. Write 1: clear this bit.	
12	INTSTS12	R/C	ANA_REGx error flag. This interrupt is used to detect the error status of ANA_REGx, an automatically check0sum and parity check is applied to ANA_REGx, when external noise cause by ESD or other problem affect the setting of ANA_REGx, this interrupt will be asserted and programmer can use this flag to determine if it is necessary to recover the setting in the ANA_REGx. Read 0: No ANA_REGx error interrupt. Read 1: ANA_REGx error is happened. Write 0: No effect. Write 1: clear this bit.	0x0
11	INTSTS11	R/C	Interrupt flag of sleep mode entry under VDCINDROP is 0(i.e. VDCIN higher than threshold), this interrupt will be generated when VDCINDROP is 0 and the entry of sleep or deep-sleep modes are detected. Programmer can enable this interrupt to force CPU wake-up from sleep or deep-sleep mode when VDCINDROP is 0. Read 0: No Sleep mode entry interrupt. Read 1: Sleep mode entry interrupt is happened. Write 0: No effect. Write 1: clear this bit.	0x0
10	INTSTS10	R/C	Interrupt flag of AVCCLV (AVCC low power status), this interrupt will be generated when AVCCLV rising or falling. Read 0: No AVCCLV interrupt. Read 1: AVCCLV interrupt is happened. Write 0: No effect. Write 1: clear this bit.	0x0
9	-	-	Reserved.	0
8	INTSTS8	R/C	Interrupt flag of VDCINDROP (VDCIN status), this	0x0

			interrupt will be generated when VDCINDROP rising or falling. Read 0: No VDCINDROP interrupt. Read 1: VDCINDROP interrupt is happened. Write 0: No effect. Write 1: clear this bit.	
7	INTSTS7	R/C	Interrupt flag of VDDALARM (VDD status), this interrupt will be generated when VDDALARM rising or falling. Read 0: No VDDALARM interrupt. Read 1: VDDALARM interrupt is happened. Write 0: No effect. Write 1: clear this bit.	0x0
6:4	-	-	Reserved.	0
3	INTSTS3	R/C	Interrupt flag of COMP2, the interrupt generate condition is controlled by COMP2_SEL. Read 0: No COMP2 interrupt. Read 1: COMP2 interrupt is happened. Write 0: No effect. Write 1: clear this bit.	0x0
2	INTSTS2	R/C	Interrupt flag of COMP1, the interrupt generate condition is controlled by COMP1_SEL. Read 0: No COMP1 interrupt. Read 1: COMP1 interrupt is happened. Write 0: No effect. Write 1: clear this bit.	0x0
1	INTSTS1	R/C	Interrupt flag of auto ADC conversion done. Read 0: Auto ADC conversion not complete. Read 1: Auto ADC conversion has done. Write 0: No effect. Write 1: clear this bit.	0x0
0	INTSTS0	R/C	Interrupt flag of manual ADC conversion done. Read 0: Manual ADC conversion not complete.	0x0

			Read 1: Manual ADC conversion has done. Write 0: No effect. Write 1: clear this bit.	

8.5.18. ANA_INTEN Register

Table 8-19 Description of ANA_INTEN Register

Bit	Name	Type	Description	Default
31:14	-	-	Reserved.	0
13	INTEN13	R/W	Interrupt and wake-up enable control of the change in TADC output value is over or equal to threshold. 0: Disable TADC interrupt and wake-up. 1: Enable TADC interrupt and wake-up.	0x0
12	INTEN12	R/W	Interrupt and wake-up enable control of ANA_REGx error. 0: Disable ANA_REGx error interrupt and wake-up. 1: Enable ANA_REGx error interrupt and wake-up.	0x0
11	INTEN11	R/W	Interrupt and wake-up enable control of sleep mode entry, when VDCINDROP is 0(i.e. VDCIN higher than threshold). Programmer can enable this interrupt to force CPU wake-up from sleep or deep-sleep mode when VDCINDROP is 0 and the entry of sleep or deep-sleep modes are detected. 0: Disable Sleep mode entry interrupt and wake-up. 1: Enable Sleep mode entry interrupt and wake-up.	0x0
10	INTEN10	R/W	Interrupt and wake-up enable control of AVCCLV. 0: Disable AVCCLV interrupt and wake-up. 1: Enable AVCCLV interrupt and wake-up.	0x0
9	-	-	Reserved.	0
8	INTEN8	R/W	Interrupt and wake-up enable control of VDCINDROP. 0: Disable VDCINDROP interrupt and wake-up. 1: Enable VDCINDROP interrupt and wake-up.	0x0
7	INTEN7	R/W	Interrupt and wake-up enable control of VDDALARM.	0x0

			0: Disable VDDALARM interrupt and wake-up. 1: Enable VDDALARM interrupt and wake-up.	
6:4	-	-	Reserved.	0
3	INTEN3	R/W	Interrupt and wake-up enable control of COMP2. 0: Disable COMP2 interrupt and wake-up. 1: Enable COMP2 interrupt and wake-up.	0x0
2	INTEN2	R/W	Interrupt and wake-up enable control of COMP1. 0: Disable COMP1 interrupt and wake-up. 1: Enable COMP1 interrupt and wake-up.	0x0
1	INTEN1	R/W	Interrupt enable control of auto ADC conversion done. 0: Disable auto ADC conversion interrupt. 1: Enable auto ADC conversion interrupt.	0x0
0	INTEN0	R/W	Interrupt enable control of manual ADC conversion done. 0: Disable manual ADC conversion interrupt. 1: Enable manual ADC conversion interrupt.	0x0

8.5.19. ANA_ADCCTRL Register

Table 8-20 Description of ANA_ADCCTRL Register

Bit	Name	Type	Description	Default
31	MTRIG	R/W	Manual ADC trigger. Write 0: No effect. Write 1: Start a manual ADC conversion. Read 0: Current manual ADC conversion is done. Read 1: Current manual ADC conversion is ongoing.	0x0
30	-	-	Reserved.	0
29	CICAON	R/W	CIC filter always on control register. 0: CIC filter will be disabled when no ADC sample process is ongoing. 1: CIC filter will be enabled for all the time.	0x0
28	CICINV	R/W	CIC filter input inversion.	0x0

			0: No invert CIC filter input. 1: Invert CIC filter input.	
27	CICSCA	R/W	CIC output scale-down selection. 0: No scale down CIC filter's output. 1: Scale down CIC filter's output to 1/2.	0x0
26:24	CICSKIP	R/W	CIC output skip control register. This register is used to control how many samples will be skipped at the beginning of ADC sample. If CICAON is 1 and the ADC channel is not changed, the CIC output will not be skipped by the ADC controller, this can be used for high speed capture to single channel. 0: Skip first 4 samples. 1: Skip first 5 samples. 2: Skip first 6 samples. 3: Skip first 7 samples. 4: No skip any sample. 5: Skip first 1 sample. 6: Skip first 2 samples. 7: Skip first 3 samples.	0x0
23:22	DSRSEL	R/W	CIC down sampling rate control register. The higher down-sampling rate, the higher output data stability, and lower sampling rate. 0: 1/512 down-sampling rate. 1: 1/256 down-sampling rate. 2: 1/128 down-sampling rate. 3: 1/64 down-sampling rate.	0x0
21	AMODE	R/W	Auto ADC mode control. 0: Capture single channel specified by ACH. 1: Capture multiple channels (0~11 channels) at one time.	0x0
20	MMODE	R/W	Manual ADC mode control. 0: Capture single channel specified by MCH. 1: Capture multiple channels (0~11 channels) at one time.	0x0

19	-	-	Reserved.	0x0
18:16	AEN	R/W	Auto ADC conversion enable control register. 0: Auto ADC conversion is off. 4: Auto ADC will be triggered by timer 0's overflow. 5: Auto ADC will be triggered by timer 1's overflow. 6: Auto ADC will be triggered by timer 2's overflow. 7: Auto ADC will be triggered by timer 3's overflow.	0x0
15:13	-	-	Reserved.	0
12	CLKSEL	R/W	ADC clock source selection. 0: 6.5M RCH 1: PLLL	0x0
11:8	CLKDIV	R/W	The ADC clock source is internal 6.5M RCH or PLLL. The typical ADC main clock is 1.6384MHz, if ADC clock source is 6.5M RCH, CLKDIV is calculated such as: CLKDIV=6.5536/1.6384-1=3.	0x0
7:4	ACH	R/W	Auto ADC channel control. 0: Auto ADC capture ADC channel 0. 1: Auto ADC capture ADC channel 1. .... 11: Auto ADC capture ADC channel 11. 12~15: Reserved. This register is valid only when AMODE is 0.	0x0
3:0	MCH	R/W	Manual ADC channel control. 0: Manual ADC capture ADC channel 0. 1: Manual ADC capture ADC channel 1. .... 11: Auto ADC capture ADC channel 11. 12~15: Reserved. This register is valid only when MMODE is 0.	0x0

8.5.20. ANA_ADCDATAx Register

Table 8-21 Description of ANA_ADCDATAx Register

Bit	Name	Type	Description	Default
31:16	-	-	Reserved.	0
15:0	ADCDATAx	R	The result of ADC conversion will be stored in these registers. DATA0: Store conversion result of ADC channel 0. DATA1: Store conversion result of ADC channel 1. … DATA11: Store conversion result of ADC channel 11. For single channel conversion (MMODE is 0 or AMODE is 0), only the channel specified by MCH or ACH will be updated. For multi-channels conversion (MMODE is 1 or AMODE is 1), DATA0~DATA11 will be updated.	0x--

8.5.21. ANA_CMPCNTx Register

Table 8-22 Description of ANA_CMPCNTx Register

Bit	Name	Type	Description	Default
31:0	CNTx	R/C	This register stores the happen times of comparator x according to the setting in COMPx_SEL. For example, when COMPx_SEL is set to 1, then this counter will increase 1 when the COMPx is rising. This register can be cleared by writing 0 to this register, but this operation is valid only when corresponded CMPPDNx is set to 1 (when the corresponded comparator is enabled).	0x0000000

8.5.22. ANA_MISC Register

Table 8-23 Description of ANA_MISC Register

Bit	Name	Type	Description	Default
31:6	-	-	Reserved.	0
5:4	TADCTH	R/W	TADC threshold setting. This register controls the threshold of TADC’s interrupt. The TADC is using internal 32K RC as clock source to sample external signal, when	0x0

			TADC’s interrupt is enable and the difference of two continuous cycles is larger than TADCTH, the INTSTS13 will be set and an interrupt will be asserted.	
3:0	-	-	Reserved.	0

9.ADC Controller

9.1. Introduction

One second-order Σ-ΔADC is designed in 12 channels of the V85X3 for analog-to-digital conversion, and their full measurement scale is 0~1.2V if no voltage division. After set voltage division, when main power supply is 3.3V, the measurement scale is 0~3.6V. When main power supply is 5V, the measurement scale is 0~4.6V in cap division mode, and the measurement scale is 0~5.2V in resistor division mode. The ADC can be used to measure the ground, temperature, VDD, BATRTC voltage and external voltage signals. The clock source is 6.5536M RC or PLLL. The ADC controller is placed in always-on domain, so all the ADC setting will be kept under deep-sleep mode.

9.2. Feature

-- ADC manual and auto sample mode.
-- ADC interrupt generation.

9.3. Block Diagram

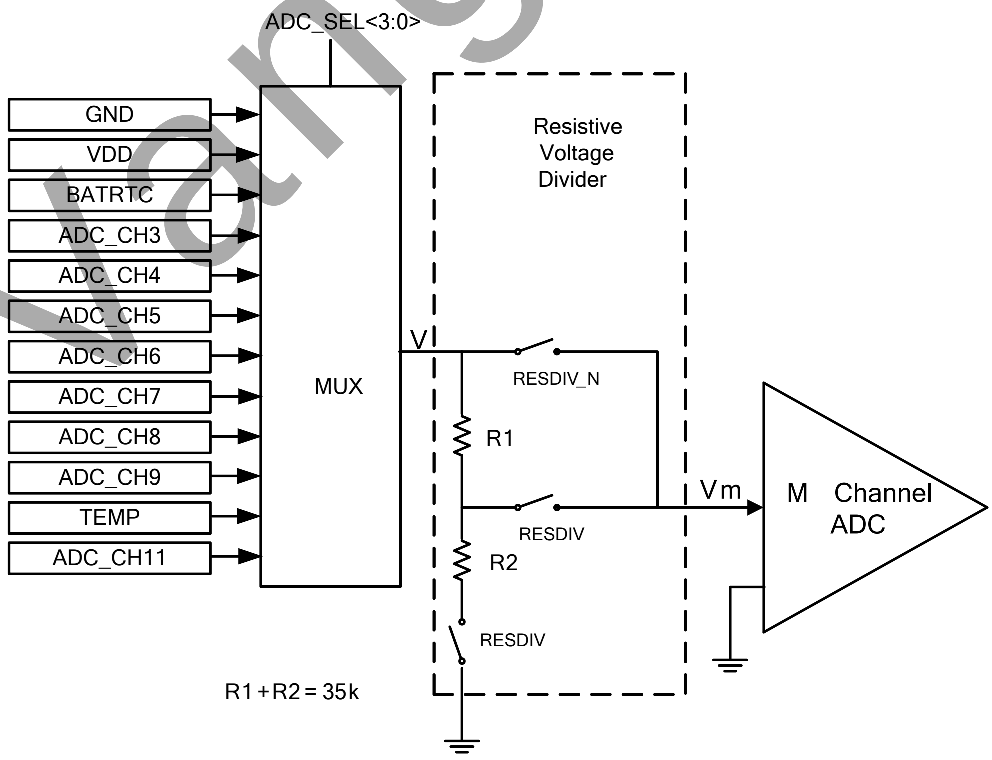


Figure 9-1 ADC Architecture

9.4. Register Location

Table 9-1 Register Location of ANA Controller for ADC (ANA Base: 0x40014200)

Name	Type	Address	Description	Default
ANA_REG0	R/W	0x0000	Analog register 0	0x00
ANA_REG1	R/W	0x0004	Analog register 1	0x00
ANA_REG3	R/W	0x000C	Analog register 3	0x00
ANA_INTSTS	R/C	0x0060	Analog interrupt status register	0x0000
ANA_INTEN	R/W	0x0064	Analog interrupt enable register	0x0000
ANA_ADCCTRL	R/W	0x0068	ADC control register	0x00000000
ANA_ADCDATA0	R	0x0070	ADC channel 0 data register	--
ANA_ADCDATA1	R	0x0074	ADC channel 1 data register	--
ANA_ADCDATA2	R	0x0078	ADC channel 2 data register	--
ANA_ADCDATA3	R	0x007C	ADC channel 3 data register	--
ANA_ADCDATA4	R	0x0080	ADC channel 4 data register	--
ANA_ADCDATA5	R	0x0084	ADC channel 5 data register	--
ANA_ADCDATA6	R	0x0088	ADC channel 6 data register	--
ANA_ADCDATA7	R	0x008C	ADC channel 7 data register	--
ANA_ADCDATA8	R	0x0090	ADC channel 8 data register	--
ANA_ADCDATA9	R	0x0094	ADC channel 9 data register	--
ANA_ADCDATAA	R	0x0098	ADC channel 10 data register	--
ANA_ADCDATAB	R	0x009C	ADC channel 11 data register	--

9.5. Register Definition

9.5.1. ANA_REG1 Register

Table 9-2 Description of each bit in ANA_REG1 of ADC

Bit	Name	Function	Notes
3:0	-	Reserved.	0

4	RESDIV	Enable resistor division for M ADC's input signal	0: Disable 1: Enable 1/4 resistor division
5	GDE4	Enable cap division for M ADC's input signal	0: Disable 1: Enable 1/4 cap division
7:6	-	Reserved.	0

9.5.2. ANA_REG3 Register

Table 9-3 Description of each bit in ANA_REG3 of ADC

Bit	Name	Function	Notes
0	ADCPDN	ADC power up control signal. ADC automatic conversion should be disabled before ADC is powered down.	0: Power-down ADC 1: Power-up ADC
3	BGPPD*	BGP power down control signal.	0: Power-up BGP 1: Power-down BGP
4	RCHPD	RCH (6.5536M RC) power down control signal	0: Power-up RCH 1: Power-down RCH
Note*: RCH and PLL and ADC are related to BGP, must power-up BGP before power-up RCH or PLL or ADC. User can power down BGP by set BGPPD to 1 when BGP was not used in program. User could not power down BGP by set BGPPD to 1 when BGP was used in program, because the system has a protection function to ensure reliability. User can power down BGP in sleep mode and deep-sleep mode whether BGP is used or not.			

9.5.3. ANA_INSTS Register

Table 9-4 Description of ANA_INTSTS Register for ADC

Bit	Name	Type	Description	Default
1	INTSTS1	R/C	Interrupt flag of auto ADC conversion done. Read 0: Auto ADC conversion not complete. Read 1: Auto ADC conversion has done. Write 0: No effect. Write 1: clear this bit.	0x0
0	INTSTS0	R/C	Interrupt flag of manual ADC conversion done.	0x0

			Read 0: Manual ADC conversion not complete. Read 1: Manual ADC conversion has done. Write 0: No effect. Write 1: clear this bit.	

9.5.4. ANA_INTEN Register

Table 9-5 Description of ANA_INTEN Register for ADC

Bit	Name	Type	Description	Default
1	INTEN1	R/W	Interrupt enable control of auto ADC conversion done. 0: Disable auto ADC conversion interrupt. 1: Enable auto ADC conversion interrupt.	0x0
0	INTEN0	R/W	Interrupt enable control of manual ADC conversion done. 0: Disable manual ADC conversion interrupt. 1: Enable manual ADC conversion interrupt.	0x0

9.5.5. ANA_ADCCTRL Register

Table 9-6 Description of ANA_ADCCTRL Register

Bit	Name	Type	Description	Default
31	MTRIG	R/W	Manual ADC trigger. Write 0: No effect. Write 1: Start a manual ADC conversion. Read 0: Current manual ADC conversion is done. Read 1: Current manual ADC conversion is ongoing.	0x0
30	-	-	Reserved.	0
29	CICAON	R/W	CIC filter always on control register. 0: CIC filter will be disabled when no ADC sample process is ongoing. 1: CIC filter will be enabled for all the time.	0x0
28	CICINV	R/W	CIC filter input inversion.	0x0

			0: No invert CIC filter input. 1: Invert CIC filter input.	
27	CICSCA	R/W	CIC output scale-down selection. 0: No scale down CIC filter's output. 1: Scale down CIC filter's output to 1/2.	0x0
26:24	CICSKIP	R/W	CIC output skip control register. This register is used to control how many samples will be skipped at the beginning of ADC sample. If CICAON is 1 and the ADC channel is not changed, the CIC output will not be skipped by the ADC controller, this can be used for high speed capture to single channel. 0: Skip first 4 samples. 1: Skip first 5 samples. 2: Skip first 6 samples. 3: Skip first 7 samples. 4: No skip any sample. 5: Skip first 1 sample. 6: Skip first 2 samples. 7: Skip first 3 samples.	0x0
23:22	DSRSEL	R/W	CIC down sampling rate control register. The higher down-sampling rate, the higher output data stability, and lower sampling rate. 0: 1/512 down-sampling rate. 1: 1/256 down-sampling rate. 2: 1/128 down-sampling rate. 3: 1/64 down-sampling rate.	0x0
21	AMODE	R/W	Auto ADC mode control. 0: Capture single channel specified by ACH. 1: Capture multiple channels (0~11 channels) at one time.	0x0
20	MMODE	R/W	Manual ADC mode control. 0: Capture single channel specified by MCH. 1: Capture multiple channels (0~11 channels) at one time.	0x0

19	-	-	Reserved.	0
18:16	AEN	R/W	Auto ADC conversion enable control register. 0: Auto ADC conversion is off. 4: Auto ADC will be triggered by timer 0's overflow. 5: Auto ADC will be triggered by timer 1's overflow. 6: Auto ADC will be triggered by timer 2's overflow. 7: Auto ADC will be triggered by timer 3's overflow. Others: Reserved.	0x0
15:13	-	-	Reserved.	0
12	CLKSEL	R/W	ADC clock source selection. The system forced ADC clock source to RCH when the RTC auto-calibration is enabled. 0: 6.5M RCH 1: PLLL	0x0
11:8	CLKDIV	R/W	The ADC clock source is internal 6.5M RCH or PLLL. The typical ADC main clock is 1.6384MHz, if ADC clock source is 6.5M RCH, CLKDIV is calculated such as: CLKDIV=6.5536/1.6384-1=3.	0x0
7:4	ACH	R/W	Auto ADC channel control. 0: Auto ADC capture ADC channel 0. 1: Auto ADC capture ADC channel 1. …. 11: Auto ADC capture ADC channel 11. 12~15: Reserved. This register is valid only when AMODE is 0. The ADC sampling channels show as the following table.	0x0
3:0	MCH	R/W	Manual ADC channel control. 0: Manual ADC capture ADC channel 0. 1: Manual ADC capture ADC channel 1. …. 11: Auto ADC capture ADC channel 11. 12~15: Reserved.	0x0

			This register is valid only when MMODE is 0. The ADC sampling channels show as the following table.	

Table 9-7 The ADC Sampling Channels

Bit	Name	value
7:4	ACH	0000: GND; 0001: VDD 0010: BATRTC; 0011: ADC_CH3 0100: ADC_CH4; 0101: ADC_CH5 0110: ADC_CH6; 0111: ADC_CH7 1000: ADC_CH8; 1001: ADC_CH9 1010: TEMP; 1011: ADC_CH11 1100~1111: Reserved.
3:0	MCH	

9.5.6. ANA_ADCDATAx Register

Table 9-8 Description of ANA_ADCDATAx Register

Bit	Name	Type	Description	Default
31:16	-	-	Reserved.	0
15:0	ADCDATAx	R	The result of ADC conversion will be stored in these registers. DATA0: Store conversion result of ADC channel 0. DATA1: Store conversion result of ADC channel 1. ... DATA11: Store conversion result of ADC channel 11. For single channel conversion (MMODE is 0 or AMODE is 0), only the channel specified by MCH or ACH will be	0x--

			updated. For multi-channels conversion (MMODE is 1 or AMODE is 1), DATA0~DATA11 will be updated.	

9.6. Measuring Battery Voltage and External Voltage

In the V85X3, ADC can be used to measure external voltage signals by ADC_CHx, and can be used to measure VDD/BATRTC signals.

ADC channel mode: single channel; multi-channel.

ADC trigger mode: auto triggered by timer; manual trigger.

Divider mode: no divider; resistive divider; capacitive divider. Resistance voltage divider has extra power consumption. Because there are 35kΩ resistors in the internal resistive divider network, this network consumes power:

$$P = U_D \times I_D = V \times \frac{V}{R_1 + R_2} = \frac{V^2}{35}$$

Equation 9-1

The voltage of ordinary channels (ADC_CHx): channel 3, 4, 5, 6, 7, 8, 9 and 11.

The voltage of VDD channels: channel 1.

The voltage of BATRTC channels: channel 2.

User needs to check whether a and b (A and B) parameters of storage area used to store ADC coefficients are legal. If so, the data of the storage area is used for calculation; if not, the ADC coefficient is used for calculation with fixed parameters. The calculation formula is shown in Table 4-20 Info Information Register, voltage measuring range and formula. A and b (a and b) of ADC coefficients are shown in Table 4-20 Info Information Register.

Table 9-9 Voltage measurement range and formula

Power	Channel	Divider Mode	Signal range (V)	Formula
3.3V	ADC_CHx	No divider	-0.2~1.2	If a and b parameters of ADC are valid, $V_{DC} = a1 \div 100000000 * X + b1 \div 100000000$ else $V_{DC} = 0.000036\,80 * X + 0.00205011$
		Resistive	-0.2~3.6	If a and b parameters of ADC are valid, $V_{DC} = a2 \div 100000000 * X + b2 \div 100000000$ else $V_{DC} = 0.00016425 * X + 0.03739179$

		Capacitive	-0.2~3.6	If a and b parameters of ADC are valid, $V_{DC} = a3 \div 100000000 * X + b3 \div 100000000$ else $V_{DC} = 0.00014051 * X - 0.00023322$
	VDD channels	Resistive	2.5~4.8	If a and b parameters of ADC are valid, $V_{DC} = a4 \div 100000000 * X + b4 \div 100000000$ else $V_{DC} = 0.00015392 * X + 0.06667986 + \mathrm{OffsetBatR} \div 1000$
		Capacitive	2.5~4.6	If a and b parameters of ADC are valid, $V_{DC} = a5 \div 100000000 * X + b5 \div 100000000$ else $V_{DC} = 0.00014107 * X - 0.00699515 + \mathrm{OffsetBatC} \div 1000$
	BATRTC channels	Resistive	0.7~4.8	If a and b parameters of ADC are valid, $V_{DC} = a6 \div 100000000 * X + b6 \div 100000000$ else $V_{DC} = 0.00015392 * X + 0.06667986 + \mathrm{OffsetBatR} \div 1000$
		Capacitive	0.7~4.6	If a and b parameters of ADC are valid, $V_{DC} = a7 \div 100000000 * X + b7 \div 100000000$ else $V_{DC} = 0.00014107 * X - 0.00699515 + \mathrm{OffsetBatC} \div 1000$
5V	ADC_CHx	No divider	-0.2~1.2	If A and B parameters of ADC are valid, $V_{DC} = A1 \div 100000000 * X + B1 \div 100000000$ else $V_{DC} = 0.000036\ 78 * X + 0.00235783$
		Resistive	-0.2~4.8	If A and B parameters of ADC are valid, $V_{DC} = A2 \div 100000000 * X + B2 \div 100000000$ else $V_{DC} = 0.00016129 * X + 0.00673599$
		Capacitive	-0.2~4.6	If A and B parameters of ADC are valid, $V_{DC} = A3 \div 100000000 * X + B3 \div 100000000$ else $V_{DC} = 0.00014076 * X - 0.00753319$
	VDD channels	Resistive	2.5~4.8	If A and B parameters of ADC are valid, $V_{DC} = A4 \div 100000000 * X + B4 \div 100000000$ else $V_{DC} = 0.00015392 * X + 0.06667986 + \mathrm{OffsetBatR} \div 1000$
		Capacitive	2.5~4.6	If A and B parameters of ADC are valid,

				$V_{DC} = A5 \div 100000000 * X + B5 \div 100000000$ else $V_{DC}=0.00014107 * X - 0.00699515 + OffsetBatC \div 1000$
	BATRTC channels	Resistive	0.7~4.8	If A and B parameters of ADC are valid, $V_{DC} = A6 \div 100000000 * X + B6 \div 100000000$ else $V_{DC}=0.00015392 * X + 0.06667986 + OffsetBatR \div 1000$
		Capacitive	0.7~4.6	If A and B parameters of ADC are valid, $V_{DC} = A7 \div 100000000 * X + B7 \div 100000000$ else $V_{DC}=0.00014107 * X - 0.00699515 + OffsetBatC \div 1000$

In the above equations,

$$X = ADC\_DATAx$$

Equation 9-2

Where:

ADC_DATAx is the content of bytes located at addresses (0x40014270+4x), x is channel 0~11.

9.7. Measuring Temperature

When the ADC channel you choose is TEMPERATURE (CH10), you should not set capacitive division. The temperature measurement range is over -40~+105°C.

It is recommended to measure temperature following steps:

1. Set ADC to start working.

Users must set ADC CLK to 1.6384 MHz, and set DSRSEL to 1/512 down-sampling rate, with no voltage division or resistor division, then start ADC conversion.

2. Wait for read 1 from ANAINSTS (0x40014260) (ANAINTSTS0 (bit 0)/ ANAINSTS1(bit 1) in auto/manual mode), and then read the register ADC_DATAA (0x40014298).

3. Calibrate temperature T: (in unit of 8.8 format ℃). The format of T is 16-bit signed value, including 8 bits integer and 8 bits fraction signed value. The actual temperature is equal to T/256.0. For example, 0x1880 means 24.5 ℃.

$$T = ((P0 * ((X * X) >> 16)) + P1 * X + P2) >> 8$$

Equation 9-3

where X is the reading of register ADC_DATAA(in hexadecimal);

where P0 is the content of bytes located at addresses 0x40D00(16bit);

where P1 is the content of bytes located at addresses 0x40D02(16bit);

where P2 is calculated by the following equation:

$P2 = P2' + (Tr - Tm) * 256$	Equation 9-4

where P2' is the content of bytes located at addresses 0x40D04(32bit);

where Tr is the content of bytes located at addresses 0x40D70(32bit);

where Tm is the content of bytes located at addresses 0x40D74(32bit).

Note:

To enhance ADC data quality in the channel 10 for the temperature sensor, four-sample moving average is implemented. The four buffers used to average are first-in first-out queues, which are reset to zero by DPOR. Every time a user makes an ADC conversion, the hardware writes a data to the buffer, and calculates the average value of the data of the four buffers inside, and puts it in the register of ADC_DATAA. Therefore, in order to get the exact temperature value of a certain temperature, users need to convert ADC four times continuously and take the last ADC_DATAA register data as ADC data.

10. Comparator Controller

10.1. Introduction

The V85X3 integrates two comparators to compare the analog signals. Three patterns can be selected as input sources:

- Positive signal input on pin CMP_P and negative signal input on pin CMP_N;
- Positive signal input on pin CMP_P and negative signal from BGPREF or VREF;
- Positive signal input on pin CMP_N and negative signal from BGPREF or VREF.

Each comparator have hysteresis voltage of 20mV.

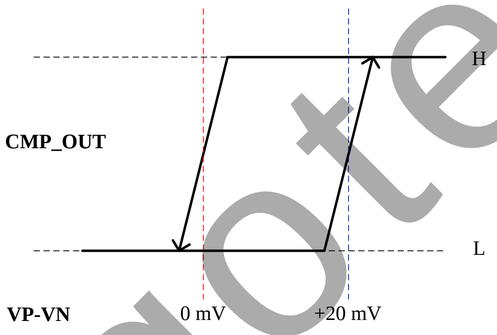


Figure 10-1 hysteresis Window of CMP Controller

10.2. Feature

-- Interrupt/wake-up signal generated for analog detect flag.

-- Comparator interrupt generation.

-- Comparator counter.

10.3. Block Diagram

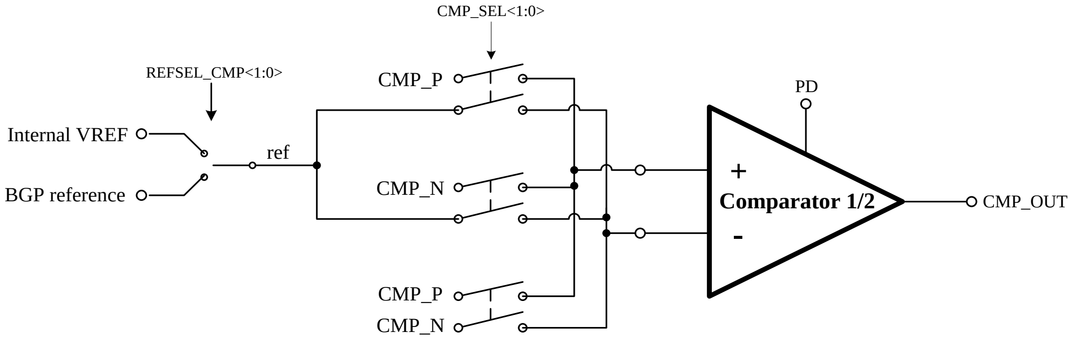


Figure 10-2 Functional Block Diagram of CMP Controller

10.4. Register Location

Table 10-1 Register Location of ANA Controller for CMP (ANA Base: 0x40014200)

Name	Type	Address	Description	Default
ANA_REG2	R/W	0x0008	Analog register 2	0x00
ANA_REG3	R/W	0x000C	Analog register 3	0x00
ANA_REG5	R/W	0x0014	Analog register 5	0x00
ANA_CTRL	R/W	0x0050	Analog control register	0x0000000
ANA_CMPOUT	R	0x0054	Comparator result register	0x0030
ANA_INTSTS	R/C	0x0060	Analog interrupt status register	0x0000
ANA_INTEN	R/W	0x0064	Analog interrupt enable register	0x0000
ANA_CMPCNT1	R/C	0x00B0	Comparator 1 counter	0x00000000
ANA_CMPCNT2	R/C	0x00B4	Comparator 2 counter	0x00000000

10.5. Register Definition

10.5.1. ANA_REG2 Register

Table 10-2 Description of each bit in ANA_REG2 for CMP

Bit	Name	Function	Notes
1:0	CMP1_SEL[1:0]	Signal source selection of comparator 1	00 CMP1_P to REF 01: CMP1_N to REF 1*: CMP1_P to CMP1_N
3:2	CMP2_SEL[1:0]	Signal source selection of comparator 2	00: CMP2_P to REF 01: CMP2_N to REF 1*: CMP2_P to CMP2_N
4	REFSEL_CMP1	REF selection of CMP1	0: VREF 1: BGPREF.
5	REFSEL_CMP2	REF selection of CMP2	0: VREF

			1: BGPREF.

10.5.2. ANA_REG3 Register

Table 10-3 Description of each bit in ANA_REG3 for CMP

Bit	Name	Function	Notes
1	CMP1PDN	CMP1 power up control signal	0: Power-down CMP1 1: Power-up CMP1
2	CMP2PDN	CMP2 power up control signal	0: Power-down CMP2 1: Power-up CMP2
3	BGPPD*	BGP power down control signal.	0: Power-up BGP 1: Power-down BGP
Note*: RCH and PLL and ADC are related to BGP, You must power-up BGP before you power-up RCH or PLL or ADC. User can power down BGP by set BGPPD to 1 when BGP was not used in program. User could not power down BGP by set BGPPD to 1 when BGP was used in program, because the system has a protection function to ensure reliability. User can power down BGP in sleep mode and deep-sleep mode whether BGP is used or not.			

10.5.3. ANA_REG5 Register

Table 10-4 Description of each bit in ANA_REG5 for CMP

Bit	Name	Function	Notes

1:0	IT_CMP1[1:0]	Bias current selection of CMP1	00: 20nA;
			01: 100nA;
			1*: 500nA;

3:2	IT_CMP2[1:0]	Bias current selection of CMP2	00: 20nA;
			01: 100nA;
			1*: 500nA;

Note: The smaller the CMP bias current, the lower the power consumption and the longer the propagation delay time; the higher the CMP bias current, the higher the power consumption and the shorter the propagation delay time.			

10.5.4. ANA_CTRL Register

Table 10-5 Description of ANA_CTRL Register for CMP

Bit	Name	Type	Description	Default
23:22	CMP2DEB	R/W	Comparator 2 de-bounce control register. 0: No de-bounce. 1: 2 RTCCLK de-bounce. 2: 3 RTCCLK de-bounce. 3: 4 RTCCLK de-bounce. When de-bounce is enabled, the input signal is valid only when the signal isn't change in multi-cycles of RTCCLK clock. And, the response time of the wake-up and interrupt will be delayed until the signal is valid. This circuit can work under all mode including sleep and deep-sleep mode.	0x0
21:20	CMP1DEB	R/W	Comparator 1 de-bounce control register. 0: No de-bounce. 1: 2 RTCCLK de-bounce. 2: 3 RTCCLK de-bounce. 3: 4 RTCCLK de-bounce. When de-bounce is enabled, the input signal is valid only when the signal isn't change in multi-cycles of RTCCLK clock. And, the response time of the wake-up and interrupt will be delayed until the signal is valid. This circuit can work under all mode including sleep and deep-sleep mode.	0x0
19:18	-	-	Reserved.	0
3:2	COMP2_SEL	R/W	This register is used to control the interrupt and wake-up signal generation of COMP2. 0: Off 1: Rising edge of COMP2. 2: Falling edge of COMP2. 3: Change of COMP2.	0x0
1:0	COMP1_SEL	R/W	This register is used to control the interrupt and wake-up signal generation of COMP1.	0x0

			0: Off 1: Rising edge of COMP1. 2: Falling edge of COMP1. 3: Change of COMP1.	

10.5.5. ANA_CMPOUT Register

Table 10-6 Description of ANA_CMPOUT Register for CMP

Bit	Name	Type	Description	Default
3	COMP2	R	This bit shows the output of comparator 2.	0x0
2	COMP1	R	This bit shows the output of comparator 1.	0x0

10.5.6. ANA_INSTS Register

Table 10-7 Description of ANA_INTSTS Register for CMP

Bit	Name	Type	Description	Default
3	INTSTS3	R/C	Interrupt flag of COMP2, the interrupt generate condition is controlled by COMP2_SEL. Read 0: No COMP2 interrupt. Read 1: COMP2 interrupt is happened. Write 0: No effect. Write 1: Clear this bit.	0x0
2	INTSTS2	R/C	Interrupt flag of COMP1, the interrupt generate condition is controlled by COMP1_SEL. Read 0: No COMP1 interrupt. Read 1: COMP1 interrupt is happened. Write 0: No effect. Write 1: Clear this bit.	0x0

10.5.7. ANA_INTEN Register

Table 10-8 Description of ANA_INTEN Register for CMP

Bit	Name	Type	Description	Default
3	INTEN3	R/W	Interrupt and wake-up enable control of COMP2. 0: Disable COMP2 interrupt and wake-up. 1: Enable COMP2 interrupt and wake-up.	0x0
2	INTEN2	R/W	Interrupt and wake-up enable control of COMP1. 0: Disable COMP1 interrupt and wake-up. 1: Enable COMP1 interrupt and wake-up.	0x0

10.5.8. ANA_CMPCNTx Register

Table 10-9 Description of ANA_CMPCNTx Register

Bit	Name	Type	Description	Default
31:0	CNTx	R/C	This register store the happen times of comparator x according to the setting in COMPx_SEL. For example, when COMPx_SEL is set to 1, then this counter will increase 1 when the COMPx is rising. This register can be cleared by writing 0 to this register, but this operation is valid only when corresponded CMPPDNx is set to 1 (when the corresponded comparator is enabled).	0x0000000

11. Tiny ADC Controller

11.1. Introduction

The Tiny ADC (2 BIT ADC) controller is used to control the Tiny ADC function of V85X3. TinyADC is powered by AVCC. TinyADC controller is placed in always-on domain, so all the tiny ADC setting will be kept under deep-sleep mode.

11.2. Feature

-- TinyADC interrupt generation.

11.3. Block Diagram

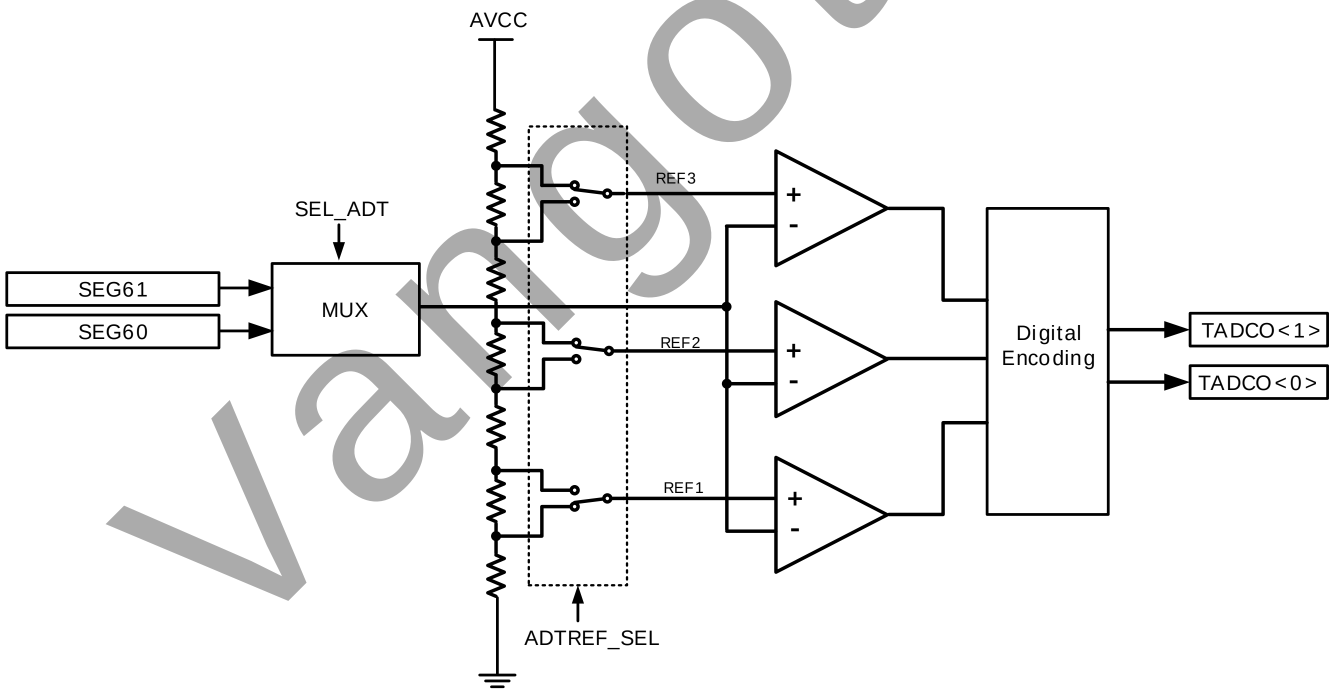


Figure 11-1 Functional Block Diagram of Analog Controller

11.4. Register Location

Table 11-1 Register Location of ANA Controller for TADC (ANA Base: 0x40014200)

Name	Type	Address	Description	Default

ANA_REGF	R/W	0x003C	Analog control register 15	0x00
ANA_CMPOUT	R	0x0054	Comparator result register	0x0030
ANA_INTSTS	R/C	0x0060	Analog interrupt status register	0x0000
ANA_INTEN	R/W	0x0064	Analog interrupt enable register	0x0000
ANA_MISC	R/W	0x00B8	Analog misc. control register	0x00

11.5. Register Definition

11.5.1. ANA_REGF Register

Table 11-2 Description of each bit in ANA_REGF for TADC

Bit	Name	Function	Notes
3	PDN_ADT	Power up Tiny ADC	0: Power down. 1: Power up
4	SEL_ADT	Signal selection for TADC	0: Connect to IOE6 1: Connect to IOE7
5	ADTREF1_SEL	REF1 of TADC selection	0: 0.9V 1: 0.7V
6	ADTREF2_SEL	REF2 of TADC selection	0: 1.8V 1: 1.6V
7	ADTREF3_SEL	REF3 of TADC selection	0: 2.7V 1: 2.5V

11.5.2. ANA_CMPOUT Register

Table 11-3 Description of ANA_CMPOUT Register for TADC

Bit	Name	Type	Description	Default
15:14	TADCO	R	Tiny ADC output. For example, if all the ADTREFx_SEL set to 0, TADCO value as follows. When signal <0.9V, TADCO =0,	-

			When signal >0.9V && <1.8V, TADCO =1, When signal >1.8V && <2.7V, TADCO =2, When signal >2.7V, TADCO =3.	

11.5.3. ANA_INSTS Register

Table 11-4 Description of ANA_INTSTS Register for TADC

Bit	Name	Type	Description	Default
31:14			Reserved.	0
13	INTSTS13	R/C	TADC change over-threshold interrupt. This interrupt will be set when the TADC is rising or falling and the change value compare to previous cycle is larger than or equal to the threshold setting in the TADCTH in ANA_MISC register, this interrupt flag will be set. Read 0: No TADC over threshold interrupt. Read 1: TADC over threshold is happened. Write 0: No effect. Write 1: Clear this bit.	0x0

11.5.4. ANA_INTEN Register

Table 11-5 Description of ANA_INTEN Register for TADC

Bit	Name	Type	Description	Default
31:14	-	-	Reserved.	0
13	INTEN13	R/W	Interrupt and wake-up enable control of TADC change over or equal to threshold. 0: Disable TADC interrupt and wake-up. 1: Enable TADC interrupt and wake-up.	0x0

11.5.5. ANA_MISC Register

Table 11-6 Description of ANA_MISC Register

Bit	Name	Type	Description	Default

31:6	-	-	Reserved.	0
5:4	TADCTH*	R/W	TADC threshold setting. This register controls the threshold of TADC's interrupt. The TADC is using internal 32K RC as clock source to sample external signal, when TADC's interrupt is enable and the difference of two continuous cycles is larger than or equal to TADCTH, the INTSTS13 will be set and an interrupt will be asserted.	0x0
3:0	-	-	Reserved.	0

Note*: Bit3:0 of ANA_MISC register should be set 0 all the time.

12. PMU_WDT Unit

12.1. Introduction

In the V85X3, the embedded 16-bit watchdog timer (WDT) counting pulses of the 32 kHz RTCCLK clock. When the program gets stuck somewhere, the timer overflows and reset the system to cause the program start from the beginning. WDT's reset level is the same as POR reset, it can provide chip's internal reset.

12.2. Features

--WDT counting period:2s\1s\0.5s\0.25s.

--Password protection to avoid close WDT in un-expected event.

12.3. WDT State in Different Modes

For different mode, the enable or disable of WDT module will be controlled by hardware or software, the following table shows the detail of WDT status under each mode when MODE (PMU_STS register bit24) is 1. If MODE (PMU_STS register bit24) is 0, WDT is invalid in all modes.

Table 12-1 WDT Enable or Disable in Different Modes (MODE=1)

<table>
<tr><th rowspan="2">WDT</th><th colspan="5">Power modes</th></tr>
<tr><th>RTC only</th><th>Deep sleep</th><th>Sleep</th><th>IDLE</th><th>Active</th></tr>
<tr><td>State</td><td>Invalid</td><td>ON(WDTEN = 1)
OFF(WDTEN = 0)</td><td>ON(WDTEN = 1)
OFF(WDTEN = 0)</td><td>ON(WDTEN = 1)
OFF(WDTEN = 0)</td><td>ON(WDTEN = 1)
OFF(WDTEN = 0)</td></tr>
<tr><th rowspan="2">WDT</th><th rowspan="2">Exit RTC only mode</th><th colspan="3">Wake up from different modes</th></tr>
<tr><th>Deep sleep</th><th>Sleep</th><th>IDLE</th></tr>
<tr><td>State</td><td>ON</td><td>ON</td><td>ON</td><td>ON(WDTEN = 1)
OFF(WDTEN = 0)</td></tr>
</table>

12.4. Block Diagram

12.5. Register Location

Table 12-2 Register Location of the PMU_WDT Controller (PMU Base: 0x40014000)

Name	Type	Address	Description	Default
PMU_WDTPASS	R/W	0x0040	Watch dog timing unlock register	0x00000000
PMU_WDTEN	R/W	0x0044	Watch dog timer enable register	0x1
PMU_WDTCLR	W	0x0048	Watch dog timer clear register	0x0000

12.6. Register Definitions

12.6.1. PMU_WDTPASS Register

Table 12-3 Description of PMU_WDTPASS Register

Bit	Name	Type	Description	Default
31:1	-	-	Reserved.	0
0	UNLOCK	R	This bit indicates the watch dog timer enable register has been unlocked and is ready to change the watch dog enable control register. To set this bit to 1, programmer should write 0xAA5555AA to this register. This bit will be cleared immediately after any register write to any PMU control register, including ICE write, so programmer should set the PMU_WDTEN immediately after the UNLOCK bit is set to 1, otherwise the UNLOCK procedure should start again.	0x0

12.6.2. PMU_WDTEN Register

Table 12-4 Description of PMU_WDTEN Register

Bit	Name	Type	Description	Default
31:4	-	-	Reserved.	0
3:2	WDTSEL	R/W	This register is used to control the WDT counting period. 0: 2 secs	0x0

			1: 1 sec 2: 0.5 secs 3: 0.25 secs To change the value of this register, UNLOCK bit of PMU_WDTPASS should be set to 1 first.	
1	-	-	Reserved.	0
0	WDTEN	R/W	This bit indicates the watch dog timer is enable. To change the value of this register, UNLOCK bit of PMU_WDTPASS should be set to 1 first.	0x1

12.6.3. PMU_WDTCLR Register

Table 12-5 Description of PMU_WDTCLR Register

Bit	Name	Type	Description	Default
31:16	-	-	Reserved.	0
15:0	WDTCNT	R/C	This register shows the current counter value of wat dog timer. When this timer count to limit value set by WDTSEL, the WDT will issue a system reset. So programmer should clear this timer in a regulator time to avoid WDT reset. To clear this timer programmer should write 0x55AAAA55 to this register. During debug mode, this register will be cleared to 0 automatically and no WDT reset will be issued under the debug mode.	0x0

13. RTC Controller

13.1. Introduction

The RTC controller is used to control time calculation and RTC auto calibration function. The time calculation function can realize the year, month, week, day, hour, minute, second automatically calculation function and the leap year detection. The auto calibration function can realize background calibration function which can detect temperature and adjust one second clock period to compensate the clock shift caused by temperature variation. There are also multi-second, multi-minutes, and multi-hours auto wake-up timer embedded in the RTC engine.

13.2. Feature

--BCD format Time Calculation from second to year.

--Automatically leap year detection.

--Automatic temperature detection and 32768 frequency compensation.

--Programmable multiple wake-up source.

--Initialize calibration engine for manufactory.

--RTC clock scaling for lower power consumption under sleep/deep-sleep mode.

13.3. Block Diagram

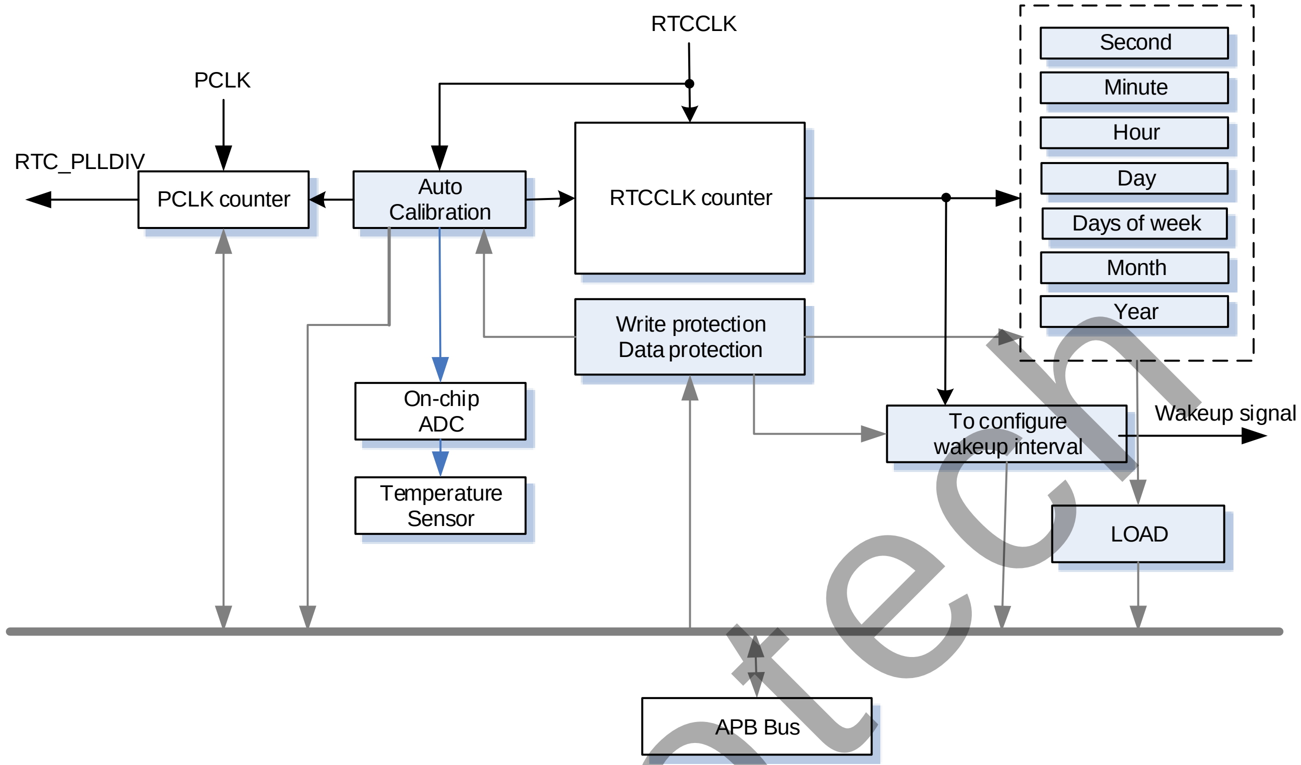


Figure 13-1 Functional Block Diagram of RTC Controller

13.4. Reading and Writing of RTC Register

13.4.1. Writing of RTC

In the V85X3, some RTC registers are protected by write protection, including RTC timing registers and RTC calibration registers and so on. For details, please refer to the table 13-1.

The MCU must write of these registers following steps as:

1. User must wait until BSY (bit1 of register RTC_CE) is 0, to ensure the state of RTC is idle;

2. Writing 0x5AA55AA5 to the register RTC_PWD to enable the RTC_CE port's access;

3. Writing 0xA55AA55B to the register RTC_CE to enable writing of write protection registers.

4. Configuring write protection registers. RTC_SEC ~ RTC_YEAR register should be configured together;

5. Writing 0x5AA55AA5 to the register RTC_PWD to enable the RTC_CE port's access;

6. Writing 0xA55AA55A to the register RTC_CE to clear CE (bit0 of register RTC_CE) flag, and BSY (bit1 of register RTC_CE) flag will be set immediately after the CE is cleared from 1 to 0. After CE is cleared to 0, the contents of write protection registers update to RTC core will be start. The update procedure take around 3 32K period, which is around 100us.

7. User must wait until BSY (bit1 of register RTC_CE) cleared to 0 automatically after sixth step configuration, to ensure RTC update is done.

The MCU can write a register that without write protection directly.

13.4.2. Reading of RTC

RTC timing registers are protected from reading. For details, please refer to the table 13-1.

To read the timing registers, the MCU must read these registers following steps as:

1. User must wait until BSY (bit1 of register RTC_CE) is 0, to ensure the state of RTC is idle;

2. The MCU must read register RTC_LOAD firstly, BSY (bit1 of register RTC_CE) will be set immediately when RTC_LOAD port is read by MCU. BSY will cleared automatically after the read procedure is done, the read procedure take around 3 32K period, which is around 100 μS;

3. After the read procedure of RTC_LOAD is done, the current timed will be latched and programmer can read data from RTC_SEC ~ RTC_YEAR register.

The MCU can read a register that without read protection directly.

13.5. Register Location

The following table shows the register location of each register. The column "Write Protect means the register can only be written when CE is set to 1, and will be updated to RTC core only when CE is cleared to 0. The column "Read protect" means the value in these register will be updated only when RTC_LOAD port is read and BSY bit is cleared to 0.

Table 13-1 Register Location of RTC Controller (RTC Base: 0x40014800)

Name	Type	Address	Description	Default	Write Protect	Read Protect
RTC_SEC	R/W	0x0000	RTC second register	--	V	V
RTC_MIN	R/W	0x0004	RTC minute register	--	V	V
RTC_HOUR	R/W	0x0008	RTC hour register	--	V	V
RTC_DAY	R/W	0x000C	RTC day register	--	V	V
RTC_WEEK	R/W	0x0010	RTC week-day register	--	V	V
RTC_MON	R/W	0x0014	RTC month register	--	V	V
RTC_YEAR	R/W	0x0018	RTC year register	--	V	V
RTC_WKUSEC	R/W	0x0020	RTC wake-up second register	0x00	V	
RTC_WKUMIN	R/W	0x0024	RTC wake-up minute register	0x00	V	

RTC_WKUHOUR	R/W	0x0028	RTC wake-up hour register	0x00	V	
RTC_WKUCNT	R/W	0x002C	RTC wake-up counter register	0x0000000	V	
RTC_CAL	R/W	0x0030	RTC calibration register	--	V	
RTC_DIV	R/W	0x0034	RTC PLL divider register	0x0000000		
RTC_CTL	R/W	0x0038	RTC PLL divider control register	0x0		
RTC_PWD	R/W	0x0044	RTC password control register	0x00000000		
RTC_CE	R/W	0x0048	RTC write enable control register	0x0		
RTC_LOAD	R/W	0x004C	RTC read enable control register	--		
RTC_INTSTS	R/W	0x0050	RTC interrupt status control register	0x000		
RTC_INTEN	R/W	0x0054	RTC interrupt enable control register	0x000		
RTC_PSCA	R/W	0x0058	RTC clock pre-scaler control register	0x0	V	
RTC_ACCTRL	R/W	0x0080	RTC auto-calibration control register	0x0000	V	
RTC_ACTI	R/W	0x0084	RTC auto-calibration center temperature control register	0x1800	V	
RTC_ACF200	R/W	0x0088	RTC auto-calibration 200*frequency control register	0x640000	V	
RTC_ACADCW	R/W	0x008C	RTC auto-calibration manual ADC value control register	0x0000	V	
RTC_ACP0	R/W	0x0090	RTC auto-calibration parameter 0 control register	0x0000	V	
RTC_ACP1	R/W	0x0094	RTC auto-calibration parameter 1 control register	0x0000	V	
RTC_ACP2	R/W	0x0098	RTC auto-calibration parameter 2 control register	0x0000	V	
RTC_ACP3	R	0x009C	RTC auto-calibration parameter 3 control register	0x0000		
RTC_ACP4	R/W	0x00A0	RTC auto-calibration parameter 4 control register	0x0000	V	
RTC_ACP5	R/W	0x00A4	RTC auto-calibration parameter 5 control register	0x0000	V	
RTC_ACP6	R/W	0x00A8	RTC auto-calibration parameter 6	0x0000	V	

			control register			
RTC_ACP7	R/W	0x00AC	RTC auto-calibration parameter 7 control register	0x0000	V	
RTC_ACK1	R/W	0x00B0	RTC auto-calibration parameter k1 control register	0x0000	V	
RTC_ACK2	R/W	0x00B4	RTC auto-calibration parameter k2 control register	0x0000	V	
RTC_ACK3	R/W	0x00B8	RTC auto-calibration parameter k3 control register	0x0000	V	
RTC_ACK4	R/W	0x00BC	RTC auto-calibration parameter k4 control register	0x0000	V	
RTC_ACK5	R/W	0x00C0	RTC auto-calibration parameter k5 control register	0x0000	V	
RTC_ACTEMP	R	0x00C4	RTC auto-calibration calculated temperature register	0x0000	V	
RTC_ACPPM	R	0x00C8	RTC auto-calibration calculated PPM register	0x0000	V	
RTC_WKUCNTR	R	0x00CC	This register is used to represent the current WKUCNT value	0x000000		
RTC_ACKTEMP	R/W	0x00D0	RTC auto-calibration k temperature section control register	0x3C2800EC	V	

13.6. Register Definition

13.6.1. RTC_SEC/MIN/DAY/WEEK/MONTH/YEAR Register

The time register is following the BCD encode, where the bit 7~4 is represent the 10's digit and bit 3~0 is for 1's digit. The value in these register can be set only when CE is high, and it will be update to RTC core only when the CE is cleared from 1 to 0. To read current time, programmer should process a read operation to RTC_LOAD register, and wait until the BSY bit is cleared. Otherwise, the register value will be invalid.

Table 13-2 Description of RTC_SEC/MIN/DAY/WEEK/MONTH/YEAR Register

Register	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0

Register		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x0000	RTC_SEC, 0~59	-	S40	S20	S10	S8	S4	S2	S1
0x0004	RTC_MIN, 0~59	-	M40	M20	M10	M8	M4	M2	M1
0x0008	RTC_HOUR,0~23	-	-	H20	H10	H8	H4	H2	H1
0x000C	RTC_DAY, 1~31	-	-	D20	D10	D8	D4	D2	D1
0x0010	RTC_WEEK, 0~6	-	-	-	-	-	W4	W2	W1
0x0014	RTC_MON, 1~12	-	-	-	Mo10	Mo8	Mo4	Mo2	Mo1
0x0018	RTC_YEAR, 00~99	Y80	Y40	Y20	Y10	Y8	Y4	Y2	Y1
Default		X	X	X	X	X	X	X	X
"week" can only be set by user, RTC will not detect automatically. After initialize setting, RTC will increase the week count automatically. For example, when user set 2010/1/1 as Friday, RTC will detect 2010/01/02 as Saturday. W4/W2/W1:000, Sunday; 001, Monday; 010, Tuesday; 011, Wednesday; 100, Thursday; 101, Friday; 110, Saturday. System can only set the last two digit of year, for example, when setting year 2010, RTC_YEAR should be set as 0b00010000.									

13.6.2. RTC_WKUSEC Register

Table 13-3 Description of RTC_WKUSEC Register

Bit	Name	Type	Description	Default
31:6	-	-	Reserved.	0
5:0	WKUSEC	R/W	This register is used to control the multi-second wake-up function. The wake-up period is (WKUSEC + 1)*1 second. When the INTEN[2] is 1 and the internal wake-up second count is reach the target value, the INTSTS[2] will be set to 1 and wake-up signal will be asserted to PMU controller. For the first interrupt generated by WKUSEC, it may have < 1 sec error if the new WKUSEC number is not equal to current WKUSEC number. If the new WKUSEC is equal to current WKUSEC, the first interrupt time may have 0~(WKUSEC +1) variation. To avoid this problem, set an alternative value (like 0) to this register and update it with RTC_CE operation. Then set the correct value to it.	0x00

13.6.3. RTC_WKUMIN Register

Table 13-4 Description of RTC_WKUMIN Register

Bit	Name	Type	Description	Default
31:6	-	-	Reserved.	0
5:0	WKUMIN	R/W	This register is used to control the multi-minute wake-up function. The wake-up period is (WKUMIN + 1)*1 minute. When the INTEN[3] is 1 and the internal wake-up minute count is reach the target value, the INTSTS[3] will be set to 1 and wake-up signal will be asserted to PMU controller. For the first interrupt generated by WKUMIN, it may have < 1 minute error if the new WKUMIN number is not equal to current WKUMIN number. If the new WKUMIN is equal to current WKUMIN, the first interrupt time may have 0~(WKUMIN +1) variation. To avoid this problem, set an alternative value (like 0) to this register and update it with RTC_CE operation. Then set the correct value to it.	0x00

13.6.4. RTC_WKUHOUR Register

Table 13-5 Description of RTC_WKUHOUR Register

Bit	Name	Type	Description	Default
31:5	-	-	Reserved.	0
4:0	WKUHOUR	R/W	This register is used to control the multi-hour wake-up function. The wake-up period is (WKUHOUR + 1)*1 hour. When the INTEN[4] is 1 and the internal wake-up hour count is reach the target value, the INTSTS[4] will be set to 1 and wake-up signal will be asserted to PMU controller. For the first interrupt generated by WKUHOUR, it may have < 1 hour error if the new WKUHOUR number is not equal to current WKUHOUR number. If the new WKUHOUR is equal to current WKUHOUR, the first interrupt time may have 0~(WKUHOUR +1) variation. To avoid this problem, set an alternative value (like 0) to this register and update it with RTC_CE operation. Then set the correct value to it.	0x00

13.6.5. RTC_WKUCNT Register

Table 13-6 Description of RTC_WKUCNT Register

Bit	Name	Type	Description	Default
31:26	-	-	Reserved.	0
25:24	CNTSEL	R/W	This is register is used to set the counter clock of WKUCNT. When PSCA is 0. 0: Counter clock is 32768Hz 1: Counter clock is 2048Hz. 2: Counter clock is 512Hz 3: Counter clock is 128Hz When PSCA is 1. 0: Counter clock is 8192Hz 1: Counter clock is 2048Hz. 2: Counter clock is 512Hz 3: Counter clock is 128Hz	0x0
23:0	WKUCNT	R/W	This register is used to control the 32K counter wake-up function. The wake-up period is (WKUCNT + 1)*Counter Clock Cycle. The counter clock is controlled by CNTSEL. When the INTEN[6] is 1 and the internal wake-up count is reach the target value, the INTSTS[6] will be set to 1 and wake-up signal will be asserted to PMU controller.	0x0000

13.6.6. RTC_CAL Register

Table 13-7 Description of RTC_CAL Register

Bit	Name	Type	Description	Default
31:14	-	-	Reserved.	0
13:0	CAL	R/W	RTC 32768 calibration register, this register is a 14 bits signed value. The RTC engine will do calibration for every 30 seconds, the internal counter will count 32768 times during 1~29 second. At the 30 second, it will count [32768-(CAL-1)] for a second, so it can let the average 1 second pulse in 30 seconds become an	--

			accurate 1 second pulse. The PPM resolution of the CAL register is 1.02ppm, and the adjustable range is ±8332.3ppm (±12 minutes/day). When the auto-calibration function is enabled, this register will be updated automatically by the auto-calibration engine.	

13.6.7. RTC_DIV Register

Table 13-8 Description of RTC_DIV Register

Bit	Name	Type	Description	Default
31:26	-	-	Reserved.	0
25:0	RTCDIV	R/W	This register is used to generate divider output. The output frequency is PCLK/(2*(RTCDIV+1)).	0x0000

13.6.8. RTC_CTL Register

Table 13-9 Description of RTC_CTL Register

Bit	Name	Type	Description	Default
31:3	-	-	Reserved.	0
2	RTCPLLOE	R/W	RTC_PLLDIV Divider output enable, this register is used to control the RTC_PLLDIV output. 0: Disable RTC_PLLDIV output. 1: Enable RTC_PLLDIV output. The RTC_PLLDIV output is at IOA[3] or IOA[7], the PMU_IOASEL bit 3 or 7 should also be set to 1 when RTC_PLLDIV output is enabled.	0x0
1:0			Reserved.	0x0

13.6.9. RTC_PWD Register

Table 13-10 Description of RTC_PWD Register

Bit	Name	Type	Description	Default
31:1	-	-	Reserved.	0
0	PWDEN	R	This register is used to protect the RTC_CE port's access. Before access the RTC_CE, programmer should write	0x0

			0x5AA55AA5 to this port, and the PWDEN will be set to 1. This bit will be cleared automatically after any write to RTC_CE port. Which means programmer should write to this port again before next access to RTC_CE port.	

13.6.10. RTC_CE Register

Table 13-11 Description of RTC_CE Register

Bit	Name	Type	Description	Default
31:2	-	-	Reserved.	0
1	BSY	R	This flag is used to indicate the RTC update procedure or RTC read procedure is ongoing. This bit will be set immediately after the CE is cleared from 1 to 0 or when RTC_LOAD port is read by CPU. This bit will be cleared automatically after the read or write procedure is done. Programmer can poll this bit to know if the RTC update is done or not. The update or read procedure take around 3 32K period, which is around 100 μS.	0x0
0	CE	R	This register is used to unlock the access to RTC register. This register can be only when PWDEN is set to 1 and 0xA55AA55B is written to this register. After this bit is set to 1, the RTC register can be programmed, but the actual update to RTC core will be start after this bit is cleared to 0. To clear this bit, the PWDEN should be set to 1 and 0xA55AA55A should be written to this register.	0x0

13.6.11. RTC_LOAD Register

Table 13-12 Description of RTC_LOAD Register

Bit	Name	Type	Description	Default
31:0	LOAD	R/W	This register is used to let RTC engine read data from RTC core. When programmer read from this port, the current time will be latched and programmer can read data from RTC_SEC ~ RTC_YEAR register. The read procedure will takes 3 RTCCLK cycles, programmer can check the BSY bit to know if the procedure is done. The read data from this port is invalid.	--

13.6.12. RTC_INTSTS Register

Table 13-13 Description of RTC_INTSTS Register

Bit	Name	Type	Description	Default
31:10	-	-	Reserved.	0
9	ACBSY	R	Auto-calibration busy flag.	0x0
8	INTSTS8	R/C	Interrupt status 8, this interrupt will be set when an illegal write to CE register is happened. The illegal write means the BSY bit is still 1 but CE is set to 1 again or RTC_LOAD port is read again. Write 1 to clear this bit.	
7	INTSTS7	R/C	Interrupt status 7, this interrupt will be set when an auto calibration is done. Write 1 to clear this bit.	0x0
6	INTSTS6	R/C	Interrupt status 6, this interrupt will be set when 32K counter interrupt period set by WKUCNT is reach. Write 1 to clear this bit.	0x0
5	INTSTS5	R/C	Interrupt status 5, this interrupt will be set when mid-night (00:00) is reach. Write 1 to clear this bit.	0x0
4	INTSTS4	R/C	Interrupt status 4, this interrupt will be set when multi-hour interrupt period set by WKUHOUR is reach. Write 1 to clear this bit.	0x0
3	INTSTS3	R/C	Interrupt status 3, this interrupt will be set when multi-minute interrupt period set by WKUMIN is reach. Write 1 to clear this bit.	0x0
2	INTSTS2	R/C	Interrupt status 2, this interrupt will be set when multi-second interrupt period set by WKUSEC is reach. Write 1 to clear this bit.	0x0
1	INTSTS1	R/C	Interrupt status 1, this interrupt will be set when illegal time format is written into RTC core. Write 1 to clear this bit.	0x0
0	-	-	Reserved.	0

13.6.13. RTC_INTEN Register

Table 13-14 Description of RTC_INTEN Register

Bit	Name	Type	Description	Default
31:9	-	-	Reserved.	0

8	INTEN8	R/W	Interrupt enable 8, when this bit is 1 and INTSTS8 is set, and interrupt will be asserted to CPU.	0x0
7	INTEN7	R/W	Interrupt enable 7, when this bit is 1, the INTSTS7 can be set, and interrupt will be asserted to CPU and wake-up signal will be asserted to PMU controller.	0x0
6	INTEN6	R/W	Interrupt enable 6, when this bit is 1, the INTSTS6 interrupt will be asserted to CPU and wake-up signal will be asserted to PMU controller.	0x0
5	INTEN5	R/W	Interrupt enable 5, when this bit is 1, the INTSTS5 interrupt will be asserted to CPU and wake-up signal will be asserted to PMU controller.	0x0
4	INTEN4	R/W	Interrupt enable 4, when this bit is 1, the INTSTS3 interrupt will be asserted to CPU and wake-up signal will be asserted to PMU controller.	0x0
3	INTEN3	R/W	Interrupt enable 3, when this bit is 1, the INTSTS3 interrupt will be asserted to CPU and wake-up signal will be asserted to PMU controller.	0x0
2	INTEN2	R/W	Interrupt enable 2, when this bit is 1, the INTSTS2 interrupt will be asserted to CPU and wake-up signal will be asserted to PMU controller.	0x0
1	INTEN1	R/W	Interrupt enable 1, when this bit is 1, the INTSTS1 interrupt will be asserted to CPU and wake-up signal will be asserted to PMU controller.	0x0
0	-	-	Reserved.	0

13.6.14. RTC_PSCA Register

Table 13-15 Description of RTC_PSCA Register

Bit	Name	Type	Description	Default
31:2	-	-	Reserved.	0
1:0	PSCA	R/W	This register is used to control the RTCCLK pre-scaler. When slow down the RTCCLK, it can significantly reduce the power under sleep or deep-sleep mode. 0: No pre-scaler, RTC clock is 32768 Hz. 1: 1/4 pre-scaler, RTC clock is 8192 Hz. 2~3: Reserved. When this register is set, all modules which is using	0x0

			RTCCLK will be affected. The RTC time counter and LCD frame rate will be automatically adjusted by hardware, so no need to modify the setting. But the RTC_WKUCNT's input clock will be changed, so programmer should modify the corresponded setting. And the UART 32K baud rate register need to be re-calculated according to new RTCCLK speed.	

13.6.15. RTC_ACCTRL Register

Table 13-16 Description of RTC_ACCTRL Register

Bit	Name	Type	Description	Default
31:14	-	-	Reserved.	0
13:8	ACPER	R/W	Auto trigger period control register, the actual period is controlled by (ACPER + 1)*ACCLK. For example, when ACCLK is set to 2 (1 minute), and ACPER is set to 5, then the auto trigger period is (5+1)*1 minute = 6 minutes.	0x0
7:6	ACDEL	R/W	Auto-calibration delay period selection, before doing auto-calibration, a specified delay will be applied to ensure the main power is stable. 0: Delay 15.625ms. 1: Delay 31.25ms. 2: Delay 62.5ms. 3: Delay 125ms.	0x0
5:4	ACCLK	R/W	Auto-trigger clock source selection. 0: Disable auto trigger function. 1: Auto trigger count clock is 1second. 2: Auto trigger count clock is 1 minute. 3: Auto trigger count clock is 1 hour.	0x0
3	ADCSEL	R/W	ADC source select register. 0: From ADC read data. 1: From port RTC_ADCW.	0x0
2	-	-	Reserved.	0
1	MANU	R/W	Auto-calibration manual trigger function. Write 1 to this register will trigger an auto-calibration procedure. This bit will be cleared to 0 when the procedure is done.	0x0

0	ACEN	R/W	Auto-calibration enable control register. 0: Disable auto-calibration function. Automatic triggering should be disabled before auto-calibration function is disabled. 1: Enable auto-calibration function.	0x0

13.6.16. RTC_ACTI Register

Table 13-17 Description of RTC_ACTI Register

Bit	Name	Type	Description	Default
31:16	-	-	Reserved.	0
15:0	ACTI	R/W	Auto-calibration Ti control register. This register is used to store the Ti value which is used as the center temperature during calibration. This register is 8 bits integer and 8 bits fraction value. This register can be updated only when CE is 1, and should be a fixed value when ACEN is 1. For example, 0x1880 means 24.5 degree (24.5*256=6272=0x1880), 0xE780 means -24.5 degree(~0x1880+1=0xE780).	0x1800

13.6.17. RTC_ACF200 Register

Table 13-18 Description of RTC_ACF200 Register

Bit	Name	Type	Description	Default
31:26	-	-	Reserved.	0
25:0	F200	R/W	Auto-calibration F200 control register. This register is used to store the current PCLK speed value which is used for the calculation of PLLDIV value. This register is 26 bits integer. For example, when current PCLK speed is 6.5536MHz, then programmer should fill 6553600/2 = 0x320000 into this register. At the same time, the P6 should also be changed according to the following equation. P6 = 0.0004096 * F200. This register can be updated only when CE is 1, and should be fixed value when ACEN is 1.	0x640000

13.6.18. RTC_ACADCW Register

Table 13-19 Description of RTC_ACADCW Register

Bit	Name	Type	Description	Default
31:16	-	-	Reserved.	0
15:0	ADCW	R/W	Auto-calibration manual ADC value control register. This register is used to store the manual ADC value which is used for the calculation for temperature. By default, the auto-calibration engine will read the ADC value automatically, but if programmer wishes to control the ADC value manually, this register can be used to control the ADC value read by the engine. This register is 16 bits integer. This register is valid only when ADCSEL is set to 1.	0x000

13.6.19. RTC_ACPx Register

Table 13-20 Description of RTC_ACPx Register

Bit	Name	Type	Description	Default
31:0	P0~P7	R/W	The P0~P7 registers are used for auto-calibration. Only P2 is 32 bits signed value, other P0~P7 is 16 bits signed value. P3 is read only and will be updated automatically according to calculated temperature. These registers can be updated only when CE is 1, and should be fixed value when ACEN is 1. The P0~P7 (exclude P3) will be updated automatically when power-up or wake-up from deep-sleep mode. Please refer to FLASH control section for detail.	0x0000

13.6.20. RTC_ACKx Register

Table 13-21 Description of RTC_ACKx Register

Bit	Name	Type	Description	Default
31:16	-	-	Reserved.	0
15:0	K1~K5	R/W	The K1~K5 registers are used for auto-calibration. These registers are 16 bits signed register. Hardware will auto select a suitable Kx according to calculated temperature T and update to RTC_ACP3 register.	0x0000

			K1: T< KTEMP1. K2: KTEMP1≤T< KTEMP2. K3: KTEMP2≤T< KTEMP3. K4: KTEMP3≤T< KTEMP4. K5: T≥KTEMP4. These registers can be updated only when CE is 1, and should be fixed value when ACEN is 1.	

13.6.21. RTC_ACKTEMP Register

Table 13-22 Description of RTC_ACKTEMP Register

Bit	Name	Type	Description	Default
31:24	KTEMP4	R/W	This register is used to control the section 4 temperature. This is a signed 8 bits value. This register can be updated only when CE is 1, and should be a fixed value when ACEN is 1.	0x3C
23:16	KTEMP3	R/W	This register is used to control the section 3 temperature. This is a signed 8 bits value. This register can be updated only when CE is 1, and should be a fixed value when ACEN is 1.	0x28
15:8	KTEMP2	R/W	This register is used to control the section 2 temperature. This is a signed 8 bits value. This register can be updated only when CE is 1, and should be a fixed value when ACEN is 1.	0x00
7:0	KTEMP1	R/W	This register is used to control the section 1 temperature. This is a signed 8 bits value. This register can be updated only when CE is 1, and should be a fixed value when ACEN is 1.	0xEC

13.6.22. RTC_ACTEMP Register

Table 13-23 Description of RTC_ACTEMP Register

Bit	Name	Type	Description	Default
31:16	-	-	Reserved.	0
15:0	TEMP	R	This register is used to store the calculated result of current temperature, and this is a 16 bits signed value.	0x0000

			This register will be updated automatically after the auto-calibration procedure is done. The format in this register is 8 bits integer and 8 bits fraction signed value. The actual temperature is equal to T/256.0. For example, 0x1880 means 24.5 degree(24.5*256=6272=0x1880), 0xE780 means -24.5 degree(~0x1880+1=0xE780).	

13.6.23. RTC_ACPPM Register

Table 13-24 Description of RTC_ACPPM Register

Bit	Name	Type	Description	Default
31:16	-	-	Reserved.	0
15:0	PPM	R	This register is used to store the calculated result the offset of 32768 external crystal's current temperature. This register will be updated automatically after the auto-calibration procedure is done. This register is a 16-bit signed value and the unit of this register is 0.1 PPM.	0x0000

13.6.24. RTC_WKUCNTR Register

Table 13-25 Description of RTC_WKUCNTR Register

Bit	Name	Type	Description	Default
31:24	-	-	Reserved.	0
23:0	WKUCNTR	R	This register is used to represent the current WKUCNT value. WKUCNTR increases from 0 to WKUCNT. Accumulating from 0, after reaching the WKUCNT setting value, continue to accumulate from 0 again.	--

13.7. Info information register（Related to RTC-Cal）

The RTC calibration data is stored in Info Sector 4 (0x40800). The address 0x40800 ~ 0x409FF data is written by SD612 tool (offline download and RTC calibration). Other data is written before leaving factory. The following table shows the details of this information.

Info Sector data can only be read and cannot be written. All information has a backup. The first data in the form is expressed in 1, and second copies in 2. Each data has a checksum data. Checksum algorithm: add up each data, and reverse the result.

Table 13-26 Info Information Register (Related to RTC-Cal)

Address	Sign	Data	Description
0x00040800	P4	RTC normal temperature offset 1	Load low 16 bits to RTC_ACP4 register, such as 0. unit(0.1ppm),
0x00040804		Check sum 1	INV(SUM(0x40800,0x40800))
0x00040808	P4	RTC normal temperature offset 2	Load low 16 bits to RTC_ACP4 register, such as 0. unit(0.1ppm),
0x0004080C		Check sum 2	INV(SUM(0x40808,0x40808))
0x00040810	K1	Crystal secondary calibration coefficient K1 1	Load to RTC_ACK1 register. K1 is calculated as follows: K1=B1/1000000*65536, B1 is the segment factor of crystal oscillator' quadratic curve. For example, the value of K1 is 20827.
0x00040814	K2	Crystal secondary calibration coefficient K2 1	Load to RTC_ACK2 register. K2 is calculated as follows: K2=B2/1000000*65536, B2 is the segment factor of crystal oscillator' quadratic curve. For example, the value of K2 is 21496.
0x00040818	K3	Crystal secondary calibration coefficient K3 1	Load to RTC_ACK3 register. K3 is calculated as follows: K3=B3/1000000*65536, B3 is the segment factor of crystal oscillator' quadratic curve. For example, the value of K3 is 22020.
0x0004081C	K4	Crystal secondary calibration coefficient K4 1	Load to RTC_ACK4 register. K4 is calculated as follows: K4=B4/1000000*65536, B4 is the segment factor of crystal oscillator' quadratic curve. For example, the value of K4 is 24517.
0x00040820	K5	Crystal secondary calibration coefficient K5 1	Load to RTC_ACK5 register. K5 is calculated as follows: K5=B5/1000000*65536, B5 is the segment factor of crystal oscillator' quadratic curve. For example, the value of K5 is 25257.
0x00040824		Check sum 1	INV(SUM(0x40810, 0x40820))
0x00040828	K1	Crystal secondary calibration coefficient K1 2	Load to RTC_ACK1 register. K1 is calculated as follows: K1=B1/1000000*65536, B1 is the segment factor of crystal oscillator' quadratic curve. For example, the value of K1 is 20827.
0x0004082C	K2	Crystal secondary calibration coefficient K2 2	Load to RTC_ACK2 register. K2 is calculated as follows: K2=B2/1000000*65536, B2 is the segment factor of crystal oscillator' quadratic curve. For example, the value of K2 is 21496.

0x00040830	K3	Crystal secondary calibration coefficient K3 2	Load to RTC_ACK3 register. K3 is calculated as follows: K3=B3/1000000*65536, B3 is the segment factor of crystal oscillator' quadratic curve. For example, the value of K3 is 22020.
0x00040834	K4	Crystal secondary calibration coefficient K4 2	Load to RTC_ACK4 register. K4 is calculated as follows: K4=B4/1000000*65536, B4 is the segment factor of crystal oscillator' quadratic curve. For example, the value of K4 is 24517.
0x00040838	K5	Crystal secondary calibration coefficient K5 2	Load to RTC_ACK5 register. K5 is calculated as follows: K5=B5/1000000*65536, B5 is the segment factor of crystal oscillator' quadratic curve. For example, the value of K5 is 25257.
0x0004083C		Check sum 2	INV(SUM(0x40828, 0x40838))
0x00040840	ACTI	Fixed point temperature of crystal 1	Load to RTC_ACTI register, such as 0x1800
0x00040844		Check sum 1	INV(SUM(0x40840,0x40840))
0x00040848	ACTI	Fixed point temperature of crystal 2	Load to RTC_ACTI register, such as 0x1800
0x0004084C		Check sum 2	INV(SUM(0x40848,0x40848))
0x00040850	KTEMPx(x=4~1)	Temperature section division settings 1	Load to RTC_ACKTEMP register, such as 0x3C2800EC
0x00040854		Check sum 1	INV(SUM(0x40850,0x40850))
0x00040858	KTEMPx(x=4~1)	Temperature section division settings 2	Load to RTC_ACKTEMP register, such as 0x3C2800EC
0x0004085C		Check sum 2	INV(SUM(0x40858,0x40858))
0x00040D00	P1/P0	RTC_ACP1/0 set 1	Load the high 16 bits to RTC_ACP1 register, such as 1060; Load the low 16 bits to RTC_ACP0, such as -214.
0x00040D04	P2'	RTC_ACP2 set 1	The value in this register is recorded as P2', such as -19746971. According to the formula P2=P2'+(Tr-Tm)*256 to calculate P2, and load P2 to RTC_ACP2 register.
0x00040D08	P5	RTC_ACP5 set 1	Load the high 16 bits to RTC_ACP5 register, such as 6444, and the low 16 bits be abandon.

0x00040D0C	P7/P6’	RTC_ACP 7/6 set 1	Load the high 16 bits to RTC_ACP7 register, such as 0; Load the low 16 bits to P6’ register, such as 1342. According to the formula: P6=a*P6’ to calculate P6, where a=PCLK/6553600.
0x00040D10		Check Sum set 1	INV(SUM(0x40DE0, 0x40DEC))
0x00040D14	P1/P0	RTC_ACP1/0 set 2	Load the high 16 bits to RTC_ACP1 register, such as 1060; Load the low 16 bits to RTC_ACP0, such as -214.
0x00040D18	P2’	RTC_ACP2 set 2	The value in this register is recorded as P2’, such as -19746971. According to the formula P2=P2’+(Tr-Tm)*256 to calculate P2, and load P2 to RTC_ACP2 register.
0x00040D1C	P5	RTC_ACP5 set 2	Load the high 16 bits to RTC_ACP5 register, such as 6444, and the low 16 bits be abandon.
0x00040D20	P7/P6’	RTC_ACP 7/6 set 2	Load the high 16 bits to RTC_ACP7 register, such as 0; Load the low 16 bits to P6’ register, such as 1342. According to the formula: P6=a*P6’ to calculate P6, where a=PCLK/6553600.
0x00040D24		Check Sum set 2	INV(SUM(0x40DF4, 0x40E00))
0x00040D70	Tr	Real Temperature 1 (from tmp275)	According to the formula P2=P2’+(Tr-Tm)*256 to calculate P2, and load P2 to RTC_ACP2 register.
0x00040D74	Tm	Measure Temperature 1 (from ADC)	
0x00040D78		Temp Check sum 1	INV(SUM(0x40D70, 0x40D74))
0x00040D7C	Tr	Real Temperature 2 (from tmp275)	According to the formula P2=P2’+(Tr-Tm)*256 to calculate P2, and load P2 to RTC_ACP2 register.
0x00040D80	Tm	Measure Temperature 2 (from ADC)	
0x00040D84		Temp Check sum 2	INV(SUM(0x40D7C, 0x40D80))

13.8. Application Note

13.8.1. Temperature Calibration

User can calculate temperature T according to the following formula, and T is 256 times larger than the actual temperature. T will be updated to RTC_ACTEMP register automatic after RTC auto- calibration.

$$T = ((P0 * ((X * X) >> 16)) + P1 * X + P2) >> 8$$

Where X is ADC sampling data, and X is 16 bits complement.

The P0~P2 is the value in RTC_ACP0~RTC_ACP2 registers, and P0~P2 is used to doing the temperature calibration.

The actual temperature is calculated as following.

$$T' = T / 256$$

13.8.2. Frequency Error Calibration

（1） User can calculate the frequency error of the chip as follows:

$$Delta = (P3 * ((T - Ti)^2 >> 16)) >> 16 + P4$$

Where *Delta* is the error rate in 0.1ppm unit of frequency deviation of 32768.

T = Actual temperature of the chip.

Ti= Setting value in RTC_ACTI register, which is the center temperature of the crystal during RTC calibration.

P4= The crystal deviation in normal temperature.

P3 is the K coefficient of the crystal for the current temperature. The hardware will select the K coefficient from Kx(x=1~5) according the actual temperature T when RTC auto-calibration, and update the K coefficient to the RTC_ACP3 register.

（2） User can calculate the frequency correction value as follows:

$$RTC\_CAL = (Delta * P5) >> 16$$

P5 is the value in RTC_ACP5 register, or user can calculate *P5* as follows:

$P5 = 65536 / 10 / (1 / 30 / 32768 / \mathrm{RTCCLK\ prescaler})$, and $(1 / 30 / 32768 / \mathrm{RTCCLK\ prescaler})$ is PPM resolution of the RTC_CAL register.

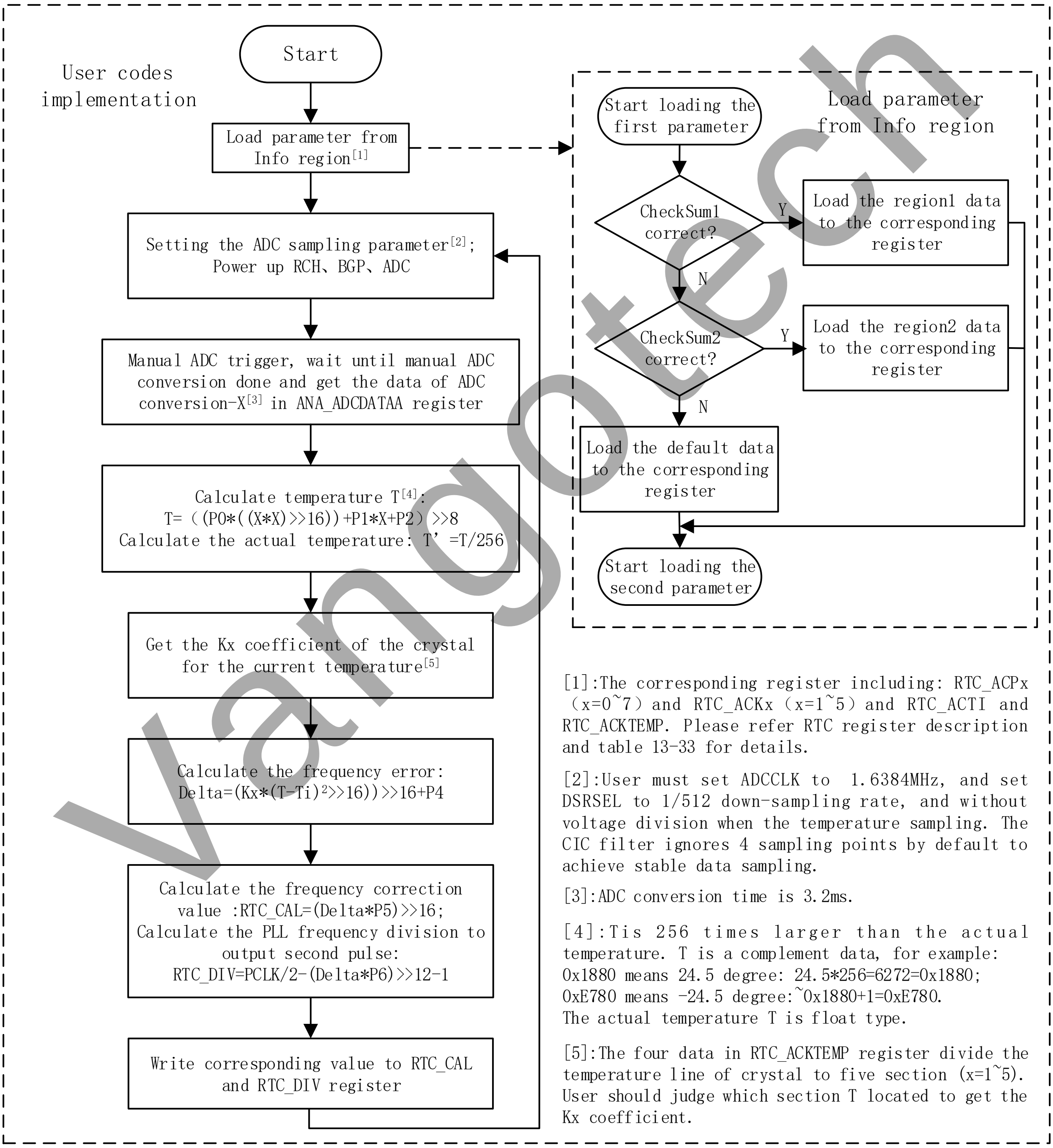
（3） User can calculate the PLL frequency division to output second pulse as follows:

$$RTC\_DIV = PCLK/2 - (Delta * P6) >> 12 - 1$$

Where *P6* is the value in RTC_ACP6 register, or user can calculate *P6* as follows:

$$P6 = PCLK * 2.048 * 10^{-4}$$

13.8.3. RTC Manual Temperature Compensation


User codes implementation
Start
Load parameter from Info region[1]
Setting the ADC sampling parameter[2]; Power up RCH、BGP、ADC
Manual ADC trigger, wait until manual ADC conversion done and get the data of ADC conversion-X[3] in ANA_ADCDATAA register
Calculate temperature T[4]:
T= ((P0*((X*X)>>16))+P1*X+P2)>>8
Calculate the actual temperature: T' =T/256
Get the Kx coefficient of the crystal for the current temperature[5]
Calculate the frequency error:
Delta=(Kx*(T-Ti)²>>16))>>16+P4
Calculate the frequency correction value :RTC_CAL=(Delta*P5)>>16;
Calculate the PLL frequency division to output second pulse:
RTC_DIV=PCLK/2-(Delta*P6)>>12-1
Write corresponding value to RTC_CAL and RTC_DIV register
Load parameter from Info region
Start loading the first parameter
CheckSum1 correct?
Y
Load the region1 data to the corresponding register
N
CheckSum2 correct?
Y
Load the region2 data to the corresponding register
N
Load the default data to the corresponding register
Start loading the second parameter

[1]:The corresponding register including: RTC_ACPx (x=0~7) and RTC_ACKx (x=1~5) and RTC_ACTI and RTC_ACKTEMP. Please refer RTC register description and table 13-33 for details.

[2]:User must set ADCCLK to 1.6384MHz, and set DSRSEL to 1/512 down-sampling rate, and without voltage division when the temperature sampling. The CIC filter ignores 4 sampling points by default to achieve stable data sampling.

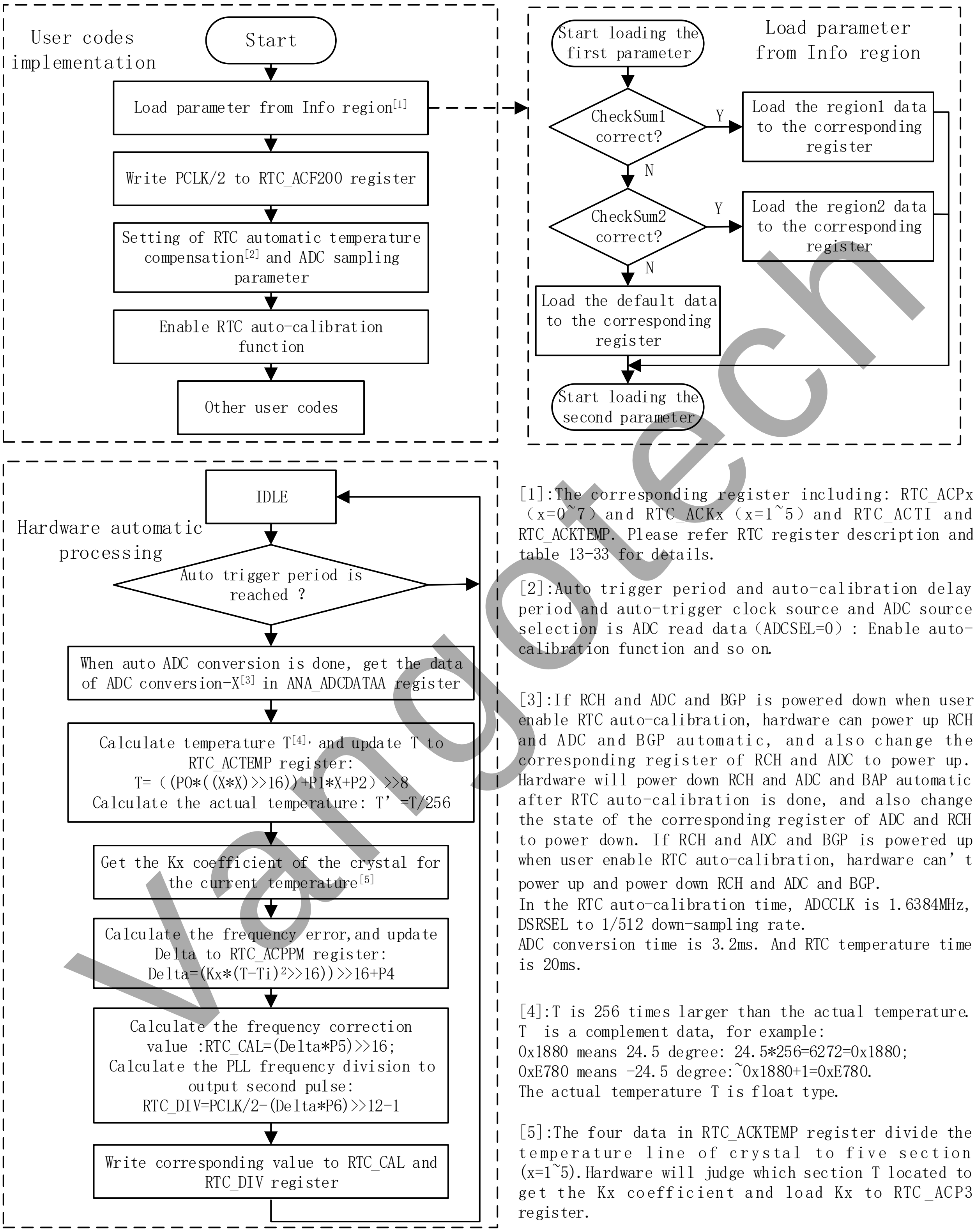
[3]:ADC conversion time is 3.2ms.

[4]:Tis 256 times larger than the actual temperature. T is a complement data, for example: 0x1880 means 24.5 degree: 24.5*256=6272=0x1880; 0xE780 means -24.5 degree:~0x1880+1=0xE780. The actual temperature T is float type.

[5]:The four data in RTC_ACKTEMP register divide the temperature line of crystal to five section (x=1~5). User should judge which section T located to get the Kx coefficient.

Figure 13-2 RTC Manual Temperature Compensation Flow Chart

13.8.4. RTC Automatic Temperature Compensation


User codes implementation
Start
Load parameter from Info region[1]
Write PCLK/2 to RTC_ACF200 register
Setting of RTC automatic temperature compensation[2] and ADC sampling parameter
Enable RTC auto-calibration function
Other user codes
Start loading the first parameter
Load parameter from Info region
CheckSum1 correct?
Y
Load the region1 data to the corresponding register
N
CheckSum2 correct?
Y
Load the region2 data to the corresponding register
N
Load the default data to the corresponding register
Start loading the second parameter
IDLE
Hardware automatic processing
Auto trigger period is reached ?
When auto ADC conversion is done, get the data of ADC conversion-X[3] in ANA_ADCDATAA register
Calculate temperature T[4], and update T to RTC_ACTEMP register:
T= ((P0*((X*X)>>16))+P1*X+P2)>>8
Calculate the actual temperature: T' =T/256
Get the Kx coefficient of the crystal for the current temperature[5]
Calculate the frequency error,and update Delta to RTC_ACPPM register:
Delta=(Kx*(T-Ti)²>>16))>>16+P4
Calculate the frequency correction value :RTC_CAL=(Delta*P5)>>16;
Calculate the PLL frequency division to output second pulse:
RTC_DIV=PCLK/2-(Delta*P6)>>12-1
Write corresponding value to RTC_CAL and RTC_DIV register

[1]:The corresponding register including: RTC_ACPx（x=0~7）and RTC_ACKx（x=1~5）and RTC_ACTI and RTC_ACKTEMP. Please refer RTC register description and table 13-33 for details.

[2]:Auto trigger period and auto-calibration delay period and auto-trigger clock source and ADC source selection is ADC read data（ADCSEL=0）: Enable auto-calibration function and so on.

[3]:If RCH and ADC and BGP is powered down when user enable RTC auto-calibration, hardware can power up RCH and ADC and BGP automatic, and also change the corresponding register of RCH and ADC to power up. Hardware will power down RCH and ADC and BAP automatic after RTC auto-calibration is done, and also change the state of the corresponding register of ADC and RCH to power down. If RCH and ADC and BGP is powered up when user enable RTC auto-calibration, hardware can't power up and power down RCH and ADC and BGP.
In the RTC auto-calibration time, ADCCLK is 1.6384MHz, DSRSEL to 1/512 down-sampling rate.
ADC conversion time is 3.2ms. And RTC temperature time is 20ms.

[4]:T is 256 times larger than the actual temperature.
T is a complement data, for example:
0x1880 means 24.5 degree: 24.5*256=6272=0x1880;
0xE780 means -24.5 degree:~0x1880+1=0xE780.
The actual temperature T is float type.

[5]:The four data in RTC_ACKTEMP register divide the temperature line of crystal to five section (x=1~5).Hardware will judge which section T located to get the Kx coefficient and load Kx to RTC_ACP3 register.

Figure 13-3 RTC Automatic Temperature Compensation Flow Chart

13.8.5. Application of RTC Auto-calibration

（1） The opened resource and anti-conflict operation when RTC auto-calibration on going

If RCH, ADC and BGP is powered down when user enable RTC auto-calibration, hardware can power up RCH and ADC and BGP automatic, and change the corresponding register of RCH and ADC to power up. Hardware will power down RCH and ADC and BAP automatic after RTC auto-calibration is done, and change the state of the corresponding register of ADC and RCH to power down. If RCH and ADC and BGP is powered up when user enable RTC auto-calibration, hardware can't power up and power down RCH and ADC and BGP. Therefore, user should avoid the operation (&= and |=) for ANA_REG3 during auto-calibration to prevent changing the value of ANA_REG3.

（2） The relationship between RTC auto-calibration and ADC division mode

ADC division mode can't be set to capacitive division mode during RTC automatic temperature compensation, user should select resistor division mode or no division mode.

If ADC start to take sample for single channel (Except temp channel) with resistor division mode, user should wait until ACBSY (RTC_INTSTS bit9) clear 0 automatically, and then disable RTC auto-calibration manually. User can enable RTC auto-calibration again after ADC conversion done.

（3） The relationship between RTC auto-calibration and auto trigger period for RTC auto-calibration

If RTC auto-calibration trigger period is several seconds, such as (ACPER + 1)*ACCLK=(5+1)*1 second=6 seconds, RTC auto-calibration will be triggered every 6 seconds.

If RTC auto-calibration trigger period is several minutes, RTC auto-calibration will be triggered on the minute, such as 00-00-00, 00-01-00, 00-02-00, 00-03-00 ...... 00-59-00 and so on. If (ACPER + 1)*ACCLK=(0+1)*1 minute=1 minutes, user enable RTC auto-calibration at the time is 00-00-30, MCU will first trigger RTC auto-calibration at the time is 00-01-00, and then trigger RTC auto-calibration on the minute. If the time enable RTC auto-calibration is not located on the minute, the first trigger time may have 1~59 seconds variation.

If RTC auto-calibration trigger period is several hours, RTC auto-calibration will be triggered on the hour, such as 00-00-00, 01-00-00, 02-00-00, 03-00-00 ...... 23-00-00. If (ACPER + 1)*ACCLK=(0+1)*1 hour=1 hours, user enable RTC auto-calibration at the time is 23-59-30, MCU will first trigger RTC auto-calibration at the time is 00-00-00, and then trigger RTC auto-calibration on the hour. If the time enable RTC auto-calibration is not located on the hour, the first trigger time may have less than 1 hour variation.

If RTC auto-calibration trigger period is 30 seconds and user disable RTC auto-calibration after 25 seconds later(ACEN=0, control by RTC_ACCTRL bit0) and the corresponding configuration unchanged, and then enable RTC auto-calibration again, RTC auto-calibration will be trigger 5 seconds later.

If RTC auto-calibration trigger period is 30 seconds and user disable RTC auto-calibration after 25 seconds later (RTC_ACCTRL=0), and then enable RTC auto-calibration again, RTC auto-calibration will be trigger 30 seconds later.

14. FLASH Controller

14.1. Introduction

The FLASH controller is used to controller the read/write program of embedded FLASH. It supports byte/half-word/word program and sector/chip erase. Programmable timing can be controlled by 1USCYCLE in MISC controller. It will automatically gate the external master access when FLASH is not ready, and always provide correct data with correct access timing. The setting in FLASH controller will be reset after wake-up from sleep or deep-sleep mode, programmer should restore the setting manually after wake-up from these two states.

14.2. Feature

--Support byte/half-word/word programming.

--Support sector/chip erase.

--Support standby mode. When MCU does not access flash, flash automatically enters standby mode. Any access to flash will wake the flash from standby with a wake-up time of 0.

--Support deep-standby mode. When MCU enters sleep mode or deep-standby mode, flash automatically enters deep-standby mode. At the same time, support the manual access to the deep-standby mode by configuration of flash FLASH_DSTB register. Any access to flash will cause flash to wake up from deep-standby with a wake-up time of 10*1ustick.

--Support automatically gate external master when FLASH is not ready.

--Support Info sector read.

--Support FLASH configuration register read/write.

--Programmable program speed.

--Support background checksum function and interrupt.

14.3. Block Diagram

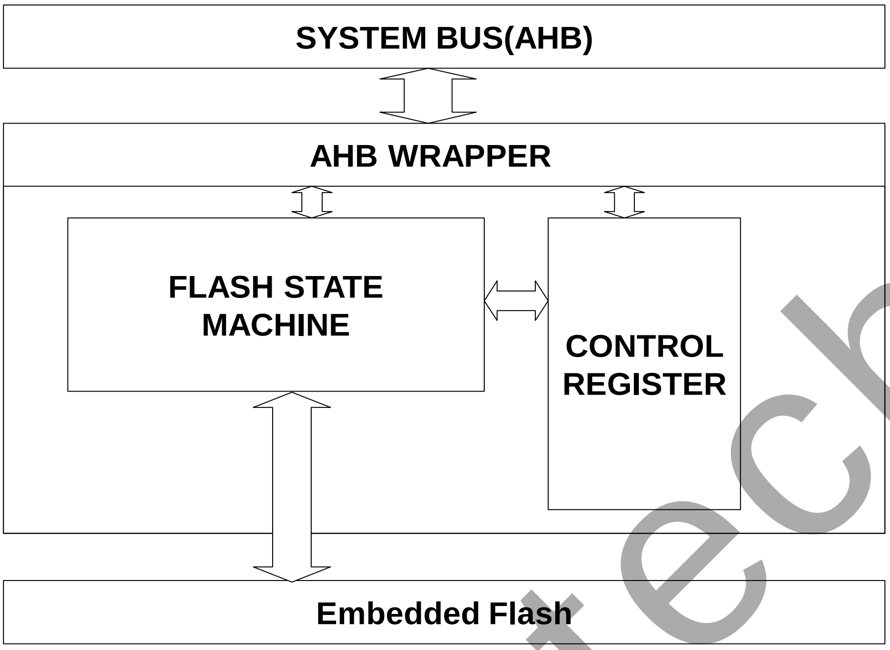


Figure 14-1 Functional Block Diagram of FLASH Controller

14.4. Register Location

Table 14-1 Register Location of FLASH Controller (FLASH Controller Base: 0x00000000)

Name	Type	Address	Description	Default
FLASH_STS	R	0xFFFBC	FLASH programming status register	0x00
FLASH_INT	R/C	0xFFFCC	FLASH Checksum interrupt status	0x0
FLASH_CSSADDR	R/W	0xFFFD0	FLASH Checksum start address	0x00000
FLASH_CSEADDR	R/W	0xFFFD4	FLASH Checksum end address	0x3FFFC
FLASH_CSVALUE	R	0xFFFD8	FLASH Checksum value register	--
FLASH_CSCVALUE	R/W	0xFFFDC	FLASH Checksum compare value register	0x00000000
FLASH_PASS	R/W	0xFFFE0	FLASH password register	0x00000000
FLASH_CTRL	R/W	0xFFFE4	FLASH control register	0x0
FLASH_PGADDR	R/W	0xFFFE8	FLASH program address register	0x00000
FLASH_PGDATA	R/W	0xFFFEC	FLASH program word data register	--

FLASH_PGB0	R/W	0xFFFEC	FLASH program byte data register 0	--
FLASH_PGB1	R/W	0xFFFED	FLASH program byte data register 1	--
FLASH_PGB2	R/W	0xFFFEE	FLASH program byte data register 2	--
FLASH_PGB3	R/W	0xFFFEF	FLASH program byte data register 3	--
FLASH_PGHW0	R/W	0xFFFEC	FLASH program half-word data register 0	--
FLASH_PGHW1	R/W	0xFFFEE	FLASH program half-word data register 1	--
FLASH_SERASE	R/W	0xFFFF4	FLASH sector erase control register	0x00000000
FLASH_CERASE	R/W	0xFFFF8	FLASH chip erase control register	0x00000000
FLASH_DSTB	R/W	0xFFFFC	FLASH deep standby control register	0x00000000

Table 14-2 Register Location of MISC2 Controller for FLASH (MISC2 Base: 0x40013E00)

Name	Type	Address	Description	Default
MISC2_FLASHWC	R/W	0x0000	FLASH wait cycle register	0x2100

14.5. Register Definition

14.5.1. FLASH_PASS Register

Table 14-3 Description of FLASH_PASS Register

Bit	Name	Type	Description	Default
31:1	-	-	Reserved.	0
0	UNLOCK	R	The UNLOCK bit is used to indicate the FLASH program has been unlocked or not. To set this bit, programmer should write 0x55AAAA55 to this register. This bit will be kept high until programmer write any other value to this register. If the UNLOCK bit is 0, all FLASH program or erase or write configuration action will be disabled.	0x0

14.5.2. FLASH_CTRL Register

Table 14-4 Description of FLASH_CTRL Register

Bit	Name	Type	Description	Default
31:4	-	-	Reserved.	0

2	CSINTEN	R/W	This register is used to control the interrupt enable of checksum error. 0: Disable checksum error interrupt. 1: Enable checksum error interrupt.	0x0
1:0	CSMODE	R/W	This register is used to control the checksum mode. 0: Disable checksum function. 1: Always-on checksum mode 2: Checksum start at overflow of timer 2. 3: Checksum start at rising edge of RTC second pulse.	0x0

14.5.3. FLASH_PGADDR Register

Table 14-5 Description of FLASH_PGADDR Register

Bit	Name	Type	Description	Default
31:18	-	-	Reserved.	0
17:0	PGADDR	R/W	This register is used to control the program address before doing program. This is byte address of FLASH IP, please refer to table 14-6 for detail about address under each mode. This address will increment automatically when a successful program is done.	0x000000

Table 14-6 Description of PGADDR and Write Data Port under Different Mode

Mode	PGADDR[17:2]	PGADDR[1:0]	Write Data Port
Normal Word Program	0x0000~0xFFFF	0	FLASH_PGDATA
Normal Byte Program	0x0000~0xFFFF	0	FLASH_PGB0
		1	FLASH_PGB1
		2	FLASH_PGB2
		3	FLASH_PGB3
Normal Half-Word Program	0x0000~0xFFFF	0	FLASH_PGHW0
		2	FLASH_PGHW1
Sector Erase	0x0000~0xFFFF	0	FLASH_SERASE

14.5.4. FLASH_PGDATA Register

Table 14-7 Description of FLASH_PGDATA Register

Bit	Name	Type	Description	Default
31:0	PGDATA	R/W	This register is used to control the program data. When UNLOCK is 1, write to this register will trigger a 4 bytes program automatically. Any access to FLASH IP during this period will be gated until the program is done. A two 32 bits FIFO is inside the FLASH controller, so programmer can do continuous program without interrupt. But if programmer needs to access FLASH IP, like execute program, during this period the FLASH program speed will become slower since more setup time is required for FLASH IP. It is suggested to put your programming program in SRAM, then the maximum program speed can be achieved. It is a must to do word write to this register to trigger a 4 bytes program, byte or half-word write will result-in single byte or two-bytes program.	

14.5.5. FLASH_PGBx Register

Table 14-8 Description of FLASH_PGBx Register

Bit	Name	Type	Description	Default
7:0	PGBx	R/W	This register is used to control the program data. When UNLOCK is 1, write to this register will trigger one-byte program automatically. Any access to FLASH IP during this period will be gated until the program is done. A two 8 bits FIFO is inside the FLASH controller, so programmer can do continuous program without interrupt. But if programmer needs to access FLASH IP, like execute program, during this period the FLASH program speed will become slower since more setup time is required for FLASH IP. It is suggested to put your programming program in SRAM, then the maximum program speed can be achieved. It is a must to do byte write to this register to trigger a single byte program, word or half-word write will result-in 4 bytes or two-bytes program.	

14.5.6. FLASH_PGHWx Register

Table 14-9 Description of FLASH_PGHWx Register

Bit	Name	Type	Description	Default

15:0	PGHWx	R/W	This register is used to control the program data. When UNLOCK is 1, write to this register will trigger a 2 bytes program automatically. Any access to FLASH IP during this period will be gated until the program is done. A two 16 bits FIFO is inside the FLASH controller, so programmer can do continuous program without interrupt. But if programmer needs to access FLASH IP, like execute program, during this period the FLASH program speed will become slower since more setup time is required for FLASH IP. It is suggested to put your programming program in SRAM, then the maximum program speed can be achieved. It is a must to do half-word write to this register to trigger a 2 bytes program, byte or word write will result-in single byte or 4-bytes program.	

14.5.7. FLASH_SERASE Register

Table 14-10 Description of FLASH_SERASE Register

Bit	Name	Type	Description	Default
31:1	-	-	Reserved.	0
0	SERASE	R	This bit is used to indicate if the sector erase is ongoing or not. This bit can be set when UNLOCK is 1 and programmer write 0xAA5555AA to this register, and it will be cleared automatically after the sector erase is done. The address of sector erase is controlled by PGADDR[17:2]. The sector erase time is 4000* 1us tick. One sector is 512 byte.	0x0

14.5.8. FLASH_CERASE Register

Table 14-11 Description of FLASH_CERASE Register

Bit	Name	Type	Description	Default
31:1	-	-	Reserved.	0
0	CERASE	R	This bit is used to indicate if the chip erase is ongoing or not. This bit can be set when UNLOCK is 1 and programmer write 0xAA5555AA to this register, and it will be cleared automatically after the chip erase is done. The chip erase time is 30000* 1us tick.	0x0

14.5.9. FLASH_DSTB Register

Table 14-12 Description of FLASH_DSTB Register

Bit	Name	Type	Description	Default
31:1	-	-	Reserved.	0
0	DSTB	R	This bit is used to indicate if the FLASH IP is entering deep standby. This bit can be set when UNLOCK is 1 and programmer write 0xAA5555AA to this register, and it will be cleared automatically after the FLASH IP wake-up from deep-standby mode. The deep standby mode can exit by any access to FLASH IP, but a 10 μS tick is required for the FLASH IP to back to normal state. During this period, the any access to FLASH will be gated until FLASH is ready.	0x0

14.5.10. FLASH_INT Register

Table 14-13 Description of FLASH_INT Register

Bit	Name	Type	Description	Default
31:1	-	-	Reserved.	0
0	CSERR	R/C	Checksum error status bit. This flag is used to indicate the previous checksum operation has error, which means compare fail from CSVALUE to CSCVALUE. When CSINTEN is 1, an interrupt will be asserted to CPU. Write 1 to clear this flag.	0x0

14.5.11. FLASH_CSSADDR Register

Table 14-14 Description of FLASH_CSSADDR Register

Bit	Name	Type	Description	Default
31:18	-	-	Reserved.	0
17:0	CSSADDR	R/W	Checksum start address register. This register is used to control the start address of checksum. The value in this register is byte address, but the LSB 2 bits are always 0.	0x00000

14.5.12. FLASH_CSEADDR Register

Table 14-15 Description of FLASH_CSEADDR Register

Bit	Name	Type	Description	Default
31:18	-	-	Reserved.	0
17:0	CSEADDR	R/W	Checksum end address register. This register is used to control the end address of checksum. The value in this register is byte address, but the LSB 2 bits are always 0. The checksum range is (CSSADDR =< ADDR =< CSSADDR).	0x3FFFC

14.5.13. FLASH_CSVALUE Register

Table 14-16 Description of FLASH_CSVALUE Register

Bit	Name	Type	Description	Default
31:0	CSVALUE	R	Checksum latched value register. This register is used to represent the checksum result of previous checksum operation.	0x00000000

14.5.14. FLASH_CSCVALUE Register

Table 14-17 Description of FLASH_CSCVALUE Register

Bit	Name	Type	Description	Default
31:0	CSCVALUE	R/W	Checksum compare value register. This register is used to store the expected checksum result. When the checksum is done but the calculated checksum value doesn't match CSCVALUE, the CSERR flag will be set. Calculating method of checksum compare value: accumulate all the values in this range (CSSADDR =< ADDR=< CSEADDR). The cumulative result is valid for 32 bits of data.	0x00000000

14.5.15. FLASH_STS Register

Table 14-18 Description of FLASH_STS Register

Bit	Name	Type	Description	Default

31:5	-	-	Reserved.	0
4:0	STS	R	FLASH controller status register. 1: FLASH operation is done. Others: FLASH controller is in busy state or idle state. Programmer can poll this register to ensure all FLASH operation is done before disabling the FLASH_PASS register.	0x0

14.5.16. MISC2_FLASHWC Register

Table 14-19 Description of MISC2_FLASHWC Register

Bit	Name	Type	Description	Default
31:14	-	-	Reserved.	0
13:8	1USCYCLE	R/W	This register is used for FLASH controller to calculate 1ustick from AHB clock 1ustick = (AHB clock period)*(1USCYCLE+1) This setting is related to the wake-up time of FLASH, and the programming time of FLASH. FLASH wake-up time =1ustick *10. It must meet 1ustick >=1 μs. For example, the clock frequency of AHB is 26.2144MHz. In order to ensure the minimum wake-up time, 1USCYCLE should be set to 26. So, the wake-up time of FLASH is 27 / 26214400 * 10, which is about 10 μs. For example, the clock frequency of AHB is 32.768KHz. In order to ensure the minimum wake-up time, 1USCYCLE should be set to 0. So, the wake-up time of FLASH is 1 / 32768 * 10, which is about 305 μs.	0x21
7:0	-	-	Reserved.	0

15. GPIO Controller

15.1. Introduction

There total 82 IOs in V85X3 and 16 IOs (GPIOA) are controlled by PMU controller with wake-up function. Other IOs (GPIOB~GPIOF) are controlled by GPIO controller which will lose its state at deep sleep mode, but keep their state at sleep mode, programmer should restore the setting manually after wake-up from deep-sleep mode.

15.2. Feature

--Each IO can be input or output mode.

--Each IO can be open drain mode.

--All pins have no pull-up and pull-down.

--GPIOA can wake up Sleep mode and Deep-sleep mode.

15.3. Block Diagram

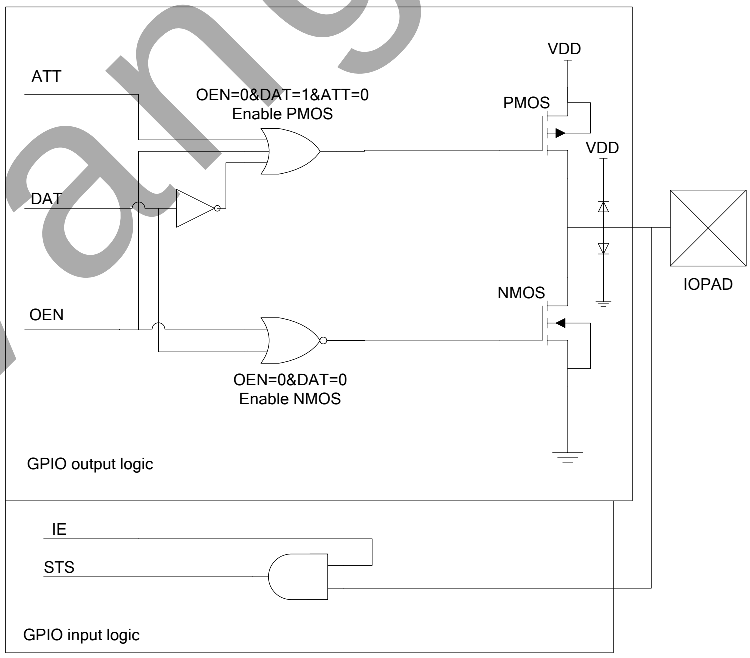


Figure 15-1 Functional Block Diagram of GPIO Controller

15.4. Register Location

Table 15-1 Register Location of the PMU_IOA Controller for GPIO (PMU Base: 0x40014000)

Name	Type	Address	Description	Default
PMU_IOAOEN	R/W	0x0010	IOA output enable register	0xFFFF
PMU_IOAIE	R/W	0x0014	IOA input enable register	0xFFFF
PMU_IOADAT	R/W	0x0018	IOA data register	0x0000
PMU_IOAATT	R/W	0x001C	IOA attribute register	0x0000
PMU_IOAWKUEN	R/W	0x0020	IOA wake-up enable register	0x00000000
PMU_IOASTS	R	0x0024	IOA input status register	--
PMU_IOAINTSTS	R/C	0x0028	IOA interrupt status register	0x0000
PMU_IOASEL	R/W	0x0038	IOA special function select register	0x0000
PMU_IOANODEG	R/W	0x0050	IOA no-deglitch control register.	0x0000

Table 15-2 Register Location of GPIO Controller (GPIO Base: 0x40000000)

Name	Type	Address	Description	Default
IOB_OEN	R/W	0x0020	IOB output enable register	0xFFFF
IOB_IE	R/W	0x0024	IOB input enable register	0xFFFF
IOB_DAT	R/W	0x0028	IOB data register	0x0000
IOB_ATT	R/W	0x002C	IOB attribute register	0x0000
IOB_STS	R	0x0030	IOB input status register	--
IOC_OEN	R/W	0x0040	IOC output enable register	0xFFFF
IOC_IE	R/W	0x0044	IOC input enable register	0xFFFF
IOC_DAT	R/W	0x0048	IOC data register	0x0000
IOC_ATT	R/W	0x004C	IOC attribute register	0x0000
IOC_STS	R	0x0050	IOC input status register	--
IOD_OEN	R/W	0x0060	IOD output enable register	0xFFFF
IOD_IE	R/W	0x0064	IOD input enable register	0xFFFF
IOD_DAT	R/W	0x0068	IOD data register	0x0000
IOD_ATT	R/W	0x006C	IOD attribute register	0x0000
IOD_STS	R	0x0070	IOD input status register	--

IOE_OEN	R/W	0x0080	IOE output enable register	0xFFFF
IOE_IE	R/W	0x0084	IOE input enable register	0xFFFF
IOE_DAT	R/W	0x0088	IOE data register	0x0000
IOE_ATT	R/W	0x008C	IOE attribute register	0x0000
IOE_STS	R	0x0090	IOE input status register	--
IOF_OEN	R/W	0x00A0	IOF output enable register	0x3
IOF_IE	R/W	0x00A4	IOF input enable register	0x3
IOF_DAT	R/W	0x00A8	IOF data register	0x0
IOF_ATT	R/W	0x00AC	IOF attribute register	0x0
IOF_STS	R	0x00B0	IOF input status register	--
IOB_SEL	R/W	0x00C0	IOB special function select register	0x00
IOE_SEL	R/W	0x00CC	IOE special function select register	0x00
IO_MISC	R/W	0x00E0	IO misc. control register	0x00

15.5. Register Definition

15.5.1. PMU_IOAOEN Register

Table 15-3 Description of PMU_IOAOEN Register

Bit	Name	Type	Description	Default
31:16	-	-	Reserved.	0
15:0	IOAOEN	R/W	Each bit controls the IOA's output enable signal, referred to Table 15-7 for detail of IO state. 0: Enable IO's output function. 1: Disable IO's output function.	0xFFFF

15.5.2. PMU_IOAIE Register

Table 15-4 Description of PMU_IOAIE Register

Bit	Name	Type	Description	Default
31:16	-	-	Reserved.	0

15:0	IOAIE	R/W	Each bit controls the IOA's input enable signal, referred to Table 15-7 for detail of IO state. 0: Disable IO's input function. 1: Enable IO's input function.	0xFFFF

15.5.3. PMU_IOADAT Register

Table 15-5 Description of PMU_IOADAT Register

Bit	Name	Type	Description	Default
31:16	-	-	Reserved.	0
15:0	IOADAT	R/W	Each bit controls the IOA's output data and pull low/high function, referred to Table 15-7 for detail of IO state.	0x0000

15.5.4. PMU_IOAATT Register

Table 15-6 Description of PMU_IOAATT Register

Bit	Name	Type	Description	Default
31:16	-	-	Reserved.	0
15:0	IOAATT	R/W	Each bit controls the IOA's attribute, referred to Table 15-7 for detail of IO state. When an IO is set to output mode (GPIO or special function), this bit is used to control the CMOS or open drain mode of the IO pad. 0: CMOS mode. 1: Open drain mode (disable PMOS output).	0x0000

Table 15-7 IO Status under Different Kind of Setting

IOx Setting			IO Status
IOxOEN	IOxDAT	IOxATT	
1	0	0	Disable output function.
1	1	0	Disable output function.
1	0	1	Disable output function.
1	1	1	Disable output function.
0	0	0	Output low

0	1	0	Output high
0	0	1	Open drain output low.
0	1	1	Open drain pull-high

15.5.5. PMU_IOAWKUEN Register

Table 15-8 Description of PMU_IOAWKUEN Register

Bit	Name	Type	Description	Default
31:0	IOAWKUEN	R/W	Every 2 bits control the IOA's wake up or interrupt enable function. Bit [1:0]: IOA0WKUEN[1：0] Bit [3:2]: IOA1WKUEN[1：0] …… Bit [31:30]: IOA15WKUEN[1：0] Refer to Table 15-9 for detail of each wake-up mode.	0x00000000

Table 15-9 Description of each IO wake-up mode

IOAyWKUEN[1：0]	IOAyDAT	Wake-up Event
0	X	Disable wake-up function
1	0	Rising edge
	1	Falling Edge
2	0	High Level
	1	Low level
3	X	Rising or falling edge

Which y=0 ... 15, indicating an IO port.

For rising edge or falling edge wake-up source, since the H/W will use the final latch IO status before entering sleep or deep-sleep mode, so the programmer needs to wait until the IO status change back to normal state. For example, when rising edge mode is chosen, the programmer should wait until the IO status back to low state to ensure the rising edge can be detected correctly. For high level or low level source, IO have no debounce in normal interrupt or wake up from sleep or deep sleep mode, but IO have four RTCCLK clock cycles debounce When CPU wake up from sleep or deep sleep mode.

15.5.6. PMU_IOASTS Register

Table 15-10 Description of PMU_IOASTS Register

Bit	Name	Type	Description	Default
31:16	-	-	Reserved.	0
15:0	IOASTS	R	Each bit represents the current IOA's input data value.	

15.5.7. PMU_IOAINTSTS Register

Table 15-11 Description of PMU_IOAINTSTS Register

Bit	Name	Type	Description	Default
31:16	-	-	Reserved.	0
15:0	IOAINTSTS	R/C	Each bit represents the IOA's interrupt status. The corresponded bit will be set to 1 when corresponded wake-up event is detected. This register can be clear to 0 by writing corresponded bit to 1.	0x0000

15.5.8. PMU_IOASEL Register

Table 15-12 Description of PMU_IOASEL Register

Bit	Name	Type	Description	Default
31:8	-	-	Reserved.	0
7	IOA_SEL7	R/W	IOA7 special function select register. 0: GPIO 1: Special function 1 (RTC_PLLDIV).	0x0
6	IOA_SEL6	R/W	IOA6 special function select register. 0: GPIO 1: Special function 2 (CMP2_O).	0x0
5:4	-	-	Reserved.	0
3	IOA_SEL3	R/W	IOA3 special function select register. 0: GPIO 1: Special function 1 (RTC_PLLDIV).	0x0
2:0	-	-	Reserved.	0

15.5.9. PMU_IOANODEG Register

Table 15-13 Description of PMU_IOANODEG Register

Bit	Name	Type	Description	Default
31:16	-	-	Reserved.	0
15:0	IOANODEG	R/W	Each bit control if the IOA wake-up signal will go through de-glitch circuit or not. If set this bit to 1, the corresponded IOA wake-up signal will not go through de-glitch circuit which can have a faster wake-up time. This bit affect the edge wake-up signal under sleep and deep-sleep mode. 0: IOA wake-up signal will go through de-glitch circuit. 1: IOA wake-up signal will not go through de-glitch circuit.	0x0000

15.5.10. IOX_OEN Register

Table 15-14 Description of IOX_OEN Register

Bit	Name	Type	Description	Default
31:16	-	-	Reserved.	0
15:0	IOXOEN*	R/W	Each bit control the IOX's output enable signal, referred to Table 15-7 for detail of IO state. 0: Enable IO's output function. 1: Disable IO's output function.	0xFFFF

Note*: The bit6 & bit7 of IOE_OEN should be set to 1.

15.5.11. IOX_IE Register

Table 15-15 Description of IOX_IE Register

Bit	Name	Type	Description	Default
31:16	-	-	Reserved.	0
15:0	IOXIE*	R/W	Each bit control the IOX's input enable signal, referred to Table 15-7 for detail of IO state. 0: Disable IO's input function. 1: Enable IO's input function.	0xFFFF

Note*: The bit6 & bit7 of IOE_IE should be set to 1.

15.5.12. IOX_DAT Register

Table 15-16 Description of IOX_DAT Register

Bit	Name	Type	Description	Default
31:16	-	-	Reserved.	0
15:0	IOXDAT	R/W	Each bit controls the IOX's output data and pull low/high function, referred to Table 15-7 for detail of IO state.	0x0000

15.5.13. IOX_ATT Register

Table 15-17 Description of IOX_ATT Register

Bit	Name	Type	Description	Default
31:16	-	-	Reserved.	0
15:0	IOXATT	R/W	Each bit controls the IOX's attribute, referred to Table 15-7 for detail of IO state. When an IO is configured to a special mode, like UART or SPI, programmer can set the corresponded IOXATT to 1 to let it become open drain mode. Which means when output high, it will become input floating, when output low, it will keep the same output low behavior.	0x0000

15.5.14. IOX_STS Register

Table 15-18 Description of IOX_STS Register

Bit	Name	Type	Description	Default
31:16	-	-	Reserved.	0
15:0	IOXSTS	R	Each bit represents the current IOX's input data value.	--

15.5.15. IOB_SEL Register

Table 15-19 Description of IOB_SEL Register

Bit	Name	Type	Description	Default
31:7	-	-	Reserved.	0

6	IOB_SEL6	R/W	IOB6 special function select register 0: GPIO or special function 1/2 1: Special function 3(RTCCLK) when special function 1/2 is not enabled.	0x0
5:3	-	-	Reserved.	0
2	IOB_SEL2	R/W	IOB2 special function select register 0: GPIO or special function 1/2 1: Special function 3 (PLLL) when special function 1/2 is not enabled.	0x0
1	IOB_SEL1	R/W	IOB1 special function select register 0: GPIO or special function 1/2 1: Special function 3 (PLLH divider) when special function 1/2 is not enabled.	0x0
0	-	-	Reserved.	0

15.5.16. IOE_SEL Register

Table 15-20 Description of IOE_SEL Register

Bit	Name	Type	Description	Default
31:8	-	-	Reserved.	0
7	IOE_SEL7	R/W	IOE7 special function select register. 1: Special function 1 (CMP1_O).	0x0
6:0	-	-	Reserved.	0

15.5.17. IO_MISC Register

Table 15-21 Description of IO_MISC Register

Bit	Name	Type	Description	Default
31:6	-	-	Reserved.	0
5	I2CIOC	R/W	This register is used to control the I2C function is at IOB or IOC. 0: I2C is at IOB13~IOB14. 1: I2C is at IOC4~IOC5.	0x0

4:3	-	-	Reserved.	0
2:0	PLLHDIV	R/W	When IOB1 is selected to special function 3, this register is used to control the divide ratio of PLLH's output. 0: /1 1: /2 2: /4 3: /8 4: /16 Others: Reserved.	0x0

15.6. Special Function of IO

15.6.1. Special Function of IOA

The following table shows the special function of IOA, the special function will be turn-on when corresponded module is enabled.

Table 15-22 Special Function of IOA

IO	Special Function 1	Special Function 2	Special Function 3	Special Function 4
IOA0	SWCLK (When MODE is 0)		LCDSEG54	
IOA1	SWDIO (When MODE is 0)		LCDSEG53	
IOA2			LCDSEG52	
IOA3	RTC_PLLDIV		LCDSEG51	
IOA4			LCDSEG66	CMP2_P
IOA5			LCDSEG67	CMP2_N
IOA6	CMP2_O		LCDSEG68	
IOA7	RTC_PLLDIV		LCDSEG69	
IOA8			LCDSEG50	ADC_CH3
IOA9			LCDSEG49	ADC_CH4

IOA10			LCDSEG48	ADC_CH5
IOA11			LCDSEG47	ADC_CH6
IOA12	UART RX0		LCDSEG71	
IOA13	UART RX1	ISO7816 RX0	LCDSEG73	
IOA14	UART RX2		LCDSEG13	
IOA15	UART RX3	ISO7816 RX1	LCDSEG15	

15.6.2. Special Function of IOB

The following table shows the special function of IOB, the special function will be turn-on when corresponded module is enabled. But when special function is LCD COM/SEG or ADC or CMP or X6_5M or VDCIN, programmer should disable GPIO input and disable GPIO output manually and disable other special function on this GPIO to ensure the correctness of these special functions.

Table 15-23 Special function of IOB

IO	Special Function 1	Special Function 2	Special Function 3	Special Function 4
IOB0	UART RX4	PWM0		LCDSEG43
IOB1	UART RX5		PLLH divider	LCDSEG45
IOB2	UART TX0		PLLL	LCDSEG70
IOB3	UART TX1	ISO7816 CLK0		LCDSEG72
IOB4	UART TX2			LCDSEG12
IOB5	UART TX3	ISO7816 CLK1		LCDSEG14
IOB6	UART TX4	PWM1	RTCCLK	LCDSEG44
IOB7	UART TX5			LCDSEG46
IOB8				LCDSEG35
IOB9	SPI1CSN			LCDSEG36
IOB10	SPI1CLK			LCDSEG37
IOB11	SPI1MISO			LCDSEG38
IOB12	SPI1MOSI			LCDSEG39
IOB13	I2CSCL (I2CIOC=0)	PWM2		LCDSEG40
IOB14	I2CSDA (I2CIOC=0)	PWM3		LCDSEG41
IOB15	TIMER EXT CLK			LCDSEG42

15.6.3. Special Function of IOC

The following table shows the special function of IOC, the special function will be turn-on when corresponded module is enabled. But when special function is LCD COM/SEG or ADC or CMP or X6_5M or VDCIN, programmer should disable GPIO input and disable GPIO output manually and disable other special function on this GPIO to ensure the correctness of these special functions.

Table 15-24 Special function of IOC

IO	Special Function 1	Special Function 2	Special Function 3
IOC0	SPI2CSN		LCDSEG16
IOC1	SPI2CLK		LCDSEG17
IOC2	SPI2MISO		LCDSEG18
IOC3	SPI2MOSI		LCDSEG19
IOC4		I2CSCL (I2CIOC=1)	LCDSEG20
IOC5		I2CSDA (I2CIOC=1)	LCDSEG21
IOC6			LCDSEG22
IOC7			LCDSEG23
IOC8			LCDSEG24
IOC9			LCDSEG25
IOC10			LCDSEG26
IOC11			LCDSEG27
IOC12			LCDSEG28
IOC13			LCDSEG29
IOC14			LCDSEG30
IOC15			LCDSEG31

15.6.4. Special Function of IOD

The following table shows the special function of IOD, the special function will be turn-on when corresponded module is enabled. But when special function is LCD COM/SEG or ADC or CMP or X6_5M or VDCIN, programmer should disable GPIO input and disable GPIO output manually and disable other special function on this GPIO to ensure the correctness of these special functions.

Table 15-25 Special function of IOD

IO	Special Function 1	Special Function 2

IOD0	LCDCOM0	
IOD1	LCDCOM1	
IOD2	LCDCOM2	
IOD3	LCDCOM3	
IOD4	LCDCOM4	LCDSEG0
IOD5	LCDCOM5	LCDSEG1
IOD6	LCDCOM6	LCDSEG2
IOD7	LCDCOM7	LCDSEG3
IOD8	LCDSEG4	
IOD9	LCDSEG5	
IOD10	LCDSEG6	
IOD11	LCDSEG7	
IOD12	LCDSEG8	
IOD13	LCDSEG9	
IOD14	LCDSEG10	
IOD15	LCDSEG11	

15.6.5. Special Function of IOE

The following table shows the special function of IOE, the special function will be turn-on when corresponded module is enabled. But when special function is LCD COM/SEG or ADC or CMP or X6_5M or VDCIN, programmer should disable GPIO input and disable GPIO output manually and disable other special function on this GPIO to ensure the correctness of these special functions.

Table 15-26 Special function of IOE

IO	Special Function 1	Special Function 2	Special Function 3
IOE0		LCDSEG74	
IOE1		LCDSEG75	
IOE2		LCDSEG76	
IOE3		LCDSEG77	
IOE4		LCDSEG63	ADC_CH7
IOE5		LCDSEG62	ADC_CH8

IOE6		LCDSEG61	ADC_CH9, Tiny ADC 0
IOE7	CMP1_O	LCDSEG60	ADC_CH11, Tiny ADC 1
IOE8		LCDSEG59	CMP1_P
IOE9		LCDSEG58	CMP1_N
IOE10		LCDSEG32	
IOE11		LCDSEG33	
IOE12		LCDSEG34	
IOE13		LCDSEG55	
IOE14		LCDSEG56	
IOE15		LCDSEG57	

15.6.6. Special Function of IOF

The following table shows the special function of IOF, the special function will be turn-on when corresponded module is enabled. But when special function is LCD COM/SEG or ADC or CMP or X6_5M or VDCIN, programmer should disable GPIO input and disable GPIO output manually and disable other special function on this GPIO to ensure the correctness of these special functions.

Table 15-27 Special function of IOF

IO	Special Function 1
IOF0	X6_5MI
IOF1	X6_5MO

16. DMA Controller

16.1. Introduction

The DMA controller is used to transfer data from memory to memory or transfer data from memory to IO or from IO to memory. The DMA controller is also integrated with an AHB to APB bridge, so when DMA is doing APB transfer, the AHB performance will not be affected by slow peripheral. There are total 4 channels integrated in V85X3 and each channel's priority is round-robin. The setting in DMA controller will be reset after wake-up from sleep or deep-sleep mode, programmer should restore the setting manually after wake-up from these two states.

16.2. Feature

--Memory to Memory Transfer

--Memory to IO Transfer

--IO to Memory Transfer

--Software mode or Hardware DMA request mode.

--Support Fix, Package Round or Frame Round Address mode

--Support Package/Frame/Data-abort IRQ generation.

--Support detection of data abort on bus.

--Integrated with AHB to APB Bridge.

--Support AES 128/192/256 encode/decode

16.3. Block Diagram

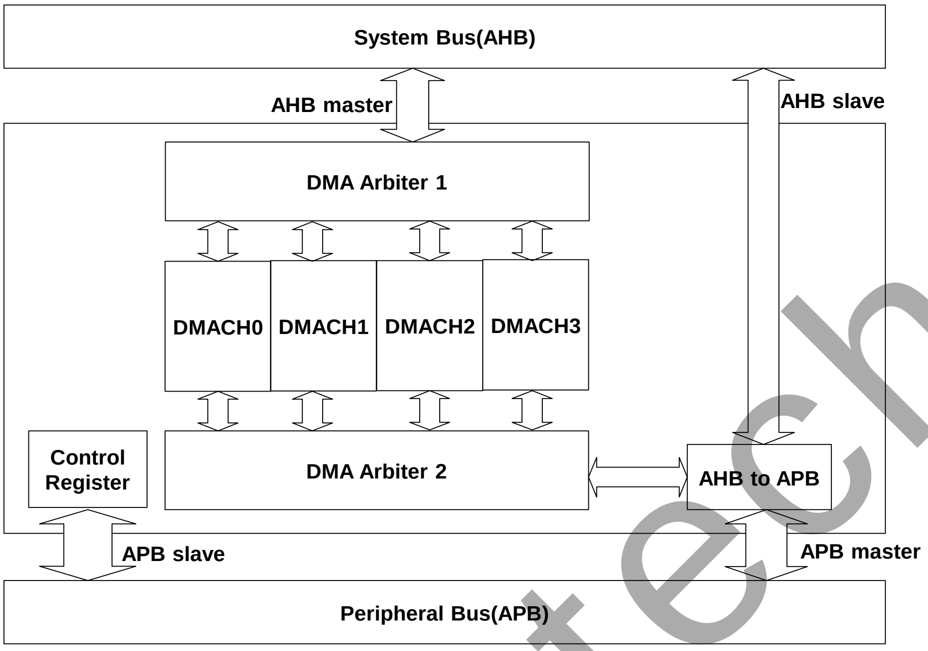


Figure 16-1 Functional Block Diagram of DMA Controller

16.4. Register Location

Table 16-1 Register Location of DMA Controller (DMA Base: 0x40010000)

Name	Type	Address	Description	Default
DMA_IE	R/W	0x0000	DMA interrupt enable register	0x000
DMA_STS	R/W	0x0004	DMA status register	0x0000
DMA_C0CTL	R/W	0x0010	DMA channel 0 control register	0x00000000
DMA_C0SRC	R/W	0x0014	DMA channel 0 source register	0x00000000
DMA_C0DST	R/W	0x0018	DMA channel 0 destination register	0x00000000
DMA_C0LEN	R	0x001C	DMA channel 0 transfer length register	0x0000
DMA_C1CTL	R/W	0x0020	DMA channel 1 control register	0x00000000
DMA_C1SRC	R/W	0x0024	DMA channel 1 source register	0x00000000
DMA_C1DST	R/W	0x0028	DMA channel 1 destination register	0x00000000
DMA_C1LEN	R	0x002C	DMA channel 1 transfer length register	0x0000
DMA_C2CTL	R/W	0x0030	DMA channel 2 control register	0x00000000

DMA_C2SRC	R/W	0x0034	DMA channel 2 source register	0x00000000
DMA_C2DST	R/W	0x0038	DMA channel 2 destination register	0x00000000
DMA_C2LEN	R	0x003C	DMA channel 2 transfer length register	0x0000
DMA_C3CTL	R/W	0x0040	DMA channel 3 control register	0x00000000
DMA_C3SRC	R/W	0x0044	DMA channel 3 source register	0x00000000
DMA_C3DST	R/W	0x0048	DMA channel 3 destination register	0x00000000
DMA_C3LEN	R	0x004C	DMA channel 3 transfer length register	0x0000
DMA_AESCTL	R/W	0x0050	DMA AES control register	0x00000000
DMA_AESKEY0	R/W	0x0060	DMA AES key 0 register	0x00000000
DMA_AESKEY1	R/W	0x0064	DMA AES key 1 register	0x00000000
DMA_AESKEY2	R/W	0x0068	DMA AES key 2 register	0x00000000
DMA_AESKEY3	R/W	0x006C	DMA AES key 3 register	0x00000000
DMA_AESKEY4	R/W	0x0070	DMA AES key 4 register	0x00000000
DMA_AESKEY5	R/W	0x0074	DMA AES key 5 register	0x00000000
DMA_AESKEY6	R/W	0x0078	DMA AES key 6 register	0x00000000
DMA_AESKEY7	R/W	0x007C	DMA AES key 7 register	0x00000000

16.5. Register Definition

16.5.1. DMA_IE Register

Table 16-2 Description of DMA_IE Register

Bit	Name	Type	Description	Default
31:12	-	-	Reserved.	0
11	C3DAIE	R/W	Channel 3 data abort interrupt enable 0: Disable 1: Enable	0x0
10	C2DAIE	R/W	Channel 2 data abort interrupt enable 0: Disable 1: Enable	0x0

9	C1DAIE	R/W	Channel 1 data abort interrupt enable 0: Disable 1: Enable	0x0
8	C0DAIE	R/W	Channel 0 data abort interrupt enable 0: Disable 1: Enable	0x0
7	C3FEIE	R/W	Channel 3 frame end interrupt enable 0: Disable 1: Enable	0x0
6	C2FEIE	R/W	Channel 2 frame end interrupt enable 0: Disable 1: Enable	0x0
5	C1FEIE	R/W	Channel 1 frame end interrupt enable 0: Disable 1: Enable	0x0
4	C0FEIE	R/W	Channel 0 frame end interrupt enable 0: Disable 1: Enable	0x0
3	C3PEIE	R/W	Channel 3 package end interrupt enable 0: Disable 1: Enable	0x0
2	C2PEIE	R/W	Channel 2 package end interrupt enable 0: Disable 1: Enable	0x0
1	C1PEIE	R/W	Channel 1 package end interrupt enable 0: Disable 1: Enable	0x0
0	C0PEIE	R/W	Channel 0 package end interrupt enable 0: Disable 1: Enable	0x0

16.5.2. DMA_STS Register

Table 16-3 Description of DMA_STS Register

Bit	Name	Type	Description	Default
31:16	-	-	Reserved.	0
15	C3DA	R/C	Channel 3 data abort interrupt flag, write 1 to clear this flag.	0x0
14	C2DA	R/C	Channel 2 data abort interrupt flag, write 1 to clear this flag.	0x0
13	C1DA	R/C	Channel 1 data abort interrupt flag, write 1 to clear this flag.	0x0
12	C0DA	R/C	Channel 0 data abort interrupt flag, write 1 to clear this flag.	0x0
11	C3FE	R/C	Channel 3 frame end interrupt flag, write 1 to clear this flag.	0x0
10	C2FE	R/C	Channel 2 frame end interrupt flag, write 1 to clear this flag.	0x0
9	C1FE	R/C	Channel 1 frame end interrupt flag, write 1 to clear this flag.	0x0
8	C0FE	R/C	Channel 0 frame end interrupt flag, write 1 to clear this flag.	0x0
7	C3PE	R/C	Channel 3 package end interrupt flag, write 1 to clear this flag.	0x0
6	C2PE	R/C	Channel 2 package end interrupt flag, write 1 to clear this flag.	0x0
5	C1PE	R/C	Channel 1 package end interrupt flag, write 1 to clear this flag.	0x0
4	C0PE	R/C	Channel 0 package end interrupt flag, write 1 to clear this flag.	0x0
3	C3BUSY	R	DMA channel 3 busy register 0: Idle 1: Busy	0x0
2	C2BUSY	R	DMA channel 2 busy register. 0: Idle 1: Busy	0x0

1	C1BUSY	R	DMA channel 1 busy register. 0: Idle 1: Busy	0x0
0	C0BUSY	R	DMA channel 0 busy register. 0: Idle 1: Busy	0x0

16.5.3. DMA_CxCTL Register

Table 16-4 shows the bit assignment of DMA_CxCTL register, the data in this register will be latched into DMA channel after the transfer is start, so any modification to this register won't affect the on-going DMA transfer. Only STOP bit can stop the DMA transfer immediately.

Table 16-4 Description of DMA_CxCTL Register

Bit	Name	Type	Description	Default
31:24	FLEN	R/W	Package number register, actual transfer package number is (FLEN + 1). Total length is (FLEN + 1) * (PLEN + 1).	0x0
23:16	PLEN	R/W	Package length register, actual transfer package length is (PLEN + 1). Total length is (FLEN + 1) * (PLEN + 1).	0x0
15	STOP	R/W	Force stop DMA transfer, write 1 to this bit will force the DMA channel back to idle state, programmer should clear this bit to 0 if another DMA transfer need to be assigned into the same channel. 0: Normal mode. 1: Force stop DMA transfer.	0x0
14	AESEN	R/W	Enable AES encrypt/decrypt function of DMA channel. Only DMA channel 3 supports AES function. When AES function is enabled, the SIZE should be set to 32 bits mode and SMODE and TMODE should be set to 1 or 2. And package size should be multiply of 4. 0: Disable. 1: Enable.	0x0
13	CONT	R/W	Continuous mode, DMA transfer will not stop until STOP bit is set to 1. Every time DMA complete all package and frame transfer, it will start from beginning and do the transfer continuously.	0x0

			0: Discontinuous mode. 1: Continuous mode.	
12	TMODE	R/W	Transfer mode selection register. 0: One DMA request only transfers one single data. 1: One DMA request transfers one package data.	0x0
11:7	DMASEL	R/W	DMA request source selection. Please refer to Table 16-5 of detail about each DMA	0x0
6:5	DMODE	R/W	Destination address mode. 0: Fix. 1: Incremental but rounded at package end. 2: Incremental but rounded at frame end. 3: Reserved.	0x0
4:3	SMODE	R/W	Source address mode. 0: Fix. 1: Incremental but rounded at package end. 2: Incremental but rounded at frame end. 3: Reserved.	0x0
2:1	SIZE	R/W	Transfer size mode. 0: Byte (8 bits). 1: Half-word (16 bits) 2: Word (32 bits) 3: Reserved.	0x0
0	EN	R/W	DMA channel enable register. 0: Disable DMA channel (no effect when CONT is 1) 1: Enable DMA channel. This bit will be cleared automatically by hardware when a DMA transfer is done at CONT is 0.	0x0

Table 16-5 DMA Source Selection

DMASEL	Source	DMASEL	Source	DMASEL	Source	DMASEL	Source
0	Software	8	UART3 TX	16	ISO78161 TX	24	UART 32K 0
1	-	9	UART3 RX	17	ISO78161 RX	25	UART 32K 1

2	UART0 TX	10	UART4 TX	18	TIMER 0	26	CMP1
3	UART0 RX	11	UART4 RX	19	TIMER 1	27	CMP2
4	UART1 TX	12	UART5 TX	20	TIMER 2	28	-
5	UART1 RX	13	UART5 RX	21	TIMER 3	29	-
6	UART2 TX	14	ISO78160 TX	22	SPI1 TX	30	SPI2 TX
7	UART2 RX	15	ISO78160 RX	23	SPI1 RX	31	SPI2 RX

16.5.4. DMA_CxSRC Register

Table 16-6 Description of DMA_CxSRC Register

Bit	Name	Type	Description	Default
31:0	SRC	R/W	DMA source address register. When SIZE in DMA_CxCTL is 1, then this register must be half-word aligned. When SIZE in DMA_CxCTL is 2, then this register must be word aligned. When the SRC is set to 0x4001xxxx, then it will be switch to IO read automatically.	0x00000000

16.5.5. DMA_CxDST Register

Table 16-7 Description of DMA_CxDST Register

Bit	Name	Type	Description	Default
31:0	DST	R/W	DMA destination address register. When SIZE in DMA_CxCTL is 1, then this register must be half-word aligned. When SIZE in DMA_CxCTL is 2, then this register must be word aligned. When the DST is set to 0x4001xxxx, then it will be switch to IO write automatically.	0x00000000

16.5.6. DMA_CxLEN Register

Table 16-8 Description of DMA_CxLEN Register

Bit	Name	Type	Description	Default
31:16	-	-	Reserved.	0
15:8	CFLEN	R	Current transferred package number. The total length	0x00

			of DMA transmission is CFLEN * (PLEN +1) + CPLEN. After all packages are transferred, it will be automatically cleared.	
7:0	CPLEN	R	Current transferred package length. The total length of DMA transmission is CFLEN * (PLEN +1) + CPLEN. After all packages are transferred, it will be automatically cleared.	0x00

16.5.7. DMA_AESCTL Register

Table 16-9 Description of DMA_AESCTL Register

Bit	Name	Type	Description	Default
31:4	-	-	Reserved.	0
3:2	MODE	R/W	AES mode selection register. 0: AES128 1: AES192 2: AES256 3: Reserved.	0x0
1	-	-	Reserved.	0
0	ENC	R/W	AES encode/decode selection register. 0: Decode 1: Encode	0x0

16.5.8. DMA_AESKEYx Register

Table 16-10 Description of DMA_AESKEYx Register

Bit	Name	Type	Description	Default
31:0	KEYx	R/W	AES KEY register. KEY0: bit 31~0 KEY1: bit 63~32 KEY2: bit 95~64 KEY3: bit 127~96 KEY4: bit 159~128	0x00000000

			KEY5: bit 191~160 KEY6: bit 223~192 KEY7: bit 255~224. When mode is AES128, only bit 127~0 is used. When mode is AES192, only bit 191~0 is used. When mode is AES256, bit 255~0 is used.	

17. UART Controller

17.1. Introduction

The UART controller is used to transmit/receive data via UART protocol. There are total 6 UART controller in V85X3, each UART controller can be program individually and has its own interrupt to CPU. The UART controller can support 8 bits transfer without parity or 9 bits transfer with even or odd parity. One data buffer and one shift register is used for transmit engine, and another set of data buffer and shift register are used for receive engine. The setting in UART controller will be reset after wake-up from sleep or deep-sleep mode, programmer should restore the setting manually after wake-up from these two states. The baud rate range of UART is 300~819200bps.

17.2. Feature

--Programmable baud rate generator

--8 bits or 9 bits with odd/even parity transfer.

--Parity error detection.

--Transmit/Receive interrupt flag.

--Transmit/Receive overrun interrupt flag.

17.3. Block Diagram

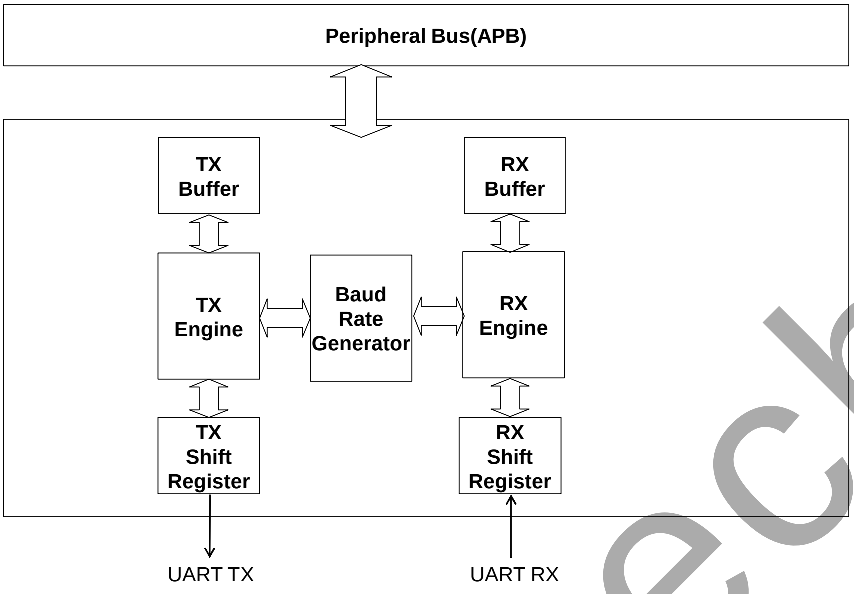


Figure 17-1 Functional Block Diagram of UART Controller

17.4. Register Location

Table 17-1 Register Location of UART Controller (UART Base: 0x40011800)

Name	Type	Address	Description	Default
UART0_DATA	R/W	0x0000	UART0 data register	0x00
UART0_STATE	R/C	0x0004	UART0 status register	0x00
UART0_CTRL	R/W	0x0008	UART0 control register	0x000
UART0_INTSTS	R/C	0x000C	UART0 interrupt status register	0x00
UART0_BAUDDIV	R/W	0x0010	UART0 baud rate divide register	0x00000
UART0_CTRL2	R/W	0x0014	UART0 control register 2	0x0
UART1_DATA	R/W	0x0020	UART1 data register	0x00
UART1_STATE	R/C	0x0024	UART1 status register	0x00
UART1_CTRL	R/W	0x0028	UART1 control register	0x000
UART1_INTSTS	R/C	0x002C	UART1 interrupt status register	0x00
UART1_BAUDDIV	R/W	0x0030	UART1 baud rate divide register	0x00000
UART1_CTRL2	R/W	0x0034	UART1 control register 2	0x0

UART2_DATA	R/W	0x0040	UART2 data register	0x00
UART2_STATE	R/C	0x0044	UART2 status register	0x00
UART2_CTRL	R/W	0x0048	UART2 control register	0x000
UART2_INTSTS	R/C	0x004C	UART2 interrupt status register	0x00
UART2_BAUDDIV	R/W	0x0050	UART2 baud rate divide register	0x00000
UART2_CTRL2	R/W	0x0054	UART2 control register 2	0x0
UART3_DATA	R/W	0x0060	UART3 data register	0x00
UART3_STATE	R/C	0x0064	UART3 status register	0x00
UART3_CTRL	R/W	0x0068	UART3 control register	0x000
UART3_INTSTS	R/C	0x006C	UART3 interrupt status register	0x00
UART3_BAUDDIV	R/W	0x0070	UART3 baud rate divide register	0x00000
UART3_CTRL2	R/W	0x0074	UART3 control register 2	0x0
UART4_DATA	R/W	0x0080	UART4 data register	0x00
UART4_STATE	R/C	0x0084	UART4 status register	0x00
UART4_CTRL	R/W	0x0088	UART4 control register	0x000
UART4_INTSTS	R/C	0x008C	UART4 interrupt status register	0x00
UART4_BAUDDIV	R/W	0x0090	UART4 baud rate divide register	0x00000
UART4_CTRL2	R/W	0x0094	UART4 control register 2	0x0
UART5_DATA	R/W	0x00A0	UART5 data register	0x00
UART5_STATE	R/C	0x00A4	UART5 status register	0x00
UART5_CTRL	R/W	0x00A8	UART5 control register	0x000
UART5_INTSTS	R/C	0x00AC	UART5 interrupt status register	0x00
UART5_BAUDDIV	R/W	0x00B0	UART5 baud rate divide register	0x00000
UART5_CTRL2	R/W	0x00B4	UART5 control register 2	0x0

Table 17-2 Register Location of MISC Controller for UART(MISC Base: 0x40013000)

Name	Type	Address	Description	Default
MISC_IREN	R/W	0x000C	IR enable control register	0x00
MISC_DUTYL	R/W	0x0010	IR Duty low pulse control register	0x0000
MISC_DUTYH	R/W	0x0014	IR Duty high pulse control register	0x0000

17.5. Register Definition

17.5.1. UARTx_DATA Register

Table 17-3 Description of UARTx_DATA Register

Bit	Name	Type	Description	Default
31:8	-	-	Reserved.	0
7:0	DATA	R/W	Read: Receive data Write: Transmit data	0x0

17.5.2. UARTx_STATE Register

Table 17-4 Description of UARTx_STATE Register

Bit	Name	Type	Description	Default
31:7	-	-	Reserved.	0
6	RXPSTS	R	Receive parity data flag. This flag show the parity bit of last receive data.	0x0
5	TXDONE	R/C	Transmit done flag. This flag will be set when a single byte data is transmitted. The bit will be cleared when programmer write 1 to this bit or write 1 to TXDONEIF bit in UARTx_INTSTS register.	0x0
4	RXPE	R/C	Receive parity error flag. This flag will be set when receive data's parity does not meet expectation. The bit will be cleared when programmer write 1 to this bit or write 1 to RXPEIF bit in UARTx_INTSTS register.	0x0
3	RXOV	R/C	Receive buffer overrun flag. This flag will be set when RXFULL is 1 and another new data is received from RX engine. The bit will be cleared when programmer write 1 to this bit or write 1 to RXOVIF bit in UARTx_INTSTS register.	0x0
2	TXOV	R/C	Transmit buffer overrun flag. This flag will be set when TXFULL is 1 and another new data is written into UARTx_DATA register. The bit will be cleared when programmer write 1 to this bit or write 1 to TXOVIF bit in UARTx_INTSTS register.	0x0
1	RXFULL	R	Receive buffer full register.	0x0

			0: Receive buffer is empty. 1: Receive buffer is full. This flag will be set when a data is receive from the UART RX engine, and will be cleared to 0 when programmer read the data from UARTx_DATA register.	
0	-	-	Reserved.	0

17.5.3. UARTx_CTRL Register

Table 17-5 Description of UARTx_CTRL Register

Bit	Name	Type	Description	Default
31:9	-	-	Reserved.	0
8	TXDONEIE	R/W	Transmit done interrupt enable register.	0x0
7	RXPEIE	R/W	Receive parity error interrupt enable register.	0x0
6	-	-	Reserved.	0
5	RXOVIE	R/W	Receive overrun interrupt enable register.	0x0
4	TXOVIE	R/W	Transmit overrun interrupt enable register.	0x0
3	RXIE	R/W	Receive interrupt enable register.	0x0
2	-	-	Reserved.	0
1	RXEN	R/W	Receive engine enable register.	0x0
0	TXEN	R/W	Transmit engine enable register.	0x0

17.5.4. UARTx_INTSTS Register

Table 17-6 Description of UARTx_INTSTS Register

Bit	Name	Type	Description	Default
31:6	-	-	Reserved.	0
5	TXDONEIF	R/C	Transmit done flag. This flag will be set when a single byte is transmitted and TXDONEIE is 1. The bit will be cleared when programmer write 1 to this bit or write 1 to TXDONE bit in UARTx_STATE register.	0x0
4	RXPEIF	R/C	Receive parity error flag. This flag will be set when receive data's parity does not meet expectation and	0x0

			RXPEIEis1.The bit will be cleared when programmer write 1 to this bit or write 1 to RXPE bit in UARTx_STATE register.	
3	RXOVIF	R/C	Receive buffer overrun flag. This flag will be set when RXOVIE is 1 and RXFULL is 1 and another new data is received from RX engine. The bit will be cleared when programmer write 1 to this bit or write 1 to RXOV bit in UARTx_STATE register.	0x0
2	TXOVIF	R/C	Transmit buffer overrun flag. This flag will be set when TXOVIE is 1 and TXFULL is 1 and another new data is written into UARTx_DATA register. The bit will be cleared when programmer write 1 to this bit or write 1 to TXOV bit in UARTx_STATE register.	0x0
1	RXIF	R/C	Receive interrupt flag. This bit will be set when a data is received and put in UARTx_DATA register. This bit will be cleared when write 1 to this register.	0x0
0	-	-	Reserved.	0

17.5.5. UARTx_BAUDDIV Register

Table 17-7 Description of UARTx_BAUDDIV Register

Bit	Name	Type	Description	Default
31:20	-	-	Reserved.	0
19:0	BAUDDIV	R/W	Baud rate divider register, this register must be set before enable UART engine. BAUDDIV = APBCLK/Baud-rate. For example, when APBCLK = 6.5536MHz and baud-rate is 9600, fill 6553600/9600 = 682 in this register.	0x0

17.5.6. UARTx_CTRL2 Register

Table 17-8 Description of UARTx_CTRL2 Register

Bit	Name	Type	Description	Default
31:4	-	-	Reserved.	0
3:2	PMODE	R/W	Parity mode control register, this register is valid only when MODE is set to 1. 0: Even parity.	0x0

			1: Odd parity. 2: Always 0 at parity bit. 3: Always 1 at parity bit.	
1	MODE	R/W	UART mode control register. 0: 1+8+1 mode. 1: 1+8+1+1 mode, the parity bit is controlled by PMODE register.	0x0
0	MSB	R/W	LSB/MSB transmit order control register. 0: LSB transmit first. 1: MSB transmit first.	0x0

17.5.7. MISC_IREN Register

Table 17-9 Description of MISC_IREN Register

Bit	Name	Type	Description	Default
31:6	-	-	Reserved.	0
5:0	IREN	R/W	IR enable control register. Each bit in this register corresponded to 1 UART TX channel. When IREN[x] is set to 1, it means UART TX[x] will be modulated with IR pulse to output.	0x00

17.5.8. MISC_DUTYL Register

Table 17-10 Description of MISC_DUTYL Register

Bit	Name	Type	Description	Default
31:16	-	-	Reserved.	0
15:0	DUTYL	R/W	IR low pulse width control register. The low pulse width will be (DUTYL + 1)*APBCLK period.	0x0000

17.5.9. MISC_DUTYH Register

Table 17-11 Description of MISC_DUTYH Register

Bit	Name	Type	Description	Default

31:16	-	-	Reserved.	0
15:0	DUTYH	R/W	IR high pulse width control register. The high pulse width will be (DUTYH + 1)*APBCLK period.	0x0000

18. UART 32K Controller

18.1. Introduction

The UART 32K controller is used to receive data via UART protocol. There are two individual UART 32K controllers in V85X3, which can select input from UART rx0 ~ rx3. UART 32K controller is designed to operate at 32K crystal frequency, so it can work under sleep or deep sleep mode. The typical baud rate is 9600. The UART 32K controller can support 8 bits transfer without parity or 9 bits transfer with even or odd parity. One data buffer and one shift register is used for receive engine. The baud rate range of UART 32K is 300~14400bps.

18.2. Feature

--Operated under sleep or deep-sleep mode.

--Wake-up capability under sleep or deep-sleep mode.

--Programmable Baud rate generator

--8 bits or 9 bits with odd/even parity transfer.

--Parity error detection.

--Receive interrupt flag.

--Receive parity error flag.

--Receive overrun interrupt flag.

18.3. Block Diagram

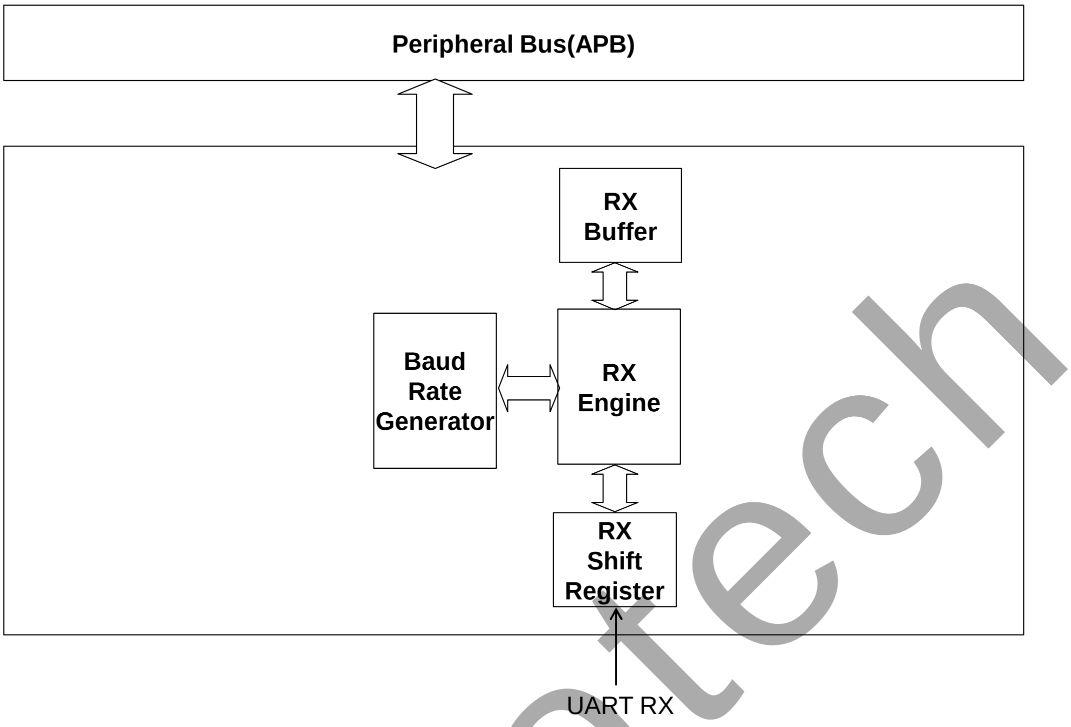


Figure 18-1 Functional Block Diagram of UART 32K Controller

18.4. Register Location

Table 18-1 Register Location of UART 32K Controller (UART 32K 0 Base: 0x40014100)

Name	Type	Address	Description	Default
U32K0_CTRL0	R/W	0x0000	UART 32K 0 control register 0	0x00
U32K0_CTRL1	R/W	0x0004	UART 32K 0 control register 1	0x00
U32K0_PHASE	R/W	0x0008	UART 32K 0 baud rate control register	0x4B00
U32K0_DATA	R	0x000C	UART 32K 0 receive data buffer	--
U32K0_STS	R/C	0x0010	UART 32K 0 interrupt status register	0x00
U32K1_CTRL0	R/W	0x0080	UART 32K 1 control register 0	0x00
U32K1_CTRL1	R/W	0x0084	UART 32K 1 control register 1	0x00
U32K1_PHASE	R/W	0x0088	UART 32K 1 baud rate control register	0x4B00
U32K1_DATA	R	0x008C	UART 32K 1 receive data buffer	--

U32K1_STS	R/C	0x0090	UART 32K 1 interrupt status register	0x00

18.5. Register Definition

18.5.1. U32Kx_CTRL0 Register

Table 18-2 Description of U32Kx_CTRL0 Register

Bit	Name	Type	Description	Default
31:9	-	-	Reserved.	0
8	WKUMODE	R/W	Wake-up mode control register. This register is valid when RXIE = 1. 0: Wake-up when a package is received no matter parity or stop bit is correct or not. 1: Wake-up only when parity bit and stop bit is correct.	0x0
7:6	DEBSEL	R/W	De-bounce control register 0: No de-bounce. 1: 2 RTCCLK clocks de-bounce. 2: 3 RTCCLK clocks de-bounce. 3: 4 RTCCLK clocks de-bounce. This register is used when the UART bus is dirty, enable the de-bounce function can reduce the noise on the receive data. But a too large de-bounce cycles may result in loss of receive data.	0x0
5:4	PMODE	R/W	Parity mode control register, this register is valid only when MODE is set to 1. 0: Even parity. 1: Odd parity. 2: Always 0 at parity bit. 3: Always 1 at parity bit.	0x0
3	MODE	R/W	UART mode control register. 0: 1+8+1 mode. 1: 1+8+1+1 mode, the parity bit is controlled by PMODE register.	0x0

2	MSB	R/W	UART receive order control register. 0: LSB receive first. 1: MSB receive first.	0x0
1	ACOFF	R/W	Auto-calibration off control register. In order to correct receive UART data under RTCCLK clock, there is a hardware auto calibration mechanism inside the controller. By default, this mode is turned on, programmer can set 1 to this bit to turn off this function. 0: Enable auto-calibration. 1: Disable auto-calibration.	0x0
0	EN	R/W	UART32K controller enable register. When this bit is set to 1, the UART32K controller will start to receive data after two 32768 Hz clock cycles. So use must set correct parameter and control register before set this register to 1. 0: Disable. 1: Enable.	0x0

18.5.2. U32Kx_CTRL1 Register

Table 18-3 Description of U32Kx_CTRL1 Register

Bit	Name	Type	Description	Default
31:6	-	-	Reserved.	0x0
5:4	RXSEL	R/W	Receive data select register. 0: From UART RX0 (IOA12). 1: From UART RX1 (IOA13). 2: From UART RX2 (IOA14). 3: From UART RX3 (IOA15).	0x0
3	-	-	Reserved.	
2	RXOVIE	R/W	Receive overrun interrupt/wake-up enable register.	0x0
1	RXPEIE	R/W	Receive parity error interrupt/wake-up enable register.	0x0
0	RXIE	R/W	Receive interrupt/wake-up enable register. When enabled, when WKUMODE is 0, it will wake up as long as it receives serial data; when WKUMODE is 1, it will wake up only when parity and stop bits are correct.	0x0

18.5.3. U32Kx_PHASE Register

Table 18-4 Description of U32Kx_PHASE Register

Bit	Name	Type	Description	Default
31:16	-	-	Reserved.	0
15:0	PHASE	R/W	Baud rate divider register, this register must be set before enable UART 32K engine. PHASE = 65536*Baud-rate/32768. For example, when baud-rate is 9600, fill 65536*9600/32768 = 19200 in this register. The maximum baud rate which UART 32K can support is 9600. When PSCA in RTC_PSCA register is not 0, the value in this register should be calculated by the divided RTCCLK frequency.	0x4B00

18.5.4. U32Kx_DATA Register

Table 18-5 Description of U32Kx_DATA Register

Bit	Name	Type	Description	Default
31:8	-	-	Reserved.	0
7:0	DATA	R	Read: Receive data.	--

18.5.5. U32Kx_STS Register

Table 18-6 Description of U32Kx_STS Register

Bit	Name	Type	Description	Default
31:3	-	-	Reserved.	0
2	RXOV	R/C	Receive buffer overrun flag. This flag will be set when receive FIFO is full and another new data is received from RX engine. The bit will be cleared when programmer write 1 to this bit.	0x0
1	RXPE	R/C	Receive parity error flag. This flag will be set when receive data’s parity does not meet expectation. The bit will be cleared when programmer write 1 to this bit.	0x0

0	RXIF	R/C	Receive interrupt flag, this bit will be set when a data is received and put in U32K_DATA register. This bit will be cleared when write 1 to this register.	0x0

19. ISO7816 Controller

19.1. Introduction

The ISO7816 controller is an enhanced UART protocol which is able to do half-duplex communication on the 2 wires bus. There are total 2 ISO7816 controller in V85X3, each ISO7816 controller can be program individually and has its own interrupt to CPU. A clock divider is also included inside the IP which is capable to generate a 1~5MHz clock for ISO7816 device. The setting in ISO7816 controller will be reset after wake-up from sleep or deep-sleep mode, programmer should restore the setting manually after wake-up from these two states.

19.2. Feature

--Programmable Baud rate generator

--Support automatically retry.

--Support half-duplex transmit/receive.

--Support clock divider.

19.3. Block Diagram

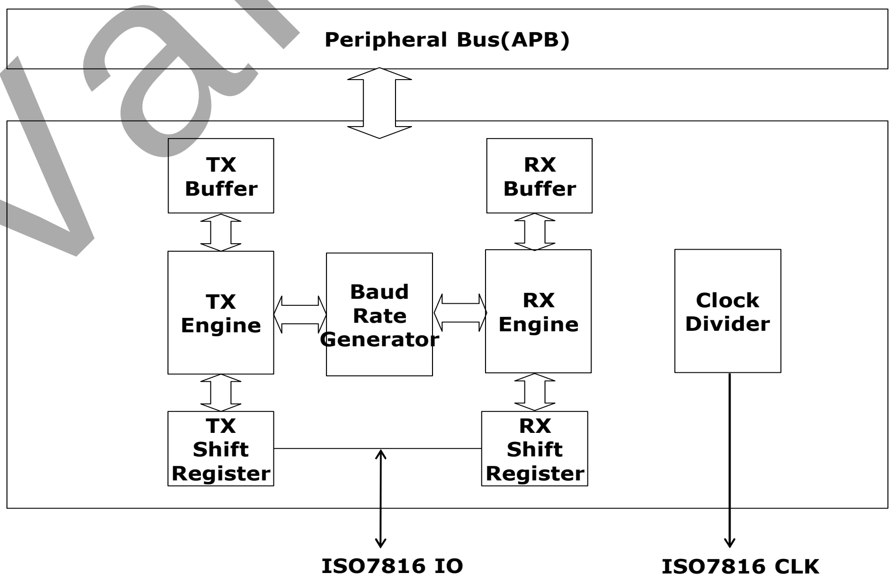


Figure 19-1 Functional Block Diagram of ISO7816 Controller

19.4. Register Location

Table 19-1 Register Location of ISO7816 Controller (ISO7816 Base: 0x40012000)

Name	Type	Address	Description	Default
ISO78160_BAUDDIVL	R/W	0x0004	ISO78160 baud-rate low byte register	0x00
ISO78160_BAUDDIVH	R/W	0x0008	ISO78160 baud-rate high byte register	0x00
ISO78160_DATA	R/W	0x000C	ISO78160 data register	0x00
ISO78160_INFO	R/C	0x0010	ISO78160 information register	0x00
ISO78160_CFG	R/W	0x0014	ISO78160 control register	0x00
ISO78160_CLK	R/W	0x0018	ISO78160 clock divider control register	0x00
ISO78161_BAUDDIVL	R/W	0x0044	ISO78161 baud-rate low byte register	0x00
ISO78161_BAUDDIVH	R/W	0x0048	ISO78161 baud-rate high byte register	0x00
ISO78161_DATA	R/W	0x004C	ISO78161 data register	0x00
ISO78161_INFO	R/C	0x0050	ISO78161 information register	0x00
ISO78161_CFG	R/W	0x0054	ISO78161 control register	0x00
ISO78161_CLK	R/W	0x0058	ISO78161 clock divider control register	0x00

19.5. Register Definition

19.5.1. ISO7816x_BAUDDIVL Register

Table 19-2 Description of ISO7816x_BAUDDIVL Register

Bit	Name	Type	Description	Default
31:8	-	-	Reserved.	0
7:0	BAUDDIVL	R/W	Low byte of baud-rate divider.	0x0

19.5.2. ISO7816x_BAUDDIVH Register

Table 19-3 Description of ISO7816x_BAUDDIVH Register

Bit	Name	Type	Description	Default
31:8	-	-	Reserved.	0

7:0	BAUDDIVH	R/W	High byte of baud-rate divider. The baud-rate counter is count from BAUDDIV to 0xFFFF, so the setting should be. BAUDDIV = 0x10000 – (APBCLK/Baud-rate). For example, when APBCLK is 6.5536MHz and baud-rate is 9600, then 0x10000-(6553600/9600) = 0xFD56 should be written into this register.	0x0

19.5.3. ISO7816x_DATA Register

Table 19-4 Description of ISO7816x_DATA Register

Bit	Name	Type	Description	Default
31:8	-	-	Reserved.	0
7:0	DATA	R/W	Read: Receive data, when receive data is not read by programmer and another data has been received, the OVIF flag will be set. Write: Transmit data, a write to this port will trigger a transmit event on the ISO7816 bus.	0x0

19.5.4. ISO7816x_INFO Register

Table 19-5 Description of ISO7816x_INFO Register

Bit	Name	Type	Description	Default
31:8	-	-	Reserved.	0
7	OVIF	R/C	Receive overflow flag. This bit will be set when a data is received by not been read by CPU but another receive data is coming in. This bit can be cleared by write 1 to this flag.	0x0
6	SDIF	R/C	Transmit interrupt flag. This bit will set when a byte has been transmitted and ACK has been received. This bit will be set no matter the received ACK is 0 or 1. This bit can be cleared by write 1 to this flag.	0x0
5	RCIF	R/C	Receive interrupt flag. This bit will set when a byte has been received and ACK has been transmitted. This bit can be cleared by write 1 to this flag.	0x0
4	LSB	R/W	MSB/LSB transmit/receive order control register.	0x0

			0: Transmit MSB first. 1: Transmit LSB first.	
3	SDERR	R/C	When the received ACK is 0 during transmit mode, this bit will be set to 1. This bit can be clear by write 1 to this bit.	0x0
2	RCERR	R/C	When received data have check sum error, this bit will be set to 1. This bit can be clear by write 1 to this bit.	0x0
1	CHKSUM	R/W	The transmitted or received data's check sum bit. This bit can be read/write by CPU, by the original message will be lost.	0x0
0	RCACK	R/W	The received ACK at the end of transmit. This bit can be read/write by CPU, by the original message will be lost.	0x0

19.5.5. ISO7816x_CFG Register

Table 19-6 Description of ISO7816x_CFG Register

Bit	Name	Type	Description	Default
31:8			Reserved.	0
7	OVIE	R/W	Receive overrun interrupt enable register.	0x0
6	SDIE	R/W	Transmit interrupt enable register.	0x0
5	RCIE	R/W	Receive interrupt enable register.	0x0
4	ACKLEN	R/W	ACK low period when receive an error data. 0: 1 bit 1: 2 bits.	0x0
3	AUTOSD	R/W	Automatic re-transmit when receive ACK is 0. 0: Disable automatic re-transmit mode. 1: Enable automatic re-transmit mode.	0x0
2	AUTORC	R/W	Automatic response ACK as 0 when receive an error data to let transmitter re-send the data. 0: Disable automatic re-receive mode. 1: Enable automatic re-receive mode.	0x0
1	CHKP	R/W	Parity mode control register. 0: Even parity	0x0

			1: Odd parity.	
0	EN	R/W	ISO7816 enable register. 0: Disable ISO7816 function. 1: Enable ISO7816 function.	0x0

19.5.6. ISO7816x_CLK Register

Table 19-7 Description of ISO7816x_CLK Register

Bit	Name	Type	Description	Default
31:8	-	-	Reserved.	0
7	CLKEN	R/W	ISO7816 clock output enable. 0: Disable clock output. 1: Enable clock output.	0x0
6:0	CLKDIV	R/W	The ISO7816 clock divider ratio. 0: APBCLK/1 1: APBCLK /2 2: APBCLK /3 ... 127: APBCLK /128	0x0

In ISO7816’s protocol, the re-transmit should be less or equal to 3 times, this part should be take care by software to disable the auto transmit or receive function after two times of failure retry.

The following table shows the ISO7816’s package format.

Table 19-8 Package format of ISO7816

bit	0	1~8	9	10	11	12	0	...
Transmit Direction	Transmitter→Receiver			Receiver→Transmitter		--	Transmitter→Receiver	
Definition	Start bit	Data	Parity bit	ACK*		Wait	Start bit	...
Value	0	MSB→LSB	P	ACK*		1	0	...
TX	0	MSB→LSB	P	1			0	...

RX	1	1	1	ACK*	1	1	...
Description	10 bits data			3 bits guarding time		Next Frame	

*If ACK is 0, then the RX will be reset from 1 to 0 at the middle of 10th bit, and set to 1 at 11th or 12th bit, which is controlled by ACKLEN in ISO7816x_CFG.

The transmit package contains totally 10 bits including a start bit and 8 bits data and 1 parity bit. And then in a 3 bits guarding time, the receiver will check the parity correctness response 1 or 2 bits ACK to transmitter. At bit 12, both transmitter and receiver should be kept at high state before next package is ready to be transmitted.

20. Timer/PWM Controller

20.1. Introduction

There are in total 8 timers in V85X3. Four of them are general purpose 32 bits timer. Another 4 timers are 16 bits timers with PWM function. Each timer can generate interrupt to CM0. Each PWM can output 3 outputs with different output waveform. The setting in timer/PWM controller will be reset after wake-up from sleep or deep-sleep mode, programmer should restore the setting manually after wake-up from these two states.

20.2. Feature

--4 32 bits general purpose count timer

--4 16 bits PWM timer.

--Each PWM timer can have at most 3 outputs.

--8 output modes.

20.3. Block Diagram

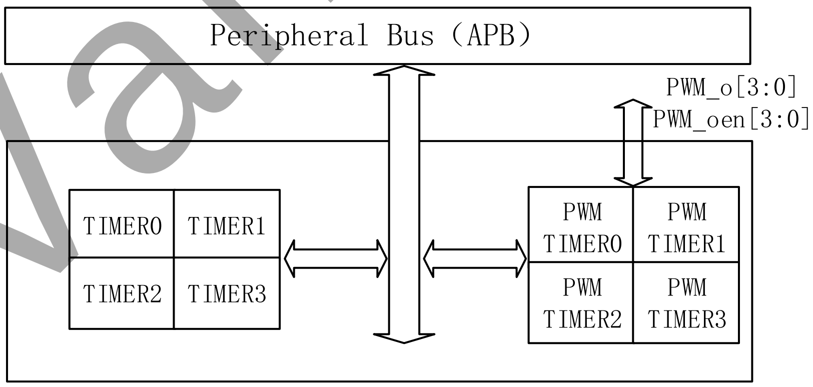


Figure 20-1 Functional Block Diagram of TIMER Controller

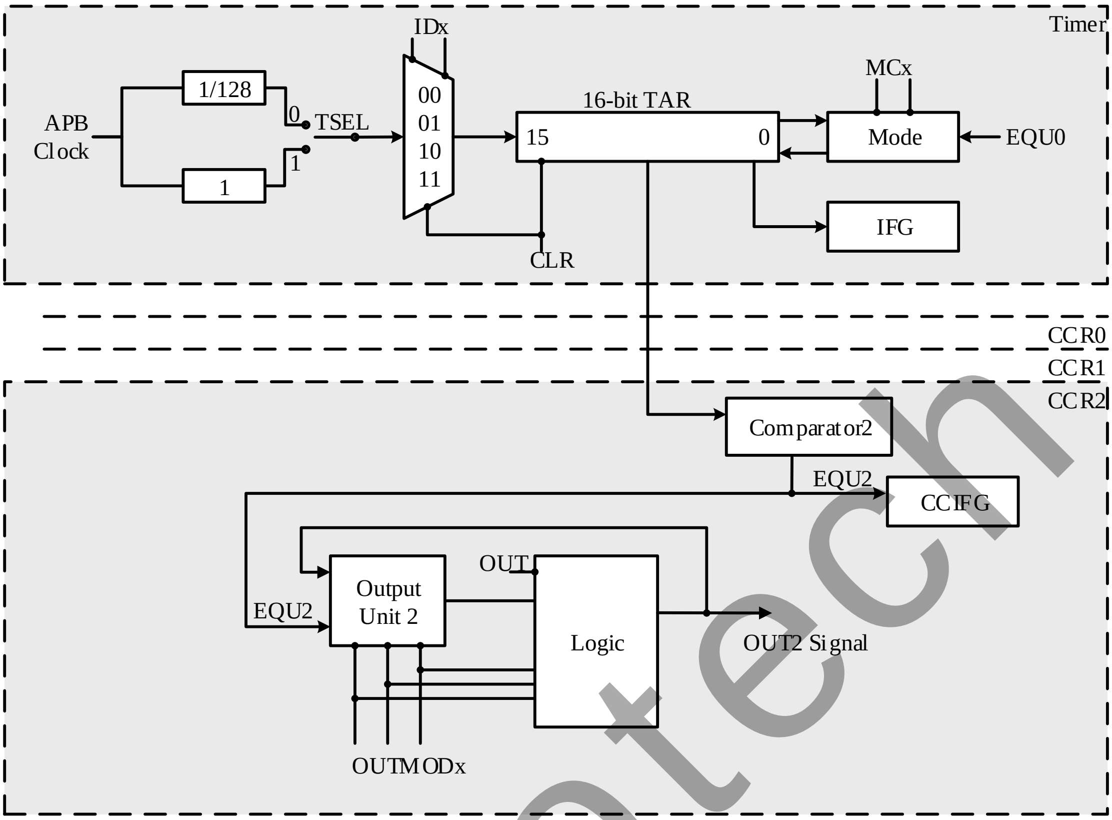


Figure 20-2 Functional Block Diagram of PWM TIMER Controller

20.4. Register Location

Table 20-1 Register Location of 32b TIMER Controller (32b TIMER Base: 0x40012800)

Name	Type	Address	Description	Default
TMR0_CTRL	R/W	0x0000	Timer 0's control register	0x0
TMR0_VALUE	R/W	0x0004	Timer 0's current count register	0x00000000
TMR0_RELOAD	R/W	0x0008	Timer 0's reload register	0x00000000
TMR0_INT	R/C	0x000C	Timer 0's interrupt status register	0x0
TMR1_CTRL	R/W	0x0020	Timer 1's control register	0x0
TMR1_VALUE	R/W	0x0024	Timer 1's current count register	0x00000000
TMR1_RELOAD	R/W	0x0028	Timer 1's reload register	0x00000000
TMR1_INT	R/C	0x002C	Timer 1's interrupt status register	0x0
TMR2_CTRL	R/W	0x0040	Timer 2's control register	0x0
TMR2_VALUE	R/W	0x0044	Timer 2's current count register	0x00000000

TMR2_RELOAD	R/W	0x0048	Timer 2's reload register	0x00000000
TMR2_INT	R/C	0x004C	Timer 2's interrupt status register	0x0
TMR3_CTRL	R/W	0x0060	Timer 3's control register	0x0
TMR3_VALUE	R/W	0x0064	Timer 3's current count register	0x00000000
TMR3_RELOAD	R/W	0x0068	Timer 3's reload register	0x00000000
TMR3_INT	R/C	0x006C	Timer 3's interrupt status register	0x0

Table 20-2 Register Location of 16b PWM TIMER Controller (16b PWM TIMER Base: 0x40012900)

Name	Type	Address	Description	Default
PWM0_CTL	R/W	0x0000	PWM Timer 0's control register	0x00
PWM0_TAR	R	0x0004	PWM Timer 0's current count register	0x0000
PWM0_CCTL0	R/W	0x0008	PWM Timer 0's compare control register 0	0x000
PWM0_CCTL1	R/W	0x000C	PWM Timer 0's compare control register 1	0x000
PWM0_CCTL2	R/W	0x0010	PWM Timer 0's compare control register 2	0x000
PWM0_CCR0	R/W	0x0014	PWM Timer 0's compare data register 0	0x0000
PWM0_CCR1	R/W	0x0018	PWM Timer 0's compare data register 1	0x0000
PWM0_CCR2	R/W	0x001C	PWM Timer 0's compare data register 2	0x0000
PWM1_CTL	R/W	0x0020	PWM Timer 1's control register	0x00
PWM1_TAR	R	0x0024	PWM Timer 1's current count register	0x0000
PWM1_CCTL0	R/W	0x0028	PWM Timer 1's compare control register 0	0x000
PWM1_CCTL1	R/W	0x002C	PWM Timer 1's compare control register 1	0x000
PWM1_CCTL2	R/W	0x0030	PWM Timer 1's compare control register 2	0x000
PWM1_CCR0	R/W	0x0034	PWM Timer 1's compare data register 0	0x0000
PWM1_CCR1	R/W	0x0038	PWM Timer 1's compare data register 1	0x0000
PWM1_CCR2	R/W	0x003C	PWM Timer 1's compare data register 2	0x0000
PWM2_CTL	R/W	0x0040	PWM Timer 2's control register	0x00
PWM2_TAR	R	0x0044	PWM Timer 2's current count register	0x0000
PWM2_CCTL0	R/W	0x0048	PWM Timer 2's compare control register 0	0x000
PWM2_CCTL1	R/W	0x004C	PWM Timer 2's compare control register 1	0x000
PWM2_CCTL2	R/W	0x0050	PWM Timer 2's compare control register 2	0x000

PWM2_CCR0	R/W	0x0054	PWM Timer 2's compare data register 0	0x0000
PWM2_CCR1	R/W	0x0058	PWM Timer 2's compare data register 1	0x0000
PWM2_CCR2	R/W	0x005C	PWM Timer 2's compare data register 2	0x0000
PWM3_CTL	R/W	0x0060	PWM Timer 3's control register	0x00
PWM3_TAR	R	0x0064	PWM Timer 3's current count register	0x0000
PWM3_CCTL0	R/W	0x0068	PWM Timer 3's compare control register 0.	0x000
PWM3_CCTL1	R/W	0x006C	PWM Timer 3's compare control register 1	0x000
PWM3_CCTL2	R/W	0x0070	PWM Timer 3's compare control register 2	0x000
PWM3_CCR0	R/W	0x0074	PWM Timer 3's compare data register 0	0x0000
PWM3_CCR1	R/W	0x0078	PWM Timer 3's compare data register 1	0x0000
PWM3_CCR2	R/W	0x007C	PWM Timer 3's compare data register 2	0x0000
PWM_O_SEL	R/W	0x00F0	PWM output selection register	0xDB51

20.5. Register Definition

20.5.1. TMRx_CTRL Register

Table 20-3 Description of TMRx_CTRL Register

Bit	Name	Type	Description	Default
31:4	-	-	Reserved.	0
3	INTEN	R/W	Timer x interrupt enable register.	0x0
2	EXTCLK	R/W	Select ext_clk (IOB15) as clock source. The ext_clk's rising edge will be used as internal down counter's enable signal. Every time when the ext_clk is rising, the internal counter will decrease by 1. Under this mode, the frequency of ext_clk should be lower than PLCK/6.	0x0
1	EXTEN	R/W	When the ext_clk (IOB15) is logic 1, the internal down counter will be decreased by 1 with the speed of PCLK. A two clocks sync logic will be applied on the ext_clk to avoid the glitch on the ext_clk. When both the EXTCLK and EXTEN bits are enabled, the EXTCLK bit has higher priority.	0x0
0	EN	R/W	Timer x enable control register.	0x0

20.5.2. TMRx_VALUE Register

Table 20-4 Description of TMRx_VALUE Register

Bit	Name	Type	Description	Default
31:0	VALUE	R/W	Timer x current value register.	0x00000000

20.5.3. TMRx_RELOAD Register

Table 20-5 Description of TMRx_RELOAD Register

Bit	Name	Type	Description	Default
31:0	RELOAD	R/W	Timer x reload value register. A write to this register sets the current value. Every time when the timer down count to 0, the value in this register will be reloaded into the counter and start to down count again. At the same time, the INT bit will be set to 1. The RELOAD of the timer can be calculated by the following equation. RELOAD = Period * APBCLK - 1.	0x00000000

20.5.4. TMRx_INT Register

Table 20-6 Description of TMRx_INT Register

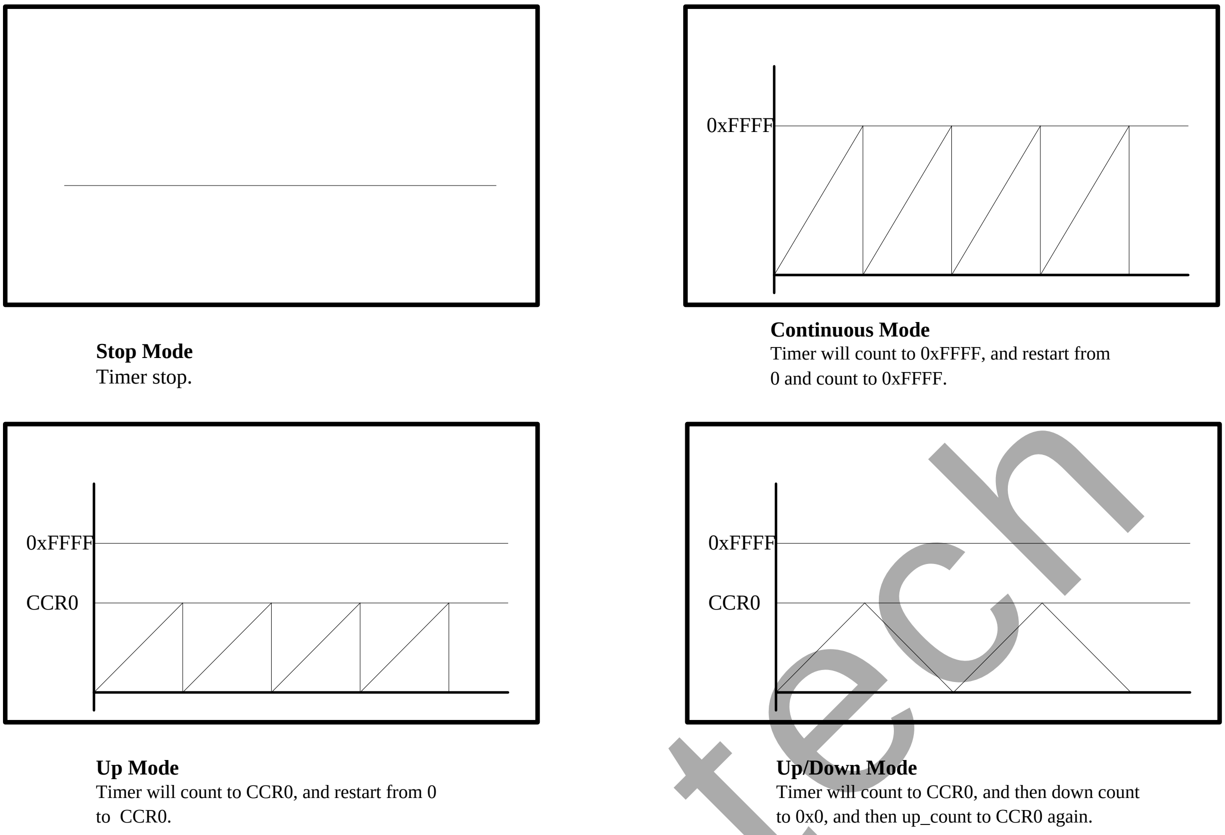
Bit	Name	Type	Description	Default
31:1	-	-	Reserved.	0
0	INT	R/C	Timer x interrupt status register, write 1 to clear this bit. When the internal down counter timer reach 0, this bit will be set to 1.	0x0

20.5.5. PWMx_CTL Register

Table 20-7 Description of PWMx_CTL Register

Bit	Name	Type	Description	Default
31:8	-	-	Reserved.	0
7:6	ID	R/W	PWM timer x's Input clock divider control.	0x0

			0: Input clock divide by 2 1: Input clock divide by 4 2: Input clock divide by 8 3: Input clock divide by 16	
5:4	MC	R/W	PWM Timer mode control 0: Timer stop. 1: Up-count mode: timer will count to CCR0 and restart from 0. 2: Continuous mode: timer will count to 0xFFFF and start from 0. 3: Up/Down mode: timer will count to CCR0 and then decrease to 0. Refer to figure 2 for each mode.	0x0
3	TSEL	R/W	Clock source selection 0: APB Clock/128. 1: APB Clock.	0x0
2	CLR	R/W	TAR clear register, when this bit is set to 1, the TAR will be clear to 0. This bit will be cleared to 0 automatically after TAR is cleared.	0x0
1	IE	R/W	PWM Timer x’s interrupt enable register.	0x0
0	IFG	R/C	PWM Timer x’s interrupt status flag, write 1 to clear this flag to 0. Up mode: Set when counter change from CCR0 to 0. Continuous mode: Set when counter change from 0xFFFF to 0. Up-Down mode: Set when counter change from 0x0001 to 0.	0x0



Stop Mode
Timer stop.

Continuous Mode
Timer will count to 0xFFFF, and restart from 0 and count to 0xFFFF.

Up Mode
Timer will count to CCR0, and restart from 0 to CCR0.

Up/Down Mode
Timer will count to CCR0, and then down count to 0x0, and then up_count to CCR0 again.

Figure 20-3 Mode description of PWM TIMER Controller

When MC is set to a non-zero value, the timer will start to work. Under up mode or up/down mode, if PWMx_CCR0 is set to 0, then timer x will stop counting. The timer will start to count again if a non-zero value is written to PWMx_CCR0.

Under up-mode, if the CCR0 is changed during the operation time and new CCR value is larger than current count value, then the timer will count to the new CCR0 then return to 0. And if the new CCR0 is smaller than current count value, the timer will count one tick and reset to 0 to start again.

Under up-down mode and the timer is under up-count process, if the CCR0 is changed during the operation time and new CCR value is larger than current count value, then the timer will count to the new CCR0 then down count to 0. And if the new CCR0 is smaller than current count value, the timer will count one tick and start to down count to 0. Under up-down mode and the timer is under down-count process, if the CCR0 is changed during the operation time, then the timer will continuously complete the down count process.

Under continuous mode, user can set the output frequency depends on the dynamic setting of CCR0~CCR2. The following diagram shows an example of this application.

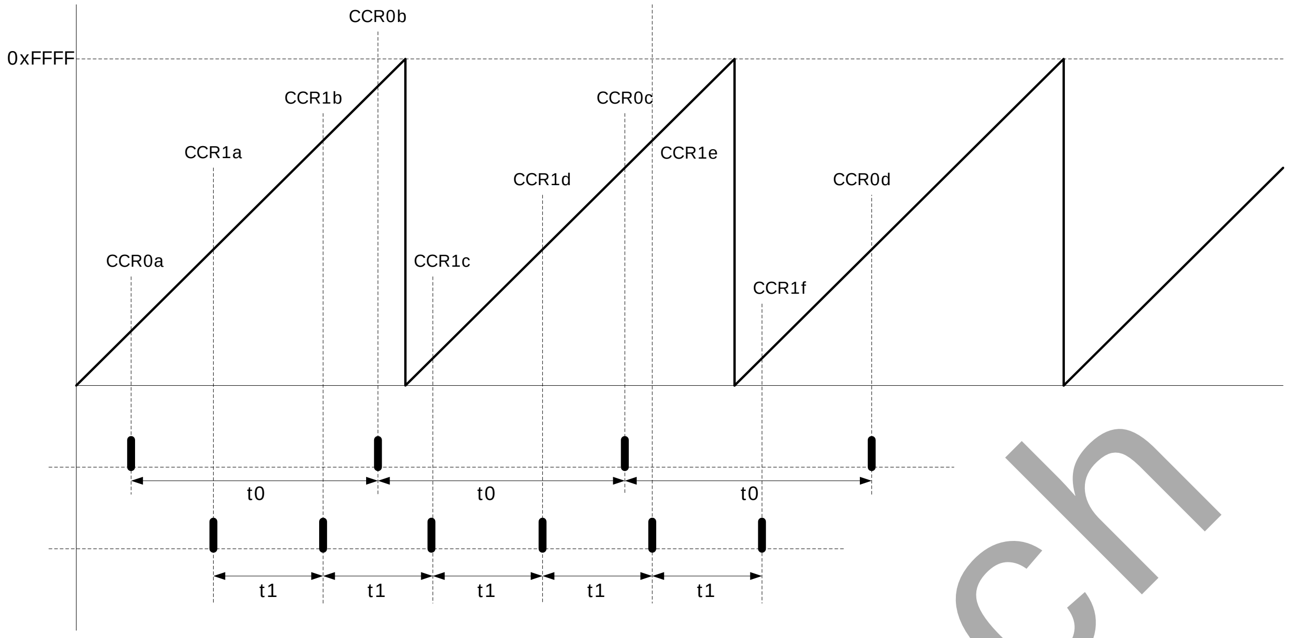


Figure 20-4 Example of Continuous Mode

In the above diagram, CCR0a or CCR1a is the CCR0 or CCR1 at Ta0 or Ta1, CCR0b or CCR1b is the CCR0 or CCR1 at Tb0 or Tb1. (Tb0=Ta0+t0, Tb1=Ta1+t1)

The above diagram shows that under continuous mode, user can use CCIFG (bit 0 of CCTLx) and CCIE (bit 4 of CCTLx) to generate a regulator interrupt by setting CCR0a and CCR1a to assert interrupt when TAR=CCR0a or TAR=CCR1a. And when TAR=CCR0b or TAR=CCR1b, it can generate another interrupt with different period. The t0 and t1 can be totally independent, so at most user can set 3 totally independent interrupt with one single PWM timer. Under this mode, the IFG flag will be set when the timer count from 0xFFFF to 0x0.

20.5.6. PWMx_CCTLx Register

Table 20-8 Description of PWMx_CCTLx Register

Bit	Name	Type	Description	Default
31:10	-	-	Reserved.	0
9	OUTEN	R/W	OUTx output enable control register. 0: OUTx output disable 1: OUTx output enable	0x0
8	-	-	Reserved.	0x0
7:5	OUTMOD	R/W	Output mode selection. 0: Constant mode, OUTx output the value of OUT bit. 1: Set mode, OUTx will be set to 1 when TAR=CCRx (x=0~2).	0x0

			2: Toggle/Reset mode, OUTx will be toggled when TAR=CCRx (x=1~2), and will be reset to 0 when TAR=CCR0. This mode can't be used on OUT0. 3: Set/Reset mode, OUTx will be set to 1 when TAR=CCRx (x=1~2), and will be reset to 0 when TAR=CCR0. This mode can't be used on OUT0. 4: Toggle mode, OUTx will be toggled when TAR=CCRx (x=0~2). 5: Reset mode, OUTx will be reset to 0 when TAR=CCRx (x=0~2). 6: Toggle/set mode, OUTx will be toggled when TAR=CCRx (x=1~2), and will be set to 1 when TAR=CCR0. This mode can't be used on OUT0. 7: Reset/set mode, OUTx will be reset to 0 when TAR=CCRx (x=1~2), and will be set to 1 when TAR=CCR0. This mode can't be used on OUT0.	
4	CCIE	R/W	Compare interrupt enable register.	0x0
3	-	-	Reserved.	
2	OUT	R/W	This bit is used to control the output value of OUTx when OUTMOD is set to 0.	0x0
1	-	-	Reserved.	0
0	CCIFG	R/C	Under compare mode, this bit will be set when TAR=CCRx. This bit can be cleared only when write 1 to this bit.	0x0

The following figure shows the PWM output under up-mode.

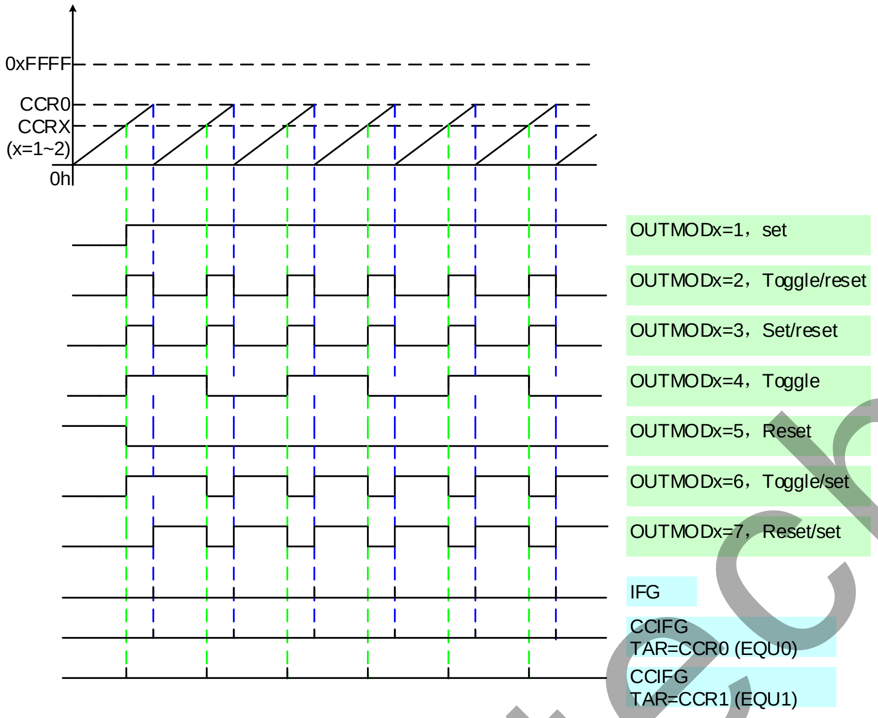


Figure 20-5 PWM Output under Up-count Mode

The following figure shows the PWM output under continuous-mode.

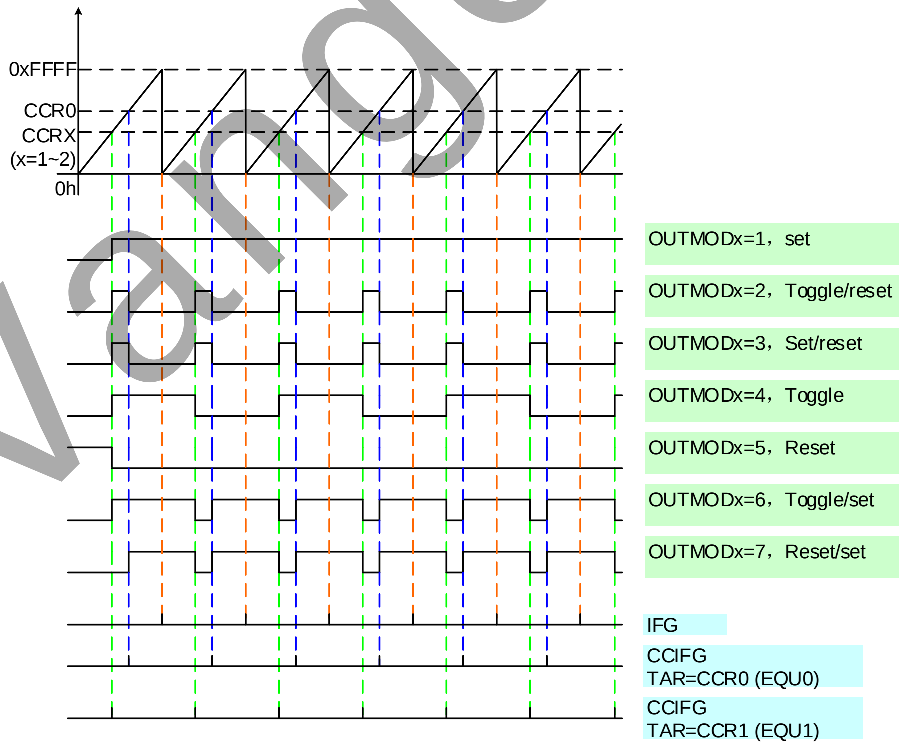


Figure 20-6 PWM Output under Continuous Mode

The following figure shows the PWM output under up/down count mode.

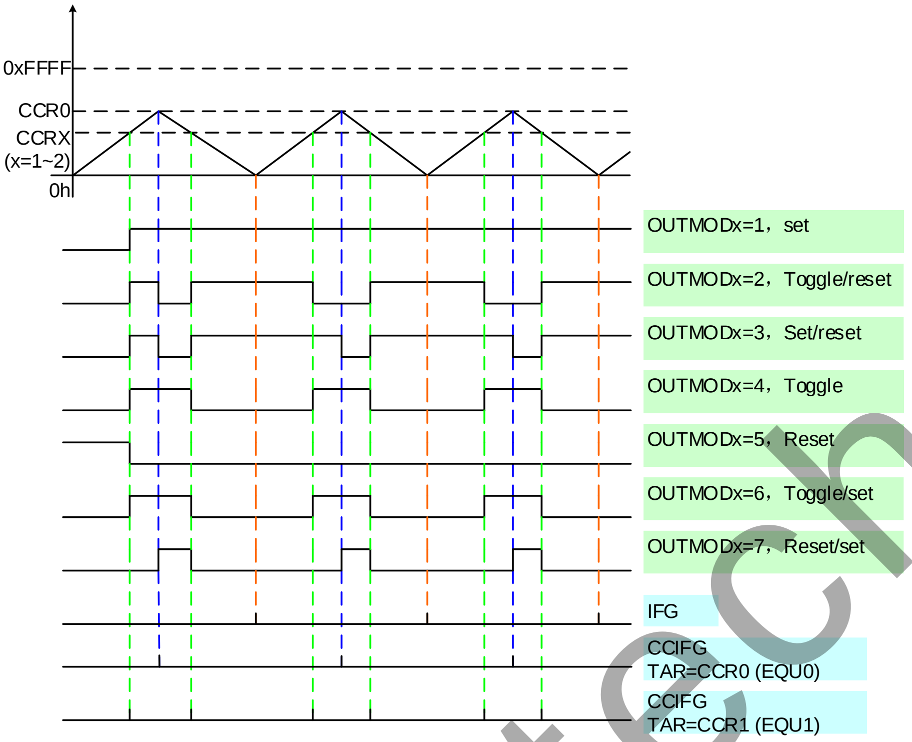


Figure 20-7 PWM Output under Up/down Count Mode

20.5.7. PWMx_CCRx Register

Table 20-9 Description of PWMx_CCRx Register

Bit	Name	Type	Description	Default
31:16	-	-	Reserved.	0
15:0	CCRx	R/W	Compare data register. This register is used to compare with TAR to generate PWM output.	0x0

20.5.8. PWM_O_SEL Register

Table 20-10 Description of PWM_O_SEL Register

Bit	Name	Type	Description	Default
31:16	-	-	Reserved.	0
15:12	O_SEL3	R/W	External output PWM3's output selection register. Same definition as O_SEL0	0xD
11:8	O_SEL2	R/W	External output PWM2's output selection register. Same definition as O_SEL0	0xB

7:4	O_SEL1	R/W	External output PWM1's output selection register. Same definition as O_SEL0	0x5
3:0	O_SEL0	R/W	External output PWM0's output selection register. 0: From PWM0's OUT0 1: From PWM0's OUT1 2: From PWM0's OUT2 4: From PWM1's OUT0 5: From PWM1's OUT1 6: From PWM1's OUT2 8: From PWM2's OUT0 9: From PWM2's OUT1 10: From PWM2's OUT2 12: From PWM3's OUT0 13: From PWM3's OUT1 14: From PWM3's OUT2 Others: Reserved.	0x1

21. LCD Controller

21.1. Introduction

The LCD controller is used to display content on the LCD panel. The LCD controller supports 4 COMs or 6COMs and 8 COMs mode, and maximum 78 segments. There are two frame buffers inside the LCD controller, which support automatically switch function. The setting in GPIO controller will be reset after wake-up from deep-sleep mode, programmer should restore the setting manually after wake-up from deep-sleep mode.

21.2. Feature

--Support 4, 6 or 8 COMs mode.

--Support maximum 4 COMs×78 SEGs, 6 COMs×76 SEGs or 8 COMs×74 SEGs.

--Support 1/3 Bias or 1/4 Bias modes

--Bias voltage generated by an individual 3.3V LDO, and can be adjusted from 3.6V-2.7V with resolution of 60mV/LSB

--An internal resistor ladder to generate the LCD waveform voltages--LCD scan frequency generated by the RTCCLK clock

--Two frame buffers which support automatically switch function.

--Adjustable frame rate.

21.3. Block Diagram

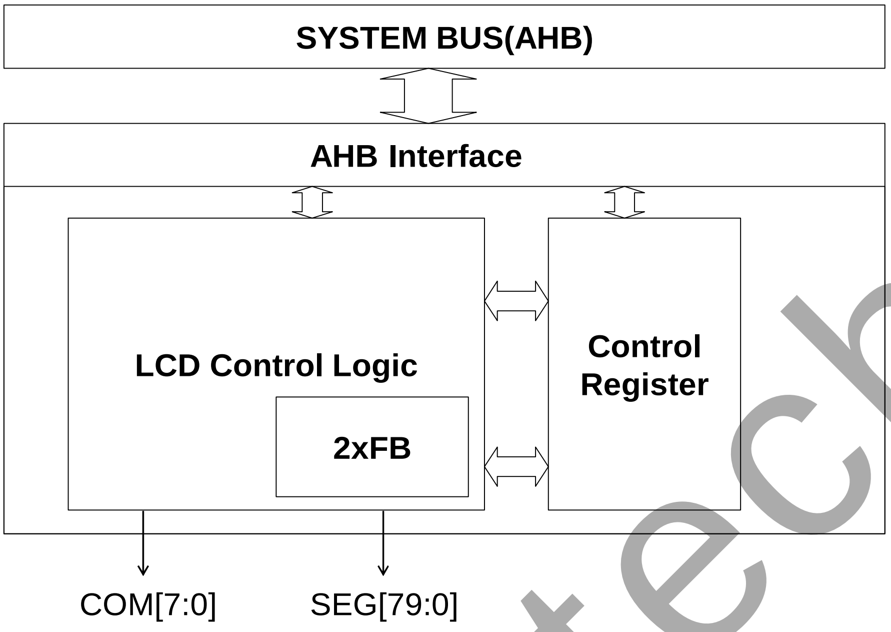


Figure 21-1 Functional Block Diagram of LCD Controller

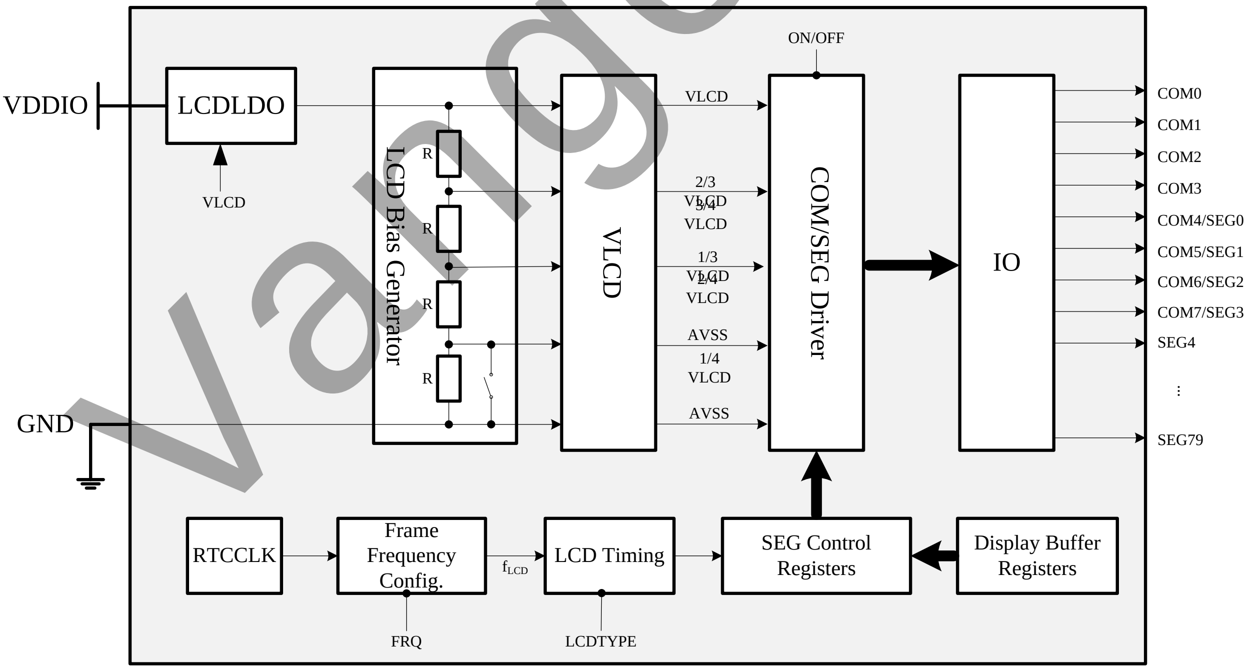


Figure 21-2 LCD Controller Structure Diagram

21.4. LCD Timing

In the V85X3, the CLK, sourced by the 32.768 KHz RTCCLK clock, provides the LCD driver with clock pulse for timing generation. Generally, the crystal oscillator keeps on running until it is powered off, so the LCD driver keeps on working even in Sleep (not Deep Sleep) state unless CLK is disabled. When the crystal stops running anomaly when power is still on, the internal RC clock will become the replacement of the XTAL clock to source the LCD driver until the crystal is stimulated to run again.

The CLK frequency is divided to generate frame frequency for the waveform. The MCU can configure bit[1:0] of LCD_CTRL to select the appropriate frame frequency. By default it is 64Hz.

21.5. LCD Waveform Voltage

In the V85X3, the bias voltage of LCD driver is generated by an individual 3.3V LDO, and an internal resistor ladder is designed to generate LCD waveform voltage (VLCD). Users can adjust the waveform voltage via bits VLCD[3:0](bit[4:1] of ANA_REG6).

21.6. LCD Operating Current

Users can adjust the resistance value of each resistor in the resistor ladder of the bias voltage generation circuits via bits DRV[1:0] (bit[3:2] of LCD_CTRL) to adjust the current through the circuits to change the lightness of the display panel. By default, the resistance value is 300 kΩ.

21.7. LCD Drive Waveform

There are 4 resistors in series in the bias voltage generation circuit, which can be configured to work in 1/3 bias mode or 1/4 bias mode. Users can configure bit LCD_BMOD (bit0 of ANA_REG6) to disable or enable one resistor in the bias voltage generation circuit to enable the LCD driver to work in 1/3 bias mode or 1/4 bias mode.

When an LCD panel of 1/4 duty 1/3 bias is applied, the LCD drive waveform is depicted in the following figure.

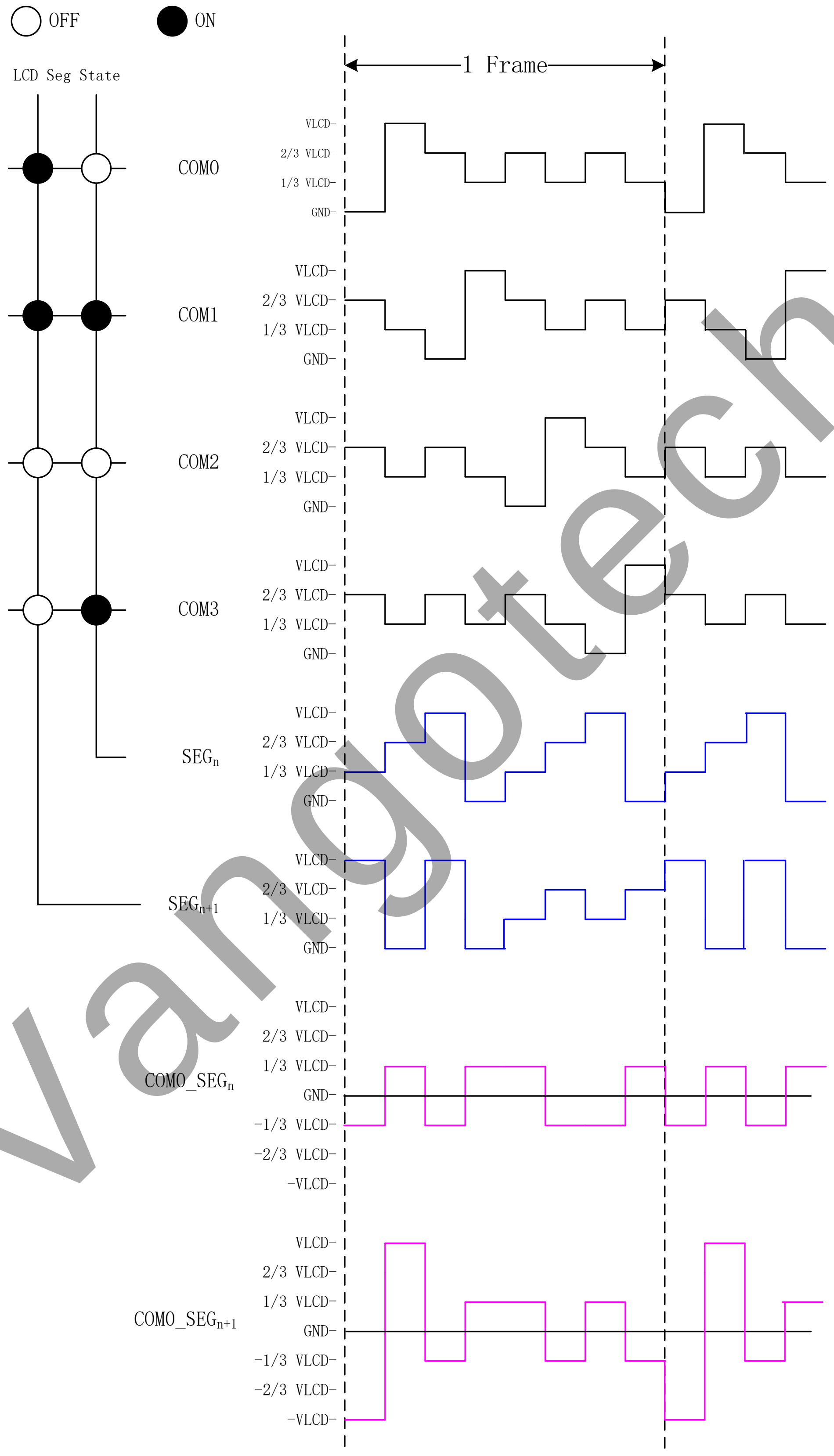


Figure 21-3 LCD Drive Waveform of 1/4 Duty and 1/3 Bias

When LCD panel of 1/6 duty and 1/3 bias is applied, the LCD drive waveform is depicted in the following figure.

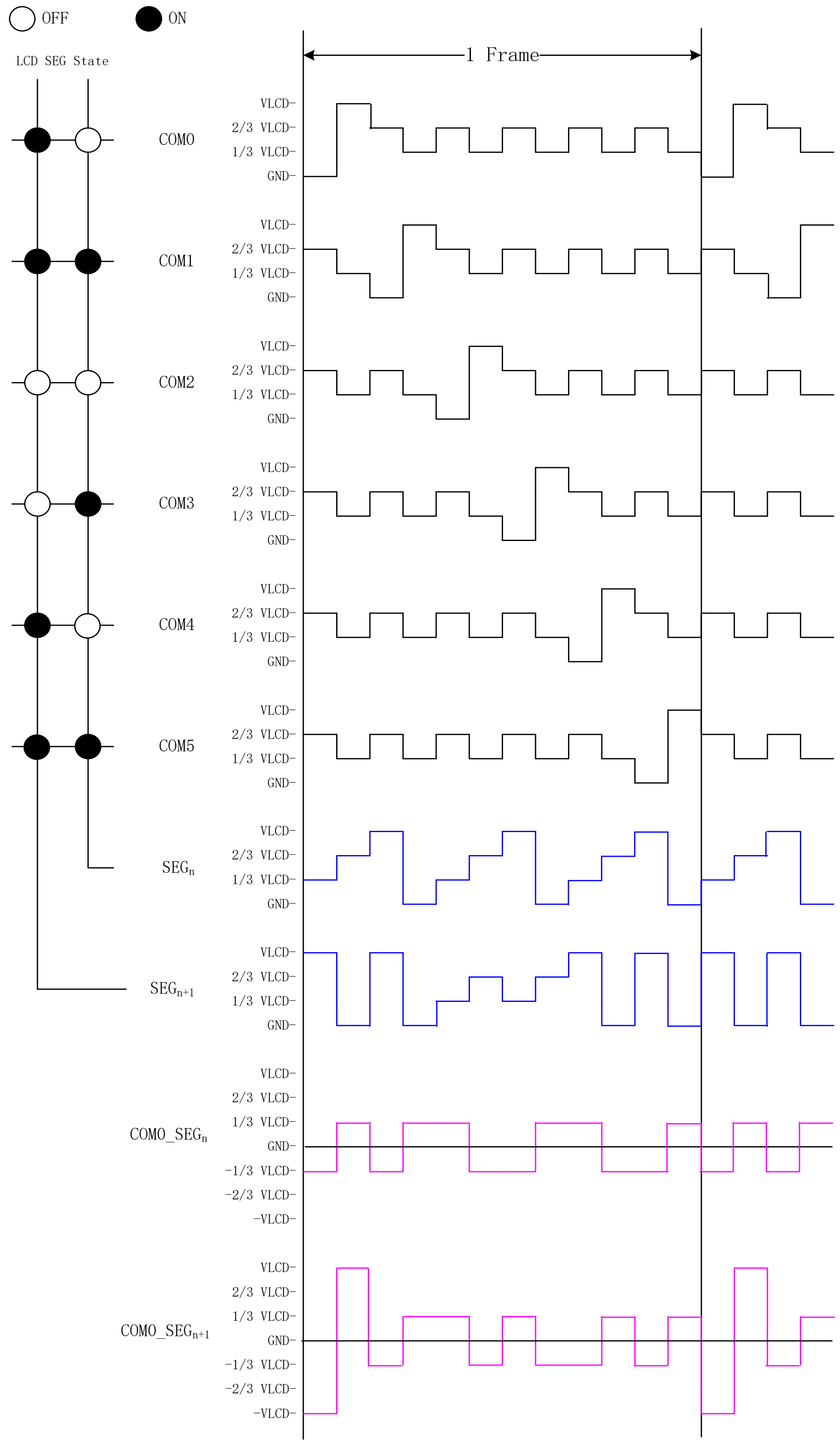


Figure 21-4 LCD Drive Waveform of 1/6 Duty and 1/3 Bias

When an LCD panel of 1/8 duty and 1/3 bias is applied, the LCD drive waveform is depicted in the following figures.

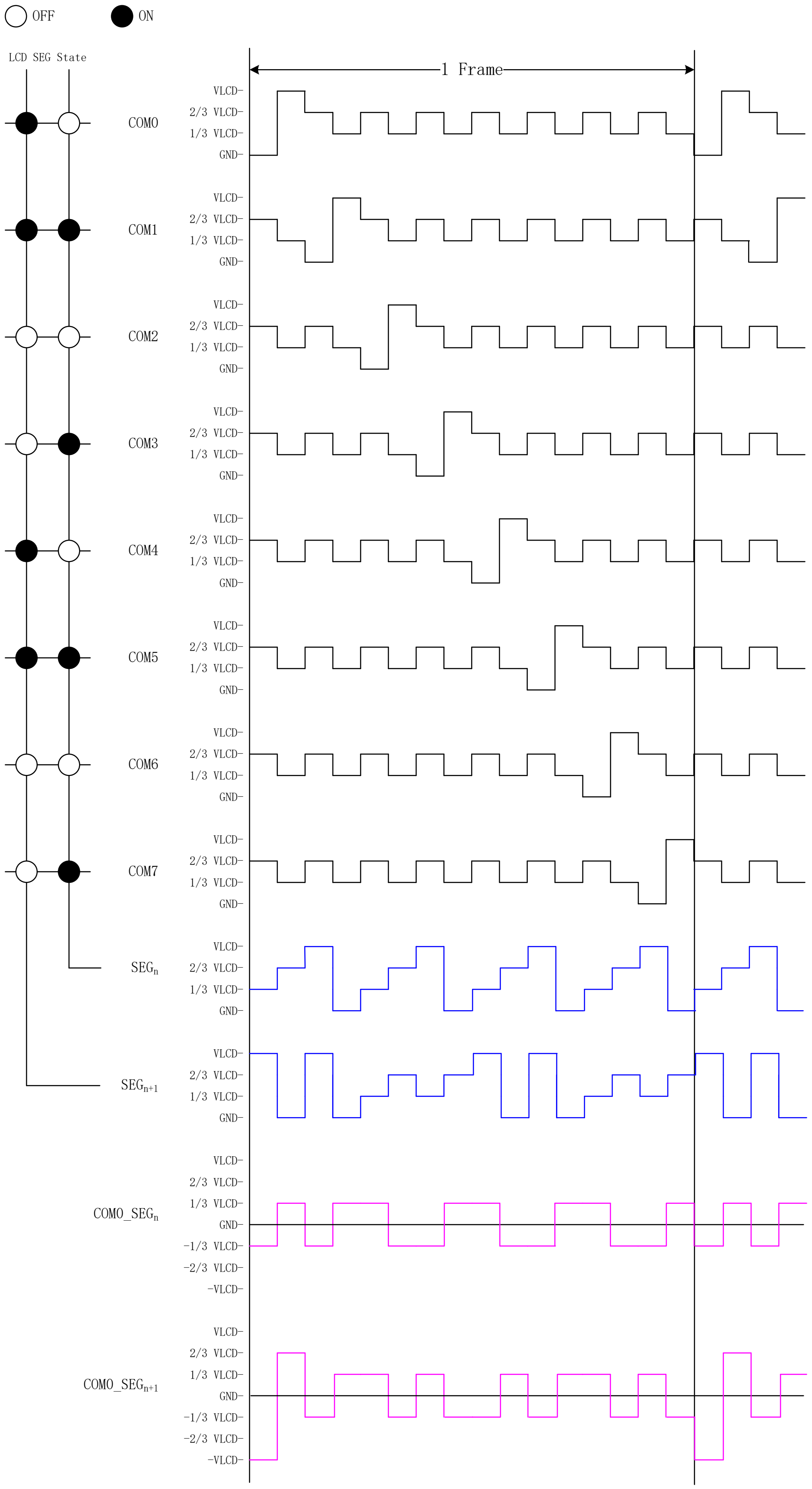


Figure 21-5 LCD Drive Waveform of 1/8 Duty and 1/3 Bias

When an LCD panel of 1/8 duty and 1/4 bias is applied, the LCD drive waveform is depicted in the following figures.

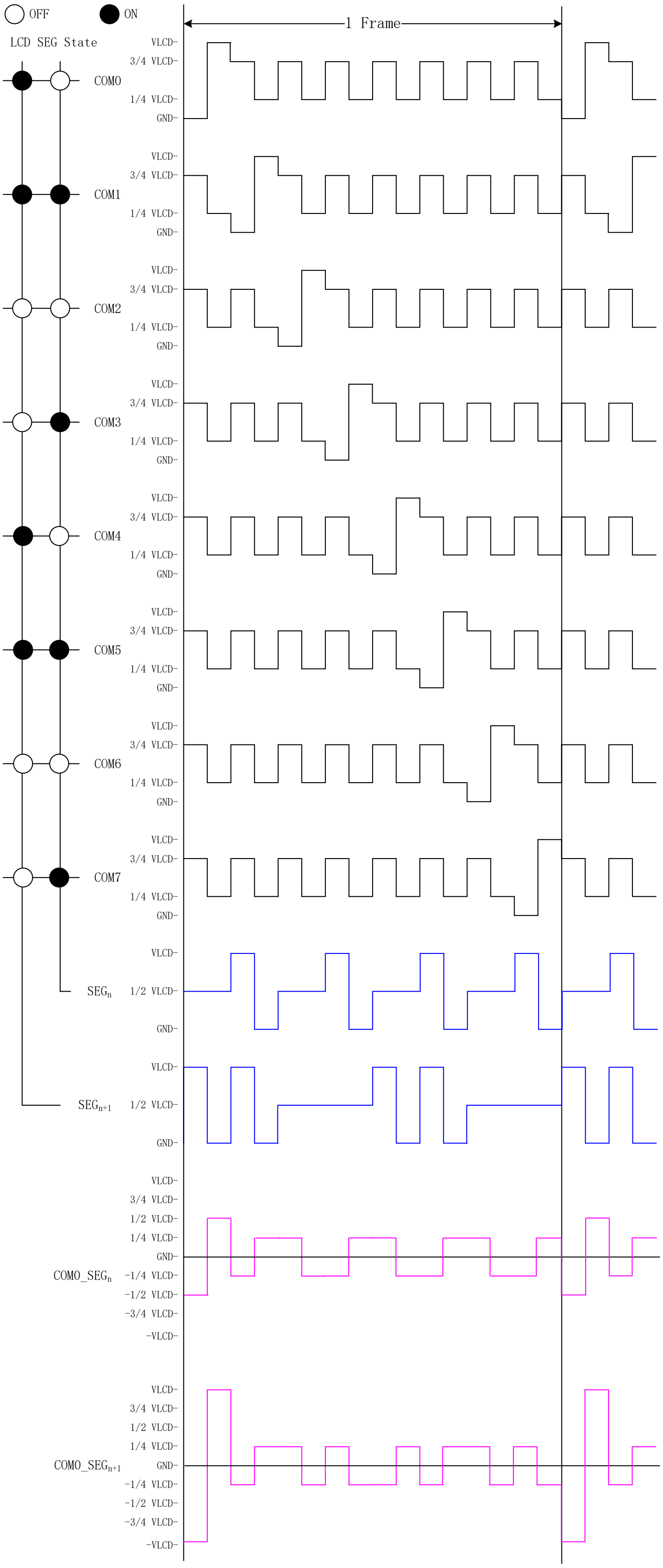


Figure 21-6 LCD Drive Waveform of 1/8 Duty and 1/4 Bias

21.8. Register Location

Table 21-1 Register Location of ANA Controller for LCD (ANA Base: 0x40014200)

Name	Type	Address	Description	Default
ANA_REG6	R/W	0x0018	Analog control register 6	0x00

Table 21-2 Register Location of LCD Controller (LCD Base: 0x40002000)

Name	Type	Address	Description	Default
LCD_FB00	R/W	0x0000	LCD Frame buffer 0 register	--
LCD_FB01	R/W	0x0004	LCD Frame buffer 1 register	--
LCD_FB02	R/W	0x0008	LCD Frame buffer 2 register	--
LCD_FB03	R/W	0x000C	LCD Frame buffer 3 register	--
LCD_FB04	R/W	0x0010	LCD Frame buffer 4 register	--
LCD_FB05	R/W	0x0014	LCD Frame buffer 5 register	--
LCD_FB06	R/W	0x0018	LCD Frame buffer 6 register	--
LCD_FB07	R/W	0x001C	LCD Frame buffer 7 register	--
LCD_FB08	R/W	0x0020	LCD Frame buffer 8 register	--
LCD_FB09	R/W	0x0024	LCD Frame buffer 9 register	--
LCD_FB0A	R/W	0x0028	LCD Frame buffer 10 register	--
LCD_FB0B	R/W	0x002C	LCD Frame buffer 11 register	--
LCD_FB0C	R/W	0x0030	LCD Frame buffer 12 register	--
LCD_FB0D	R/W	0x0034	LCD Frame buffer 13 register	--
LCD_FB0E	R/W	0x0038	LCD Frame buffer 14 register	--
LCD_FB0F	R/W	0x003C	LCD Frame buffer 15 register	--
LCD_FB10	R/W	0x0040	LCD Frame buffer 16 register	--
LCD_FB11	R/W	0x0044	LCD Frame buffer 17 register	--
LCD_FB12	R/W	0x0048	LCD Frame buffer 18 register	--
LCD_FB13	R/W	0x004C	LCD Frame buffer 19 register	--
LCD_FB14	R/W	0x0050	LCD Frame buffer 20 register	--
LCD_FB15	R/W	0x0054	LCD Frame buffer 21 register	--

LCD_FB16	R/W	0x0058	LCD Frame buffer 22 register	--
LCD_FB17	R/W	0x005C	LCD Frame buffer 23 register	--
LCD_FB18	R/W	0x0060	LCD Frame buffer 24 register	--
LCD_FB19	R/W	0x0064	LCD Frame buffer 25 register	--
LCD_FB1A	R/W	0x0068	LCD Frame buffer 26 register	--
LCD_FB1B	R/W	0x006C	LCD Frame buffer 27 register	--
LCD_FB1C	R/W	0x0070	LCD Frame buffer 28 register	--
LCD_FB1D	R/W	0x0074	LCD Frame buffer 29 register	--
LCD_FB1E	R/W	0x0078	LCD Frame buffer 30 register	--
LCD_FB1F	R/W	0x007C	LCD Frame buffer 31 register	--
LCD_FB20	R/W	0x0080	LCD Frame buffer 32 register	--
LCD_FB21	R/W	0x0084	LCD Frame buffer 33 register	--
LCD_FB22	R/W	0x0088	LCD Frame buffer 34 register	--
LCD_FB23	R/W	0x008C	LCD Frame buffer 35 register	--
LCD_FB24	R/W	0x0090	LCD Frame buffer 36 register	--
LCD_FB25	R/W	0x0094	LCD Frame buffer 37 register	--
LCD_FB26	R/W	0x0098	LCD Frame buffer 38 register	--
LCD_FB27	R/W	0x009C	LCD Frame buffer 39 register	--
LCD_CTRL	R/W	0x0100	LCD control register	0x00
LCD_CTRL2	R/W	0x0104	LCD control register 2	0x0000
LCD_SEGCTRL0	R/W	0x0108	LCD segment enable control register 0	0x00000000
LCD_SEGCTRL1	R/W	0x010C	LCD segment enable control register 1	0x00000000
LCD_SEGCTRL2	R/W	0x0110	LCD segment enable control register 2	0x00000000

21.9. Register Definition

21.9.1. LCD_FBx Register

Table 21-3 Description of LCD_FBx Register

Bit	Name	Type	Description	Default

31:0	DATAx	R/W	Each bit represents a data in the display array; see Table 3~6 for detail of data arrangement under different mode. These registers can do byte read or write, so programmer can use CPU or DMA to fill these registers.	--

The LCD_FB00~LCD_FB13 is frame buffer A.

The LCD_FB14~LCD_FB27 is frame buffer B.

The following tables show only for frame buffer A, if FBMODE is select to 1, the frame buffer B has the same data layout as frame buffer A.

Table 21-4 Data arrangement of LCD_FBx

Register	Data bit			
	31:24	23:16	15:8	7:0
LCD_FB00	COM[7:0] of SEG3	COM[7:0] of SEG2	COM[7:0] of SEG1	COM[7:0] of SEG0
LCD_FB01	COM[7:0] of SEG7	COM[7:0] of SEG6	COM[7:0] of SEG5	COM[7:0] of SEG4
…..				
LCD_FB13	COM[7:0] of SEG79	COM[7:0] of SEG78	COM[7:0] of SEG77	COM[7:0] of SEG76

When 4 or 6 COMs mode is selected, the high bit of COM will be discarded, so the data format is the same as 8 COMs mode.

21.9.2. LCD_CTRL Register

Table 21-5 Description of LCD_CTRL Register

Bit	Name	Type	Description	Default
31:8			Reserved.	0
7	EN	R/W	LCD controller enable register. 0: Disable 1: Enable	0x0
6			Reserved.	0
5:4	TYPE	R/W	LCD type control register. 0: 4 COM mode 1: 6 COM mode	0x0

			2: 8 COM mode 3: Reserved.	
3:2	DRV	R/W	LCD driving resistance control register. 0: 300 kohm 1: 600 kohm 2: 150 kohm 3: 200 kohm	0x0
1:0	FRQ	R/W	LCD scan frequency 0: 64Hz 1: 128 Hz 2: 256Hz 3: 512Hz The scan frequency here means the scan speed of each COM, so if total COM is 4, then the overall frame rate will be this value divided by 4.	0x0

Note: If user want to switch COM type, user should disable LCD controller (bit7 of LCD_CTRL register) firstly, and then wait for a delay to ensure the current frame transmission is completed. The delay is calculated according to the current frame rate (bit7 and bit1:0 of LCD_CTRL register). For example, the current LCD scan frequency is 64Hz, and user want switch 4 COM to 6 COM, the delay is calculated as following: $T_{Delay}=1/(64/4)=62.5ms$

21.9.3. LCD_CTRL2 Register

Table 21-6 Description of LCD_CTRL2 Register

Bit	Name	Type	Description	Default
31:16			Reserved.	0
15:8	SWPR	R/W	Frame buffer switch period. The switch period is calculated by the following equation. 0.5 sec * (SWPR + 1).	0x0
7:6	FBMODE	R/W	LCD frame buffer switch mode control register. 0: Always show frame buffer A. 1: Switch between frame buffer A and frame buffer B. 2: Switch between frame buffer A and blank. 3: Reserved.	0x0

5	-	-	Reserved.	0
4	BKFILL	R/W	Fill value at blank period. This register is used to control the filling value during blank period.	0x0
3:0	-	-	Reserved.	0

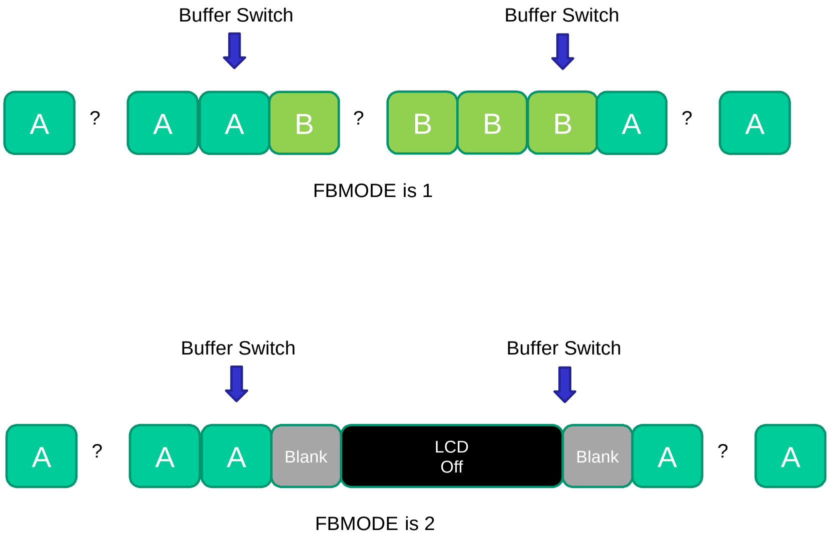


Figure 21-7 Frame buffer operation mode under different FBMODE

21.9.4. LCD_SEGCTRL0 Register

Table 21-7 Description of LCD_SEGCTRL0 Register

Bit	Name	Type	Description	Default
31:0	SEGCTRL	R/W	Each bit control the SEG0~SEG31's LCD signal enable. Bit 0: SEG 0's enable control. Bit 1: SEG 1's enable control. …. Bit 31: SEG 31's enable control. 0: Disable SEG's output. 1: Enable SEG's output.	0x00000000

21.9.5. LCD_SEGCTRL1 Register

Table 21-8 Description of LCD_SEGCTRL1 Register

Bit	Name	Type	Description	Default
31:0	SEGCTRL	R/W	Each bit control the SEG32~SEG63's LCD signal enable. Bit 0: SEG 32's enable control. Bit 1: SEG 33's enable control. …. Bit 31: SEG 63's enable control. 0: Disable SEG's output. 1: Enable SEG's output.	0x00000000

21.9.6. LCD_SEGCTRL2 Register

Table 21-9 Description of LCD_SEGCTRL2 Register

Bit	Name	Type	Description	Default
31:16	-	-	Reserved.	0
15:0	SEGCTRL	R/W	Each bit control the SEG64~SEG79's LCD signal enable. Bit 0: SEG 64's enable control. Bit 1: SEG 65's enable control. …. Bit 15: SEG 79's enable control. 0: Disable SEG's output. 1: Enable SEG's output.	0x00000000

21.9.7. ANA_REG6 Register

Table 21-10 Description of each bit in ANA_REG6

Bit	Name	Function	Notes
0	LCD_BMODE	LCD BIAS mode selection	0: 1/3 bias; 1: 1/4 bias.

4:1	VLCD[3:0]	LCD driving voltage	When VLCD=0:default When VLCD=0~5: adjust range =+60mV*VLCD When VLCD=6~15: adjust range =-60mV* (VLCD-5)

For Each COM and SEG, before enable the corresponding pin’s LCD function, programmer should disable corresponding IO input and output function manually, and disable all special function of the corresponding IO to ensure LCD function work correctly.

22. SPI Controller

22.1. Introduction

Two independent Serial Peripheral Interface (SPI) controllers are built in V85X3 to facilitate communicating with other devices and components. The setting in SPI controller will be reset after wake-up from sleep or deep-sleep mode, programmer should restore the setting manually after wake-up from these two states. The SPICLK range supported by SPI host mode is APBCLK /2/4/8/16/32/64/128. The maximum SPICLK clock supported by SPI slave mode is APBCLK /2.

22.2. Features

--Support both master and slave mode.

--Support single byte and consecutive bytes transferring.

--Support receive overrun error indication

--Support transmitting / receiving interrupt request

--Programmable phase and polarity of master clock

--Selectable data sampling time (end or middle of clock period)

--Programmable master SCK clock frequency: APB Clock / 2, / 4, /8, /16, /32, /64, /128

--Built-in 8-depth 8-bits FIFO in both transmit and receive direction, the interrupt level of these two FIFOs is both programmable.

22.3. Block Diagram

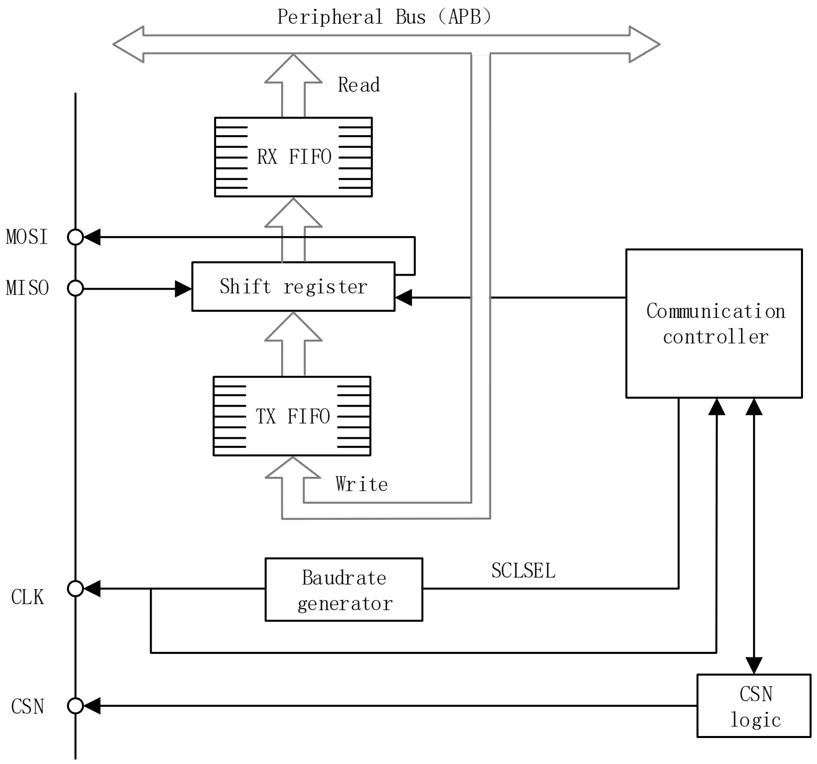


Figure 22-1 Functional Block Diagram of SPI Controller

Usually, the SPI is connected to the external device by 4 pins.

MOSI: The output pin in master mode/the input pin in slave mode. In general, MOSI is used to send data in master mode and receive data in slave mode.

MISO: The input pin in master mode/the output pin in slave mode. In general, MISO is used to receive data in master mode and send data in slave mode.

CLK: SPI serial clock pin, and controlled by master.

CSN: Slave chip select pin, According to the setting of SPI and CSN, CSN can be used as following:

--Select a slave to communication.

--Synchronous data frame.

Note: The maximum SPICLK clock supported by SPI slave mode is 1/2 APBCLK.

22.4. Register Location

Table 22-1 Register Location of SPI1 Controller (SPI1 Base: 0x40011000)

Name	Type	Address	Description	Default

SPI1_CTRL	R/W	0x0000	SPI1 Control Register	0x0000
SPI1_TXSTS	R/W	0x0004	SPI1 Transmit Status Register	0x8200
SPI1_TXDAT	R/W	0x0008	SPI1 Transmit FIFO register	--
SPI1_RXSTS	R/W	0x000C	SPI1 Receive Status Register	0x0000
SPI1_RXDAT	R	0x0010	SPI1 Receive FIFO Register	--
SPI1_MISC	R/W	0x0014	SPI1 Misc. Control Register	0x0003

Table 22-2 Register Location of SPI2 Controller (SPI2 Base: 0x40015800)

Name	Type	Address	Description	Default
SPI2_CTRL	R/W	0x0000	SPI2 Control Register	0x0000
SPI2_TXSTS	R/W	0x0004	SPI2 Transmit Status Register	0x8200
SPI2_TXDAT	R/W	0x0008	SPI2 Transmit FIFO register	--
SPI2_RXSTS	R/W	0x000C	SPI2 Receive Status Register	0x0000
SPI2_RXDAT	R	0x0010	SPI2 Receive FIFO Register	--
SPI2_MISC	R/W	0x0014	SPI2 Misc. Control Register	0x0003

22.5. Register Definition

22.5.1. SPIx_CTRL Register

The SPIx_CTRL register is used to control the SPIx controller’s behavior.

Table 22-3 Description of SPIx_CTRL Register

Bit	Name	Type	Description	Default
15	SPIEN	R/W	SPI enable For SPI1 engine if this bit is set to “1”, IOB[12:9] becomes SPI1 Interface. These pins cannot be used as GPIO. Therefore, any further corresponding setting on the selected GPIOs will be no effect. For SPI2 engine, if this bit is set to 1, IOC[3:0] becomes SPI2 interface. 0: Disabled 1: Enabled	0x0

14:12	-	-	Reserved.	0
11	SPIRST	W	SPI Soft Reset. If this bit is written by "1", the state machine of SPI controller and FIFO pointer will return to the original value. 0: No effect 1: Reset SPI Controller	
10	CSGPIO	R/W	SPI CS pin is controlled by GPIO or H/W. For Master mode. 0: SPI CS pin control by SPI H/W. 1: SPI CS pin control by GPIO setting. For Slave mode. 0: SPI CS pin is controlled by external master. 1: SPI CS pin is connected to logic 0.	0x0
9	SWAP	R/W	SPI MISO/MOSI swap control register. 0: No swap MISO/MOSI 1: Swap MISO/MOSI.	0x0
8	MOD	R/W	SPI Mode Selection register 0: Master mode 1: Slave mode	0x0
7:6	-	-	Reserved.	0
5	SCKPHA	R/W	SPI clock phase, refer to timing scheme on following section.	0x0
4	SCKPOL	R/W	SPI clock polarity, refer to timing scheme on following section.	0x0
3	-	-	Reserved.	0
2:0	SCKSEL	R/W	Master mode clock selection 000: APBCLK / 2 001: APBCLK / 4 010: APBCLK / 8 011: APBCLK / 16 100: APBCLK / 32 101: APBCLK / 64	0x0

			110: APBCLK / 128 111: Reserved.	

22.5.2. SPIx_TXSTS Register

The SPIx_TXSTS register is used to control the SPIx transmit FIFO and related interrupt.

Table 22-4 Description of SPIx_TXSTS Register

Bit	Name	Type	Description	Default
31:16	-	-	Reserved.	0
15	SPITXIF	R/C	SPI Transmit Interrupt flag. This bit is set to “1” by hardware when the transmit FIFO level is lower than the value set by the user. When SMART is set in SPI_MISC register, the bit will be cleared as long as the transmit FIFO level is high than interrupt level, else you should write “1” to this control bit to clear this flag. Read 0: Not Occurred Read 1: Occurred Write 0: No effect Write 1: Clear the flag	0x1
14	SPITXIEN	R/W	SPI Transmit Interrupt Enable If this bit is set to “1”, and SPI interrupt (when 8-bit TX FIFO level in lower then interrupt level) occurs, hardware will issue an interrupt to CPU. If this bit is cleared to “0”, this interrupt will be masked. 0: Disabled 1: Enabled	0x0
13:10	-	-	Reserved.	0
9	TXEMPTY	R	Transmit FIFO empty register. This bit will be set by hardware when the transmit FIFO is empty. And will be clear by hardware when the transmit FIFO is not empty. 0: Not Empty 1: Empty	0x1

8	TXFUR	R	Transmit FIFO under run register This will be set when transmit FIFO is empty and more data is requested by external SPI master, this bit will be set only at SPI slave mode. This bit will be cleared when programmer write 1 to SPITXIF flag.	0x0
7	-	-	Reserved.	0
6:4	TXFLEV	R/W	Transmit FIFO interrupt level register. This register is used to indicated how much bytes is stored in transmit FIFO when issued interrupt. The lower value is set, the lower interrupt penalty you have. Since you can write more data in one interrupt. FIFO Full Interrupt issue timing 000: data no. in FIFO <1, 8 write is allowed. 001: data no. in FIFO <2, 7 write is allowed. 010: data no. in FIFO <3, 6 write is allowed. 011: data no. in FIFO <4, 5 write is allowed. 100: data no. in FIFO <5, 4 write is allowed. 101: data no. in FIFO <6, 3 write is allowed. 110: data no. in FIFO <7, 2 write is allowed. 111: data no. in FIFO <8, 1 write is allowed.	0x0
3	-	-	Reserved	0
2:0	TXFFLAG	R	Transmit FIFO Data Level. The register is used to indicate how much data is still in the FIFO. 0000: No data in FIFO or 8 bytes in FIFO. 0001: 1 byte in FIFO. 0010: 2 bytes in FIFO. 0011: 3 bytes in FIFO. 0100: 4 bytes in FIFO. 0101: 5 bytes in FIFO. 0110: 6 bytes in FIFO. 0111: 7 bytes in FIFO.	0x0

22.5.3. SPIx_TXDAT Register

The SPIx_TXDAT register is used to write data to transmit FIFO of SPIx engine and shift out to external master or slave.

Table 22-5 Description of SPIx_TXDAT Register

Bit	Name	Type	Description	Default
31:8	-	-	Reserved.	0
7:0	SPITXD	W	Write data to SPI Transmit FIFO.	--

22.5.4. SPIx_RXSTS Register

The SPIx_RXSTS register is used to control the SPIx receive FIFO and related interrupt. Table 18-5 shows the bit assignment of SPIx_RXSTS register.

Table 22-6 Description of SPIx_RXSTS Register

Bit	Name	Type	Description	Default
31:16	-	-	Reserved.	0
15	SPIRXIF	R/C	SPI Receive Interrupt flag. This bit is set to "1" by hardware when the receive FIFO level is higher than the value set by the user. When SMART is set in SPI_MISC register, the bit will be cleared as long as the receive FIFO level is lower than interrupt level, else you should write "1" to this control bit to clear this flag. Read 0: Not Occurred Read 1: Occurred Write 0: No effect Write 1: Clear the flag	0x0
14	SPIRXIEN	R/W	SPI Receive Interrupt Enable. If this bit is set to "1", and SPI interrupt (when 8-bit RX FIFO level in higher than interrupt level) occurs, hardware will issue an interrupt to CPU. If this bit is cleared to "0", this interrupt will be masked. 0: Disabled 1: Enabled	0x0

13:10	-	-	Reserved.	0
9	RXFULL	R	Receive FIFO full register. This bit will be set by hardware when the receive FIFO is full. And will be clear by hardware when the receive FIFO is not full. 0: Not Full 1: Full	0x0
8	RXFOV	R	Receive FIFO over run register. This will be set when receive FIFO is full and more data is receive on the SPI data bus. This bit will be cleared when write 1 to SPIRXIF.	0x0
7	-	-	Reserved.	0
6:4	RXFLEV	R/W	Receive FIFO interrupt level register. This register is used to indicated how much bytes is stored in receive FIFO when issued interrupt. The larger value is set, the lower interrupt penalty you have. Since you can read more data in one interrupt. FIFO Full Interrupt issue timing. 000: data no. in FIFO >= 1, 1 read is allowed. 001: data no. in FIFO >= 2, 2 read is allowed. 010: data no. in FIFO >= 3, 3 read is allowed. 011: data no. in FIFO >= 4, 4 read is allowed. 100: data no. in FIFO >= 5, 5 read is allowed. 101: data no. in FIFO >= 6, 6 read is allowed. 110: data no. in FIFO >= 7, 7 read is allowed. 111: data no. in FIFO >= 8, 8 read is allowed.	0x0
3	-	-	Reserved	0
2:0	RXFFLAG	R	Receive FIFO Data Level The register is used to indicate how much data is still in the FIFO. 0000: No data in FIFO or 8 bytes in FIFO 0001: 1 byte in FIFO 0010: 2 bytes in FIFO	0x0

			0011: 3 bytes in FIFO 0100: 4 bytes in FIFO 0101: 5 bytes in FIFO 0110: 6 bytes in FIFO 0111: 7 bytes in FIFO	

22.5.5. SPIx_RXDAT Register

The SPIx_RXDAT register is used to read data from receive FIFO of SPIx engine.

Table 22-7 Description of SPIx_RXDAT Register

Bit	Name	Type	Description	Default
31:8	-	-	Reserved.	0
7:0	SPIRXD	R	Read data from SPI Receive FIFO.	--

22.5.6. SPIx_MISC Register

The SPIx_MISC register is used to control misc. features of SPIx engine.

Table 22-8 Description of SPIx_MISC Register

Bit	Name	Type	Description	Default
31:10	-	-	Reserved.	0
9	OVER	R/W	SPI FIFO Over Write Mode This register is used to control the data will be overwrite or skipped when TX/RX FIFO is full. 0: The further write to the full FIFO will be skipped. 1: The further write to the full FIFO will overwrite the last written data in the FIFO.	0x0
8	SMART	R/W	SPI FIFO SMART Mode Register When this bit is set to “1”, programmer don’t need to clear the transmit/receive interrupt flag when the FIFO status is reach, programmer only needs write-to/read-from transmit/receive FIFO and let the FIFO level lower/higher than the interrupt level, and the interrupt flag will clear automatically. When DMA mode is selected, this bit must be set to 1 to ensure the DMA	0x0

			operation correctly. 0: Normal Interrupt Clear 1: Smart Interrupt Clear	
7:5	-	-	Reserved.	0
4	BSY	R	SPI Controller Busy Flag This bit is used to indicate if the SPI controller is busy or not. 0: Idle 1: Busy	0x0
3	RFF	R	Receive FIFO Full Flag This bit is used to indicate if the SPI controller is real full or not. If the receive FIFO is full, that means any data read from SPI bus can't be written into the FIFO, and the RFOV bit will be set in this situation. 0: Receive FIFO not full 1: Receive FIFO full.	0x0
2	RNE	R	Receive FIFO Not Empty Flag This bit is used to indicated if there is any data currently in the receive FIFO. 0: Receive FIFO is empty 1: Receive FIFO is not empty	0x0
1	TNF	R	Transmit FIFO Not Full Flag. This bit is used to indicated if there is any empty slots in the transmit FIFO. 0: Transmit FIFO is full, you can't write any more data into it. 1: Transmit FIFO is not full.	0x1
0	TFE	R	Transmit FIFO Empty Flag This bit is used to indicated if the transmit FIFO is empty or not. 0: Transmit FIFO is not empty. 1: Transmit FIFO is empty.	0x1

22.6. Application Note

22.6.1. Master Mode

When in master mode, the shifting clock (SPICLK) is generated by V85X3. There are two control bits to control the clock phase and polarity. The transmission starts immediately from a register writes to the SPI_TXDAT register. As long as there is data in the FIFO, the transmission will start automatically when one byte is transferred.

The SPI shifts the data from MSB to LSB through the SDO pin. The 8-bit data is shifted out after 8 SCK cycles. At the same time, the data is also shifted in through slave device SDI pin. When the transmit FIFO level is lower than the interrupt trigger level, the SPITXIF flag bit will be set; besides, a SPI interrupt will be generated if the SPITXIEN bit is set. When the receive FIFO level is higher than the interrupt trigger level, the SPIRXIF flag bit will be set; besides, a SPI interrupt will be generated if the SPIRXIEN bit is set. Programmer can read SPI data from SPI_RXDAT register.

The following diagram depicts the timing scheme on SPI master mode for different operation types (polarity control bit equals "1" or "0", phase control bit equals "1" or "0", and sample strobe control bit equals "1" or "0").

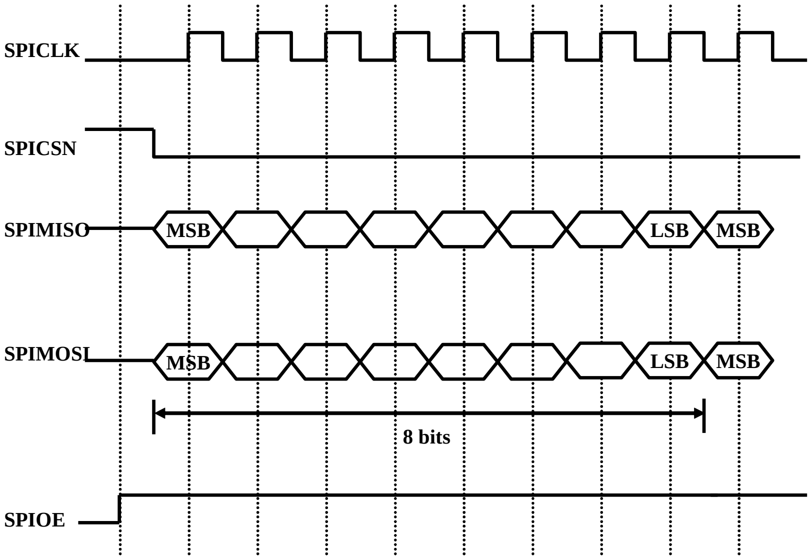


Figure 22-2Master Mode, SPO = 0, SPH=0

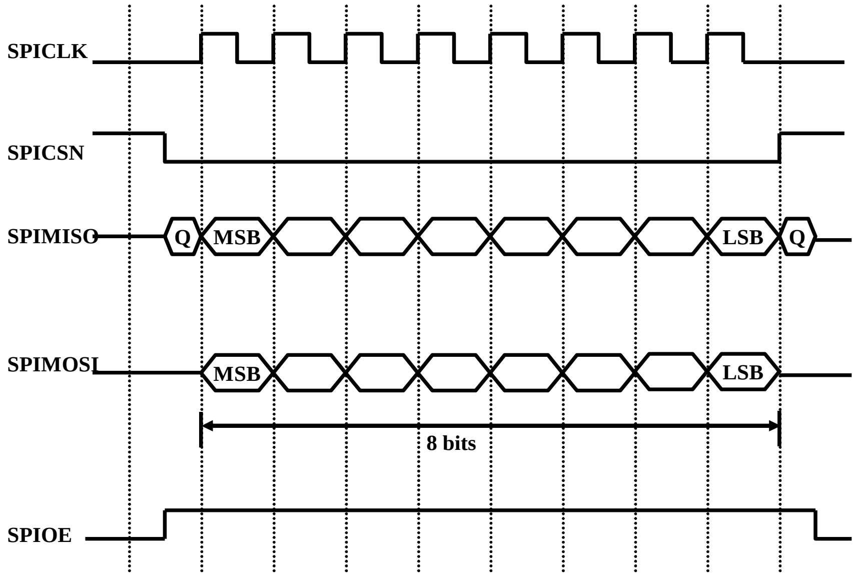


Figure 22-3 Master Mode, SPO = 0, SPH=1

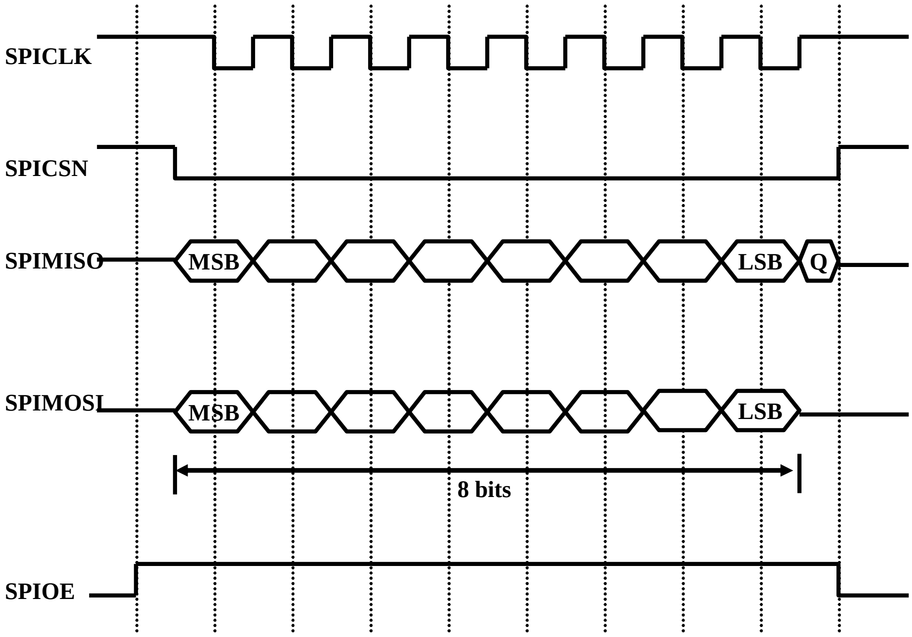


Figure 22-4 Master Mode, SPO = 1, SPH=0

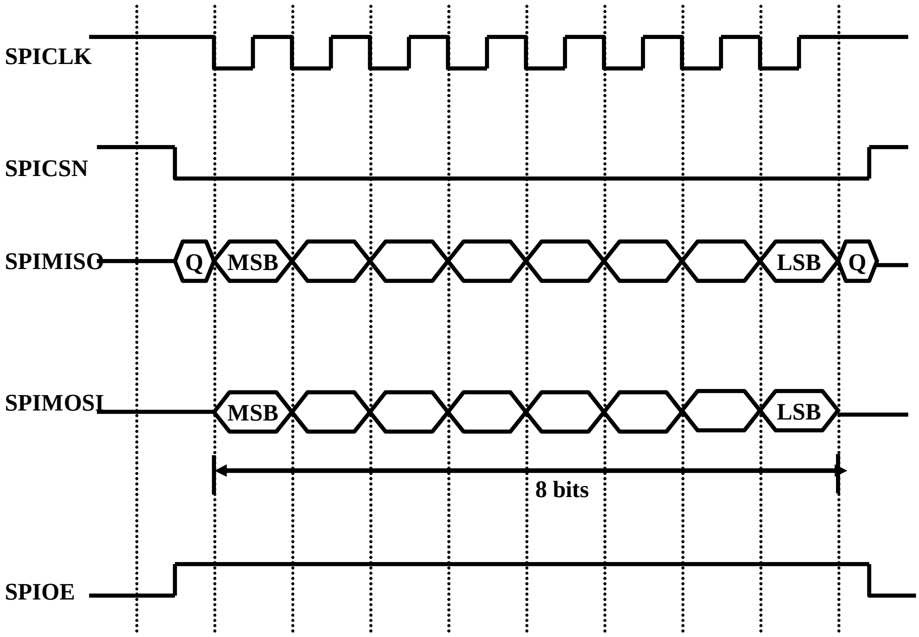


Figure 22-5 Master Mode, SPO = 1, SPH=1

22.6.2. Salve Mode

During SPI salve mode, the SPICLK and SPICSN is generated by the external master. The SPI slave mode is supported only for SPO=0 and SPH=0. The same SPI_TXDAT and SPI_RXDAT registers are used for data transmit and receive. The maximum allowed SPICLK during SPI slave mode is 1/2 APBCLK. And DMA transfer is recommended when the receive clock is fast.

22.6.3. Consecutive Bytes Transfer

Consecutive bytes transfer is available in master and slave modes. In transmission, software is able to send the data consecutively as long as the TNF bit is 1. In reception, software will check for overrun error to monitor if there is any missing data due to the polling rate is too low.

23. I2C Controller

23.1. Introduction

The I2C subcomponent is the I2C Bus Controller which provides an interface that meets the Philips I2C bus specification and supports all transfer modes from and to the I2C bus. The I2C bus uses two wires to transfer information between devices connected to the bus: "scl" (serial clock line) and "sda" (serial data line). The I2C logic handles bytes transfer autonomously. It also keeps track of serial transfers, and a status register reflects the status of the I2C Bus Controller and the I2C bus. The setting in I2C controller will be reset after wake-up from sleep or deep-sleep mode, programmer should restore the setting manually after wake-up from these two states. The I2C Bus supports fSCL = 1MHz (period: 1us) and can be realized by setting the overflow frequency of timer 3.

23.2. Feature

--Master transmit/receive mode supported.

--Slave transmit/receive mode supported.

--Detection of bus arbitration fail.

--Interrupt generation.

--Programmable ACK generation.

--Programmable clock speed in master mode.

--Input de-bounce circuit.

23.3. Block Diagram

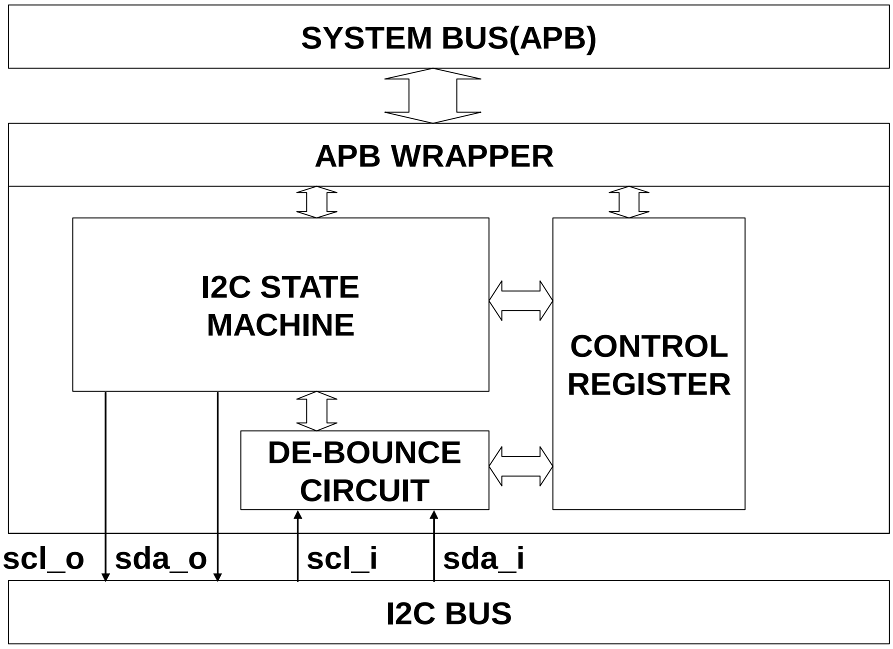


Figure 23-1 Functional Block Diagram of I2C Controller

23.4. Register Location

Table 23-1 Register Location of I2C Controller (I2C Base: 0x40010800)

Name	Type	Address	Description	Default
I2C_DATA	R/W	0x0000	I2C data register	0x00
I2C_ADDR	R/W	0x0004	I2C address register	0x00
I2C_CTRL	R/W	0x0008	I2C control/status register	0x00
I2C_STS	R	0x000c	I2C status register	0xF8
I2C_CTRL2	R/W	0x0018	I2C interrupt enable register	0x0

23.5. Register Definition

23.5.1. I2C_DATA Register

Table 23-2 Description of I2C_DATA Register

Bit	Name	Type	Description	Default
31:8	-	-	Reserved.	0
7:0	DATA	R/W	The I2C_DATA register contains a byte to be transmitted through I2C bus or a byte which has just been received through I2C bus. The CPU can read from and write to this 8-bit register while it is not in the process of byte shifting. The I2C_DATA register is not shadowed or double buffered so the user should only read I2C_DATA when an I2C interrupt occurs.	0x00

23.5.2. I2C_ADDR Register

Table 23-3 Description of I2C_ADDR Register

Bit	Name	Type	Description	Default
31:8	-	-	Reserved.	0
7:1	SLA	R/W	Own I2C slave address (7 bit)	0x00
0	GC	R/W	General Call Address Acknowledge If this bit is set, the general call address is recognized; otherwise it is ignored.	0x0

23.5.3. I2C_CTRL Register

Table 23-4 Description of I2C_CTRL Register

Bit	Name	Type	Description	Default
31:8	-	-	Reserved.	0
7	CR2	R/W	Clock rate bit 2	0x0
6	EN	R/W	I2C enable bit When EN='0' the "sdao" and "sclo" outputs are set to 1, that drives the output pads of the chip in high impedance, and "sdai" and "scli" input signals are ignored. When EN='1' I2C component is enabled and corresponded GPIO will be set to I2C function automatically.	0x0
5	STA	R/W	START Flag	0x0

			When STA=’1’, the I2C component checks the I2C bus status and if the bus is free a START condition is generated.	
4	STO	R/W	STOP Flag When STO=’1’ and I2C interface is in master mode, a STOP condition is transmitted to the I2C bus.	0x0
3	SI	R/C	Serial Interrupt Flag The “SI“ is set by hardware when one of 25 out of 26 possible I2C states is entered. The only state that does not set the “SI” is state F8h, which indicates that no relevant state information is available. The “SI” flag must be cleared by software. In order to clear the “SI” bit, ‘0’ must be written to this bit. Writing a ‘1’ to “SI” bit does not change value of the “SI”. When an interrupt is occurred, clear SI means the trigger of next action, so all the necessary control register or data must be set before SI is cleared.	0x0
2	AA	R/W	Assert Acknowledge Flag When AA=’1’, an “acknowledge” will be returned when: - the “own slave address” has been received - the general call address has been received while GC bit in i2caddr register was set - a data byte has been received while I2C was in master receiver mode - a data byte has been received while I2C was in slave receiver mode When AA=’0’, an “not acknowledge” will be returned when: - a data byte has been received while I2C was in master receiver mode - a data byte has been received while I2C was in slave receiver mode	0x0
1	CR1	R/W	Clock rate bit 1	0x0
0	CR0	R/W	Clock rate bit 0	0x0

Table 23-5 shows the SCL clock frequency at master mode under different CR2~CR0 setting.

Table 23-5 SCL clock speed setting

CR2	CR1	CR0	SCL Frequency (KHz)				Clock Divided by
			PCLK = 6.5536 MHz	PCLK = 13.1072 MHz	PCLK = 19.6608 MHz	PCLK = 26.2144 MHz	
0	0	0	25.6	51.2	76.8	102.4	256
0	0	1	29.2	58.4	87.6	116.8	224
0	1	0	34.1	68.2	102.3	136.4	192
0	1	1	40.9	81.9	122.9	163.8	160
1	0	0	6.8	13.7	20.5	27.3	960
1	0	1	54.6	109.2	163.8	218.4	120
1	1	0	109.2	218.4	327.7	436.9	60
1	1	1	TIMER3’s overflow frequency divide by 8				

23.5.4. I2C_STS Register

Table 23-6 Description of I2C_STS Register

Bit	Name	Type	Description	Default
31:8	-	-	Reserved.	0
7:3	STS	R	I2C Status Code.	0x1F
2:0	-	-	Reserved.	0

Table 23-7~Table 23-11 shows the status code under different kind of I2C modes.

Table 23-7 I2C Status in Master Transmitter Mode

STS	Status of I2C	Application Software Response					Next Action taken by I2C hardware
		Read/Write I2C_DATA	To I2C_CTRL				
			STA	STO	SI	AA	
0x08	A START condition has been transmitted.	Write SLA+W*	X	0	0	X	SLA+W will be transmitted ACK will be received
0x10	A repeated START condition has been transmitted.	Write SLA+W	X	0	0	X	SLA+W will be transmitted ACK will be received
		Write SLA+R*	X	0	0	X	SLA+R will be transmitted I2C will be switched to master receive mode

0x18	SLA+W has been transmitted. ACK has been received.	Write data byte	0	0	0	X	Data byte will be transmitted. ACK will be received
		no action	1	0	0	X	Repeated START will be transmitted.
		no action	0	1	0	X	STOP condition will be transmitted. STO flag will be reset
		no action	1	1	0	X	STOP condition followed by a START condition will be transmitted. STO flag will be reset
0x20	SLA+W has been transmitted. NACK has been received.	Write data byte	0	0	0	X	Data byte will be transmitted. ACK will be received
		no action	1	0	0	X	Repeated START will be transmitted.
		no action	0	1	0	X	STOP condition will be transmitted. STO flag will be reset
		no action	1	1	0	X	STOP condition followed by a START condition will be transmitted. STO flag will be reset
0x28	Data byte in i2cdat has been transmitted. ACK has been received.	Write data byte	0	0	0	X	Data byte will be transmitted. ACK bit will be received
		no action	1	0	0	X	Repeated START will be transmitted.
		no action	0	1	0	X	STOP condition will be transmitted. STO flag will be reset.
		no action	1	1	0	X	STOP condition followed by a START condition will be transmitted. STO flag will be reset.
0x30	Data byte in i2cdat has been transmitted. NACK has been received.	Write data byte *	0	0	0	X	Data byte will be transmitted. ACK will be received.
		no action	1	0	0	X	Repeated START will be transmitted.
		no action	0	1	0	X	STOP condition will be transmitted. STO flag will be

							reset.
		no action	1	1	0	X	STOP condition followed by a START condition will be transmitted. STO flag will be reset.

*: SLA+W: Slave address [7:1] and write bit as bit 0, write bit is 0.

*: SLA+R: Slave address [7:1] and read bit as bit 0, read bit is 1.

Table 23-8 I2C Status in Master Receiver Mode

STS	Status of I2C	Application Software Response					Next Action taken by I2C hardware
		Read/Write	To I2C_CTRL				
		I2C_DATA	STA	STO	SI	AA	
0x08	A START condition has been transmitted	Write SLA+R	X	0	0	X	SLA+R will be transmitted. ACK will be received
0x10	A repeated START condition has been transmitted.	Write SLA+R	X	0	0	X	SLA+R will be transmitted. ACK will be received
		Write SLA+W	X	0	0	X	SLA+W will be transmitted. I2C will be switched to master transmit mode
0x40	SLA+R has been transmitted. ACK has been received.	no action	0	0	0	0	Data byte will be received. not ACK will be returned
		no action	0	0	0	1	Data byte will be received. ACK will be returned
0x48	SLA+R has been transmitted. Not ACK has been received.	no action	1	0	0	X	Repeated START condition will be transmitted
		no action	0	1	0	X	STOP condition will be transmitted. STO flag will be reset
		no action	1	1	0	X	STOP condition followed by a START condition will be transmitted. STO flag will be reset
0x50	Data byte has been received. ACK has been returned.	Read data byte	0	0	0	0	Data byte will be received. not ACK will be returned
		Read data byte	0	0	0	1	Data byte will be received. ACK will be returned
0x58	Data byte has been	Read data	1	0	0	X	Repeated START condition will

	received. Not ACK has been returned.	byte					be transmitted
		Read data byte	0	1	0	X	STOP condition will be transmitted. STO flag will be reset
		Read data byte	1	1	0	X	STOP condition followed by a START condition will be transmitted. STO flag will be reset

Table 23-9 I2C Status in Slave Receiver Mode

STS	Status of I2C	Application Software Response					Next Action taken by I2C hardware
		Read/Write I2C_DATA	To I2C_CTRL				
			STA	STO	SI	AA	
0x60	Own SLA+W has been received. ACK has been returned.	no action	X	0	0	0	Data byte will be received and not ACK will be returned.
		no action	X	0	0	1	Data byte will be received and ACK will be returned.
0x68	Arbitration lost in SLA+R/W as master. Own SLA+W has been received, ACK returned.	no action	X	0	0	0	Data byte will be received and not ACK will be returned.
		no action	X	0	0	1	Data byte will be received and ACK will be returned.
0x70	General call address (00H) has been received. ACK has been returned.	no action	X	0	0	0	Data byte will be received and not ACK will be returned.
		no action	X	0	0	1	Data byte will be received and ACK will be returned.
0x78	Arbitration lost in SLA+R/W as master. General call address has been received, ACK returned.	no action	X	0	0	0	Data byte will be received and not ACK will be returned.
		no action	X	0	0	1	Data byte will be received and ACK will be returned.
0x80	Previously addressed with own SLV address. DATA has been received. ACK returned.	Read data byte	X	0	0	0	Data byte will be received and not ACK will be returned.
		Read data byte	X	0	0	1	Data byte will be received and ACK will be returned.
0x88	Previously addressed with own SLA. DATA byte has been received. Not ACK returned.	Read data byte	0	0	0	0	Switched to not addressed SLV mode. No recognition of own SLA or general call address.

		Read data byte	0	0	0	1	Switched to not addressed SLV mode. Own SLA or general call address will be recognized.
		Read data byte	1	0	0	0	Switched to not addressed SLV mode. No recognition of own SLA or general call address. START condition will be transmitted when the bus becomes free.
		Read data byte	1	0	0	1	Switched to not addressed SLV mode. Own SLA or general call address will be recognized. START condition will be transmitted when the bus becomes free.
0x90	Previously addressed with general call address. DATA has been received. ACK returned.	Read data byte	X	0	0	0	Data byte will be received and not ACK will be returned.
		Read data byte	X	0	0	1	Data byte will be received and ACK will be returned.
0x98	Previously addressed with general call address. DATA has been received. Not ACK returned.	Read data byte	0	0	0	0	Switched to not addressed SLV mode. No recognition of own SLA or general call address
		Read data byte	0	0	0	1	Switched to not addressed SLV mode. Own SLA or general call address will be recognized.
		Read data byte	1	0	0	0	Switched to not addressed SLV mode; no recognition of own SLA or general call address. START condition will be transmitted when the bus becomes free.
		Read data byte	1	0	0	1	Switched to not addressed SLV mode. Own SLA or general call address will be recognized. START condition will be transmitted when the bus becomes free
0xA0	A STOP condition or	no action	0	0	0	0	Switched to not addressed

	repeated START condition has been received while still addressed as slave receive or slave transmit mode.						SLV mode. No recognition of own SLA or general call address.
		no action	0	0	0	1	Switched to not addressed slave mode. Own SLA or general call address will be recognized.
		no action	1	0	0	0	Switched to not addressed SLV mode. No recognition of own SLA or general call address. START condition will be transmitted when the bus becomes free
		no action	1	0	0	1	Switched to not addressed SLV mode. Own SLA or general call address will be recognized. START condition will be transmitted when the bus becomes free.

Table 23-10 I2C Status in Slave Transmitter Mode

STS	Status of I2C	Application Software Response					Next Action taken by I2C hardware
		Read/Write	To I2C_CTRL				
		I2C_DATA	STA	STO	SI	AA	
0xA8	Own SLA+R has been received. ACK has been returned.	Write data byte	X	0	0	0	Last data byte will be transmitted and ACK will be received.
		Write data byte	X	0	0	1	Data byte will be transmitted. ACK will be received.
0xB0	Arbitration lost in SLA+R/W as master. Own SLA+R has been received. ACK has been returned.	Write data byte	X	0	0	0	Last data byte will be transmitted and ACK will be received.
		Write data byte	X	0	0	1	Data byte will be transmitted. ACK will be received.
0xB8	Data byte has been transmitted. ACK has been received.	Write data byte	X	0	0	0	Last data byte will be transmitted and ACK will be received.
		Write data byte	X	0	0	1	Data byte will be transmitted; ACK will be received.
0xC0	Data byte has been	no action	0	0	0	0	Switched to not addressed

	transmitted. NACK has been received.						SLV mode. No recognition of own SLA or general call address.
		no action	0	0	0	1	Switched to not addressed SLV mode. Own SLA or general call address will be recognized.
		no action	1	0	0	0	Switched to not addressed SLV mode. No recognition of own SLA or general call address. START condition will be transmitted when the bus becomes free.
		no action	1	0	0	1	Switched to not addressed SLV mode. Own SLA or general call address will be recognized. START condition will be transmitted when the bus becomes free.
0xC8	Last data byte has been transmitted. ACK has been received.	no action	0	0	0	0	Switched to not addressed SLV mode. No recognition of own SLA or general call address.
		no action	0	0	0	1	Switched to not addressed SLV mode. Own SLA or general call address will be recognized.
		no action	1	0	0	0	Switched to not addressed SLV mode. No recognition of own SLA or general call address. START condition will be transmitted when the bus becomes free.
		no action	1	0	0	1	Switched to not addressed SLV mode. Own SLA or general call address will be recognized. START condition will be transmitted when the bus becomes free.

Table 23-11 I2C Misc. Status

STS	Status of I2C	Application Software Response	Next Action taken by I2C

		Read/Write	To I2C_CTRL				hardware
		I2C_DATA	STA	STO	SI	AA	
0x38	Arbitration lost	No action	0	0	0	X	I2C bus will be released; A start condition will be transmitted.
		No action	1	0	0	X	when the bus becomes free (enter to a master mode)
0xF8	No relevant state information available; si=0	No action	X	X	X	X	Wait or proceed current transfer
0x00	Bus error during MST or selected slave modes	No action	0	1	0	X	Only the internal hardware is affected in the MST or addressed SLV modes. In all cases, the bus is released and I2C is switched to the not addressed SLV mode. Sto flag is reset.

23.5.5. I2C_CTRL2 Register

Table 23-12 Description of I2C_CTRL2 Register

Bit	Name	Type	Description	Default
31:1	-	-	Reserved.	0
0	INTEN	R/W	Interrupt enable control of I2C controller. 0: Disable. 1: Enable.	0x0

23.6. Application Notes

23.6.1. I2C Bus Protocol: Start/Stop Generation

A Start condition can transfer a one-byte serial data over the SDA line, and a stop condition can terminate the data transfer. A stop condition is a Low-to-High transition of the SDA line while SCL is high. Start and Stop conditions are always generated by the master. The I2C-bus is busy when a Start condition is generated. A few clocks after a Stop condition, the IIC-bus will be free, again.

When a master initiates a Start condition, it should send a slave address to notify the slave device. The one byte of address field consists of a 7-bit address and a 1-bit transfer direction indicator (that is, write or read). If bit 8 is 0, it indicates a write operation (transmit operation); if bit 8 is 1, it indicates a request for data read (receive operation).

The master will finish the transfer operation by transmitting a Stop condition. If the master wants to continue the data transmission to the bus, it should generate another Start condition as well as a slave address. In this way, the read/write operation can be performed in various formats.

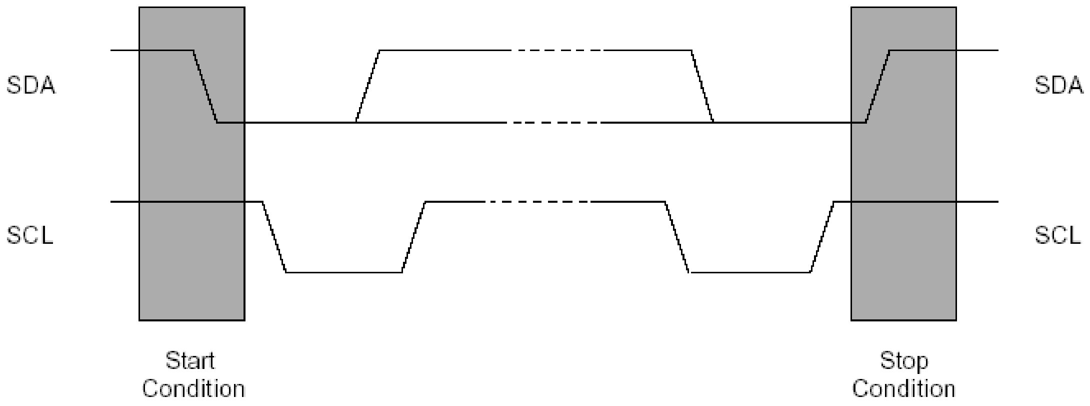


Figure 23-2 Start and Stop Conditions

23.6.2. Data Transfer Format

Every byte placed on the SDA line should be eight bits in length. The number of bytes which can be transmitted per transfer is unlimited. The first byte following a Start condition should have the address field. The address field can be transmitted by the master when the IIC-bus is operating in master mode. Each byte should be followed by an acknowledgement (ACK) bit. The MSB bit of the serial data and addresses are always sent first.

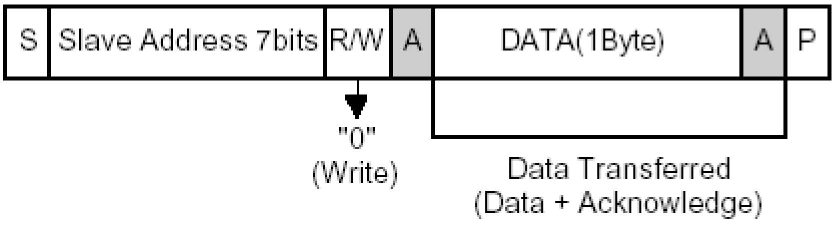


Figure 23-3 Write Mode with 7-bits Address

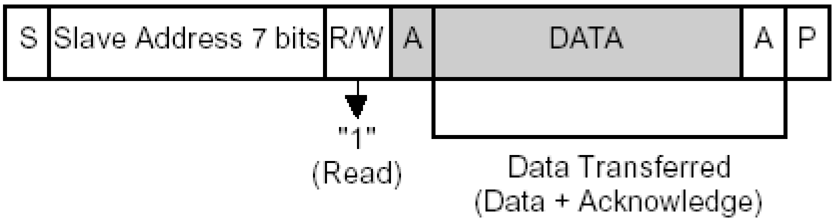


Figure 23-4 Read Mode with 7-bits Address

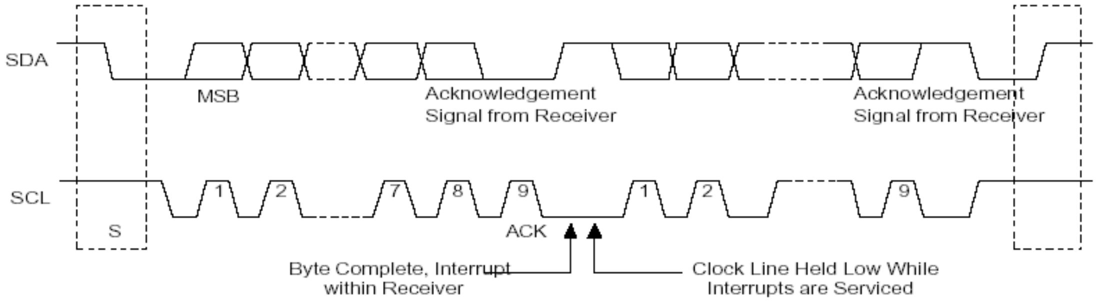

SDA
SCL
S
MSB
Acknowledgement Signal from Receiver
Acknowledgement Signal from Receiver
1
2
7
8
9
1
2
9
ACK
Byte Complete, Interrupt within Receiver
Clock Line Held Low While Interrupts are Serviced

Figure 23-5 Data Transfer on The I2C bus

23.6.3. ACK Signal Transmission

To finish a one-byte transfer operation completely, the receiver should send an ACK bit to the transmitter. The ACK pulse should occur at the ninth clock of the SCL line. Eight clocks are required for the one-byte data transfer. The master should generate the clock pulse required to transmit the ACK bit.

The transmitter should release the SDA line by making the SDA line High when the ACK clock pulse is received. The receiver should also drive the SDA line Low during the ACK clock pulse so that the SDA is Low during the High period of the ninth SCL pulse.

The ACK bit transmit function can be enabled or disabled by software (AA). However, the ACK pulse on the ninth clock of SCL is required to complete a one-byte data transfer operation.

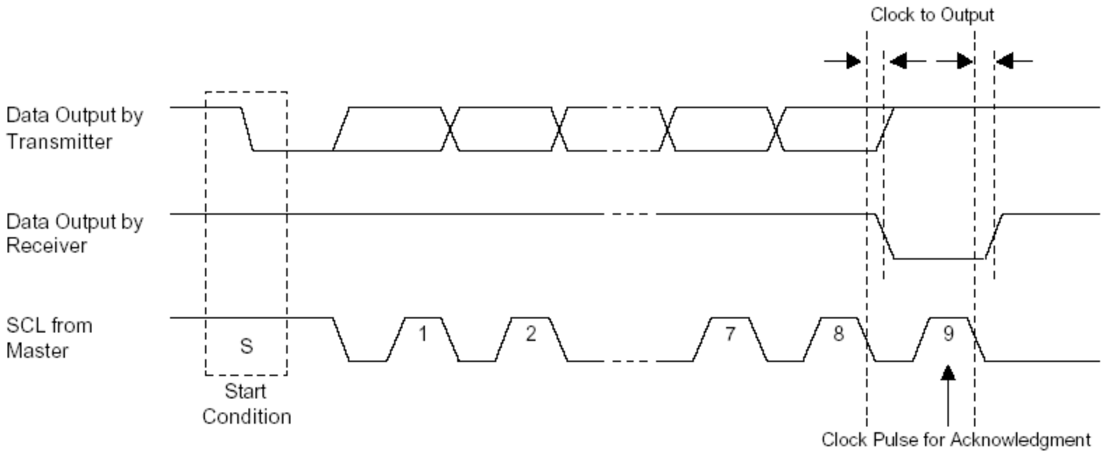


Figure 23-6 Acknowledge on The I2C bus

23.6.4. Read-Write Operation

In the transmitter mode, after the data is transferred, the I2C-bus interface will wait until pending interrupt is cleared. Until the interrupt is cleared, the SCL line will be held low. After the interrupt is cleared, the SCL line will be released. After the CPU receives the interrupt request, it should write a new data into I2C_DATA before clear the pending interrupt.

In the receive mode, after a data is received, the I2C-bus interface will wait until pending interrupt is cleared. Until the pending interrupt is cleared, the SCL line will be held low. After the pending interrupt is cleared, the SCL line will be released. After the CPU receives the interrupt request, it should read the data from I2C_DATA before clear the pending interrupt.

Bus Arbitration Procedures

Arbitration takes place on the SDA line to prevent the contention on the bus between two masters. If a master with a SDA High level detects another master with a SDA active Low level, it will not initiate a data transfer because the current level on the bus does not correspond to its own. The arbitration procedure will be extended until the SDA line turns high.

However when the masters simultaneously lower the SDA line, each master should evaluate whether or not the mastership is allocated to itself. For the purpose of evaluation, each master should detect the address bits. While each master generates the slaver address, it should also detect the address bit on the SDA line because the

Lowering of SDA line is stronger than maintaining High on the line. For example, one master generates a Low as first address bit, while the other master is maintaining High. In this case, both masters will detect Low on the bus because Low is stronger than high even if first master is trying to maintain high on the line. When this happens, low (as the first bit of address) -generating master will get the mastership and high (as the first bit of address) - generating master should withdraw the mastership. If both masters generate Low as the first bit of address, there should be an arbitration for second address bit, again. This arbitration will continue to the end of last address bit.

Abort Condition

If a slave receiver can't acknowledge the confirmation of the slave address, it should hold the level of the SDA line High. In this case, the master should generate a Stop condition and abort the transfer.

If a master receiver is involved in the aborted transfer, it should signal the end of the slave transmit operation by canceling the generation of an ACK after the last data byte received from the slave. The slave transmitter should then release the SDA to allow a master to generate a Stop condition.

23.6.5. Interface Timing

The following diagram shows the interface connection of I2C bus.

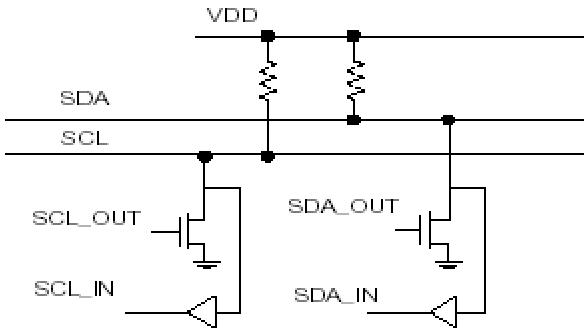


Figure 23-7 I2C Bus Connection Example

To control the frequency of the serial clock (SCL), programmer can use CR2~CR0 in the I2C_CTRL register.

The I2C Bus supports fSCL = 1MHz (period: 1us).

— Rise Time of the SCL and SDA: fSCL= 100kHz：1000ns；fSCL= 400kHz：300ns

— Fall Time of the SCL and SDA: fSCL= 100kHz：300ns；fSCL= 400kHz：300ns

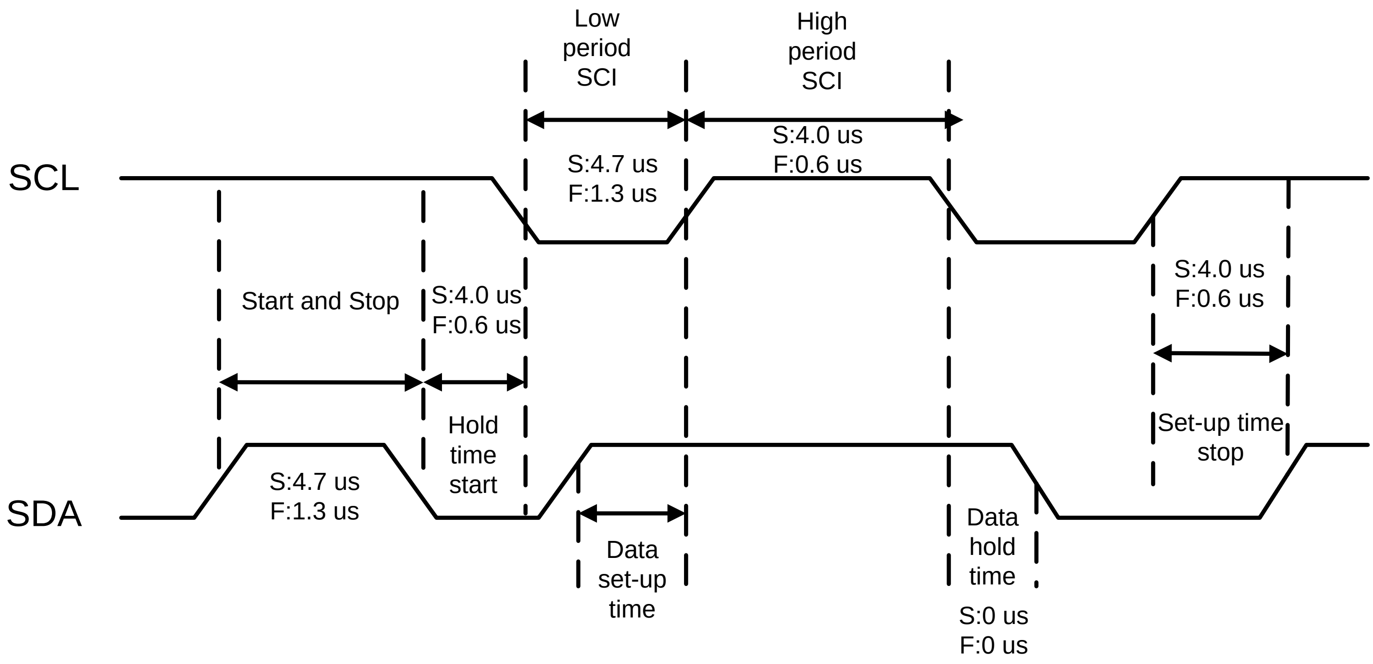


Figure 23-8 Timing on the SCL and SDA

Table 23-13 I2C AC Characteristics

Time	I2C – master mode (CR<7)		I2C – master mode (CR=7)	
tHD:STA	scl/4	min(15 clk)	scl/4	(2 bclk)
tLOW	scl/2	min(30 clk)	scl/2	(4 bclk)
tHIGH	scl/2	min(30 clk)	scl/2	(4 bclk)
tSU:STA	scl/4	min(15 clk)	scl/2 – if (scl/4<7 clk)	
			scl/4 – others	
tHD:DAT	6*clk	(6 clk)	6*clk	(6 clk)
tSU:DAT	1*clk (-for first bit)*	(1 clk)	1*clk (-for first bit)*	(1 clk)
	scl/2 - 6*clk	min(24 clk)	scl/2 - 6*clk	min(1clk)
tSU:STO	scl/4 + 7*clk	min(22 clk)	min(bclk +9)	
tBUF	(¾ scl)+9*clk	min(54 clk)	min (¾ scl)	

*- is a case when write to data register is close to the scl rising edge of the first bit data byte.

clk: APB clock period

bclk: Timer 3’s overflow period

scl: I2C clock period

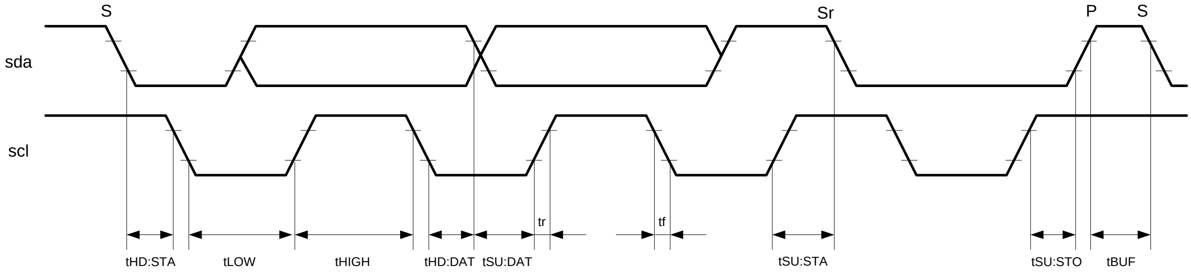


Figure 23-9 AC Timing of I2C Controller

23.6.6. The Resolution for SDA Pin Lock-Status

In the process of I2C communication, when the chip is reset (software reset, WDT reset, external reset), it may cause the I2C data line (SDA is locked in low level) is stuck LOW, the master should send nine clock pulses. The device that held the bus LOW should release it within those nine clocks. If I2C is not stuck LOW in the current time, the nine clock pulses add by user will not affect I2C usage.

23.7. Firmware Flow

23.7.1. Master Transmit Mode

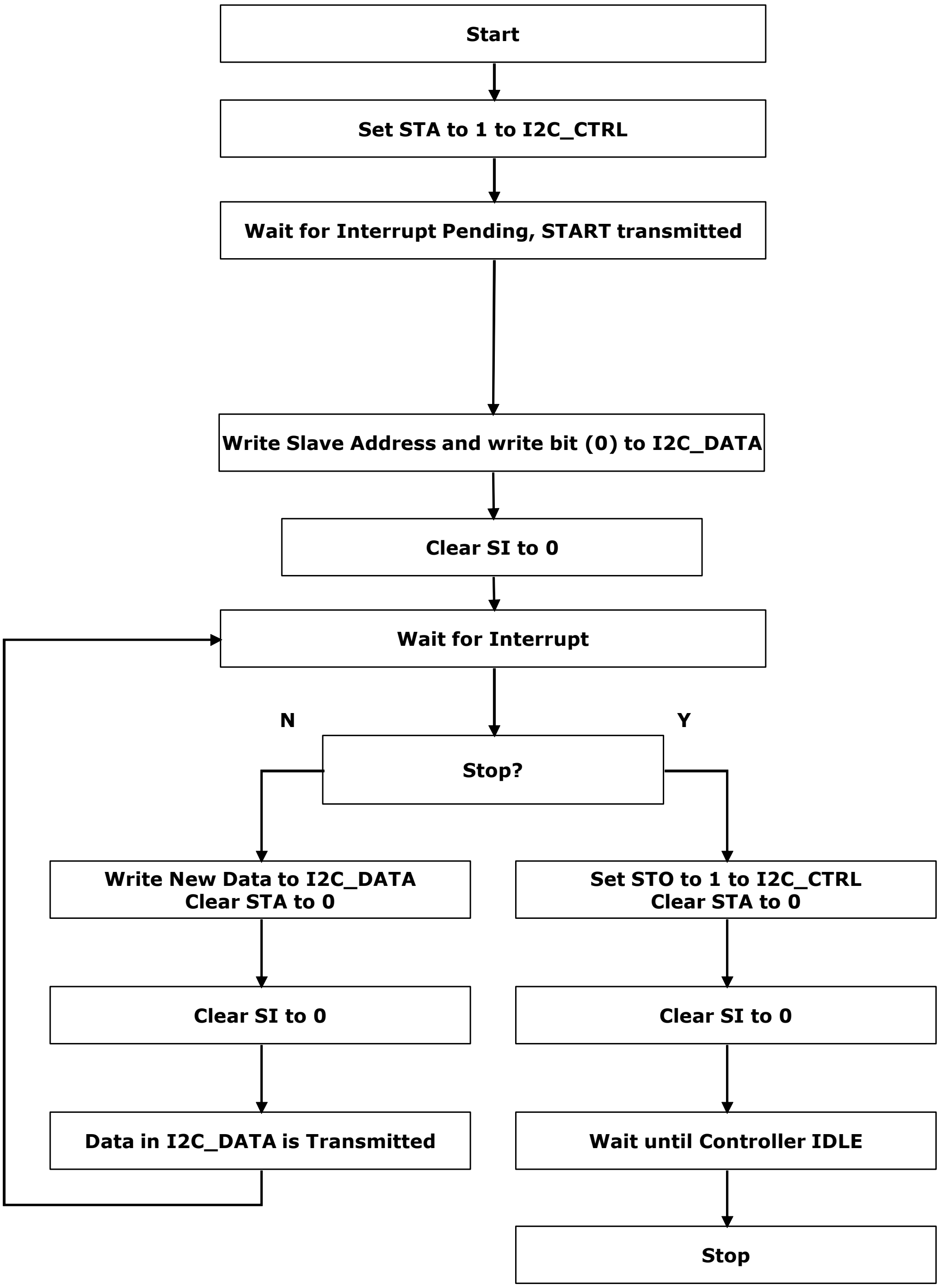

Start
Set STA to 1 to I2C_CTRL
Wait for Interrupt Pending, START transmitted
Write Slave Address and write bit (0) to I2C_DATA
Clear SI to 0
Wait for Interrupt
N
Y
Stop?
Write New Data to I2C_DATA
Clear STA to 0
Clear SI to 0
Data in I2C_DATA is Transmitted
Set STO to 1 to I2C_CTRL
Clear STA to 0
Clear SI to 0
Wait until Controller IDLE
Stop

Figure 23-10 Operations for Master Transmitter Mode

23.7.2. Master Receive Mode

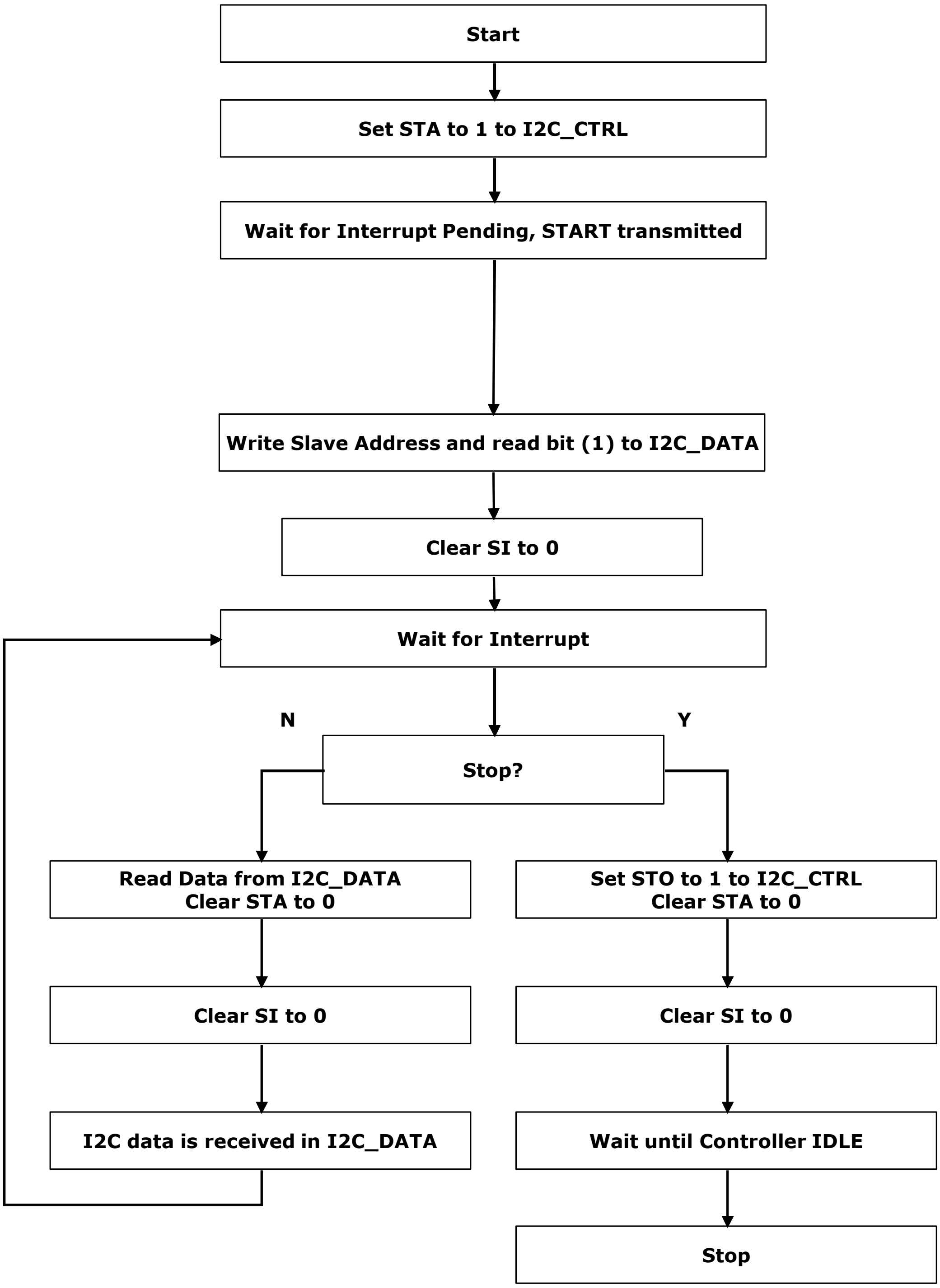


Figure 23-11 Operations for Master Receiver Mode

23.7.3. Slave Transmit Mode

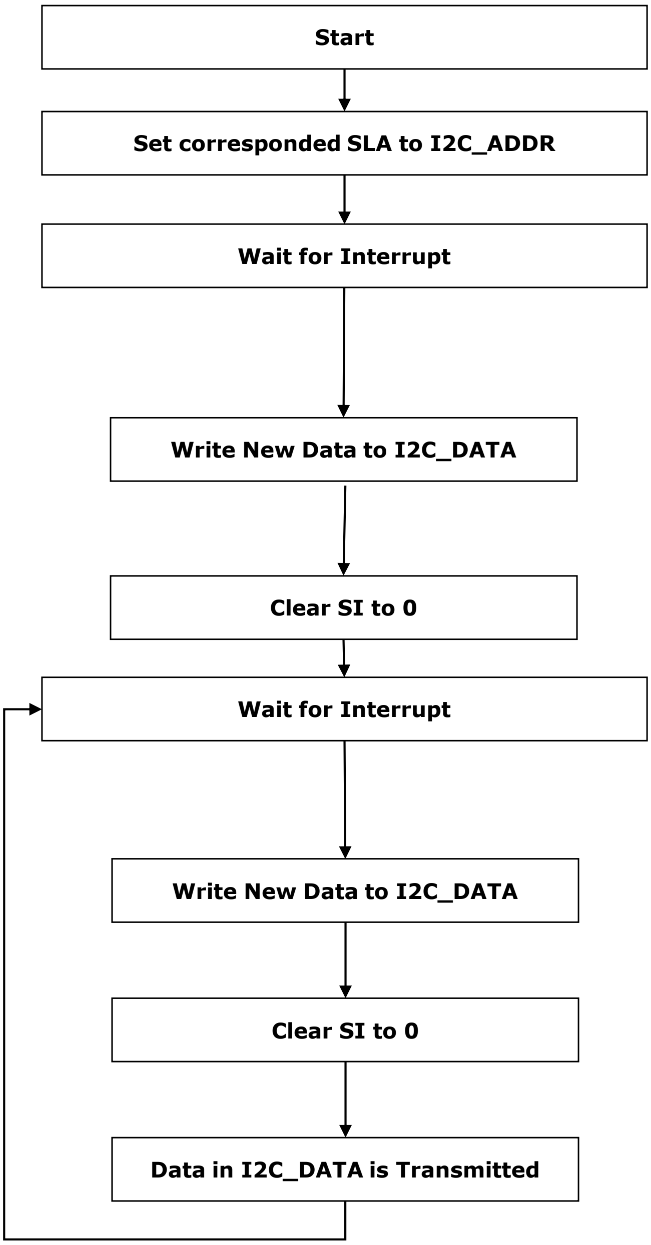

Start
Set corresponded SLA to I2C_ADDR
Wait for Interrupt
Write New Data to I2C_DATA
Clear SI to 0
Wait for Interrupt
Write New Data to I2C_DATA
Clear SI to 0
Data in I2C_DATA is Transmitted

Figure 23-12 Operations for Slave Transmitter Mode

23.7.4. Slave Receive Mode

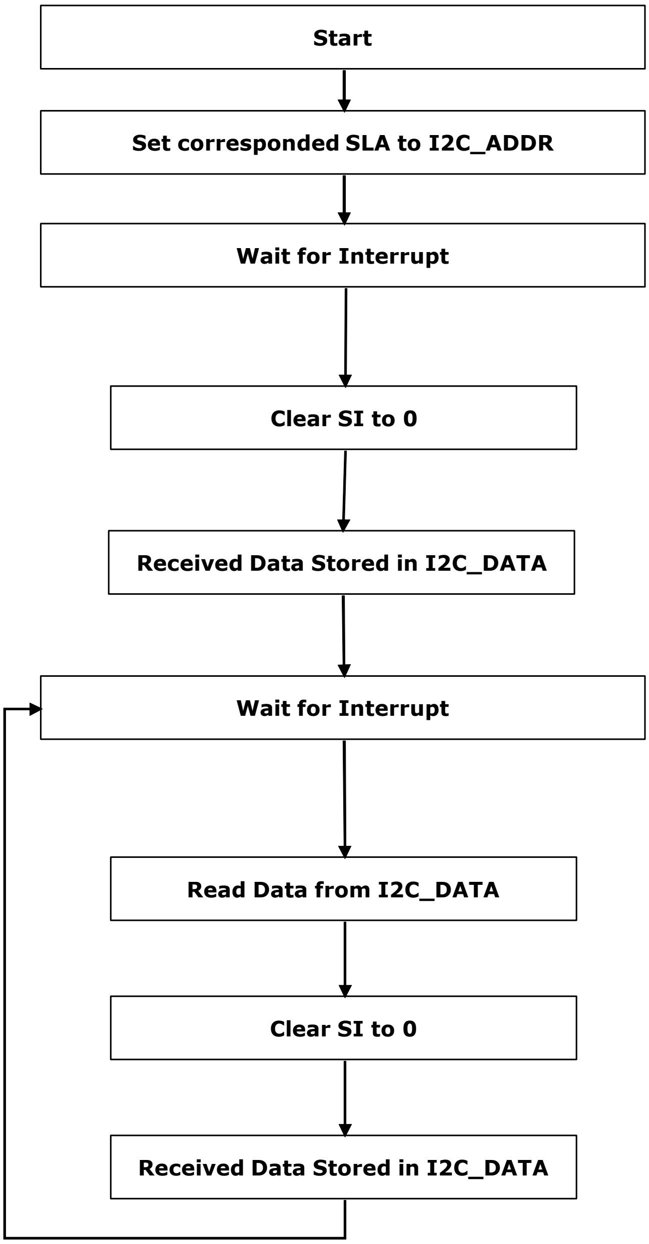

Start
Set corresponded SLA to I2C_ADDR
Wait for Interrupt
Clear SI to 0
Received Data Stored in I2C_DATA
Wait for Interrupt
Read Data from I2C_DATA
Clear SI to 0
Received Data Stored in I2C_DATA

Figure 23-13 Operations for Slave Receiver Mode

24. Interrupt Controller

24.1. Introduction

Any interrupt can wake up the system from IDLE, some of them can wake up the system from sleep, some of them can wake up the system from deep sleep.

24.2. Feature

24.3. Interrupt Sources

Table 24-1 Interrupt sources

Item	Vector address	Interrupt Nom.	Description	Enable bit of peripheral event	Flag of peripheral event	Wake-up source	
						Deep Sleep	Sleep
NMI	00000008h	-14	NMI				
HardFault	0000000Ch	-13	HardFault				
SVCall	0000002Ch	-5	SVCall				
PendSV	00000038h	-2	PendSV				
SysTick	0000003Ch	-1	SysTick				
PMU	00000040h	0	IOA0~15	PMU_CONTROL.0 and PMU_IOAWKUEN.0~15	PMU_IOAINTSTS.0~15	V	V
			32K crystal is removed or broken	PMU_CONTROL.2	PMU_STS.0	V	V
			6M crystal is removed or broken	PMU_CONTROL.3	PMU_STS.1		
RTC	00000044h	1	Reserved.	RTC_INTEN.0	RTC_INTSTS.0	V	V

			illegal time format	RTC_INTEN.1	RTC_INTSTS.1	V	V
			multi-second period is reach	RTC_INTEN.2	RTC_INTSTS.2	V	V
			multi-minute period is reach	RTC_INTEN.3	RTC_INTSTS.3	V	V
			multi-hour period is reach	RTC_INTEN.4	RTC_INTSTS.4	V	V
			mid-night (00:00) is reach	RTC_INTEN.5	RTC_INTSTS.5	V	V
			32K counter period is reach	RTC_INTEN.6	RTC_INTSTS.6	V	V
			auto calibration is done	RTC_INTEN.7	RTC_INTSTS.7	V	V
			illegal write to CE register	RTC_INTEN.8	RTC_INTSTS.8		
U32K0~1	00000048h 0000004Ch	2\3	Receiver data input	U32Kx_CTRL1.0	U32Kx_STS.0	V	V
			Receive parity error	U32Kx_CTRL1.1	U32Kx_STS.1	V	V
			Receive buffer overrun	U32Kx_CTRL1.2	U32Kx_STS.2	V	V
I2C	00000050h	4	Serial Interrupt	I2C_CTRL2.0	I2C_CTRL.3		
SPI1~2	00000054h \000000ACh	5\27	SPI Transmit	SPIx_TXSTS.14	SPIx_TXSTS.15		
			SPI Receive	SPIx_RXSTS.14	SPIx_RXSTS.15		
UART0~5	00000058h ~ 0000006Ch	6\7\8\9\10\11	Receive	UARTx_CTRL.3	UARTx_INTSTS.1		
			Transmit overrun	UARTx_CTRL.4	UARTx_INTSTS.2		
			Receive overrun	UARTx_CTRL.5	UARTx_INTSTS.3		
			Receive parity error	UARTx_CTRL.7	UARTx_INTSTS.4		
			Transmit done	UARTx_CTRL.8	UARTx_INT		

					STS.5		
ISO78160~1	00000070h ~ 00000074h	12\13	Receive	ISO7816x_CFG.5	ISO7816x_INFO.5		
			Transmit	ISO7816x_CFG.6	ISO7816x_INFO.6		
			Receive overrun	ISO7816x_CFG.7	ISO7816x_INFO.7		
Timer0~3	00000078h ~ 00000084h	14\15\16\17	Timer x overflow	TMRx_CTRL.3	TMRx_INT.0		
PWM0~3	00000088h ~000094h	18\19\20\21	PWM timer overflow	PWMx_CTL.1	PWMx_CTL.0		
			Compare 0	PWMx_CCTL0.4	PWMx_CCTL0.0		
			Compare 1	PWMx_CCTL1.4	PWMx_CCTL1.0		
			Compare 2	PWMx_CCTL2.4	PWMx_CCTL2.0		
DMA	00000098h	22	Channel 0 package end	DMA_IE.0	DMA_STS.0		
			Channel 1 package end	DMA_IE.1	DMA_STS.1		
			Channel 2 package end	DMA_IE.2	DMA_STS.2		
			Channel 3 package end	DMA_IE.3	DMA_STS.3		
			Channel 0 frame end	DMA_IE.4	DMA_STS.4		
			Channel 1 frame end	DMA_IE.5	DMA_STS.5		
			Channel 2 frame end	DMA_IE.6	DMA_STS.6		
			Channel 3 frame end	DMA_IE.7	DMA_STS.7		
			Channel 0 data abort	DMA_IE.8	DMA_STS.8		

			Channel 1 data abort	DMA_IE.9	DMA_STS.9		
			Channel 2 data abort	DMA_IE.10	DMA_STS.10		
			Channel 3 data abort	DMA_IE.11	DMA_STS.11		
FLASH	0000009Ch	23	checksum error	FLASH_CTRL.2	FLASH_INT.0		
ANA	000000A0h	24	manual ADC conversion done	ANA_INTEN.0	ANA_INTSTS.0		
			auto ADC conversion done	ANA_INTEN.1	ANA_INTSTS.1		
			COMP1 rising or falling	ANA_INTEN.2	ANA_INTSTS.2	V	V
			COMP2 rising or falling	ANA_INTEN.3	ANA_INTSTS.3	V	V
			VDDALARM rising or falling	ANA_INTEN.7	ANA_INTSTS.7	V	V
			VDCIN rising or falling	ANA_INTEN.8	ANA_INTSTS.8	V	V
			AVCCLV rising or falling	ANA_INTEN.10	ANA_INTSTS.10	V	V
			VDCINDROP is 0 and the entry of sleep or deep-sleep modes are detected	ANA_INTEN.11	ANA_INTSTS.11	V	V
			ANA_REGx error	ANA_INTEN.12	ANA_INTSTS.12	V	V
			TADC change over threshold	ANA_INTEN.13	ANA_INTSTS.13	V	V

25. MISC Controller

25.1. Introduction

The MISC controller is used to control some special function of V85X3. There are two MISC controllers inside V85X3, one is in core domain (MISC controller) which will be power-off during sleep and deep-sleep mode. The setting in MISC controller will be reset after wake-up from sleep or deep-sleep mode, programmer should restore the setting manually after wake-up from these two states. Another one (MISC2 controller) is in retention domain which will be power-off at deep-sleep mode. The setting in MISC2 controller will be reset after wake-up from deep-sleep mode, programmer should restore the setting manually after wake-up from deep-sleep mode.

25.2. Feature

--Clock control of each sub-module

--Clock divider of AHBCLK and APBCLK.

--FLASH program tick control

--IR duty control.

--SRAM parity check interrupt control.

25.3. Block Diagram

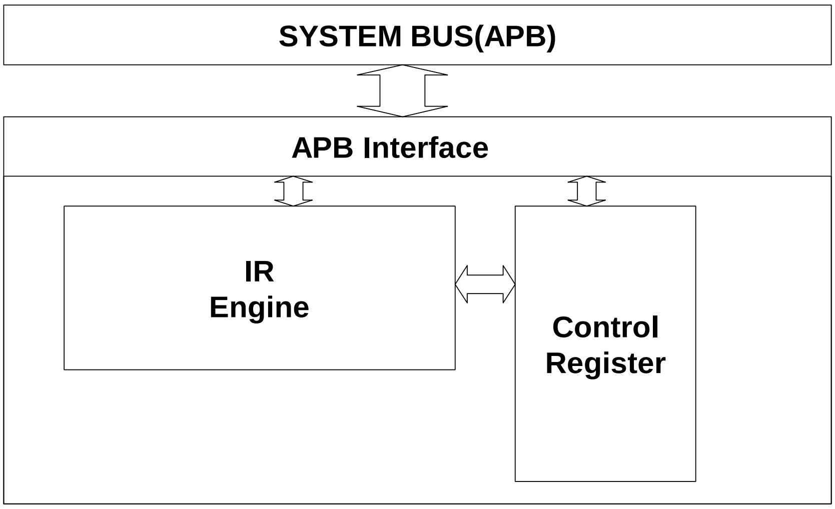


Figure 25-1 Functional Block Diagram of MISC Controller

25.4. Register Location

Table 25-1 Register Location of MISC Controller (MISC Base: 0x40013000)

Name	Type	Address	Description	Default
MISC_SRAMINT	R/C	0x0000	SRAM Parity Error Interrupt.	0x00
MISC_SRAMINIT	R/W	0x0004	SRAM initialize register	0x01
MISC_PARERR	R	0x0008	SRAM Parity Error address register	0x0000
MISC_IREN	R/W	0x000C	IR enable control register	0x00
MISC_DUTYL	R/W	0x0010	IR Duty low pulse control register	0x0000
MISC_DUTYH	R/W	0x0014	IR Duty high pulse control register	0x0000
MISC_IRQLAT	R/W	0x0018	Cortex-M0 IRQ latency control register	0x00
MISC_HIADDR	R	0x0020	AHB invalid access address	--
MISC_PIADDR	R	0x0024	APB invalid access address	--

Table 25-2 Register Location of MISC2 Controller (MISC2 Base: 0x40013E00)

Name	Type	Address	Description	Default
MISC2_FLASHWC	R/W	0x0000	FLASH wait cycle register.	0x2100
MISC2_CLKSEL	R/W	0x0004	Clock selection register.	0x0
MISC2_CLKDIVH	R/W	0x0008	AHB clock divider control register	0x00
MISC2_CLKDIVP	R/W	0x000C	APB clock divider control register	0x01
MISC2_HCLKEN	R/W	0x0010	AHB clock enable control register	0x1FF
MISC2_PCLKEN	R/W	0x0014	APB clock enable control register	0xFFFFFFFF

25.5. Register Definition

25.5.1. MISC_SRAMINT Register

Table 25-3 Description of MISC_SRAMINT Register

Bit	Name	Type	Description	Default
31:5	-	-	Reserved.	0

4	LOCKUP	R/C	This bit indicates the CM0 lockup has happened. Write 1 to clear this flag.	0x0
3	PIAC	R/C	This bit indicates that an invalid address access on APB bus is occurred. At the same time, the failure address is latched into MISC_PIADDR. The invalid APB address means not in the region of 0x40010000 ~ 0x40017FFF. If PIACIE is 1, then a NMI will be issued to CM0. Write 1 to clear this flag.	0x0
2	HIAC	R/C	This bit indicates that an invalid address access on AHB bus is occurred. At the same time, the failure address is latched into MISC_HIADDR. The invalid AHB address means not in the region of FLASH or SRAM or IO. If HIACIE is 1, then a NMI will be issued to CM0. Write 1 to clear this flag.	0x0
1	-	-	Reserved.	0
0	PERR	R/C	This bit indicates that a SRAM parity error is happened during the SRAM read process. If PERRIE is 1, then a NMI will be issued to CM0. Write 1 to clear this flag.	0x0

25.5.2. MISC_SRAMINIT Register

Table 25-4 Description of MISC_SRAMINIT Register

Bit	Name	Type	Description	Default
31:8	-	-	Reserved.	0
7	LOCKIE	R/W	CM0 lockup NMI enable register.	0x0
6	PIACIE	R/W	APB invalid address access NMI enable register.	0x0
5	HIACIE	R/W	AHB invalid address access NMI enable register.	0x0
4:3	-	-	Reserved.	0
2	INIT	R/W	SRAM initialize register, set this register to 1 will initialize the SRAM with all zero value with correct parity. This bit will be clear to 0 automatically, during the initialize time, it is not allowed for access of any master on the bus (CPU or DMA), wrong data maybe get during this period.	0x0
1	PERRIE	R/W	SRAM parity error NMI enable register.	0x0
0	PEN	R/W	Parity check enable register. When this bit is 1, all the write access to internal SRAM will also write the parity information into additional parity buffer. When doing	0x1

			SRAM read, automatically parity check will be done and generate the parity error interrupt when parity check fail. By default, this function is turned on, so no need special effort on the software side. But if CPU or DMA access some un-initialize region, parity may happen because the parity information didn't exist in those non-initialize area. At this moment, programmer can use INIT bit to do SRAM initialize automatically.	

25.5.3. MISC_PARERR Register

Table 25-5 Description of MISC_PARERR Register

Bit	Name	Type	Description	Default
31:12	-	-	Reserved.	0
11:0	PEADDR	R	Parity error address. This register store the information of parity error address, when PE NMI is happened, programmer can check this register to know which SRAM address has defect bit. SRAM parity error address =0x20000000+4* PEADDR.	--

25.5.4. MISC_IREN Register

Table 25-6 Description of MISC_IREN Register

Bit	Name	Type	Description	Default
31:6	-	-	Reserved.	0
5:0	IREN	R/W	IR enable control register. Each bit in this register corresponded to 1 UART TX channel. When IREN[x] is set to 1, it means UART TX[x] will be modulated with IR pulse to output.	0x00

25.5.5. MISC_DUTYL Register

Table 25-7 Description of MISC_DUTYL Register

Bit	Name	Type	Description	Default
31:16	-	-	Reserved.	0
15:0	DUTYL	R/W	IR low pulse width control register. The low pulse width will be (DUTYL + 1)*APBCLK period.	0x0000

25.5.6. MISC_DUTYH Register

Table 25-8 Description of MISC_DUTYH Register

Bit	Name	Type	Description	Default
31:16	-	-	Reserved.	0
15:0	DUTYH	R/W	IR high pulse width control register. The high pulse width will be (DUTYH + 1)*APBCLK period.	0x0000

25.5.7. MISC_IRQLAT Register

Table 25-9 Description of MISC_IRQLAT Register

Bit	Name	Type	Description	Default
31:10	-	-	Reserved.	0
9	NOHARDFAULT	R/W	This register is used to disable the hard fault generation to CPU. 0: Enable hard fault generation when bus error is happened. 1: Disable hard fault generation when bus error is happened, the HIAL hard-fault is not able to be disabled by this bit. When CM0 detect hard fault is happened, it will jump to the hard fault service routine. After it complete the hard fault service, it will jump back to normal code and execute the same instruction again. So if the hard fault happens again, it will stop in this loop and never come out. This register is used for CPU to temporary disable the hard fault generation.	0x0
8	LOCKRESET	R/W	This register is used to control if the lockup will issue a system reset. 0: Disable reset generation of CM0 lockup. 1: Enable reset generation of CM0 lockup.	0x0
7:0	IRQLAT	R/W	This register is used to control the Cortex-M0 IRQ latency. The Cortex-M0 processor supports zero jitter interrupt latency for zero wait-state memory. IRQLAT specifies the minimum number of cycles between an interrupt that becomes pended in the NVIC, and the vector fetch for that interrupt being issued on the	0x00

			AHB-Lite interface. If this bus is set to 0, interrupts are taken as quickly as possible. For zero jitter in a zero wait state memory system, set this bus to at least a decimal value of 13. For non-zero wait state memory, zero jitter can be achieved with a higher value on IRQLAT.	

25.5.8. MISC2_FLASHWC Register

Table 25-10 Description of MISC2_FLASHWC Register

Bit	Name	Type	Description	Default
31:14	-	-	Reserved.	0
13:8	1USCYCLE	R/W	This register is used for FLASH controller to calculate 1ustick from AHB clock 1ustick = (AHB clock period)*(1USCYCLE+1) This setting is related to the wake-up time of FLASH, and the programming time of FLASH. FLASH wake-up time =1ustick *10. It must meet 1ustick >=1 μs. For example, the clock frequency of AHB is 26.2144MHz. In order to ensure the minimum wake-up time, 1USCYCLE should be set to 26. So, the wake-up time of FLASH is 27 / 26214400 * 10, which is about 10 μs. For example, the clock frequency of AHB is 32.768KHz. In order to ensure the minimum wake-up time, 1USCYCLE should be set to 0. So, the wake-up time of FLASH is 1 / 32768 * 10, which is about 305 μs.	0x21
7:0	-	-	Reserved.	0x00

25.5.9. MISC2_CLKSEL Register

Table 25-11 Description of MISC2_CLKSEL Register

Bit	Name	Type	Description	Default
31:3	-	-	Reserved.	0
2:0	CLKSEL	R/W	This register is used to control AHB clock source. 0: RCH (6.5MHz RC) 1: XOH (6.5536MHz XTAH). 2: PLLH.	0x0

			3: RTCCLK (controlled by RTCCLK_SEL in PMU_CONTROL register). 4: PLLL. Before clock select to one of the clock source, programmer should enable the corresponded module first by setting PMU_CONTROL register.	

25.5.10. MISC2_CLKDIVH Register

Table 25-12 Description of MISC2_CLKDIVH Register

Bit	Name	Type	Description	Default
31:8	-	-	Reserved.	0
7:0	CLKDIVH	R/W	This register is used to control AHB clock divider. 0: Clock source divide by 1 1: Clock source divide by 2. 2: Clock source divide by 3. .... 255: Clock source divide by 256.	0x00

25.5.11. MISC2_CLKDIVP Register

Table 25-13 Description of MISC2_CLKDIVP Register

Bit	Name	Type	Description	Default
31:8	-	-	Reserved.	0
7:0	CLKDIVP	R/W	This register is used to control APB clock divider. 0: AHB clock divide by 1. 1: AHB clock divide by 2. 2: AHB clock divide by 3. .... 255: AHB clock divide by 256.	0x01

25.5.12. MISC2_HCLKEN Register

Table 25-14 Description of MISC2_HCLKEN Register

Bit	Name	Type	Description	Default
31:9	-	-	Reserved.	0
8:0	HCLKEN	R/W	This register is used to control clock enable of each AHB module. The corresponded module can be turned-off only when its function is not been used. Refer to Table 25-15 for detail about each module. 0: Disable. 1: Enable.	0x1FF

Table 25-15 HCLK Clock Enable of Each Module

Bit	Module	Note
0	--	
1	Arbiter & Bus Matrix	Shouldn't off when CPU or DMA is active.
2	FLASH Controller	Shouldn't off
3	SRAM Controller	Shouldn't off
4	DMA Controller	
5	GPIO Controller	
6	LCD Controller	
7	--	
8	CRYPT Controller	

25.5.13. MISC2_PCLKEN Register

Table 25-16 Description of MISC2_PCLKEN Register

Bit	Name	Type	Description	Default
31:0	PCLKEN	R/W	This register is used to control clock enable of each APB module. The corresponded module can be turned-off only when its function is not been used. Refer to Table 25-17 for detail about each module. 0: Disable.	0xFFFFFFFF

			1: Enable.	

Table 25-17 PCLK clock Enable of Each Module

Bit	Module	Note
0	AHB2APB Bridge	Shouldn't off when CPU or DMA is access APB peripheral.
1	DMA Controller	
2	I2C	
3	SPI1	
4	UART0	
5	UART1	
6	UART2	
7	UART3	
8	UART4	
9	UART5	
10	ISO78160	
11	ISO78161	
12	Timer	
13	MISC	
14	MISC2	
15	PMU	
16	RTC	
17	ANA	
18	U32K 0	
19	U32K 1	
20	Reserved	
21	SPI2	
31:22	Reserved	

26. CRYPT Controller

26.1. Introduction

The CRYPT controller is used to accelerate the ECC's sign and verify process speed. The major feature of CRYPT controller is the VLI (variable length integer) multiply, add, sub, and shift. It can achieve overall about 4 times faster than pure software process. Every encryption algorithm use VLI can use this hardware to accelerate the process speed. The CRYPT controller can access internal SRAM directly without affect the M0's access, it can also generate the carry or borrow bit automatically.

26.2. Feature

--Support VLI from 32 bits to 512 bits.

--VLI multiplier.

--VLI add and carry bit generation.

--VLI substrate and borrow bit generation.

--VLI right shift 1 bit.

--Internal SRAM direct access.

26.3. Block Diagram

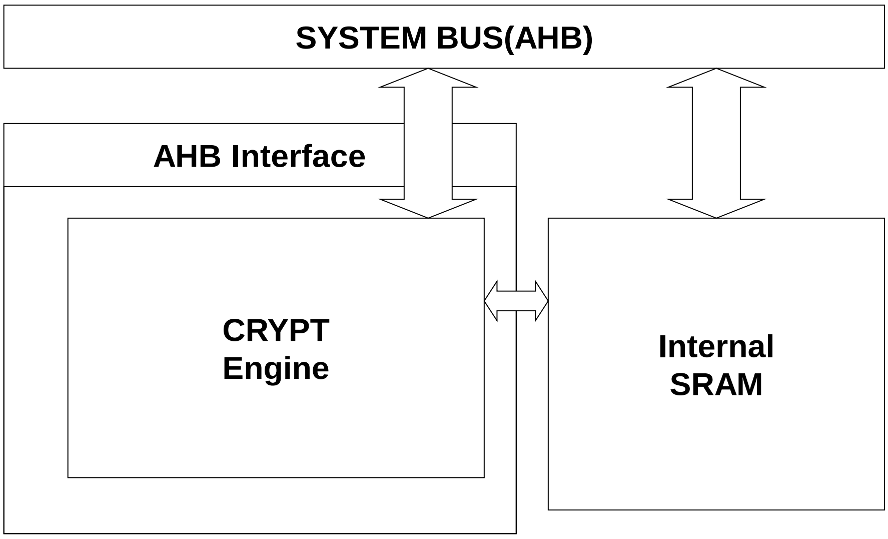


Figure 26-1 Functional Block Diagram of CRYPT Controller

26.4. Register Location

Table 26-1 Register Location of CRYPT Controller (MISC Base: 0x40006000)

Name	Type	Address	Description	Default
CRYPT_CTRL	R/W	0x0000	CRYPT control register	0x0000
CRYPT_PTRA	R/W	0x0004	CRYPT pointer A	0x0000
CRYPT_PTRB	R/W	0x0008	CRYPT pointer B	0x0000
CRYPT_PTRO	R/W	0x000C	CRYPT pointer O	0x0000
CRYPT_CARRY	R	0x0010	CRYPT carry/borrow bit register	0x0

26.5. Register Definition

26.5.1. CRYPT_CTRL Register

Table 26-2 Description of CRYPT_CTRL Register

Bit	Name	Type	Description	Default
31:16	-	-	Reserved.	0
15	NOSTOP	R/W	This register is used to control if the CPU will be stop by CRYPT engine when the CRYPT engine is busy and CPU read or write CRYPT engine register. 0: Stop CPU when CRYPT engine is busy. 1: No stop CPU when CRYPT engine is busy. This register only affect the behavior when CPU access the CRYPT register, if CPU didn't access the crypt register, this bit has no effect.	0x0
14:12	-	-	Reserved.	0
11:8	LENGTH	R/W	This bit is used to control the VLI length of current operation. Programmer can set this register together with write 1 to ACT bit, but should not change this register when ACT is 1. 0: 32 bits VLI 1: 64 bits VLI 2: 96 bits VLI ...... 15: 512 bits VLI	0x0
7	-	-	Reserved.	0
6:4	MODE	R/W	This register controls the operation mode of crypt engine. Programmer can set this register together with write 1 to ACT bit, but should not change this register when ACT is 1. 0: Multiply mode, *PTRO = *PTRA x *PTRB 1: Add mode, *PTRO = *PTRA + *PTRB 2: Sub mode, *PTRO = *PTRA - *PTRB 3: RSHIFT1 mode, *PTRO = (*PTRA>>1) 4~7: Reserved.	0x0
3:1	-	-	Reserved.	0
0	ACT	R/W	Write 1 to this bit will start an operation specified in the MODE register. And this bit will be cleared automatically after the operation is done. Write 0 to this bit has no effect.	0x0

26.5.2. CRYPT_PTRA Register

Table 26-3 Description of CRYPT_PTRA Register

Bit	Name	Type	Description	Default
31:15	-	-	Reserved.	0
14:0	PTRA	R/W	This is the PTRA register of CRYPT controller. The value here defines an address in the SRAM (byte unit). The data in this address will be read out to do the CRYPT calculation. Since the CRYPT control only support 32 bits process, the PTRA[1:0] should be 0 for all the time.	0x0000

26.5.3. CRYPT_PTRB Register

Table 26-4 Description of CRYPT_PTRB Register

Bit	Name	Type	Description	Default
31:15	-	-	Reserved.	0
14:0	PTRB	R/W	This is the PTRB register of CRYPT controller. The value here defines an address in the SRAM (byte unit). The data in this address will be read out to do the CRYPT calculation. Since the CRYPT control only support 32 bits process, the PTRB[1:0] should be 0 for all the time.	0x0000

26.5.4. CRYPT_PTRO Register

Table 26-5 Description of CRYPT_PTRO Register

Bit	Name	Type	Description	Default
31:15	-	-	Reserved.	0
14:0	PTRO	R/W	This is the PTRO register of CRYPT controller. The value here defines an address in the SRAM (byte unit). The CRYPT engine will write calculation result into this address. Since the CRYPT control only support 32 bits process, the PTRO[1:0] should be 0 for all the time.	0x0000

26.5.5. CRYPT_CARRY Register

Table 26-6 Description of CRYPT_CARRY Register

Bit	Name	Type	Description	Default
31:1	-	-	Reserved.	0
0	CARRY	R	This bit represent the carry bit after add operation is done. The bit represent borrow bit after sub operation is done. Programmer can read this register immediately after the ACT bit is clear to 0.	0x0

26.6. Application Note

26.6.1. Data Format

The VLI is a positive integer with 32~512 bits. So all the operations here are unsigned processes. The following table shows the data sequence in the SRAM.

Address	Data
PTR + 0	VLI[31:0]
PTR + 4	VLI[63:32]
PTR + 8	VLI[95:64]
PTR + 12	VLI[127:96]
......	......
PTR + 60	VLI[511:480]

When different kind of LENGTH mode is selected, only the selected range of VLI will be used as input data. The following table shows the valid VLI bits under different LENGTH setting.

LENGTH	Data
0	VLI[31:0]
1	VLI[63:0]
2	VLI[95:0]
3	VLI[127:0]
......	......
15	VLI[511:0]

26.6.2. Operation Detail

For each operation, they will have different behavior on many ways, like the process cycles and the output width. The following tables shows detail of each mode.

	MULT	ADD	SUB	RSHIFT1
Operation	*PTRO = *PTRA x *PTRB	*PTRO = *PTRA + *PTRB	*PTRO = *PTRA - *PTRB	*PTRO = (*PTRA>>1)
Output length	2*input length	input length	input length	input length
CARRY bit	X	0: Output not overflow. 1: Output overflow	0: *PTRA > *PTRB 1: *PTRA < *PTRB	X
LENGTH	**Operation Cycles**			
0	8	6	6	6
1	17	8	8	8
2	32	12	12	10
3	53	14	14	12
4	80	18	18	14
5	113	20	20	16
6	152	24	24	18
7	197	26	26	20
8	248	30	30	22
9	305	32	32	24
10	368	36	36	26
11	437	38	38	28
12	512	42	42	30
13	593	44	44	32
14	680	48	48	34
15	773	50	50	36

By default, during the operation cycle, if the CPU accesses any of the register of CRYPT engine, the CPU will be halted until the operation is done. This is to prevent the configuration change during the operation. So if there is any high priority task in the system, it may block until the CPU is released by CRYPT engine. Set NOSTOP bit in the CRYPT_CTRL register to prevent this kind of situation. Under this condition, programmer should take care not to change the CRYPT configuration during the operation busy time.

Since the CRYPT only supports operations in the SRAM, when one of the input is not in the SRAM (ex. In FLASH or ROM), it is necessary to copy it into SRAM before do any operation.

27. Debug Features

V85X3 uses the Cortex-M0 core, which contains the hardware debug module.

27.1. Feature

The Cortex-M0 processor supports a number of useful debug features:

--Halting, resuming, and single stepping of program execution

--Access to processor core registers and special registers

--Hardware breakpoints (up to four comparators)

--Software breakpoints (BKPT instruction)

--Data watch points (up to two comparators)

--On-the-fly memory access (system memory can be accessed without stopping the processor)

--PC sampling for basic profiling

--Support of serial wire debug (SWD) protocol

27.2. SWD Port

Table 27-1 Special Function of SW Port

MODE	Function 1	Function 2
Debug (PIN MODE is L)	SWCLK	SWDIO
Normal (PIN MODE is H)	LCDSEG54/IOA0	LCDSEG53/IOA1

28. Cortex-M0 Core Brief Description

The ARM Cortex-M0 processor is designed to meet the needs of modern ultra-low-power microcontroller units (MCUs) and mixed-signal devices. The ARM Cortex-M0 processor is as small as an 8-bit or 16-bit processor, but it is a full 32-bit processor that incorporates advanced technologies with many compelling benefits over 8-bit or 16-bit devices. The ARM Cortex-M0 processor can achieve high Energy Efficiency and Code Density.

28.1. CMSIS Function Specification

Table 28-1 CMSIS Function

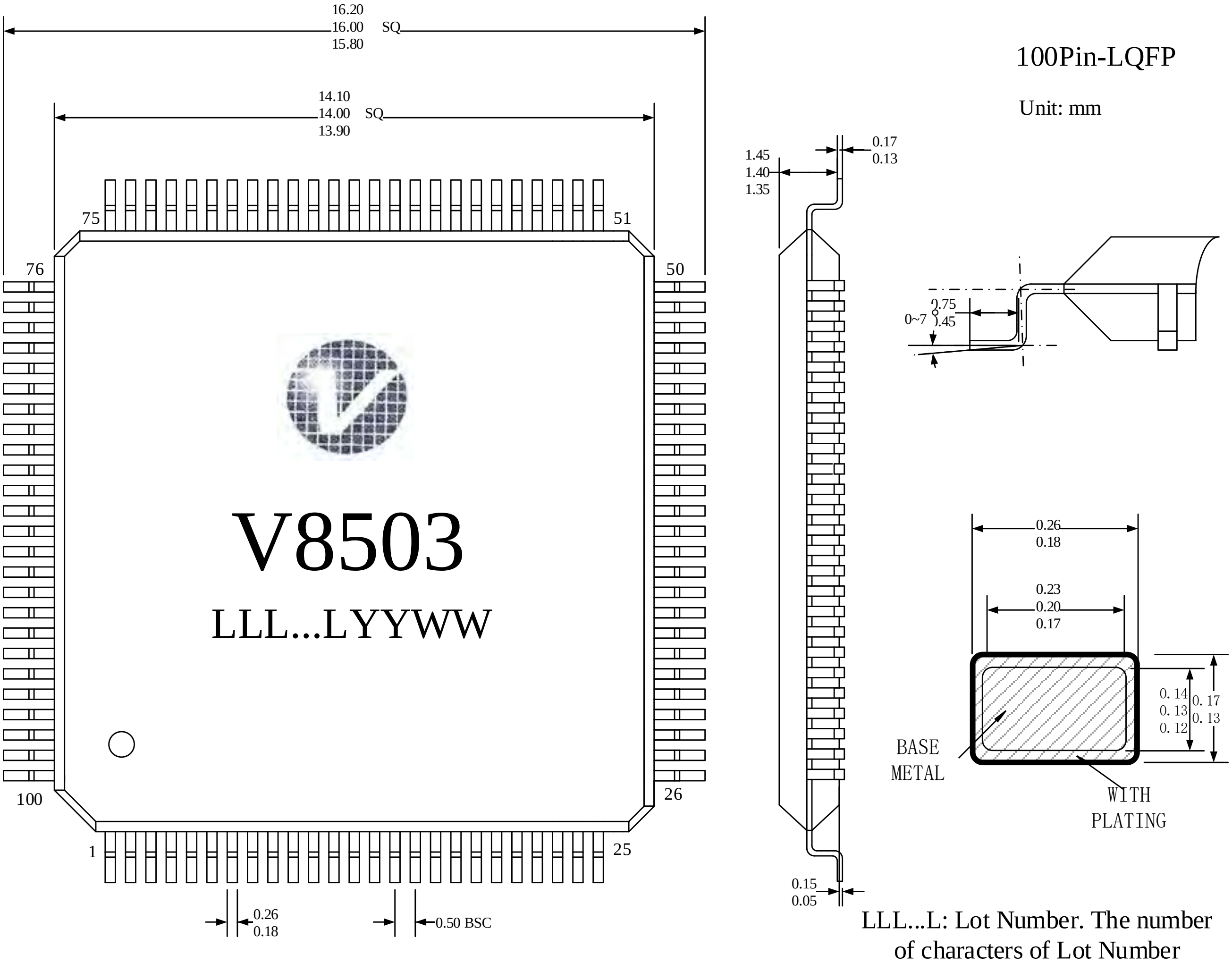
function	specification
void NVIC_EnableIRQ(IRQn_Type IRQn);	Enable an interrupt. This function does not apply to system exceptions.
void NVIC_DisableIRQ(IRQn_Type IRQn);	Disable an interrupt. This function does not apply to system exceptions.
void VIC_SetPendingIRQ(IRQn_Type IRQn);	Set the pending status of an interrupt. This function does not apply to system exceptions.
void NVIC_ClearPendingIRQ(IRQn_Type IRQn);	Clear the pending status of an interrupt. This function does not apply to system exceptions.
uint32_t NVIC_GetPendingIRQ(IRQn_Type IRQn);	Obtain the interrupt pending status of an interrupt. This function does not apply to system exceptions.
void NVIC_SetPriority(IRQn_Type IRQn,uint32_t priority);	Set up the priority level of an interrupt or system exception. The priority level value is automatically shifted to the implemented bits in the priority level register.
uint32_t NVIC_GetPriority(IRQn_TypeIRQn);	Obtain the priority level of an interrupt or system exception. The priority level is automatically shifted to remove unimplemented bits in the priority level values.
void __enable_irq(void);	Clear PRIMASK. Enable interrupts and system exceptions.
void __disable_irq(void);	Set PRIMASK. Disable all interrupts including system exceptions (apart from hard fault and NMI).
uint32_t SysTick_Config(uint32_t ticks);	Initialize and start the SysTick counter and its interrupt; this function programs the SysTick to generate SysTick except ionfor every "ticks" number of core clock cycles.
void NVIC_SystemReset(void);	M0-soft reset.
SCB->SCR |= SCB_SCR_SLEEPDEEP_Msk;	Wait for interrupt (enter sleep mode).

void __WFI(void);	

SCB->SCR &=
(uint32_t)~((uint32_t)SCB_SCR_SLEEPDEEP_Msk);
void __WFI(void);
	Wait for interrupt (enter idle mode).

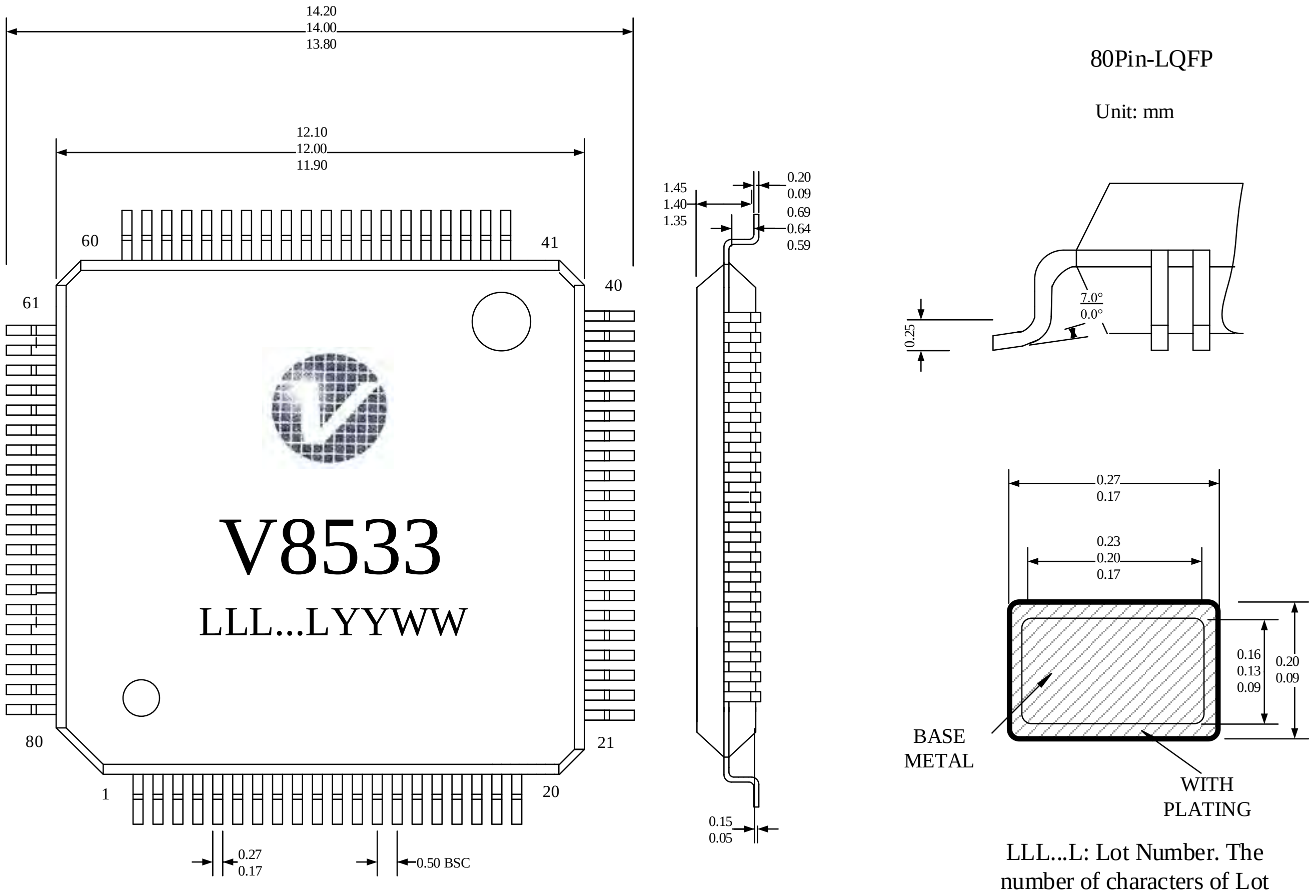
29. Outline Dimensions

29.1. Outline Dimensions_V8503



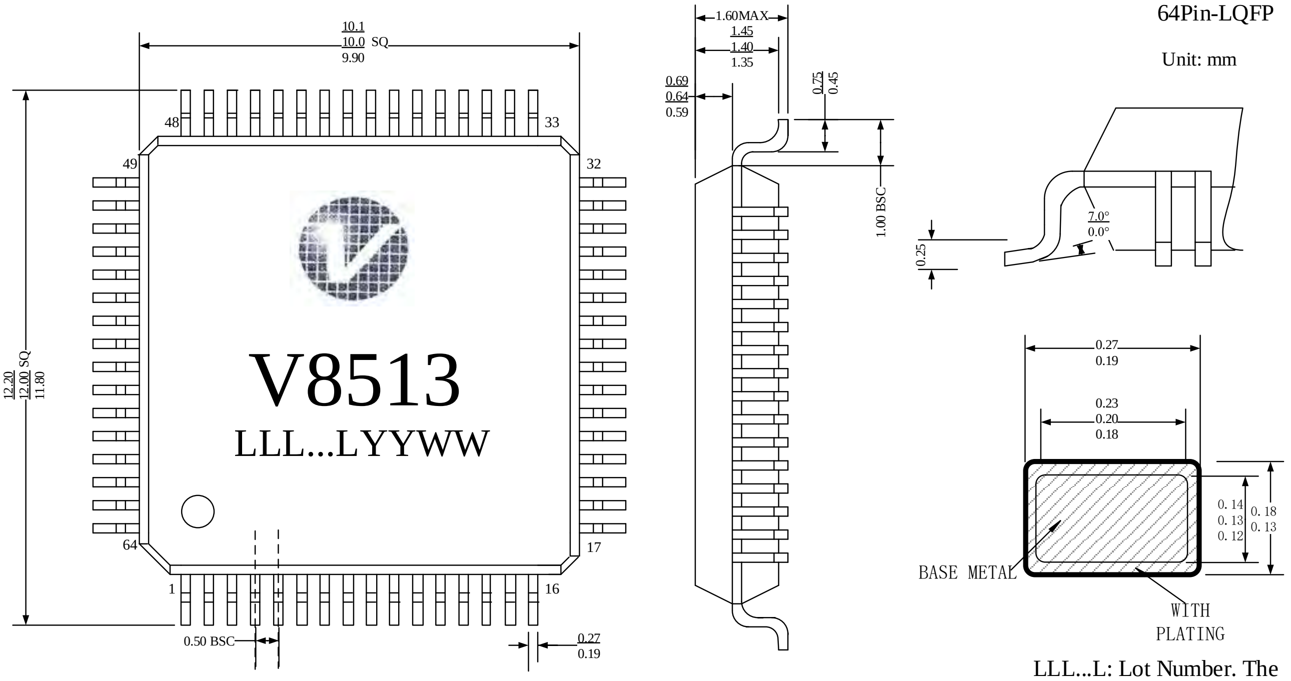
LLL...L: Lot Number. The number of characters of Lot Number varies between 8 to 11.
YY: Year
WW: Week

29.2. Outline Dimensions_V8533



LLL...L: Lot Number. The number of characters of Lot Number varies between 8 to 11.
YY: Year
WW: Week

29.3. Outline Dimensions_V8513



LLL...L: Lot Number. The number of characters of Lot Number varies between 8 to 11.
YY: Year
WW: Week