V94XX(A)
Datasheet

Specifications are subject to change without notice.

Revision History

Date	Version	Description
2021.04.13	V1.0	Initial release.
2021.06.24	V1.1	Add the description of electric energy metering module for V94XX(A) overview.
2021.07.06	V1.2	Modify UART number of V9430
2022.03.10	V1.3	Increase the working voltage of ADC and metering modules Remove the description of Rogowski coil, including register, etc Modify PM_SYS_INTSTS and PM_SYS_INTEN registers，increase the overflow interrupt of high-speed energy accumulator Modify the description of DMA_MODE bit in PM_WAVE_CTRL register (added description: at least one channel of waveform buffer and upload must be opened before enabling DMA transmission). Modify the description of bit3 and bit4 in PM_WAVE_CTRL registers, description of DMA channel manual switch for waveform upload. Modify the function description of UPERIOD and IPERIOD from half cycle unit to cycle unit Modify the description of forced shutdown energy accumulator and CF output function in SYS_MISC register
2022.09.02	V1.4	Add V9400 and V9410

General Description

V94XX (A) is a high-performance, low-power single-phase electric energy metering SoC chip, integrating Cortex-M0 core, analog front-end, electric energy metering module, 256KB FLASH at most (128KB flash for V94XXA), 32KB SRAM (16KB SRAM for V94XXA), UART/SPI/I2C interface, LCD, WDT and RTC. V94XX (A) series supports multiple low power consumption working modes.

The V94XX(A) is integrated with an electric energy metering module which supports the total-wave and fundamental-wave of various modes and supports various power grids to monitor events. Furthermore, the waveform data can be transmitted via Px by SPI protocol, or storage locally through the waveform buffer.

Features

- Working voltage: 2.2V~3.6V

  ADC and metering working voltage: 2.6V ~ 3.6V
- Working Current:
  - -Normal mode without metering: 1.633mA@6.5536MHz
  - -Normal mode with metering: 4.233mA@6.5536MHz
  - Idle mode: 0.379 mA @6.5536MHz
  - Sleep mode (LCD active, RTC_PSCA=0, VDD=3.3Vn): 9.3μA
  - Sleep mode (LCD inactive, RTC_PSCA=0, VDD=3.3Vn): 3.1μA
  - Deep Sleep mode (RTC_PSCA=0, VDD=3.3V): 2.9μA
- Package:
  - LQFP80(V9430)
- Operation Temperature: -40~+85℃
- Storage Temperature: -55~+150℃
- MCU
  - 32 bits Cortex-M0 with maximum 26.2144MHz operation speed.
  - Single cycle multiplier.
  - Standard 2-wires SWD debug interface.
  - 256KB FLASH memory is built in V94XX, and 128KB FLASH memory is built in V94XXA. FLASH has write protection and encryption functions, and supports ISP and IAP
  - V94XX has built-in 32K byte SRAM, and V94XX has built-in 16K byte SRAM. SRAM with parity, data can be retained in shallow sleep mode
  - 256 bytes SRAM with data retention under deep-sleep mode.
  - Support abort exception detection including FLASH check-sum error, SRAM parity error, memory address error and memory align error.
- Interface Controller
  - Maximum 5 UART controllers with parity check.
  - Each UART TX channel can be coupled with IR carrier for IR transmission.
  - Maximum 1 ISO7816 controllers.
  - Maximum 1 SPI master/slave controllers.
  - Maximum 1 I2C master/slave controller.
  - 4 32 bits timers.

- 4 16 bits PWM timers.
- 4 channels DMA controller.
- 128/192/256 bits AES CODEC.
- ECC encrypt/decrypt accelerated engine.
- Dual frame buffer LCD controller
  - ✓ 4COM/6COM/8COM.
  - ✓ 1/3 or 1/4 bias.
  - ✓ Support multi-kinds of scan frequency.
  - ✓ LCD voltage: The default output is about 3.3V. Adjustment range: 2.7~3.6V, 0.06V per step.
- Watch dog timers with programmable period.
- Support multiple wake-up sources under each mode.
- Maximum 75 GPIOs.
- Maximum 14 GPIOs can be external interrupt and wakeup sources under all modes.

- Analog Controller
  - 16bits ADC with 10Ksps.
  - Maximum 9 external input.
  - ADC supports manual sample mode or auto sample mode.
  - Maximum 2 comparators with single end input or differential input.
  - Embedded 32 KHz and 6.5 MHz RCO.
  - Embedded 2 PLLs.
  - Support external 32.768 KHz crystal or 6.5536MHz crystal (optional).
  - Support crystal absent detect for both 32.768 KHz and 6.5536 MHz crystal.
  - Each clock can be selected to be system clock.
  - Support digital clock divider up-to 1/256.
  - Support low voltage detection with programmable level.
  - Support DVCC1 power on reset
- RTC
  - Support 1ppm RTC manual calibration.
- Metering Features
  - 3 independent oversampling Σ/Δ ADCs: one of the ADC (channel A) can measure voltage, the other ADC with multifunction measure current or temperature etc.
  - Highly Metering Accurate:

    Supports the requirements of IEC 62053-21:2020/ IEC 62053-22:2020 and IEC 62053-23:2020.

    Less than 0.1% error in active energy metering over a dynamic range of 5000:1

    Less than 0.2% error in reactive energy metering over a dynamic range of 5000:1

    Less than 0.5% error in current/voltage RMS over a dynamic range of 5000:1.
  - Supports various measurements:
  - DC components of voltage and current signal
  - Total/ fundamental instantaneous/ average current/voltage RMS
  - Total instantaneous/ average active /reactive/apparent power
  - 10 or 12 cycles of total RMS
  - Fundamental instantaneous/average active /reactive/apparent power
  - active/ reactive energy, active/ reactive/ apparent power, Irms, constant value, and fundamental wave are selectable
  - Line frequency and phase

- DC signals measurement
- Software calibration
- Accelerating calibration when weak current is applied.
- Supports detection for over-current, over-voltage, under-current, under-voltage, voltage dip, and voltage swell
- Supports waveform buffer and waveform transmitted
- Current input: current shunt resistor, CT, Hall cell, and TMR supportive

V94XX(A) series product

	V9400(A)	V9430	V9431(A)	V9410(A)	V9420A
ADC channel	9	8	8	5	4
Tiny ADC channel	2	2	2	1	2
UART	5	3	5	5	5
UART32K	2	2	2	2	2
ISO7816	1	0	1	1	1
SPI	1	1	1	1	1
I2C	1	1	1	1	1
Comparator	2	2	2	1	1
GPIO	75	59	63	48	32
External interrupt IO	14	11	14	10	8
32-bit Timer	4	4	4	4	4
16-bit PWM Timer	4	4	4	4	4
PWM out	4	4	4	4	4
DMA channel	4	4	4	4	4
LCD	65x4，63x6，61x8	51x4，49x6，47x8	55x4，53x6，51x8	41x4，39x6，37x8	25x4，23x6
FLASH	256KB(94XX) 128KB(94XXA)	256KB	256KB(94XX) 128KB(94XXA)	256KB(94XX) 128KB(94XXA)	128KB
SRAM	32KB(94XX) 16KB(94XXA)	32KB	32KB(94XX) 16KB(94XXA)	32KB(94XX) 16KB(94XXA)	16KB
Energy Metering channel	3	3	3	3	3
Package type	100-LQFP	80-LQFP	80-LQFP	64-LQFP	48-LQFP

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Table List

1.Electrical Characteristics

1.1. Absolute Maximum Ratings

Stresses above those listed as "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Unless otherwise specified, the data are based on the test results of TA = 25 ℃, VDD = 3.3 V.

Table 1-1 Absolute Maximum Ratings

Symbol	Ratings	Min	Max	Unit
V_{VDD}-V_{SS}	External supply voltage	-0.3	+3.63	V
V_{IN}-V_{SS}	External signal input to GPIO pins.	-0.3	+3.63	V
Analog Input Voltage	IAP/IAN/IBP/IBN	-0.3	+3.3	V
Analog Input Voltage	UP/UN	-0.3	+3.3	V
S_{VDD}	IO power-on slope	3.3V/sec	1V/usec	--
I_{INJ_PAD}	Single pin input injection current	-10	+10	mA
I_{INJ_SUM}	Sum of all input injected current	-50	+40	mA
T_W	Working temperature range	-40	+85	℃
T_S	Storage temperature	-55	+150	℃
T_J	PN junction temperature	-40	+125	℃

1.2. Normal Operating Voltage

Unless otherwise specified, the data are based on the test results of TA = 25 ℃, VDD = 3.3 V.

Table 1-2 Operating Voltage

Symbol	Parameter	Conditions(-40~+85℃)	Min	Typ	Max	Unit
$V_{IN,VDD}$	Input voltage range of VDD*[1]		2.2	3.3	3.6	V

*[1]: ADC and metering working voltage: 2.6V ~ 3.6V

1.3. Driving Capability Characteristics

Unless otherwise specified, the data are based on the test results of TA = 25 ℃, VDD = 3.3 V.

Table 1-3 Driving Condition of Power PINs

Symbol	Parameter	Conditions(-40~+85℃)	Min	Typ	Max	Unit
$I_{DRV,DVCC}$	Driving Capability of DVCC				35	mA
$I_{DRV,VDDOUT}$	Driving Capability of VDD_OUT				20	mA

1.4. Power consumption

Unless otherwise specified, the data are based on the test results of TA = 25 ℃, VDD = 3.3 V.

Table 1-4 General Operating Conditions

Symbol	Parameter	Conditions (25 ℃, VDD=3.3V)	Min	Typ	Max	Unit
I_{ACTIVE}	Active current.	26.2144MHz system clock		5082		μA
		13.1072MHz system clock		2792		
		6.5536MHz system clock		1633		
		3.2768MHz system clock		1016		
		1.6384MHz system clock		713		
		819.2kHz system clock		548		
		409.6kHz system clock		461		
		204.8kHz system clock		418		
		32K RC system clock(FLASH deep-standby)		10.0		
		32K RC system clock(power on FLASH)		75.0		
I_{IDLE}	Idle current.	26.2144MHz system clock		1114		μA
		13.1072MHz system clock		625		
		6.5536MHz system clock		379		
		3.2768MHz system clock		256		
		1.6384MHz system clock		195		
		819.2kHz system clock		164		
		409.6kHz system clock		149		
		204.8kHz system clock		141		
		32K RC system clock		5.1		
I_{SLP1}	Sleep current at LCD off.	RTCCLK no frequency division		3.1 6.3@80℃		μA
		RTCCLK 4 frequency		2.8		

		division				
I_{SLP2}	Sleep current at LCD on.	RTCCLK no frequency division		9.3		μA
		RTCCLK 4 frequency division		9.0		
I_{DSLP}	Deep-sleep current, VDD=3.3V	RTCCLK no frequency division		2.9		μA
		RTCCLK 4 frequency division		2.6		

Table 1-5 Power Consumption of Each Module

module	**Power consumption(μA)**	**State (25℃, VDD=3.3V)**
CMP 1/2	0.08	IT_CMP=00(Bias current=20nA)
	0.4	IT_CMP=01(Bias current=100nA)
	2	IT_CMP=1*(Bias current=500nA)
ADCBGP	108	
ADC	230	
TinyADC	0.7	
Temp sensor	370	
LCD	5	LCD driving res=600k
	9.9	LCD driving res=300k
	14.5	LCD driving res=200k
	19	LCD driving res=150k
32768 XTAL	0.6	
32K RC	0.2	
6.5M RC	80	
6.5M XTAL	120	
PLL_L	20	
PLL_H	40	
EM	2600	IA, IB and U channels work simultaneously.

1.5. Embedded Reset and Power Control Block Characteristics

Unless otherwise specified, the data are based on the test results of TA = 25 ℃, VDD = 3.3 V.

Table 1-6 Embedded Reset and Power Control Block Characteristics

Symbol	**Parameter**	**Conditions (25℃)**	**Min**	**Typ**	**Max**	**Unit**
t_{RST}	Reset de-bounce time.			20		μS
V_{LPREF}	Reference voltage V_{LPREF}		1.222	1.3	1.352	V
V_{PORH}	PORH detect voltage		1.955	2.08	2.163	V

	(VDD).					
V_{PORL}	PORL detect voltage (DVCCLDO1).		1.222	1.3	1.352	V
V_{VDCIN}	V_{DCIN} detect level.		1.222	1.3	1.352	V
$V_{VDDALRAM}$	VDD supervisor voltage threshold	V_{TH} configurable, V_{TH}=2.9V;	2.726	2.9	3.016	V
LCDLDO	LCDLDO voltage		3.2	3.3	3.4	V
V_{LCDLDO_Drop}	LCDLDO voltage drop				20	mV

Table 1-7 Hysteresis Voltage Characteristics

Symbol	Parameter	Conditions (25℃)	Min	Typ	Max	Unit
V_{PORH_HTRES}	PORH detect hysteresis voltage.		53.2	66.5	79.8	mV
V_{PORL_HTRES}	PORL detect hysteresis voltage.		33.6	42.0	50.4	mV
V_{VDCIN_HTRES}	VDCIN detect hysteresis voltage.		33.6	42.0	50.4	mV
$V_{VDDALRAM\_HTRES}$	VDD supervisor hysteresis voltage.	$V_{TH\_VDDALARM}$ = 3.6V	91.2	114.0	136.8	mV
		$V_{TH\_VDDALARM}$ = 3.2 V	81.1	101.4	121.6	mV
		$V_{TH\_VDDALARM}$ = 2.9 V	73.5	91.9	110.2	mV
		$V_{TH\_VDDALARM}$ = 2.6 V	65.9	82.4	98.8	mV
		$V_{TH\_VDDALARM}$ = 2.3 V	58.3	72.9	87.4	mV

1.6. GPIO Characteristics

Unless otherwise specified, the data are based on the test results of TA = 25 ℃, VDD = 3.3 V.

Table 1-8 GPIO Characteristics

Symbol	Parameter	V_{VDD}	Conditions (-40~85 ℃)	Min	Max	Unit
V_{IH}	Input high voltage	3.3V		2		V
V_{IL}	Input low voltage	3.3V			0.3* V_{VDD}	V
V_{HSYS}	Schmitt trigger hysteresis	3.3V		0.1* V_{VDD}		V
I_{IH}	Input high current	3.3V			+1	μA
I_{IL}	Input low current	3.3V		-1		μA
V_{OH}	Output high voltage	3.3V	5.6mA	2.4	V_{VDD}	V
V_{OL}	Output low voltage	3.3V	5.6mA		0.4	V
C_{IN}	Input capacitance	3.3V			10	pF

1.7. Generic ADC Characteristics

Unless otherwise specified, the data are based on the test results of TA = 25 ℃, VDD = 3.3 V.

Table 1-9 ADC Characteristics

Symbol	Parameter	Conditions (25℃)	Min	Typ	Max	Unit
ADCREF	ADCBGP Voltage		1.207	1.225	1.243	V
PSRR	Power Supply Rejection Ratio of ADCBGP			-92		dB
V_{ADC}	ADC operation voltage		2.7	3.3	3.6	V
I_{ADC}	ADC operation current.		170	230	350	μA
f_{ADCLK}	ADC sampling clock.			1.6384		MHz
C_{ADC}	Internal sample and hold capacitance.			1		pF
INL	Integrated non linearity.			2		LSB
DNL	Differential non linearity.			1		LSB
Offset	Offset error			5		mV
$V_{WITHSTAND}$	Withstand voltage (input of ADC Channel)		-0.7		V_{DD}	V

1.8. Comparator Characteristics

Unless otherwise specified, the data are based on the test results of TA = 25 ℃, VDD = 3.3 V.

Table 1-10 Comparator Characteristics

Symbol	Parameter	Conditions (25℃)	Min	Typ	Max	Unit
V_{CMP}	Comparator operation voltage(VDD)		2.2	3.3	3.6	V
I_{CMP}	Comparator operation current.	Input bias current 20nA, input 50kHz square wave.		0.08		μA
		Input bias current 100nA, input 50kHz square wave.		0.4		μA
		Input bias current 500nA, input 50kHz square wave.		2		μA
td	Propagation delay	Input bias current 20nA, input 50kHz square wave.		1.6		μS
		Input bias current 100nA, input 50kHz square wave.		0.63		μS

		Input bias current 500nA, input 50kHz square wave.		0.27		μS
V_{CMPIN}	Comparator input voltage range.		0.8		VDD-0.3	V
V_{CMPREF}	Comparator reference voltage	Reference voltage is LPREF	1.222	1.3	1.352	V
		Reference voltage is ADCREF	1.18	1.2	1.22	V
V_{HTRES}	Comparator hysteresis voltage		20.0	25.0	30.0	mV

1.9. Clock and PLL Characteristics

Unless otherwise specified, the data are based on the test results of TA = 25 ℃, VDD = 3.3 V.

Table 1-11 Clock and PLL Characteristics

Symbol	Parameter	Conditions (-40~85 ℃)	Min	Typ	Max	Unit
V_{DDPLLL}	PLLL operating voltage (DVCC)		1.35	1.5	1.65	V
$I_{VDDPLLL}$	PLLL operating current			30		μA
V_{DDPLLH}	PLLH operating voltage (DVCC)		1.35	1.5	1.65	V
$I_{VDDPLLH}$	PLLH operating current			40		μA
V_{DDRCL}	RCL operating voltage (VDD)		2.2	3.3	3.6	V
I_{VDDRCL}	RCL operating current			0.2		μA
f_{RCL}	RCL frequency.		29.7	32	35.5	kHz
V_{DDRCH}	RCH operating voltage (VDD)		2.2	3.3	3.6	V
I_{VDDRCH}	RCH operating current			45		μA
f_{RCH}	RCH frequency.		6.357	6.5	6.75	MHz
V_{DDXOH}	XOH operating voltage (VDD)		2.2	3.3	3.6	V
I_{VDDXOH}	XOH operating current			150		μA
f_{XOH}	XOH frequency.			6.5536		MHz

1.10. FLASH and SRAM Characteristics

Unless otherwise specified, the data are based on the test results of TA = 25 ℃, VDD = 3.3 V.

Table 1-12 FLASH and SRAM Characteristics

Parameter	Conditions	Min	Typ	Max	Unit
FLASH word read access time.		38			ns
FLASH program time	-40~85℃	20000			time
FLASH data retention time	-40~85℃	20			year
FLASH byte program time		6		7.5	μS
FLASH page erase time (512 bytes)		4		5	ms
FLASH chip erase time		30		40	ms
FLASH active read current	26MHz access.		2.5	3.5	mA
FLASH active program current				3.5	mA
FLASH active erase current				2	mA
FLASH standby current (DVCC)			80	150	μA
FLASH deep standby current (DVCC)			0.1	6	μA
SRAM data retention voltage (DVCC)	-40~85℃	1.35	1.5	1.65	V

1.11. ESR Characteristics of Crystal Oscillator

Unless otherwise specified, the data are based on the test results of TA = 25 ℃, VDD = 3.3 V.

Table 1-13 ESR Characteristics of Crystal Oscillator

Parameter	Conditions (-40~85℃)	Min	Typ	Max	Unit
ESR of 6.5536M crystal oscillator				40	Ω
ESR of 32768K crystal oscillator				50	KΩ

*: ESR (Equivalent series resistance)

1.12. Electric energy metering related characteristics

Table 1-14 Parameters

Unless otherwise specified, the data are based on the test results of TA = 25 ℃, VDD = 3.3 V.

Parameter	Min.	Typ.	Max.	Unit	Remark
Phase Error Between Channels					
PF=0.8 Capacitive		±0.05		Degree	
PF=0.5 Inductive		±0.05		Degree	
Active Energy Metering Error		0.1		%	Dynamic Range 5000:1 @ 25°C Fundamental frequency deviation within ± 25%

Parameter	Min.	Typ.	Max.	Unit	Remark
Active Energy Metering Bandwidth		1.6		kHz	
Reactive Energy Metering Error		0.2		%	Dynamic Range 5000:1 @ 25°C Fundamental frequency deviation within ± 25%
Reactive Energy Metering Bandwidth	0.4	3.2	6.4	kHz	
VRMS Metering Error		0.5		%	Dynamic Range 5000:1 @ 25°C Fundamental frequency deviation within ± 25%
VRMS Metering Bandwidth	0.4	3.2	6.4	kHz	
IRMS Metering Error		0.5		%	Dynamic Range 5000:1 @ 25°C Fundamental frequency deviation within ± 25%
IRMS Metering Bandwidth	0.4	3.2	6.4	kHz	
Frequency Measurement					
Range	40		70	Hz	
Error		0.01		Hz	
Analog Input					
Maximum Signal Level			±200	mV	Peak value
ADC					
DC Offset			10	mV	
Resolution		23		Bit	Sign bit is included.
Bandwidth (-3dB)	0.4	3.2	6.4	kHz	
On-chip Reference					
Reference Error	-18		18	mV	@ 25°C
Output voltage		1.21		V	
Power Supply Rejection Ratio		92		dB	
Temperature Coefficient		10	30	ppm/°C	
Power Supply					
VDD2	2.6	3.3	3.6	V	
Digital Power Supply (DVCC2)					
Voltage		1.5		V	Programmable. Error: ±10%
Current			35	mA	
Clock					
High frequency clock of metering module (EM_PCLKDIV)		6.5536		MHz	
High frequency clock inside metering module (EM_RCH)	-20%	6.5536	+20%	MHz	

Low frequency clock of energy tank of metering module（EM_X32KIN）		32.768		KHz	

1.13. Stabilization Time of Clock and Wake up Time

Unless otherwise specified, the data are based on the test results of TA = 25 ℃, VDD = 3.3 V.

Table 1-15 Stabilization Time of Clock and Wake-up Time

Parameter	Conditions (-40~85℃)	Min	Typ	Max	Unit
PLLL lock time				1	ms
PLLH lock time				15	μS
Stabilization time of RCL				200	μS
Stabilization time of RCH				5	μS
Stabilization time of ADCBGP				10	μS
Wake up time from sleep mode when RCH as system clock			18.4		μS
Wake up time from sleep mode when PLLL as system clock			1.03		mS
Wake up time from sleep mode when PLLH as system clock			22.8		μS
Interrupt response time in IDLE mode when RCH as system clock			6		μS
Interrupt response time in IDLE mode when PLLL as system clock			1.6		μS
Interrupt response time in IDLE mode when PLLH as system clock			1.6		μS

1.14. ADC conversion time

Unless otherwise specified, the data are based on the test results of TA=25 ℃ and VDD=3.3V.

The configuration of ADC clock frequency, CIC filter downsampling rate, and CIC filter ignoring sampling points are different, and the MADC conversion time is different. Please refer to the table below for details.

Table 1-16 ADC conversion time (CIC filter down sampling rate and ADC clock frequency)

ADC clock frequency/MHz CIC filter Down sampling rate / ADC typical conversion time/ms	6.5536	3.2768	1.6384	0.8192	0.4096
1/512	0.937	0.937	1.875	3.750	7.500
1/256	0.468	0.468	0.937	1.875	3.750

1/128	0.234	0.234	0.468	0.937	1.875
1/64	0.117	0.117	0.234	0.468	0.937

Other parameter configurations: CICSKIP=6, CIC filter ignores the first two sampling points.

Note 1: ADC is a third-order CIC, ignoring the first two sampling points, and the data is stable.

Note 2: $\textbf{ADC conversion time} = \frac{1}{\text{CIC Down Sampling rate} \times \frac{\text{ADC Clock frequency}}{2}} \times \textbf{Sampling point}$

(except when ADC clock frequency is 6.5536MHz), for example, CIC downsampling rate is 1/512, ADC clock frequency is 3.2768MHz, and the first two sampling points are ignored,

$$\textbf{ADC conversion time} = \frac{1}{\left(\frac{1}{512} \times \frac{3.2768\ MHz}{2}\right)} \times 3 = 0.937ms$$

Table 1-17 ADC conversion time (CIC filter ignores sampling points)

Parameter	Conditions (Ignore number of sampling points)	Type	Unit
ADC conversion time	2	1.875	ms
	3	2.520	ms
	4	3.150	ms
	5	3.780	ms
	6	4.410	ms
	7	5.040	ms
Other parameter configurations: the down sampling rate is 1/512, and the ADC clock frequency is 1.6384MHz.			

1.15. TinyADC Conversion Time

Unless otherwise specified, the data are based on the test results of TA = 25 ℃, VDD = 3.3 V.

Table 1-18 TinyADC Conversion Time

Parameter	Conditions	Min	Typ	Max	Unit
TinyADC conversion time			40		μS

1.16. ESD handling ratings

Unless otherwise specified, the data are based on the test results of TA = 25 ℃, VDD = 3.3 V.

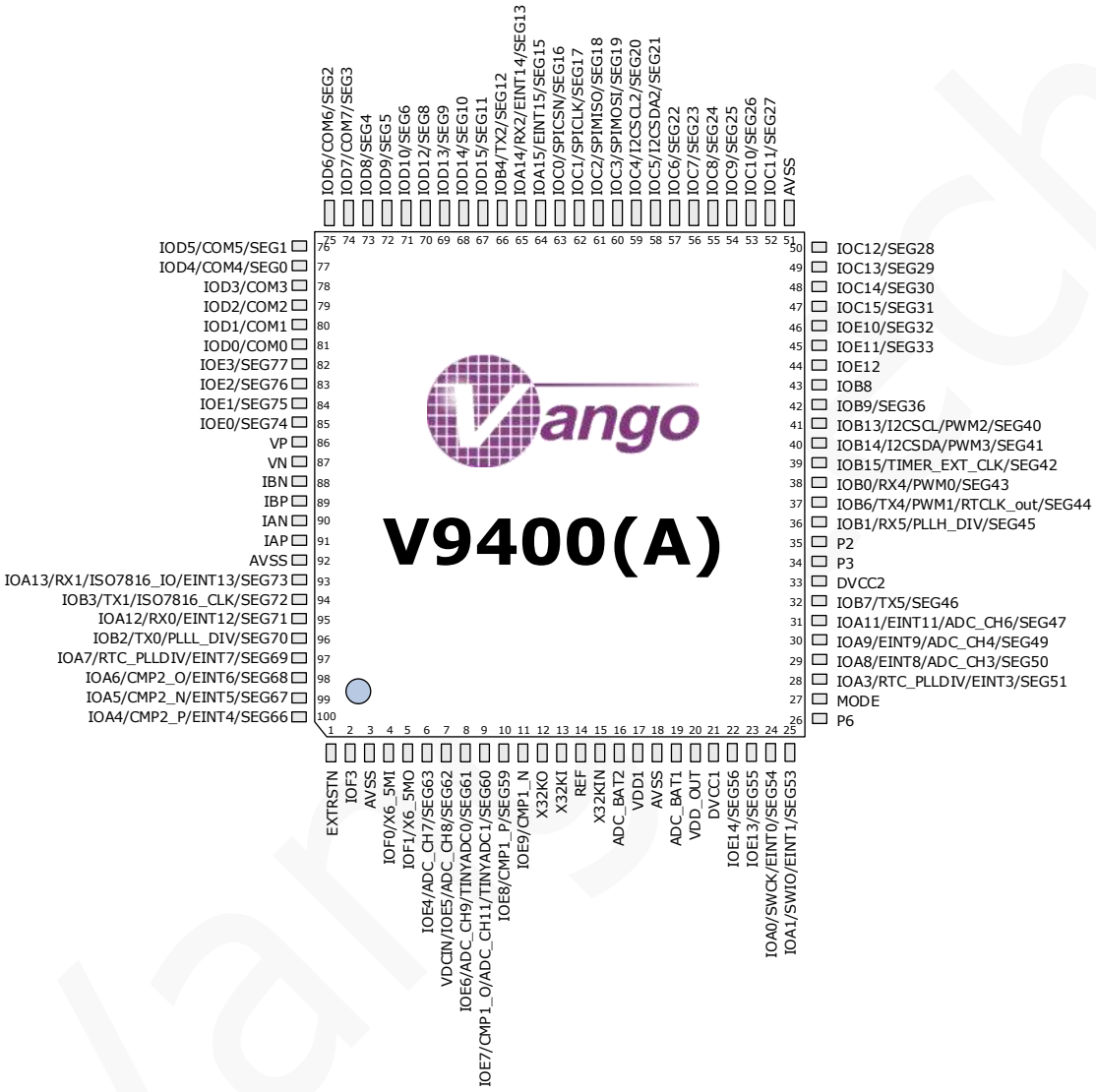
Table 1-19 ESD handling ratings

Parameter	Conditions	Min	Max

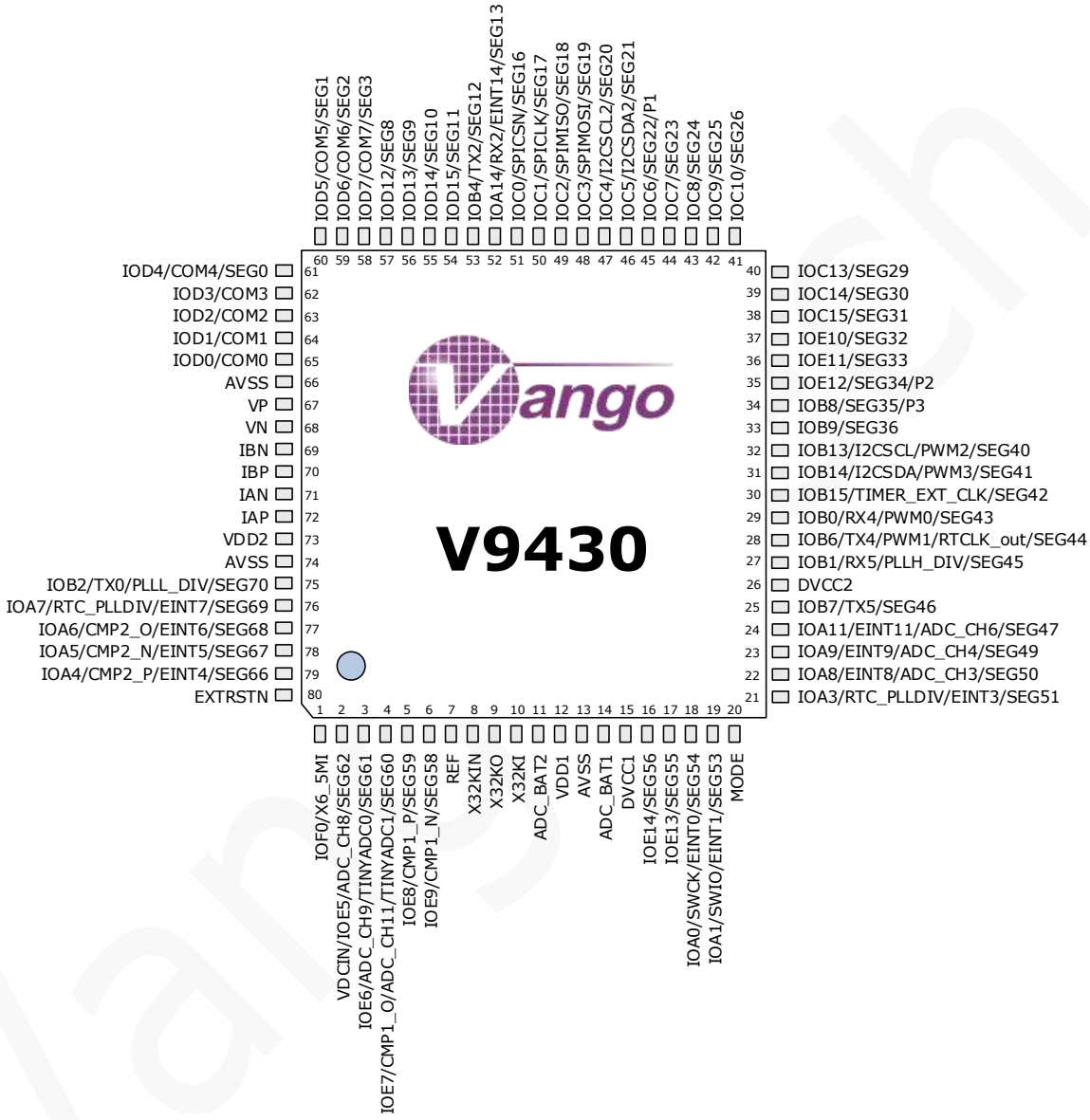
HBM	Mil-Std-883J Method 3015.9	-4KV	+4KV
MM	EDEC EIA/JESD22-A115	-300V	+300V
LATCH-UP	JEDEC EIA/JESD78E	-200mA	+200mA

2.Pin Assignments

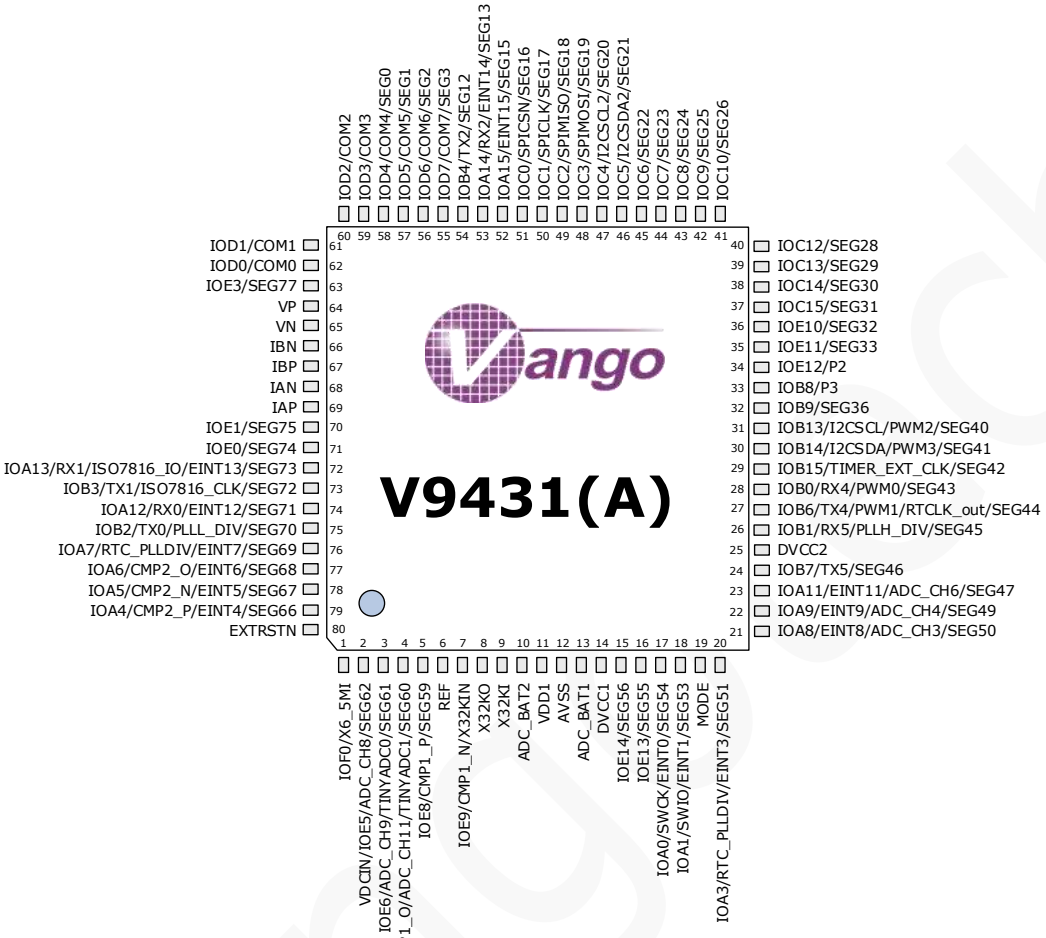
2.1. V9400(A) Pin Assignments



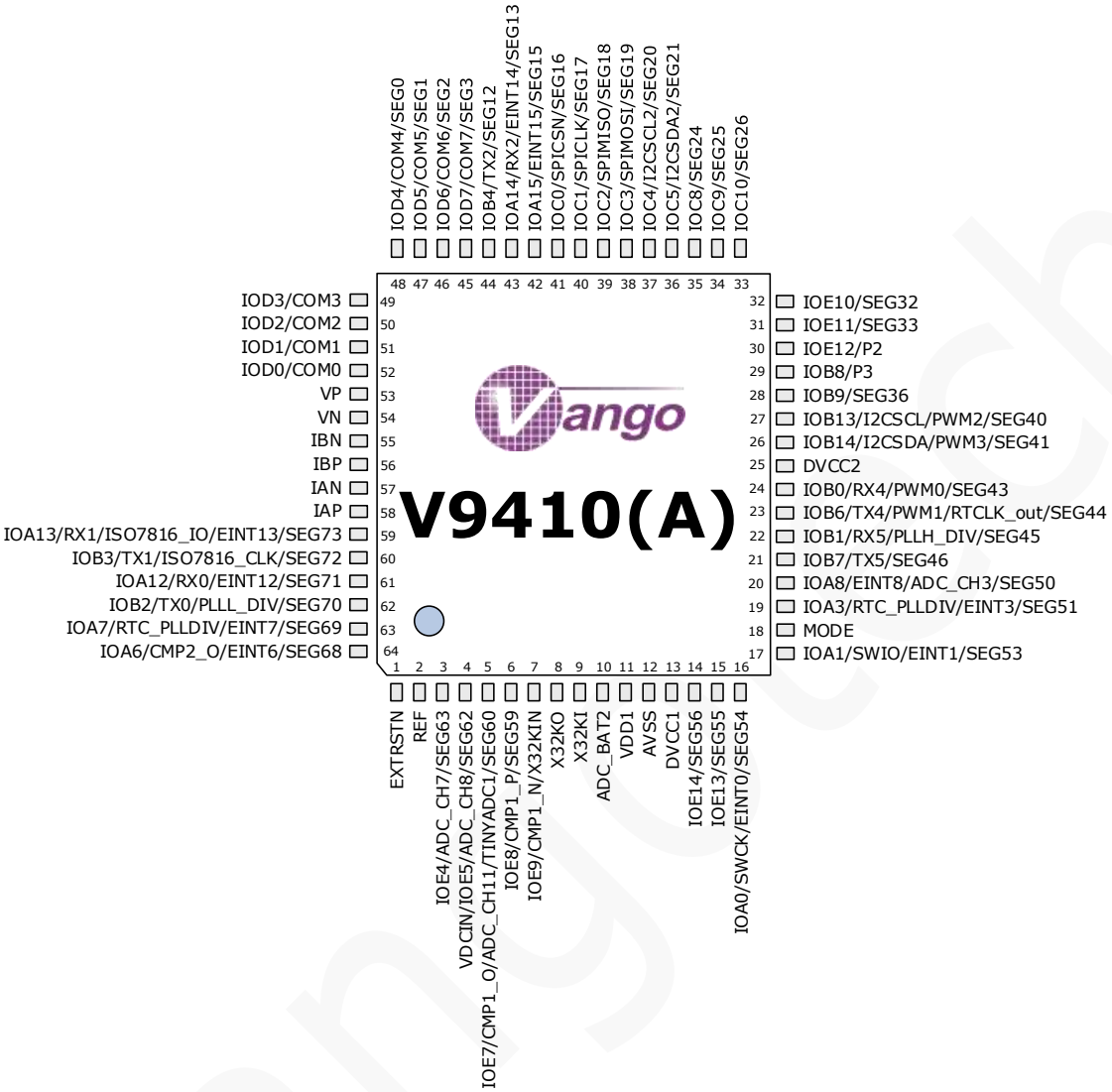
2.2. V9430 Pin Assignments



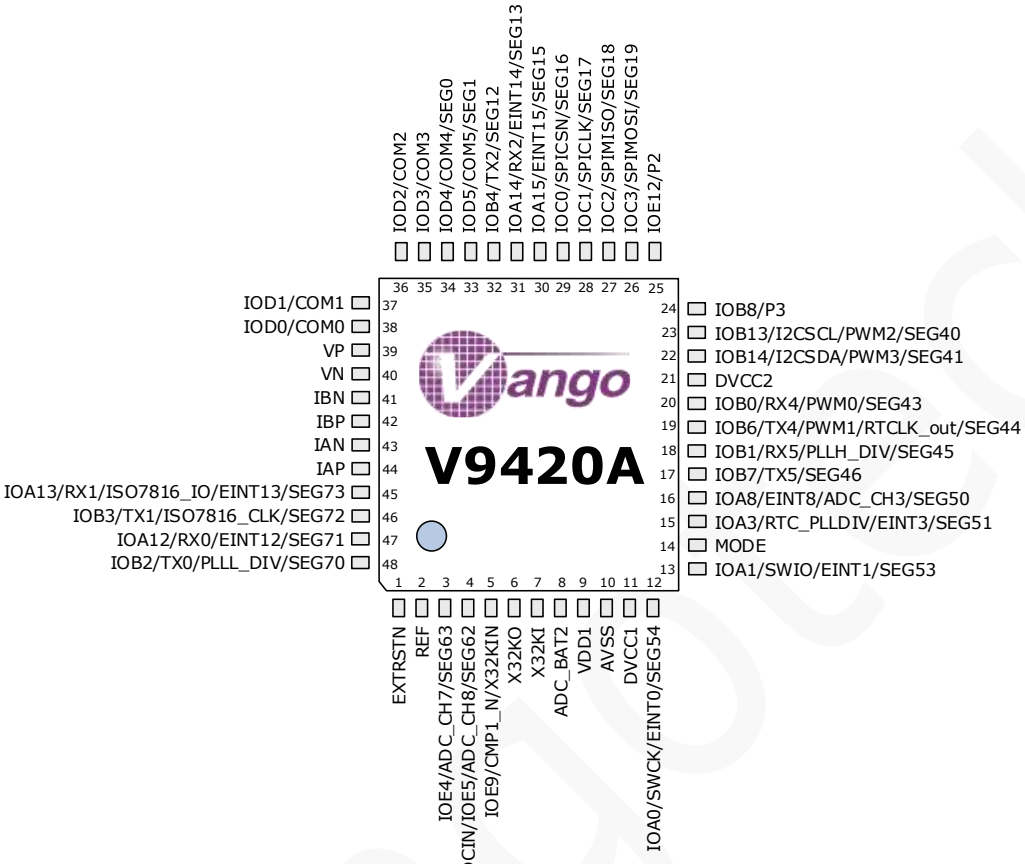
2.3. V9431(A) Pin Assignments



2.4. V9410(A) Pin Assignments



2.5. V9420A Pin Assignments



2.6. V94XX(A) Pin Descriptions

Table 2-1 V94XX(A) Pin Descriptions

Pin Number						Pin Name	Type	Description
V94XX(A)	V9400(A)	V9430	V9431(A)	V9410(A)	V9420A			
1	4	1	1			IOF0	I/O	Default: IOF0 Function 1: 6.5536M crystal input
2	5					IOF1	I/O	Default: IOF1 Function 1: 6.5536M crystal output
3	6			3	3	IOE4	I/O	Default: IOE4 Function 1: ADC_CH7 input Function 2: SEG63
4	7	2	2	4	4	IOE5	I/O	Default: VDCIN input. Function 1: ADC_CH8 input Function 2: IOE5 Function 3: SEG62
5	8	3	3			IOE6	I/O	Default: IOE6 Function 1: ADC_CH9 input and tiny ADC channel 0 input Function 2: SEG61
6	9	4	4	5		IOE7	I/O	Default: IOE7 Function 1: Comparator 1 output Function 2: ADC_CH11 input and tiny ADC channel 1 input Function 3: SEG60
7	10	5	5	6		IOE8	I/O	Default: IOE8 Function 1: Comparator 1 P input Function 2: SEG59
8	11	6	7	7	5	IOE9	I/O	Default: IOE9 Function 1: Comparator 1 N input

								IOE9 and X32KIN share one pin in V9431(A)/V9410(A)/V9420A
9	14	7	6	2	2	REF	I/O	On-chip reference voltage. This pin must be connected to a 1μF capacitor, and then grounded.
10	15	8	7	7	5	X32KIN	I	32K CLK input pin (Digital IO interface). IOE9 and X32KIN share one pin in V9431(A)/V9410(A)/V9420A
11	12	9	8	8	6	X32KO	O	32768 Hz crystal output pin. The internal matching capacitance is 12 pF.
12	13	10	9	9	7	X32KI	I	32768 Hz crystal input pin
13	16	11	10	10	8	ADC_BAT2	I	Input of ADC channel 2 for battery voltage measurement
14	17	12	11	11	9	VDD1	P	Main VDD power input. User should connect a 0.1uF de-couple capacitor at this pin.
15	18	13	12	12	10	AVSS	G	Analog ground
16	19	14	13			ADC_BAT1	I	Input of ADC channel 1 for battery voltage measurement
17	20					VDD_OUT	O	VDD voltage output pin. This pin has the same electrical level as VDD, user can be used to drive small power modules.
18	21	15	14	13	11	DVCC1	O/P	Internal digital power output pin, user should connect a 0.1uF and 10uF de-couple capacitor at this pin.
19	22	16	15	14		IOE14	I/O	Default: IOE14 Function 2: SEG56
20	23	17	16	15		IOE13	I/O	Default: IOE13 Function 2: SEG55
21	24	18	17	16	12	IOA0	I/O	Default: IOA0 (MODE=1), SWCLK(MODE=0) Function 1: EINT0 Function 2: SEG54

22	25	19	18	17	13	IOA1	I/O	Default: IOA1 (MODE=1), SWDIO(MODE=0) Function 1: EINT1 Function 2: SEG53
23	27	20	19	18	14	MODE	I	Debug mode or normal mode selection. 0: Debug mode 1: Normal mode The signal level of this pin should be the same as VDD, and the state of this IO should not change during normal or debug operation.
24	28	21	20	19	15	IOA3	I/O	Default: IOA3 Function 1: Second pulse output (RTC_PLLDIV output) Function 2: EINT3 Function 3: SEG51
25	26	21				P6	I/O	Default: P6. CF1/CF2/ single interruption/ all interruption/ wave output
26	29	22	21	20	16	IOA8	I/O	Default: IOA8 Function 1: EINT8 Function 2: ADC_CH3 input Function 3: SEG50
27	30	23	22			IOA9	I/O	Default: IOA9 Function 1: EINT9 Function 2: ADC_CH4 input Function 3: SEG49
28	31	24	23			IOA11	I/O	Default: IOA11 Function 1: EINT11 Function 2: ADC_CH6 input Function 3: SEG47
29	32	25	24	21	17	IOB7	I/O	Default: IOB7 Function 1: UART TXD5 Function 2: SEG46
30	33	26	25	25	21	DVCC2	O/P	Internal digital power output pin, user should connect a 0.1uF and 10uF de-couple capacitor at this pin.

31	36	27	26	22	18	IOB1	I/O	Default: IOB1 Function 1: UART RXD5 Function 3: PLLH divider output Function 4: SEG45
32	37	28	27	23	19	IOB6	I/O	Default: IOB6 Function 1: UART TXD4 Function 2: PWM1 In/Out line Function 3: RTCCLK output Function 4: SEG44
33	38	29	28	24	20	IOB0	I/O	Default: IOB0 Function 1: UART RXD4 Function 2: PWM0 In/Out line Function 3: SEG43
34	39	30	29			IOB15	I/O	Default: IOB15 Function 1: Timer external clock input Function 2: SEG42
35	40	31	30	26	22	IOB14	I/O	Default: IOB14 Function 1: I2C SDA Function 2: PWM3 In/Out line Function 3: SEG41
36	41	32	31	27	23	IOB13	I/O	Default: IOB13 Function 1: I2C SCL Function 2: PWM2 In/Out line Function 3: SEG40
37	42	33	32	28		IOB9	I/O	Default: IOB9 Function 1: SEG36
38	43	34	33	29	24	IOB8	I/O	Default: IOB8
39	34	34	33	29	24	P3	I/O	Default: P3. CF1/ CF2/ single interruption/ all interruption/ wave output
40	44	35	34	30	25	IOE12	I/O	Default: IOE12

41	35	35	34	30	25	P2	I/O	Default: P2. CF1/ CF2/ single interruption/ all interruption/ wave output
42	45	36	35	31		IOE11	I/O	Default: IOE11 Function 1: SEG33
43	46	37	36	32		IOE10	I/O	Default: IOE10 Function 1: SEG32
44	47	38	37			IOC15	I/O	Default: IOC15 Function 1: SEG31
45	48	39	38			IOC14	I/O	Default: IOC14 Function 1: SEG30
46	49	40	39			IOC13	I/O	Default: IOC13 Function 1: SEG29
47	50		40			IOC12	I/O	Default: IOC12 Function 1: SEG28
48	51					AVSS	G	Analog ground
49	52					IOC11	I/O	Default: IOE11 Function 1: SEG27
50	53	41	41	33		IOC10	I/O	Default: IOE10 Function 1: SEG26
51	54	42	42	34		IOC9	I/O	Default: IOC9 Function 1: SEG25
52	55	43	43	35		IOC8	I/O	Default: IOC8 Function 1: SEG24
53	56	44	44			IOC7	I/O	Default: IOC7 Function 1: SEG23
54	57	45	45			IOC6	I/O	Default: IOC6 Function 1: SEG22
55	58	46	46	36		IOC5	I/O	Default: IOC5 Function 1: I2C SDA (2) Function 2: SEG21

56	59	47	47	37		IOC4	I/O	Default: IOC4 Function 1: I2C SCL (2) Function 2: SEG20
57	60	48	48	38	26	IOC3	I/O	Default: IOC3 Function 1: SPIMOSI Function 2: SEG19
58	61	49	49	39	27	IOC2	I/O	Default: IOC2 Function 1: SPI MISO Function 2: SEG18
59	62	50	50	40	28	IOC1	I/O	Default: IOC1 Function 1: SPICLK Function 2: SEG17
60	63	51	51	41	29	IOC0	I/O	Default: IOC0 Function 1: SPICSN Function 2: SEG16
61	64		52	42	30	IOA15	I/O	Default: IOA15 Function 1: Reserved Function 2: Reserved Function 3: EINT15 Function 4: SEG15
62	65	52	53	43	31	IOA14	I/O	Default: IOA14 Function 1: UART RXD 2 Function 2: EINT14 Function 3: SEG13
63	66	53	54	44	32	IOB4	I/O	Default: IOB4 Function 1: UART TXD 2 Function 2: SEG12
64	67	54				IOD15	I/O	Default: IOD15 Function 1: SEG11
65	68	55				IOD14	I/O	Default: IOD14 Function 1: SEG10

66	69	56				IOD13	I/O	Default: IOD13 Function 1: SEG9
67	70	57				IOD12	I/O	Default: IOD12 Function 1: SEG8
68	71					IOD10	I/O	Default: IOD10 Function 1: SEG6
69	72					IOD9	I/O	Default: IOD9 Function 1: SEG5
70	73					IOD8	I/O	Default: IOD8 Function 1: SEG4
71	74	58	55	45		IOD7	I/O	Default: IOD7 Function 1: COM7/SEG3
72	75	59	56	46		IOD6	I/O	Default: IOD6 Function 1: COM6/SEG2
73	76	60	57	47	33	IOD5	I/O	Default: IOD5 Function 1: COM5/SEG1
74	77	61	58	48	34	IOD4	I/O	Default: IOD4 Function 1: COM4/SEG0
75	78	62	59	49	35	IOD3	I/O	Default: IOD3 Function 1: COM3
76	79	63	60	50	36	IOD2	I/O	Default: IOD2 Function 1: COM2
77	80	64	61	51	37	IOD1	I/O	Default: IOD1 Function 1: COM1
78	81	65	62	52	38	IOD0	I/O	Default: IOD0 Function 1: COM0
79	82		63			IOE3	I/O	Default: IOE3 Function 1: SEG77
80	83					IOE2	I/O	Default: IOE2 Function 1: SEG76
81	84		70			IOE1	I/O	Default: IOE1 Function 1: SEG75

82	85		71			IOE0	I/O	Default: IOE0 Function 1: SEG74
83		66				AVSS	G	Analog ground
84	86	67	64	53	39	UP	I	Positive input pin for Voltage Channel Sampling.
85	87	68	65	54	40	UN	I	Negative input pin for Voltage Channel Sampling.
86	88	69	66	55	41	IBN	I	Negative input pin for current channel B sampling.
87	89	70	67	56	42	IBP	I	Positive input pin for current channel B sampling.
88	90	71	68	57	43	IAN	I	Negative input pin for current channel A sampling.
89	91	72	69	58	44	IAP	I	Positive input pin for current channel A sampling.
90		73				VDD2	P	Metering main power input pin. The user should connect a 0.1uF decoupling capacitor to this pin. When the pin is not led out, the user can control the power input through the software.
91	92	74				AVSS	G	Analog ground.
92	93		72	59	45	IOA13	I/O	Default: IOA13 Function 1: UART RXD 1 Function 2: ISO7816_IO Function 3: EINT13 Function 4: SEG73
93	94		73	60	46	IOB3	I/O	Default: IOB3 Function 1: UART TXD 1 Function 2: ISO7816_CLK Function 3: SEG72

94	95		74	61	47	IOA12	I/O	Default: IOA12 Function 1: UART RXD 0 Function 2: EINT12 Function 3: SEG71
95	96	75	75	62	48	IOB2	I/O	Default: IOB2 Function 1: UART TXD 0 Function 2: PLLL output Function 3: SEG70
96	97	76	76	63		IOA7	I/O	Default: IOA7 Function 1: Second pulse output (RTC_PLLDIV output) Function 2: EINT7 Function 3: SEG69
97	98	77	77	64		IOA6	I/O	Default: IOA6 Function 1: Comparator 2 output Function 2: EINT6 Function 3: SEG68
98	99	78	78			IOA5	I/O	Default: IOA5 Function 1: Comparator 2 N input Function 2: EINT5 Function 3: SEG67
99	100	79	79			IOA4	I/O	Default: IOA4 Function 1: Comparator 2 P input Function 2: EINT4 Function 3: SEG66
100	1	80	80	1	1	EXTRSTN	I	External reset pin, low active. 510k ohm resistor and 0.1uF capacitor are recommended for RC filter circuit.
101	2					IOF3	I/O	Default: IOF3
102						IOF2	I/O	Default: IOF2

								The chip is internally grounded.
103	3					AVSS	G	Analog ground.

Note: To ensure the system works normally, the IOF2 pins cannot be operated.

3.Functional Block Diagram

3.1. Functional Block Diagram

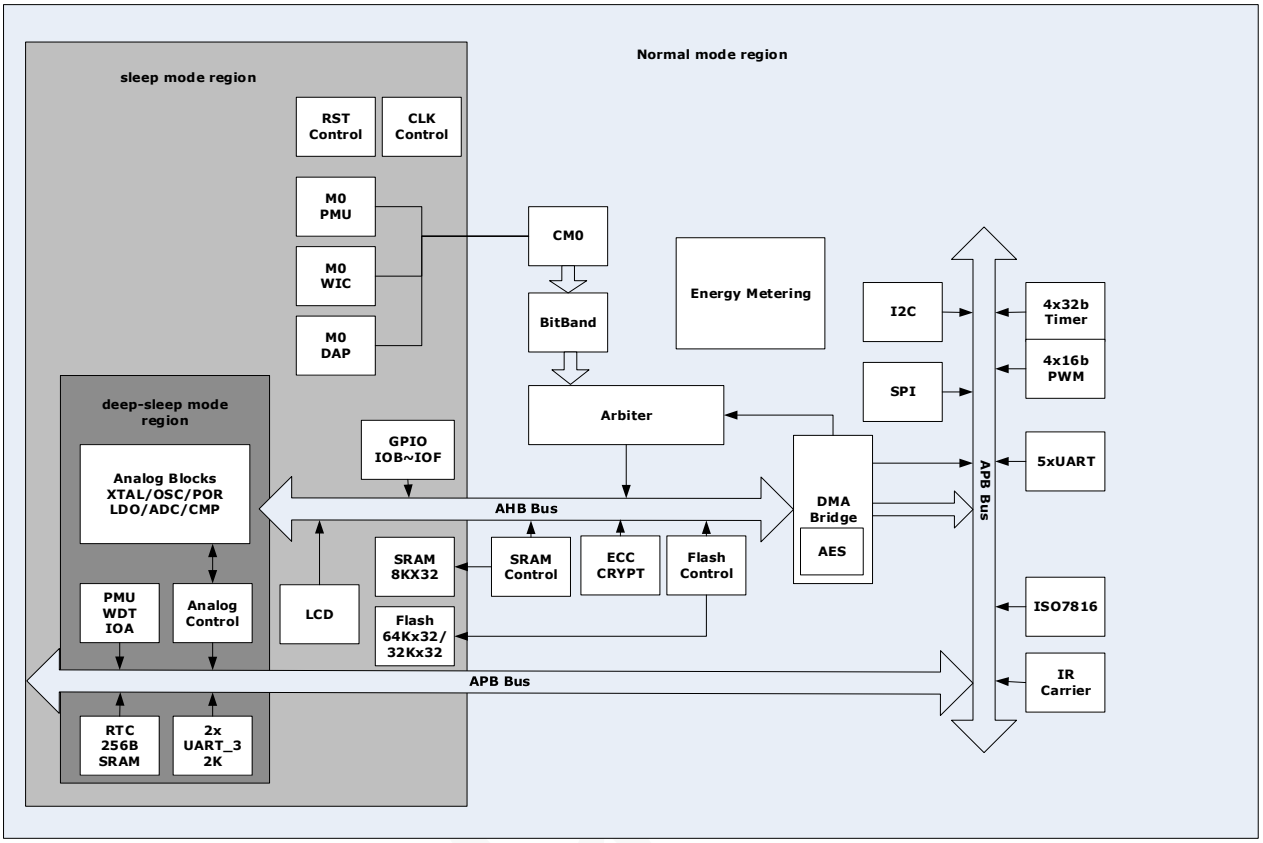


Figure 3-1 V94XX(A) Functional Block Diagram

3.2. Power System Block Diagram

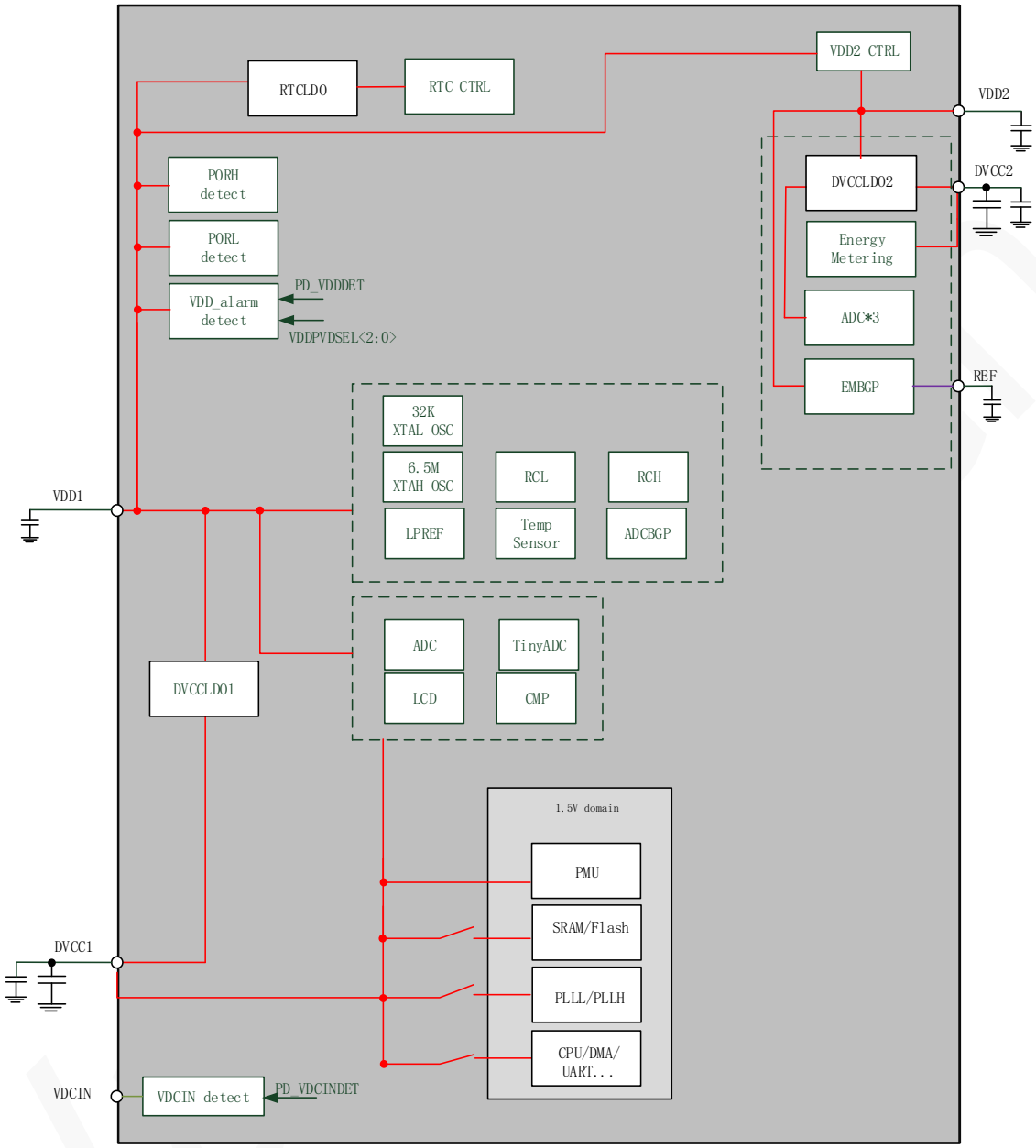


Figure 3-2 V94XX(A) Power System Block Diagram

3.3. Clock Block Diagram

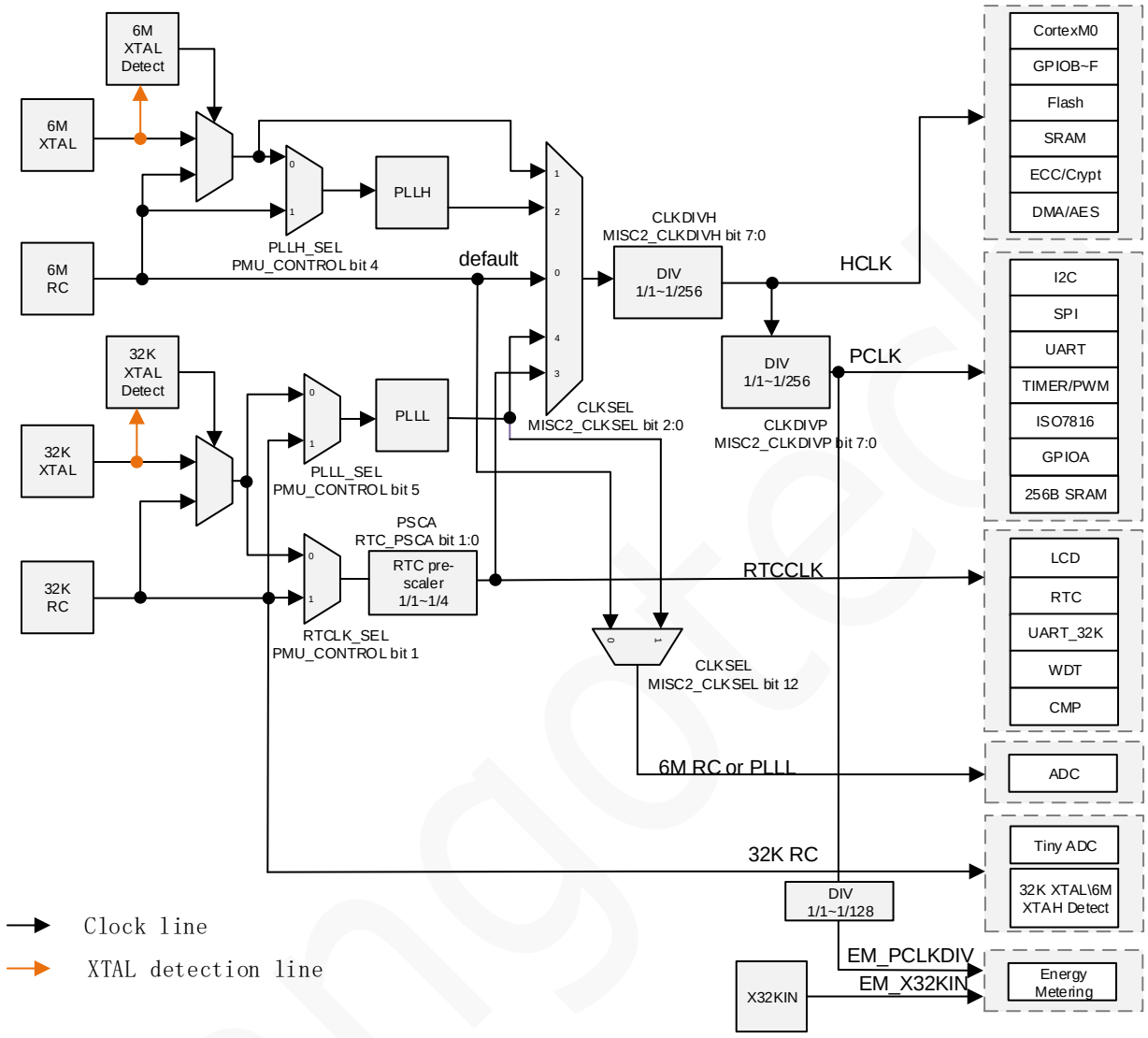


Figure 3-3 V94XX(A) Clock Block Diagram

4.Memory Maps

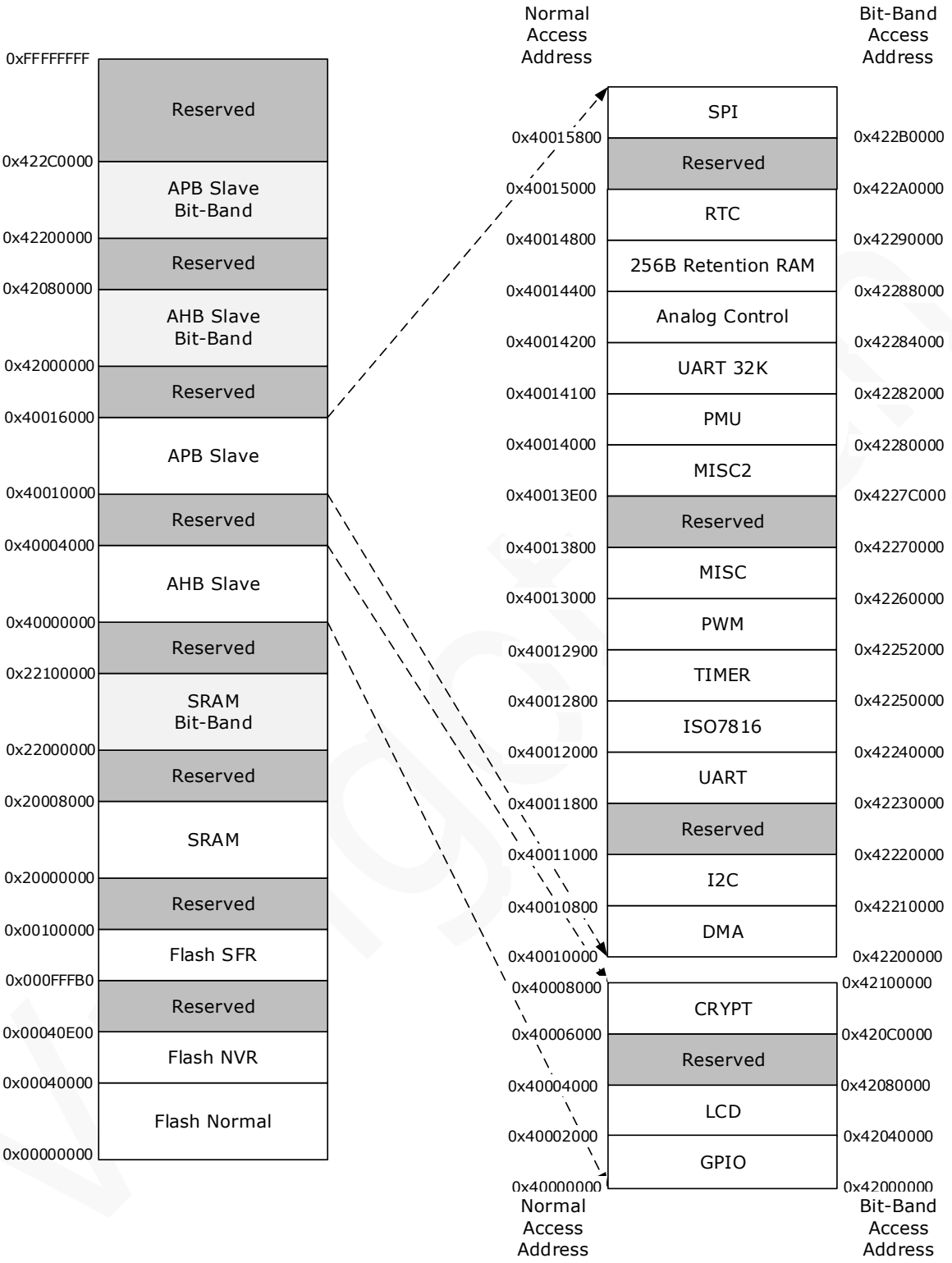


Figure 4-1 V94XX(A) Memory Maps

The bit-band region can only be accessed by Cortex-M0. The DMA controller can't access these regions. For all other regions, they can be accessed by both Cortex-M0 and DMA controller.

Table 4-1 System Memory Map

Address Aread Start	Address Aread End	Size	Peripherals
0x0000_0000	0x0003_FFFF	256K	Flash Normal

0x0004_0000	0x0004_0FFF	4K	Flash NVR
0x000F_FF00	0x000F_FFFF	256B	FLASH_SFR
0x2000_0000	0x2000_7FFF	32K	SRAM
0x2200_0000	0x220F_FFFF	1M	SRAM Bit-Band
0x4000_0020	0x4000_003F	32B	GPIOB
0x4000_0040	0x4000_005F	32B	GPIOC
0x4000_0060	0x4000_007F	32B	GPIOD
0x4000_0080	0x4000_009F	32B	GPIOE
0x4000_00A0	0x4000_00BF	32B	GPIOF
0x4000_00C0	0x4000_00FF	64B	GPIOAF
0x4000_2000	0x4000_3FFF	8K	LCD
0x4000_6000	0x4000_7FFF	8K	CRYPT
0x4001_0000	0x4001_07FF	2K	DMA
0x4001_0800	0x4001_0FFF	2K	I2C
0x4001_1800	0x4001_181F	32B	UART0
0x4001_1820	0x4001_183F	32B	UART1
0x4001_1840	0x4001_185F	32B	UART2
0x4001_1860	0x4001_187F	32B	-
0x4001_1880	0x4001_189F	32B	UART4
0x4001_18A0	0x4001_18BF	32B	UART5
0x4001_2000	0x4001_203F	64B	ISO7816
0x4001_2800	0x4001_281F	32B	TMR0
0x4001_2820	0x4001_283F	32B	TMR1
0x4001_2840	0x4001_285F	32B	TMR2
0x4001_2860	0x4001_287F	32B	TMR3
0x4001_2900	0x4001_291F	32B	PWM0
0x4001_2920	0x4001_293F	32B	PWM1
0x4001_2940	0x4001_295F	32B	PWM2
0x4001_2960	0x4001_297F	32B	PWM3
0x4001_29F0	0x4001_29FF	16B	PWMMUX
0x4001_3000	0x4001_37FF	2K	MISC
0x4001_3E00	0x4001_3FFF	512B	MISC2
0x4001_4000	0x4001_40FF	256B	PMU
0x4001_4100	0x4001_417F	128B	U32K0
0x4001_4180	0x4001_41FF	128B	U32K1
0x4001_4200	0x4001_43FF	512B	ANA
0x4001_4400	0x4001_44FF	256B	RETRAM
0x4001_4800	0x4001_4FFF	2K	RTC
0x4001_5800	0x4001_5FFF	2K	SPI

4.1. Info Information

The analog trim data and boot option is stored in Info Sector 6 (0x40C00); the RTC calibration data is stored in Info Sector 4 (0x40800). The address 0x40800 ~ 0x409FF data is written by special tool (offline download and RTC calibration). Other data is written before leaving factory. The following table shows the details of this information.

Info Sector data can only be read and cannot be written. All information has a backup. The first data in the form is expressed in 1, and second copies in 2. Each data has a checksum data. Checksum algorithm: add up each data, and reverse the result.

Table 4-2 Info Information Register

Address	Sign	Data	Description
0x00040000		Count	6
0x00040004		Check_sum1	
0x00040008		address0	GPIOA_IE
0x0004000C		value0	Write 0 to the corresponding bit of the non-packaged pin, write 1 to the corresponding bit of other packaged pins.
0x00040010		Check_sum1	
0x00040014		address1	GPIOB_IE
0x00040018		value1	Write 0 to the corresponding bit of the non-packaged pin, write 1 to the corresponding bit of other packaged pins.
0x0004001C		Check_sum1	
0x00040020		address2	GPIOC_IE
0x00040024		value2	Write 0 to the corresponding bit of the non-packaged pin, write 1 to the corresponding bit of other packaged pins.
0x00040028		Check_sum1	
0x0004002C		address3	GPIOD_IE
0x00040030		value3	Write 0 to the corresponding bit of the non-packaged pin, write 1 to the corresponding bit of other packaged pins.
0x00040034		Check_sum1	
0x00040038		address4	GPIOE_IE
0x0004003C		value4	Write 0 to the corresponding bit of the non-packaged pin, write 1 to the corresponding bit of other packaged pins.
0x00040040		Check_sum1	
0x00040044		address5	GPIOF_IE
0x00040048		value5	Write 0 to the corresponding bit of the non-packaged pin, write 1 to the corresponding bit of other packaged pins.
0x0004004C		Check_sum1	
…		…	…
0x00040800	P4	RTC normal temperature offset 1	Load low 16 bits to RTC_ACP4 register, such as 0. (Unit: 0.1ppm).
0x00040804		Check sum 1	INV (SUM (0x40800, 0x40800))
0x00040808	P4	RTC normal temperature offset 2	Load low 16 bits to RTC_ACP4 register, such as 0. (Unit: 0.1ppm).
0x0004080C		Check sum 2	INV (SUM (0x40808, 0x40808))

0x00040810	K1	Crystal secondary calibration coefficient K1 1	Load to RTC_ACK1 register. K1 is calculated as follows: K1=B1/1000000*65536, B1 is the segment factor of crystal oscillator' quadratic curve. For example, the value of K1 is 20827.
0x00040814	K2	Crystal secondary calibration coefficient K2 1	Load to RTC_ACK2 register. K2 is calculated as follows: K2=B2/1000000*65536, B2 is the segment factor of crystal oscillator' quadratic curve. For example, the value of K2 is 21496.
0x00040818	K3	Crystal secondary calibration coefficient K3 1	Load to RTC_ACK3 register. K3 is calculated as follows: K3=B3/1000000*65536, B3 is the segment factor of crystal oscillator' quadratic curve. For example, the value of K3 is 22020.
0x0004081C	K4	Crystal secondary calibration coefficient K4 1	Load to RTC_ACK4 register. K4 is calculated as follows: K4=B4/1000000*65536, B4 is the segment factor of crystal oscillator' quadratic curve. For example, the value of K4 is 24517.
0x00040820	K5	Crystal secondary calibration coefficient K5 1	Load to RTC_ACK5 register. K5 is calculated as follows: K5=B5/1000000*65536, B5 is the segment factor of crystal oscillator' quadratic curve. For example, the value of K5 is 25257.
0x00040824		Check sum 1	INV (SUM (0x40810, 0x40820))
0x00040828	K1	Crystal secondary calibration coefficient K1 2	Load to RTC_ACK1 register. K1 is calculated as follows: K1=B1/1000000*65536, B1 is the segment factor of crystal oscillator' quadratic curve. For example, the value of K1 is 20827.
0x0004082C	K2	Crystal secondary calibration coefficient K2 2	Load to RTC_ACK2 register. K2 is calculated as follows: K2=B2/1000000*65536, B2 is the segment factor of crystal oscillator' quadratic curve. For example, the value of K2 is 21496.
0x00040830	K3	Crystal secondary calibration coefficient K3 2	Load to RTC_ACK3 register. K3 is calculated as follows: K3=B3/1000000*65536, B3 is the segment factor of crystal oscillator' quadratic curve. For example, the value of K3 is 22020.
0x00040834	K4	Crystal secondary calibration coefficient K4 2	Load to RTC_ACK4 register. K4 is calculated as follows: K4=B4/1000000*65536, B4 is the segment factor of crystal oscillator' quadratic curve. For example, the value of K4 is 24517.
0x00040838	K5	Crystal secondary calibration coefficient K5 2	Load to RTC_ACK5 register. K5 is calculated as follows: K5=B5/1000000*65536, B5 is the segment factor of crystal oscillator' quadratic curve. For example, the value of K5 is 25257.
0x0004083C		Check sum 2	INV (SUM (0x40828, 0x40838))
0x00040840	ACTI	Fixed point temperature of crystal 1	Load to RTC_ACTI register, such as 0x1800
0x00040844		Check sum 1	INV (SUM (0x40840, 0x40840))
0x00040848	ACTI	Fixed point temperature of	Load to RTC_ACTI register, such as 0x1800

		crystal 2	
0x0004084C		Check sum 2	INV (SUM (0x40848, 0x40848))
0x00040850	KTEMPx(x=4~1)	Temperature section division settings 1	Load to RTC_ACKTEMP register, such as 0x3C2800EC
0x00040854		Check sum 1	INV (SUM (0x40850, 0x40850))
0x00040858	KTEMPx(x=4~1)	Temperature section division settings 2	Load to RTC_ACKTEMP register, such as 0x3C2800EC
0x0004085C		Check sum 2	INV (SUM (0x40858, 0x40858))
…			Reserved.
0x00040CE0		BAT_R offset 1	(3.6-BAT measure result) * 1000, resister division
0x00040CE4		BAT_C offset 1	(3.6-BAT measure result) * 1000, cap division
0x00040CE8		Check sum 1	INV (SUM (0x40CE0, 0x40CE4))
0x00040CEC			Reserved.
0x00040CF0		BAT_R offset 2	(3.6-BAT measure result) * 1000, resister division
0x00040CF4		BAT_C offset 2	(3.6-BAT measure result) * 1000, cap division
0x00040CF8		Check sum 2	INV (SUM (0x40CF0, 0x40CF4))
0x00040CFC			Reserved.
0x00040D00	P1/P0	RTC_ACP1/0 set 1	Load the high 16 bits to RTC_ACP1 register, such as 1060; Load the low 16 bits to RTC_ACP0, such as -214.
0x00040D04	P2’	RTC_ACP2 set 1	The value in this register is recorded as P2’, such as -19746971. According to the formula P2=P2’+(Tr-Tm)*256 to calculate P2, and load P2 to RTC_ACP2 register.
0x00040D08	P5	RTC_ACP5 set 1	Load the high 16 bits to RTC_ACP5 register, such as 6444 and the low 16 bits are abandoned.
0x00040D0C	P7/P6’	RTC_ACP 7/6 set 1	Load the high 16 bits to RTC_ACP7 register, such as 0. Load the low 16 bits to P6’ register, such as 1342. According to the formula: P6=a*P6’ to calculate P6, where a=PCLK/6553600.
0x00040D10		Check Sum set 1	INV (SUM (0x40DE0, 0x40DEC))
0x00040D14	P1/P0	RTC_ACP1/0 set 2	Load the high 16 bits to RTC_ACP1 register, such as 1060; Load the low 16 bits to RTC_ACP0, such as -214.
0x00040D18	P2’	RTC_ACP2 set 2	The value in this register is recorded as P2’, such as -19746971. According to the formula P2=P2’+(Tr-Tm)*256 to calculate P2, and load P2 to RTC_ACP2 register.
0x00040D1C	P5	RTC_ACP5 set 2	Load the high 16 bits to RTC_ACP5 register, such as 6444 and the low 16 bits are abandoned.
0x00040D20	P7/P6’	RTC_ACP 7/6 set 2	Load the high 16 bits to RTC_ACP7 register, such as 0; Load the low 16 bits to P6’ register, such as 1342. According to the formula: P6=a*P6’ to calculate P6, where a=PCLK/6553600.
0x00040D24		Check Sum set 2	INV (SUM (0x40DF4, 0x40E00))

0x00040D28		VDD_OUT gain 1	Pre-trim result/3.3 * 10000
0x00040D2C		DVCC1 gain 1	Pre-trim result/3.3 * 10000
0x00040D30		ADCBGP gain 1	Pre-trim result/1.2 * 10000
0x00040D34		RCL gain 1	Pre-trim result/32768 * 10000
0x00040D38		RCH gain 1	Pre-trim result/6553600 * 10000
0x00040D3C		Check sum 1	INV(SUM(0x40D28, 0x40D38))
0x00040D40		VDD_OUT gain 2	Pre-trim result/3.3 * 10000
0x00040D44		DVCC1 gain 2	Pre-trim result/3.3 * 10000
0x00040D48		ADCBGP gain 2	Pre-trim result/1.2 * 10000
0x00040D4C		RCL gain 2	Pre-trim result/32768 * 10000
0x00040D50		RCH gain 2	Pre-trim result/6553600 * 10000
0x00040D54		Check sum 2	INV(SUM(0x40D40, 0x40D50))
0x00040D58		ID word 0, Backup 1	
0x00040D5C		ID word 1, Backup 1	
0x00040D60		ID Check sum 1	INV (SUM (0x40D58, 0x40D5C))
0x00040D64		ID word 0, Backup 2	
0x00040D68		ID word 1, Backup 2	
0x00040D6C		ID Check sum 2	INV (SUM (0x40D64, 0x40D68))
0x00040D70	Tr	Real Temperature 1 (from tmp275)	According to the formula P2=P2'+(Tr-Tm)*256 to calculate P2, and load P2 to RTC_ACP2 register.
0x00040D74	Tm	Measure Temperature 1 (from ADC)	
0x00040D78		Temp Check sum 1	INV(SUM(0x40D70, 0x40D74))
0x00040D7C	Tr	Real Temperature 2 (from tmp275)	According to the formula P2=P2'+(Tr-Tm)*256 to calculate P2, and load P2 to RTC_ACP2 register.
0x00040D80	Tm	Measure Temperature 2 (from ADC)	
0x00040D84		Temp Check sum 2	INV (SUM (0x40D7C, 0x40D80))
0x00040D88			Reserved.
0x00040D8C			Reserved.
0x00040D90		Measure LCD LDO gain 1	Pre-trim result/3.3 * 10000
0x00040D94		VLCD setting 1	
0x00040D98		LCD LDO Check sum 1	INV (SUM (0x40D90, 0x40D94))
0x00040D9C		Measure LCD LDO gain 2	Pre-trim result/3.3 * 10000
0x00040DA0		VLCD setting 2	
0x00040DA4		LCD LDO Check sum 2	INV (SUM (0x40D9C, 0x40DA0))
0x00040DC0		Analog trim data1	Program during CP flow for analog parameter

0x00040DC4		0xFFFFFFFF	
0x00040DC8		0xFFFFFFFF	
0x00040DCC		Checksum1	INV (SUM (0x40DC0, 0x40DC8)), the data of 0x00040DC8 address is replaced by 0xFFFFFFFF.
0x00040DD0		Analog trim data2.	Program during CP flow for analog parameter
0x00040DD4		0xFFFFFFFF	
0x00040DD8		0xFFFFFFFF	
0x00040DDC		Checksum2	INV (SUM (0x40DD0, 0x40DD8)), the data of 0x00040DD8 address is replaced by 0xFFFFFFFF.
…			
0x00040400	a1	ADC coefficient 1 of ADC_CHx channel in 3.3V system under no divider mode condition	Vdc=a1/100000000*X+b1/100000000 (32 bits complement)
0x00040404	b1		
0x00040408	a2	ADC coefficient 1 of ADC_CHx channel in 3.3V system under resistive divider mode condition	Vdc=a2/100000000*X+b2/100000000 (32 bits complement)
0x0004040C	b2		
0x00040410	a3	ADC coefficient 1 of ADC_CHx channel in 3.3V system under capacitive divider mode condition	Vdc=a3/100000000*X+b3/100000000 (32 bits complement)
0x00040414	b3		
0x00040418	a4	ADC coefficient 1 of BAT1 channel in 3.3V system under resistive divider mode condition	Vdc=a4/100000000*X+b4/100000000 (32 bits complement)
0x0004041C	b4		
0x00040420	a5	ADC coefficient 1 of BAT1 channel in 3.3V system under capacitive divider mode condition	Vdc=a5/100000000*X+b5/100000000 (32 bits complement)
0x00040424	b5		
0x00040428	a6	ADC coefficient 1 of BAT2 channel in 3.3V system under resistive divider mode condition	Vdc=a6/100000000*X+b6/100000000 (32 bits complement)
0x0004042C	b6		
0x00040430	a7	ADC coefficient 1 of BAT2 channel in 3.3V system under capacitive divider mode condition	Vdc=a7/100000000*X+b7/100000000 (32 bits complement)
0x00040434	b7		

0x00040438		Checksum1	INV(SUM(0x00040400, 0x00040434))
0x0004043C			Reserved.
0x00040440	a1	ADC coefficient 2 of ADC_CHx channel in 3.3V system under no divider mode condition	Vdc=a1/100000000*X+b1/100000000 (32 bits complement)
0x00040444	b1		
0x00040448	a2	ADC coefficient 2 of ADC_CHx channel in 3.3V system under resistive divider mode condition	Vdc=a2/100000000*X+b2/100000000 (32 bits complement)
0x0004044C	b2		
0x00040450	a3	ADC coefficient 2 of ADC_CHx channel in 3.3V system under capacitive divider mode condition	Vdc=a3/100000000*X+b3/100000000 (32 bits complement)
0x00040454	b3		
0x00040458	a4	ADC coefficient 2 of BAT1 channel in 3.3V system under resistive divider mode condition	Vdc=a4/100000000*X+b4/100000000 (32 bits complement)
0x0004045C	b4		
0x00040460	a5	ADC coefficient 2 of BAT1 channel in 3.3V system under capacitive divider mode condition	Vdc=a5/100000000*X+b5/100000000 (32 bits complement)
0x00040464	b5		
0x00040468	a6	ADC coefficient 2 of BAT2 channel in 3.3V system under resistive divider mode condition	Vdc=a6/100000000*X+b6/100000000 (32 bits complement)
0x0004046C	b6		
0x00040470	a7	ADC coefficient 2 of BAT2 channel in 3.3V system under capacitive divider mode condition	Vdc=a7/100000000*X+b7/100000000 (32 bits complement)
0x00040474	b7		
0x00040478		Checksum2	INV(SUM(0x00040440, 0x00040474))

5.Interrupt Controller

5.1. Introduction

Any interrupt can wake up the system from IDLE, some of them can wake up the system from sleep, some of them can wake up the system from deep sleep.

5.2. Feature

5.3. Interrupt Sources

Table 5-1 Interrupt Sources Table

Item	Vector address	Interrupt Num.	Description	Enable bit of peripheral event	Flag of peripheral event	Wake-up source	
						Deep Sleep	Sleep
NMI	00000008h	-14	NMI				
HardFault	0000000Ch	-13	HardFault				
SVCall	0000002Ch	-5	SVCall				
PendSV	00000038h	-2	PendSV				
SysTick	0000003Ch	-1	SysTick				
PMU	00000040h	0	IOA0~1	PMU_CONTROL.0 and PMU_IOAWKUEN.0~1	PMU_IOAINTSTS.0~1	V	V
			Measurement interrupt 0	PMU_CONTROL.0 and PMU_IOAWKUEN.2	PMU_IOAINTSTS.2	V	V
			IOA3~9	PMU_CONTROL.0 And PMU_IOAWKUEN.3~9	PMU_IOAINTSTS.3~9	V	V
			Measurement interrupt 1	PMU_CONTROL.0 and PMU_IOAWKUEN.10	PMU_IOAINTSTS.10	V	V

			IOA11~15	PMU_CONTROL.0 And PMU_IOAWKUEN.11~15	PMU_IOAINTSTS.11~15	V	V
			32K crystal is removed or broken	PMU_CONTROL.2	PMU_STS.0	V	V
			6M crystal is removed or broken	PMU_CONTROL.3	PMU_STS.1		
RTC	00000044h	1	illegal time format	RTC_INTEN.1	RTC_INTSTS.1	V	V
			multi-second period is reach	RTC_INTEN.2	RTC_INTSTS.2	V	V
			multi-minute period is reach	RTC_INTEN.3	RTC_INTSTS.3	V	V
			multi-hour period is reach	RTC_INTEN.4	RTC_INTSTS.4	V	V
			mid-night (00:00) is reach	RTC_INTEN.5	RTC_INTSTS.5	V	V
			32K counter period is reach	RTC_INTEN.6	RTC_INTSTS.6	V	V
			illegal write to CE register	RTC_INTEN.8	RTC_INTSTS.8		
U32K0	00000048h	2	Receiver data input	U32K_CTRL1.0	U32K_STS.0	V	V
			Receive parity error	U32K_CTRL1.1	U32K_STS.1	V	V
			Receive buffer overrun	U32K_CTRL1.2	U32K_STS.2	V	V
U32K1	0000004Ch	3	Same as U32K0				
I2C	00000050h	4	Serial Interrupt	I2C_CTRL2.0	I2C_CTRL.3		
UART0	00000058h	6	Receive	UART_CTRL.3	UART_INTSTS.1		
			Transmit	UART_CTRL.4	UART_INT		

			overrun		STS.2		
			Receive overrun	UART_CTRL.5	UART_INT STS.3		
			Receive parity error	UART_CTRL.7	UART_INT STS.4		
			Transmit done	UART_CTRL.8	UART_INT STS.5		
UART1	0000005Ch	7	Same as UART0				
UART2	00000060h	8	Same as UART0				
-	00000064h	9	-				
UART4	00000068h	10	Same as UART0				
UART5	0000006Ch	11	Same as UART0				
ISO7816	00000070h	12	Receive	ISO7816_CFG.5	ISO7816_ INFO.5		
			Transmit	ISO7816_CFG.6	ISO7816_ INFO.6		
			Receive overrun	ISO7816_CFG.7	ISO7816_ INFO.7		
TMR0	00000078h	14	Timer overflow	TMR_CTRL.3	TMR_INT. 0		
TMR1	0000007Ch	15	Same as TMR0				
TMR2	00000080h	16	Same as TMR0				
TMR3	00000084h	17	Same as TMR0				
PWM0	00000088h	18	PWM timer overflow	PWM_CTL.1	PWM_CTL .0		
			Compare 0	PWM_CCTL0.4	PWM_CCT L0.0		
			Compare 1	PWM_CCTL1.4	PWM_CCT L1.0		
			Compare 2	PWM_CCTL2.4	PWM_CCT L2.0		
PWM1	0000008Ch	19	Same as PWM0				
PWM2	00000090h	20	Same as PWM0				
PWM3	00000094h	21	Same as PWM0				
DMA	00000098h	22	Channel 0 package end	DMA_IE.0	DMA_STS. 4		
			Channel 1 package end	DMA_IE.1	DMA_STS. 5		
			Channel 2 package end	DMA_IE.2	DMA_STS. 6		

			Channel 3 package end	DMA_IE.3	DMA_STS.7		
			Channel 0 frame end	DMA_IE.4	DMA_STS.8		
			Channel 1 frame end	DMA_IE.5	DMA_STS.9		
			Channel 2 frame end	DMA_IE.6	DMA_STS.10		
			Channel 3 frame end	DMA_IE.7	DMA_STS.11		
			Channel 0 data abort	DMA_IE.8	DMA_STS.12		
			Channel 1 data abort	DMA_IE.9	DMA_STS.13		
			Channel 2 data abort	DMA_IE.10	DMA_STS.14		
			Channel 3 data abort	DMA_IE.11	DMA_STS.15		
FLASH	0000009Ch	23	checksum error	FLASH_CTRL.2	FLASH_INT.0		
ANA	000000A0h	24	manual ADC conversion done	ANA_INTEN.0	ANA_INTSTS.0		
			auto ADC conversion done	ANA_INTEN.1	ANA_INTSTS.1		
			COMP1 rising or falling	ANA_INTEN.2	ANA_INTSTS.2	V	V
			COMP2 rising or falling	ANA_INTEN.3	ANA_INTSTS.3	V	V
			VDDALARM rising or falling	ANA_INTEN.7	ANA_INTSTS.7	V	V
			VDCIN rising or falling	ANA_INTEN.8	ANA_INTSTS.8	V	V
			VDDLV rising or falling	ANA_INTEN.10	ANA_INTSTS.10	V	V
			VDCINDROP is 0 and the entry of	ANA_INTEN.11	ANA_INTSTS.11	V	V

			sleep or deep-sleep modes are detected				
			ANA_REGx error	ANA_INTEN.12	ANA_INTSTS.12	V	V
			TADC change over threshold	ANA_INTEN.13	ANA_INTSTS.13	V	V
SPI	000000ACh	27	SPI Transmit	SPI_TXSTS.14	SPI_TXSTS.15		
			SPI Receive	SPI_RXSTS.14	SPI_RXSTS.15		

6.Power system

V94XX(A) power supply has the following features:

- Supporting 2.2~3.6V power supply;

ADC and metering working voltage: 2.6V ~ 3.6V

- When RTCBAT is out of the battery power, RTC will be supplied by the main power.
- The GPIO ports are powered by VDD.
- The analog circuitry inside the chip is powered by VDD;
- The digital circuitry inside the chip and PLL circuitry are powered by DVCC;
- Supporting low voltage monitoring and real-time monitoring battery voltage.

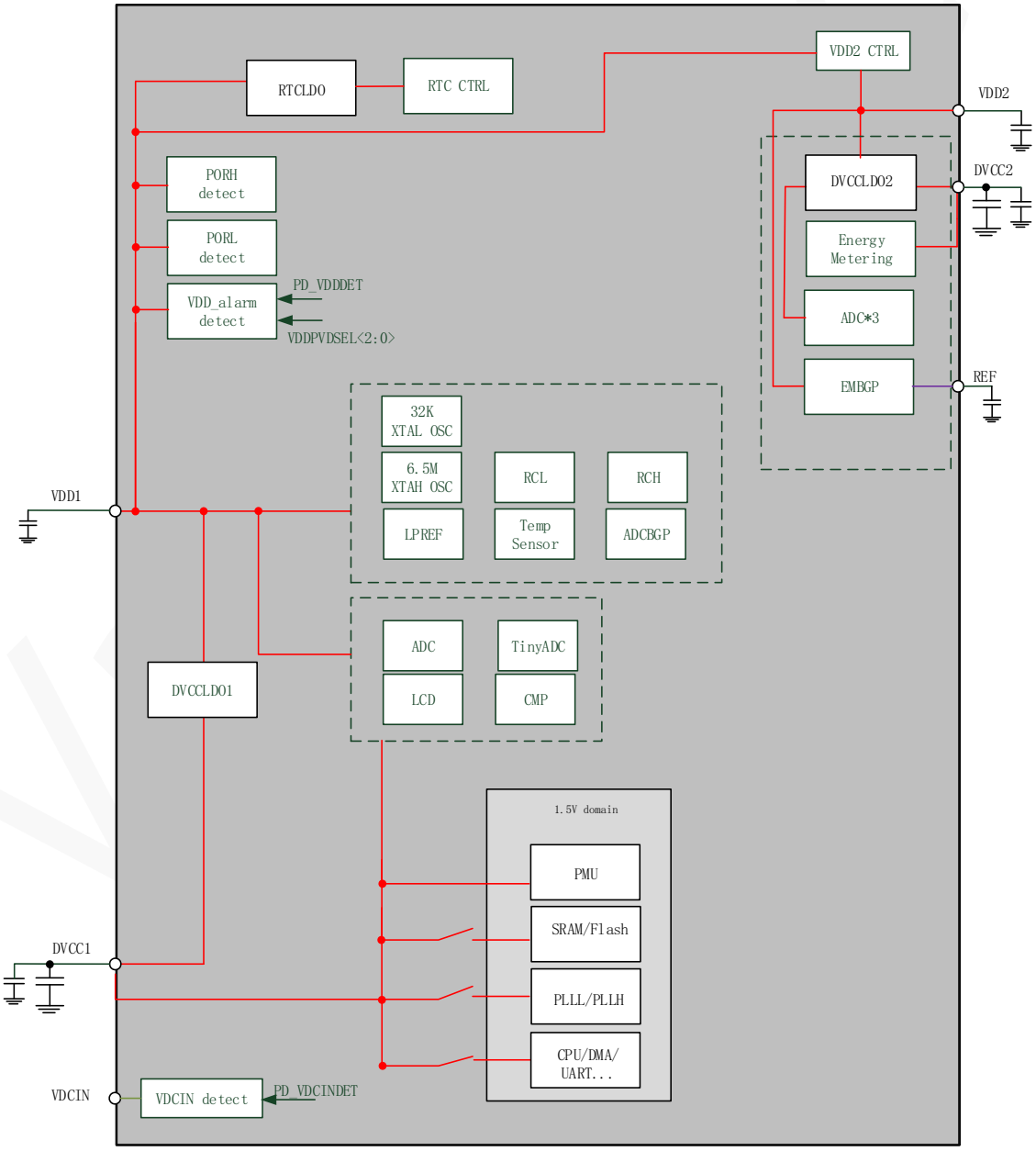


Figure 6-1 V94XX(A) Power System Block Diagram

6.1. Register Location

Table 6-1 Register Location of ANA Controller for Power (ANA Base: 0x40014200)

Name	Type	Address	Description	Default
ANA_REG5	R/W	0x0014	Analog register 5	0x00
ANA_REG6	R/W	0x0018	Analog register 6	0x00
ANA_REG7	R/W	0x001C	Analog register 7	0x00
ANA_REG8	R/W	0x0020	Analog register 8	0x00
ANA_REGA	R/W	0x0028	Analog register 10	0x00
ANA_REGF	R/W	0x003C	Analog register 15	0x00
ANA_CTRL	R/W	0x0050	Analog control register	0x0000000
ANA_CMPOUT	R	0x0054	Comparator result register	0x0030
ANA_INTSTS	R/C	0x0060	Analog interrupt status register	0x0000
ANA_INTEN	R/W	0x0064	Analog interrupt enable register	0x0000

6.2. Register Definition

6.2.1. ANA_REG5 Register

Table 6-2 Description of Each Bit in ANA_REG5 for Power

Bit	Name	Function	Notes
6	VDDLVDETPD	Disable VDD low-voltage detection module. 0: enable 1: disable	0

6.2.2. ANA_REG6 Register

Table 6-3 Description of Each Bit in ANA_REG6 for Power

Bit	Name	Function	Notes
6	BAT1DISC	Discharge the BAT1 battery. Discharge resistance is 1.7k, and the discharge current is VBAT1/1.7k.	0: Disable 1.7k resistor from BAT1 to GND. 1: Enable 1.7k resistor from BAT1 to GND.
7	BAT2DISC	Discharge the BAT2 battery. Discharge resistance is 1.7k, and the discharge current is VBAT2/1.7k.	0: Disable 1.7k resistor from BAT2 to GND. 1: Enable 1.7k resistor from BAT2 to GND.

6.2.3. ANA_REG7 Register

Table 6-4 Description of Each Bit in ANA_REG7 for Power

Bit	Name	Function	Notes
7:0	-	Reserved.	0

6.2.4. ANA_REG8 Register

Table 6-5 Description of Each Bit in ANA_REG8 for Power

Bit	Name	Function	Notes
3:0	-	Reserved.	0
6:4	VDDPVDSEL[2:0]	Voltage selection of VDD power detector, the setting in this register will affect the status of VDDALARM.	000: Reserved 001: Reserved 010: Reserved 011: 3.6V 100: 3.2V 101: 2.9V 110: 2.6V 111: 2.3V
7	-	Reserved.	The default value is 0, which must be configured as 1.

6.2.5. ANA_REG9 Register

Table 6-6 Description of Each Bit in ANA_REG9 for Power

Bit	Name	Function	Notes
7	PD_VDDDET	Power down VDD input VDDALARM detector. This module powered by VDD.	0: Power up. 1: Power down.

6.2.6. ANA_REGA Register

Table 6-7 Description of Each Bit in ANA_REGA for Power

Bit	Name	Function	Notes
6:0		Reserved.	Default value is 0x00, and must be set to 0x0A.
7	PD_VDCINDET	Power down VDCIN detector.	0: Power up. 1: Power down.

6.2.7. ANA_REGF Register

Table 6-8 Description of Each Bit in ANA_REGF for Power

Bit	Name	Function	Notes
1:0		Reserved.	0
2	VDDO_EN	Enable VDD_OUT pin to output VDD level.	0: High resistance. 1: VDD_OUT pin output VDD level, and it can be used to drive small power module.

6.2.8. ANA_CTRL Register

Table 6-9 Description of ANA_CTRL Register for Power

Bit	Name	Type	Description	Default
26	PDNS2	R/W	This register is used to set the deep sleep behavior when VDDALARM is 0. (Still need to consider the PDNS setting). 0: Can't enter deep-sleep mode when VDDALARM is 0. When VDDALARM is 1, the system can enter deep-sleep mode. The system will wake-up from deep-sleep mode automatically as long as VDDALARM is 0. 1: Can enter deep-sleep mode no-matter which state VDDALARM is.	0x0
17:16			Reserved.	0
6	PDNS	R/W	This register is used to set the deep sleep behavior when VDCINDROP is 0. (Still need to consider the PDNS setting) 0: Can't enter deep-sleep mode when VDCINDROP is 0. When VDCINDROP is 1, the system can enter deep-sleep mode. The system will wake-up from deep-sleep mode automatically as long as VDCINDROP became 0. 1: Can enter deep-sleep mode no-matter which state VDCINDROP is.	0x0
5:4			Reserved.	0

6.2.9. ANA_CMPOUT Register

Table 6-10 Description of ANA_CMPOUT Register for Power

Bit	Name	Type	Description	Default
8	VDCINDROP	R	VDCIN drop status. 0: VDCIN is not drop (VDCIN higher than threshold). 1: VDCIN is drop (VDCIN lower than threshold).	0x0
7	VDDALARM	R	This bit shows the output of VDDALARM. 0: Voltage of VDD is higher than voltage setting by VDDPVDSEL. 1: Voltage of VDD is lower than voltage setting by VDDPVDSEL.	0x0
6:0		R	Reserved.	0

6.2.10. ANA_INSTS Register

Table 6-11 Description of ANA_INTSTS Register for Power

Bit	Name	Type	Description	Default
11	INTSTS11	R/C	Interrupt flag of sleep mode entry under VDCINDROP is	0x0

			0(i.e. VDCIN higher than threshold), this interrupt will be generated when VDCINDROP is 0 and the entry of sleep or deep-sleep modes are detected. Programmer can enable this interrupt to force CPU awake from sleep or deep-sleep mode when VDCINDROP is 0 and the entry of sleep or deep-sleep modes are detected. Read 0: No Sleep mode entry interrupt. Read 1: Sleep mode entry interrupt is happened. Write 0: No effect. Write 1: clear this bit.	
10	INTSTS10	R/C	Interrupt flag of VDDLV (VDD low power status), this interrupt will be generated when VDDLV rising or falling. Read 0: No VDDLV interrupt. Read 1: VDDLV interrupt is happened. Write 0: No effect. Write 1: clear this bit.	0x0
8	INTSTS8	R/C	Interrupt flag of VDCINDROP (VDCIN status), this interrupt will be generated when VDCINDROP rising or falling. Read 0: No VDCIN interrupt. Read 1: VDCIN interrupt is happened. Write 0: No effect. Write 1: clear this bit.	0x0
7	INTSTS7	R/C	Interrupt flag of VDDALARM (VDD status), this interrupt will be generated when VDDALARM rising or falling. Read 0: No VDDALARM interrupt. Read 1: VDDALARM interrupt is happened. Write 0: No effect. Write 1: clear this bit.	0x0
6:0	-	-	Reserved.	0

6.2.11. ANA_INTEN Register

Table 6-12 Description of ANA_INTEN Register for Power

Bit	Name	Type	Description	Default
11	INTEN11	R/W	Interrupt and wake-up enable control of sleep mode entry, when VDCINDROP is 0 (i.e. VDCIN higher than threshold). Programmer can enable this interrupt to force CPU to wake from sleep or deep-sleep mode when VDCINDROP is 0 and the entry of sleep or deep-sleep modes are detected. 0: Disable Sleep mode entry interrupt and wake-up. 1: Enable Sleep mode entry interrupt and wake-up.	0x0
10	INTEN10	R/W	Interrupt and wake-up enable control of VDDLV rising or falling. 0: Disable VDDLV interrupt and wake-up. 1: Enable VDDLV interrupt and wake-up.	0x0

9			Reserved.	0
8	INTEN8	R/W	Interrupt and wake-up enable control of VDCINDROP rising or falling. 0: Disable VDCIN interrupt and wake-up. 1: Enable VDCIN interrupt and wake-up.	0x0
7	INTEN7	R/W	Interrupt and wake-up enable control of VDDALARM rising or falling. 0: Disable VDDALARM interrupt and wake-up. 1: Enable VDDALARM interrupt and wake-up.	0x0
6:0			Reserved.	0

6.3. Digital Power Supply(DVCC)

In V94XX(A), PLL clock generation circuit and core digital blocks are powered by the digital power supply circuit. This circuit will output a stable voltage (DVCC, i.e. 1.5V) when power input (VDD) is higher than 1.7V.

The digital power supply circuit has a driving capability of 35mA. When the load current through the circuits is less than 35mA, the digital power supply will be stable; when the load current is higher than 35mA, the higher the load current is, the lower the digital power supply will be.

This power supply circuit will not stop working until the system is powered off.

It is recommended to externally decouple the pin 'DVCC' with a 10uF capacitor in parallel with a 0.1-uF capacitor.

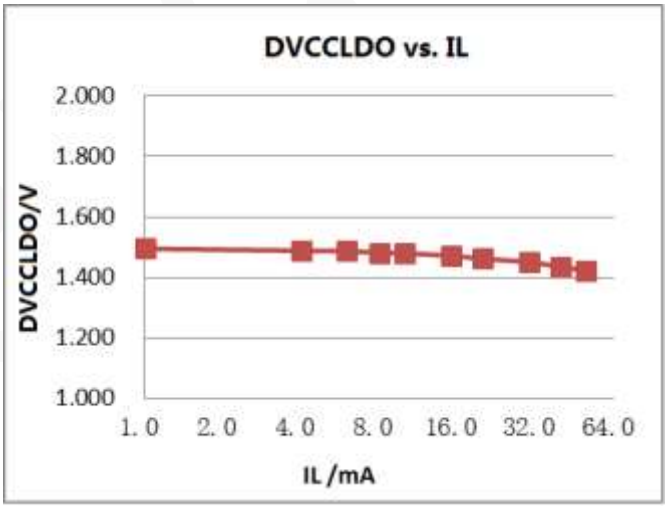


Figure 6-2 DVCCLDO Output and The Load Current

Power Supply Supervisor

6.4. Power Supervisor

6.4.1. VDCIN Supervisor

In V94XX(A), the main power is input into the pin 'VDCIN' after a resistive divider. The input voltage on the pin 'VDCIN' is monitored continuously by the power supply supervisor.

When the input voltage on the pin 'VDCIN' is lower than 1.3V(typical), a power-down event will occur, the bit 'VDCINDROP'('bit 8' of 'ANACMP_OUT') will be set to '1', and a power-down interrupt will be generated to MCU.

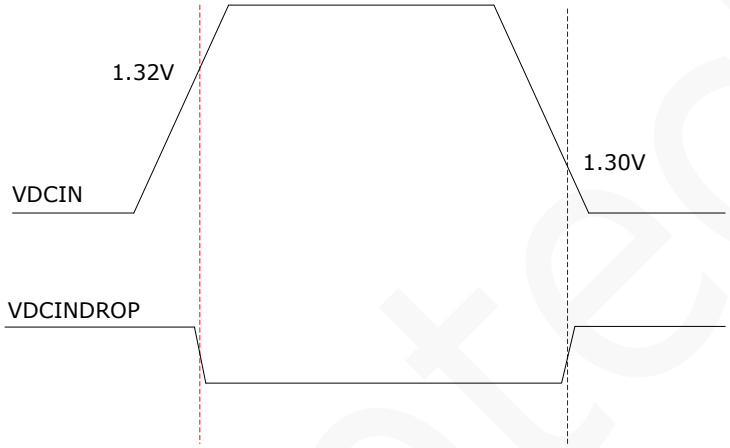


Figure 6-3 Relation Between VDCIN Input Signal and States of Flag Bits VDCINDROP

6.4.2. VDD Supervisor

Power alarm detector is designed to supervise the power state of VDD. When VDD is lower than the specified voltage threshold defined by VDDPVDSEL<2:0> in ANA_REG8, the power alarm signal will inform MCU by interrupt.

VDDPVDSEL<2:0>	Voltage selection of power detector	000: Reserved; 001: Reserved; 010: Reserved; 011: 3.6V; 100: 3.2V; 101: 2.9V; 110: 2.6V; 111: 2.3V

VDDLV module is designed to supervise the power state of VDD. When VDD is lower than 2.5V, an LV signal will inform MCU by interrupt, in this situation, the ADC precision will be degraded much, so do not use ADC to measure any signal.

7.Working Model

7.1. Introduction

The PMU controller is used to control the sleep and deep sleep mode of V94XX(A). There are 16 IOs integrated inside the PMU controller which can wake-up the chip from sleep or deep-sleep mode. The deep sleep mode will power off CPU and all peripherals including system SRAM, LCD controller and other GPIOs not included in PMU controller.

7.2. Features

--Deep mode entry/exit control, and corresponding module be reset when MCU wake up from deep sleep mode, the program starts to run from 0 address.

--Password protection to avoid entry deep-sleep mode in un-expected event.

--16 GPIOs with wake-up and interrupt function.

--Interrupt generation.

--When entry sleep and deep sleep mode, system clock will power down. When MCU wake up from sleep mode, hardware will switch the system clock to the setting before entry sleep mode. When MCU wake up from deep sleep mode, the hardware will switch the system clock to RCH automatically.

-- When wake up from deep sleep mode, the program will start from beginning and reset some corresponding modules.

--Crystal absent detect and interrupt.

--Embedded 256 Bytes Retention SRAM which can keep necessary data under deep-sleep mode.

7.3. Functional Block Diagram

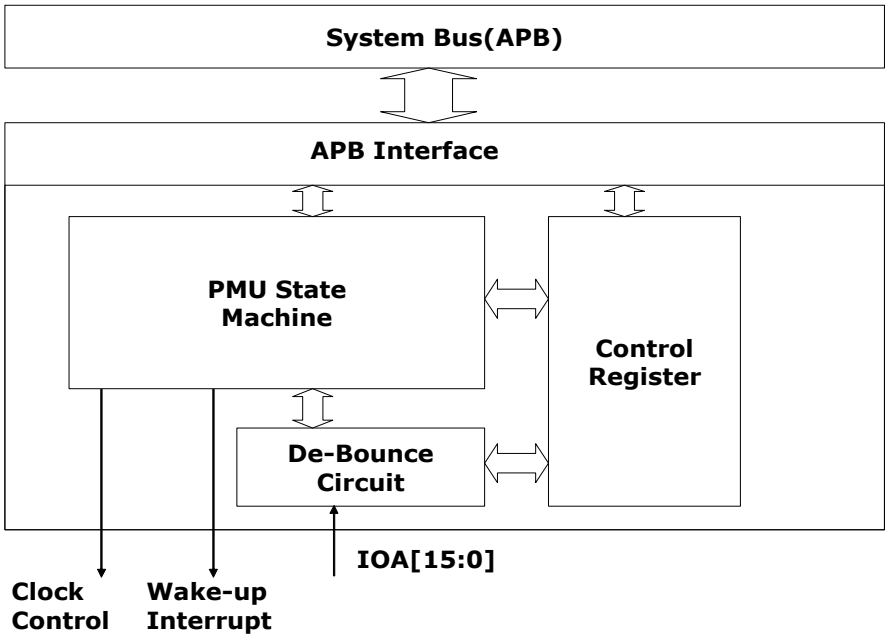


Figure 7-1 Functional Block Diagram of PMU Controller

7.4. PMU Register Location

Table 7-1 PMU Registers Map

Register Name	Offset	Type	Reset Value	Description
PMU_DSLEEPEN	0x0000	rw	0x0000_0000	PMU deep sleep enable register
PMU_DSLEEPPASS	0x0004	rw	0x0000_0000	PMU deep sleep password register
PMU_CONTROL	0x0008	rw	0x0000_0000	PMU control register
PMU_STS	0x000C	rc_w1	0x0000_0074	PMU Status register
PMU_IOAOEN	0x0010	rw	0x0000_FFFF	IOA output enable register
PMU_IOAIE	0x0014	rw	0x0000_FFFF	IOA input enable register
PMU_IOADAT	0x0018	rw	0x0000_0000	IOA data register
PMU_IOAATT	0x001C	rw	0x0000_0000	IOA attribute register
PMU_IOAWKUEN	0x0020	rw	0x0000_0000	IOA wake-up enable register
PMU_IOASTS	0x0024	r	0x0000_0000	IOA input status register
PMU_IOAINTSTS	0x0028	rc_w1	0x0000_0000	IOA interrupt status register
PMU_IOASEL	0x0038	rw	0x0000_0000	IOA special function select register
PMU_WDTPASS	0x0040	rw	0x0000_0000	Watch dog timing unlock register
PMU_WDTEN	0x0044	rw	0x0000_0001	Watch dog timer enable register
PMU_WDTCLR	0x0048	w	0x0000_0000	Watch dog timer clear register
PMU_IOANODEG	0x0050	rw	0x0000_0000	IOA no-deglitch control register.

7.5. PMU Register Definitions

7.5.1. PMU_DSLEEPEN Register

To enable the deep sleep mode, programmer should write the correct password (0xAA5555AA) into PMU_DSLEEPPASS register first, and then write 0x55AAAA55 to PMU_DSLEEPEN register. Under debug mode (MODE is 0), it is not allowed to enter deep-sleep mode, and all writes to this register will be discarded. If the chip is in deep-sleep mode and MODE change from normal mode to debug mode, it will wake-up automatically to enable the access of ICE interface.

Table 7-2 PMU_DSLEEPEN Register Description

Bit	Name	Type	Description
31	WKU	r	Current wake-up signal status, this bit reflects the wake-up status received by PMU controller, programmer must make sure this bit is 0 before entering deep-sleep mode, otherwise the system will wake-up immediately because of non-clear WKU event.
30:0	Rsvd	-	Reserved.

7.5.2. PMU_DSLEEPPASS Register

Table 7-3 PMU_DSLEEPPASS Register Description

Bit	Name	Type	Description
31:1	Rsvd	-	Reserved.
0	UNLOCK	r	This bit indicates the entry of deep-sleep mode has been unlocked and is ready to entry deep-sleep mode. To unlock the deep sleep mode, programmer should write 0xAA5555AA to this register first. This bit will be cleared immediately after any register read or write to any PMU register, including ICE read/write. So programmer should set correct password to PMU_DSLEEPEN immediately.

7.5.3. PMU_CONTROL Register

Table 7-4 PMU_CONTROL Register Description

Bit	Name	Type	Description
31:16	Rsvd	-	Reserved.
15:8	PWUPCYC	rw	Power-up cycle count, this register controls the power-up wait time when a wake-up even is received. The unit is 32K clock period.
7:6	Rsvd	-	Reserved.
5	PLLL_SEL	rw	Low speed PLL input clock selection. 0: 32K XTAL 1: 32K RC.

4	PLLH_SEL	rw	High speed PLL input clock selection. 0: 6.5MHz RC 1: 6.5536MHz XTAL
3	INT_6M_EN	rw	6.5536M XTAL absent interrupt enable register. This bit is used to control the interrupt signal output to CPU. When this bit is set to 1, if 6.5536M crystal is removed or broken, an interrupt will be issued to CPU. And if this event is happened during sleep or deep sleep, CPU will be waked up.
2	INT_32K_EN	rw	32K XTAL absent interrupt enable register. This bit is used to control the interrupt signal output to CPU. When this bit is set to 1, if 32K crystal is removed or broken, an interrupt will be issued to CPU. And if this event is happened during sleep or deep sleep, CPU will be waked up.
1	RTCCLK_SEL	rw	RTC Clock selection. 0: 32K XTAL 1: 32K RC
0	INT_IOA_EN	rw	IOA0~15 interrupt enable register. This bit is used to control the interrupt signal output to CPU. User can set some of the IO pins as wake-up source during sleep or deep sleep.

7.5.4. PMU_STS Register

Table 7-5 PMU_STS Register Description

Bit	Name	Type	Description
31:25	Rsvd	-	Reserved.
24	MODE	r	This register shows the current status of MODE pin. 0: Debug mode. 1: Normal mode.
23:7	Rsvd	-	Reserved.
6	DPORST	rc_w1	This bit indicated if the last reset is caused by internal digital power-on reset signal, and this bit is set to 1 only when the chip power supply first time. Write 1 to clear this bit.
5	PORST	rc_w1	This bit indicated if the last reset is caused by PORH reset or PORL reset. PORH reset is caused when VDD voltage is lower than 2.08V. PORL reset is caused when DVCCLDO1 voltage is lower than 1.3V. Write 1 to clear this bit.
4	EXTRST	rc_w1	This bit indicated if the last interrupt is cause by external reset signal. Write 1 to clear this bit.
3	EXIST_6M	r	6.5536M XTAL exist status register. This bit represents 6.5536M XTAL is existed or absent. After 6.5536MHz XTAL (BIT7 of ANA_REG3 is configured as 1) is turned on, the state bit will refresh, otherwise it will remain in its previous state. 0: 6.5536M crystal is absent. 1: 6.5536M crystal is existed.
2	EXIST_32K	r	32K XTAL exist status register. This bit represents 32K XTAL is existed or absent.

			0: 32K crystal is absent. 1: 32K crystal is existed.
1	INT_6M	rc_w1	This bit represents the 6.5536M crystal absent interrupt status. When this bit is set to 1, it means the 6.5536M crystal is removed or broken. When the EXIST_6M state goes from 1 to 0, the state position is 1. Write 1 to this bit can clear this flag to 0.
0	INT_32K	rc_w1	This bit represents the 32K crystal absent interrupt status. When this bit is set to 1, it means the 32K crystal is removed or broken. When the EXIST_32K state goes from 1 to 0, the state position is 1. Write 1 to this bit can clear this flag to 0.

7.5.1. PMU_IOAOEN Register

Table 7-6 PMU_IOAOEN Register Description

Bit	Name	Type	Description
31:16	Rsvd	-	Reserved.
15:0	IOAOEN	rw	Each bit controls the IOA output enable signal Refer to Table 16-6 for detail of IO state. 0: Enable IO's output function. 1: Disable IO's output function.

7.5.2. PMU_IOAIE Register

Table 7-7 PMU_IOAIE Register Description

Bit	Name	Type	Description
31:16	Rsvd	-	Reserved.
15:0	IOAIE	rw	Each bit controls the IOA input enable signal Refer to Table 16-6 for detail of IO state. 0: Disable IO's input function. 1: Enable IO's input function.

7.5.3. PMU_IOADAT Register

Table 7-8 PMU_IOADAT Register Description

Bit	Name	Type	Description
31:16	Rsvd	-	Reserved.
15:0	IOADAT	rw	Each bit controls the IOA output data and pull low/high function Refer to Table 16-6 for detail of IO state.

7.5.4. PMU_IOAATT Register

Table 7-9 PMU_IOAATT Register Description

Bit	Name	Type	Description
31:16	Rsvd	-	Reserved.
15:0	IOAATT	rw	Each bit controls the IOA attribute Refer to Table 16-6 for detail of IO state. When an IO is set to output mode (GPIO or special function), this bit is used to control the CMOS or open drain mode of the IO pad. 0: CMOS mode. 1: Open drain mode (disable PMOS output).

Table 7-10 IO Status under Different Kind of Setting

IOx Setting			IO Status
IOxOEN	IOxDAT	IOxATT	
1	0	0	Disable output function.
1	1	0	Disable output function.
1	0	1	Disable output function.
1	1	1	Disable output function.
0	0	0	Output low
0	1	0	Output high
0	0	1	Open drain output low.
0	1	1	Open drain pull-high

7.5.5. PMU_IOAWKUEN Register

Table 7-11 PMU_IOAWKUEN Register Description

Bit	Name	Type	Description
31:0	IOAWKUEN	rw	Every 2 bits control the IOA wake up or interrupt enable function. Bit [1:0]: IOA0WKUEN[1:0] Bit [3:2]: IOA1WKUEN[1:0] …… Bit [31:30]: IOA15WKUEN[1:0] Refer to Table 16-8 for detail of each wake-up mode.

Table 7-12 Description of each IO wake-up mode

IOAyWKUEN[1:0]	IOAyDAT	Wake-up Event
0	X	Disable wake-up function
1	0	Rising edge
	1	Falling Edge
2	0	High Level
	1	Low level
3	X	Rising or falling edge

Which y=0 ... 15, indicating an IO port.

For rising edge or falling edge wake-up source, since the H/W will use the final latch IO status before entering sleep or deep-sleep mode, so the programmer needs to wait until the IO status change back to normal state. For example, when rising edge mode is chosen, the programmer should wait until the IO status back to low state to ensure the rising edge can be detected correctly. For high level or low level source, IO have no debounce in normal interrupt or wake up from sleep or deep sleep mode, but IO have four RTCCLK clock cycles debounce When CPU wake up from sleep or deep sleep mode.

7.5.6. PMU_IOASTS Register

Table 7-13 PMU_IOASTS Register Description

Bit	Name	Type	Description
31:16	Rsvd	-	Reserved.
15:0	IOASTS	r	Each bit represents the current IOA input data value.

7.5.7. PMU_IOAINTSTS Register

Table 7-14 PMU_IOAINTSTS Register Description

Bit	Name	Type	Description
31:16	Rsvd	-	Reserved.
15:0	IOAINTSTS	rc_w1	Each bit represents the IOA interrupt status. The corresponded bit will be set to 1 when corresponded wake-up event is detected. This register can be clear to 0 by writing corresponded bit to 1.

7.5.8. PMU_IOASEL Register

Table 7-15 PMU_IOASEL Register Description

Bit	Name	Type	Description
31:8	Rsvd	-	Reserved.
7	IOA_SEL7	rw	IOA7 special function select register. 0: GPIO 1: Special function 1 (RTC_PLLDIV).
6	IOA_SEL6	rw	IOA6 special function select register. 0: GPIO 1: Special function 2 (CMP2_O).
5:4	Rsvd	-	Reserved.
3	IOA_SEL3	rw	IOA3 special function select register. 0: GPIO 1: Special function 1 (RTC_PLLDIV).
2:0	Rsvd	-	Reserved.

7.5.1. PMU_WDTPASS Register

Table 7-16 PMU_WDTPASS Register Description

Bit	Name	Type	Description
31:1	Rsvd	-	Reserved.
0	UNLOCK	r	This bit indicates the watch dog timer enable register has been unlocked and is ready to change the watch dog enable control register. To set this bit to 1, programmer should write 0xAA5555AA to this register. This bit will be cleared immediately after any register write to any PMU control register, including ICE write, so programmer should set the PMU_WDTEN immediately after the UNLOCK bit is set to 1, otherwise the UNLOCK procedure should start again.

7.5.2. PMU_WDTEN Register

Table 7-17 PMU_WDTEN Register Description

Bit	Name	Type	Description
31:4	Rsvd	-	Reserved.
3:2	WDTSEL	rw	This register is used to control the WDT counting period. 0: 2 secs 1: 1 sec 2: 0.5 secs 3: 0.25 secs To change the value of this register, UNLOCK bit of PMU_WDTPASS should be set to 1 first.
1	Rsvd	-	Reserved.
0	WDTEN	rw	This bit indicates the watch dog timer is enable. To change the value of this register, UNLOCK bit of PMU_WDTPASS should be set to 1 first.

7.5.3. PMU_WDTCLR Register

Table 7-18 PMU_WDTCLR Register Description

Bit	Name	Type	Description
31:16	Rsvd	-	Reserved.
15:0	WDTCNT	rc_w1	This register shows the current counter value of wat dog timer. When this timer count to limit value set by WDTSEL, the WDT will issue a system reset. So programmer should clear this timer in a regulator time to avoid WDT reset. To clear this timer programmer should write 0x55AAAA55 to this register. During debug mode, this register will be cleared to 0 automatically and no WDT reset will be issued under the debug mode.

7.5.4. PMU_IOANODEG Register

Table 7-19 PMU_IOANODEG Register Description

Bit	Name	Type	Description
31:16	Rsvd	-	Reserved.
15:0	IOANODEG	rw	Each bit control if the IOA wake-up signal will go through de-glitch circuit or not. If set this bit to 1, the corresponded IOA wake-up signal will not go through de-glitch circuit which can have a faster wake-up time. This bit affect the edge wake-up signal under sleep and deep-sleep mode. 0: IOA wake-up signal will go through de-glitch circuit. 1: IOA wake-up signal will not go through de-glitch circuit.

7.6. Retention RAM Location

Table 7-20 RETRAM Registers Map

Register Name	Offset	Type	Reset Value	Description
RETRAM_RAMx[0..63,0x4]	0x0000	rw	0x0000_0000	PMU 32 bits Retention RAM x

7.7. Retention RAM Definition

7.7.1. RETRAM_RAMx Register

Table 7-21 RETRAM_RAMx Register Description

Bit	Name	Type	Description
31:0	RAM	rw	There is a 256 bytes (64x32) SRAM is embedded in the PMU controller. This RAM can retain data in deep-sleep mode. Only word access is allowed to these ports.

7.8. Register Address

Table 7-22 Register Location of ANA Controller for Working Mode (ANA Base: 0x40014200)

Name	Type	Address	Description	Default
ANA_CTRL	R/W	0x0050	Analog control register	0x0000000

7.9. Register Definitions

7.9.1. ANA_CTRL Register

Table 7-23 Description of ANA_CTRL Register

Bit	Name	Type	Description	Default
26	PDNS2	R/W	This register is used to set the deep sleep behavior when	0x0

			VDDALARM is 0. (Still need to consider the PDNS setting). 0: Can't enter deep-sleep mode when VDDALARM is 0. When VDDALARM is 1, the system can enter deep-sleep mode. The system will wake-up from deep-sleep mode automatically as long as VDDALARM became 0. 1: Can enter deep-sleep mode no-matter which state VDDALARM is.	
6	PDNS	R/W	This register is used to set the deep sleep behavior when VDCINDROP is 0 (Still need to consider the PDNS setting). 0: Can't enter deep-sleep mode when VDCINDROP is 0. When VDCINDROP is 1, the system can enter deep-sleep mode. The system will wake-up from deep-sleep mode automatically as long as VDCINDROP became 0. 1: Can enter deep-sleep mode no-matter which state VDCINDROP is.	0x0

7.10. Reset

After exit from each mode, some of the hardware module will be reset automatically, the following table shows the detail of reset of each module.

Table 7-24 Reset of Each Module under Different Events

Module	External Reset	Power-on Reset	Watch-dog Reset	M0-soft Reset	Wake up from		
					deep sleep	sleep	idle
Cortex-M0	V	V	V	V	V	-	-
System SRAM	-	-	-	-	Data lost	-	-
Retention SRAM	-	-	-	-	-	-	-
PMU (IOA)	V	V	V	-	-	-	-
WDT	V	V	V	-	-	-	-
RTC	V*	V*	V*	-	-	-	-
UART 32K 0	V	V	V	-	-	-	-
UART 32K 1	V	V	V	-	-	-	-
Analog Controller	V	V	V	-	-	-	-
LCD	V	V	V	V	V	-	-
GPIO (IOB~IOF)	V	V	V	V	V	-	-
MISC2	V	V	V	V	V	-	-
MISC	V	V	V	V	V	V	-
I2C	V	V	V	V	V	V	-
SPI	V	V	V	V	V	V	-
UART	V	V	V	V	V	V	-
ISO7816	V	V	V	V	V	V	-
TIMER	V	V	V	V	V	V	-
PWM	V	V	V	V	V	V	-
DMA	V	V	V	V	V	V	-

SRAM Controller	V	V	V	V	V	V	-
FLASH Controller	V	V	V	V	V	V	-
Electric Energy Metering	V	V	V	V	V	V	-

Note (V*): RTC registers without write protection can be reset under external reset or power-on reset or watch-dog reset, other registers cannot be reset under one of reset external reset or power-on reset or watch-dog reset events.

For different mode, the enable or disable of clock generated module will be controlled by hardware or software, the following tables shows the detail of clock status under each mode.

Table 7-25 Clock Source Enable or Disable in Different Modes

Clock Source	Power modes			
	Deep sleep	Sleep	IDLE	Active
6.5536M RC	OFF	OFF	Controlled by RCHPD	
6.5536M XTAL	OFF	OFF	Controlled by XOHPDN	
PLLH	OFF	OFF	Controlled by PLLHPDN	
PLLL	OFF	OFF	Controlled by PLLLPDN	
32K RC	ON	ON	ON	
32K XTAL	ON	ON	ON	

Clock Source	Wake up from different modes		
	Deep sleep	Sleep	IDLE
6.5536M RC	ON	Controlled by RCHPD	
6.5536M XTAL	OFF	Controlled by XOHPDN	
PLLH	OFF	Controlled by PLLHPDN	
PLLL	OFF	Controlled by PLLLPDN	
32K RC	ON	ON	
32K XTAL	ON	ON	

7.10.1. External Reset

The external reset pin (EXTRSTN) can reset most of the modules inside V94XX(A). In order to prevent the external noise couple into this pin, a de-glitch circuit is embedded in V94XX(A). The following diagram shows an example of how this de-glitch circuit works. The de-glitch time will increase accordingly when the RTCCLK pre-scaler is set to a non-zero value. For example, when RTCCLK pre-scaler is set to 1/4, the de-glitch time will be increased to 91*4 = 364 μs.

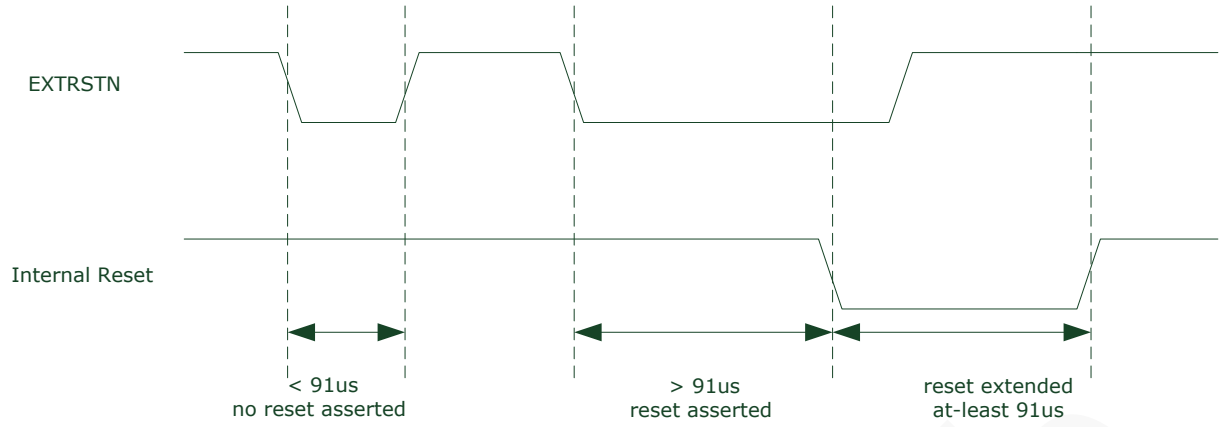


Figure 7-2 External Reset De-glitch Timing

7.10.2. WDT Reset

WDT's reset level is the same as POR.

7.10.3. POR Reset

The POR module can provide chip's internal reset, should work with external reset together.

7.10.4. M0-soft Reset

M0-soft reset instruction can reset the most modules in V94XX(A), details please refer to Figure 6-2.

7.10.5. Wake up from sleep /deep sleep/IDLE

Any interrupt can wake up the system from IDLE, some of them can wake up the system from sleep, and some of them can wake up the system from deep sleep.

Table 7-26 Interrupt Sources

Item	Vector address	Interrupt Nom.	Description	Enable bit of peripheral event	Flag of peripheral event	Wake-up source	
						Deep Sleep	Sleep
NMI	00000008h	-14	NMI				
HardFault	0000000Ch	-13	HardFault				
SVCall	0000002Ch	-5	SVCall				
PendSV	00000038h	-2	PendSV				
SysTick	0000003Ch	-1	SysTick				
PMU	00000040h	0	IOA0~1	PMU_CONTROL.0 and PMU_IOAWKUEN.0~1	PMU_IOAINTSTS.0~1	V	V
			Measurement interrupt 0	PMU_CONTROL.0 and	PMU_IOAINTSTS.2	V	V

				PMU_IOAWKUEN.2			
			IOA3~9	PMU_CONTROL.0 And PMU_IOAWKUEN.3~9	PMU_IOAINTSTS.3~9	V	V
			Measurement interrupt 1	PMU_CONTROL.0 and PMU_IOAWKUEN.10	PMU_IOAINTSTS.10	V	V
			IOA11~15	PMU_CONTROL.0 And PMU_IOAWKUEN.11~15	PMU_IOAINTSTS.11~15	V	V
			32K crystal is removed or broken	PMU_CONTROL.2	PMU_STS.0	V	V
			6M crystal is removed or broken	PMU_CONTROL.3	PMU_STS.1		
RTC	00000044h	1	illegal time format	RTC_INTEN.1	RTC_INTSTS.1	V	V
			multi-second period is reach	RTC_INTEN.2	RTC_INTSTS.2	V	V
			multi-minute period is reach	RTC_INTEN.3	RTC_INTSTS.3	V	V
			multi-hour period is reach	RTC_INTEN.4	RTC_INTSTS.4	V	V
			mid-night (00:00) is reach	RTC_INTEN.5	RTC_INTSTS.5	V	V
			32K counter period is reach	RTC_INTEN.6	RTC_INTSTS.6	V	V
			illegal write to CE register	RTC_INTEN.8	RTC_INTSTS.8		
U32K0~1	00000048h 0000004Ch	2\3	Receiver data input	U32Kx_CTRL1.0	U32Kx_STS.0	V	V
			Receive parity error	U32Kx_CTRL1.1	U32Kx_STS.1	V	V
			Receive buffer overrun	U32Kx_CTRL1.2	U32Kx_STS.2	V	V
I2C	00000050h	4	Serial Interrupt	I2C_CTRL2.0	I2C_CTRL.3		

SPI	000000ACh	27	SPI Transmit	SPI_TXSTS.14	SPI_TXSTS.15		
			SPI Receive	SPI_RXSTS.14	SPI_RXSTS.15		
UART0/1/2/4/5	00000058h/ 0000005Ch/ 00000060h/ 00000068h/ 0000006Ch	6\7\8\10\11	Receive	UARTx_CTRL.3	UARTx_INTSTS.1		
			Transmit overrun	UARTx_CTRL.4	UARTx_INTSTS.2		
			Receive overrun	UARTx_CTRL.5	UARTx_INTSTS.3		
			Receive parity error	UARTx_CTRL.7	UARTx_INTSTS.4		
			Transmit done	UARTx_CTRL.8	UARTx_INTSTS.5		
ISO7816	00000070h	12	Receive	ISO7816_CFG.5	ISO7816_INFO.5		
			Transmit	ISO7816_CFG.6	ISO7816_INFO.6		
			Receive overrun	ISO7816_CFG.7	ISO7816_INFO.7		
Timer0~3	00000078h ~ 00000084h	14\15\16\17	Timer x overflow	TMRx_CTRL.3	TMRx_INT.0		
PWM0~3	00000088h ~ 00000094h	18\19\20\21	PWM timer overflow	PWMx_CTL.1	PWMx_CTL.0		
			Compare 0	PWMx_CCTL0.4	PWMx_CCTL0.0		
			Compare 1	PWMx_CCTL1.4	PWMx_CCTL1.0		
			Compare 2	PWMx_CCTL2.4	PWMx_CCTL2.0		
DMA	00000098h	22	Channel 0 package end	DMA_IE.0	DMA_STS.4		
			Channel 1 package end	DMA_IE.1	DMA_STS.5		
			Channel 2 package end	DMA_IE.2	DMA_STS.6		
			Channel 3 package end	DMA_IE.3	DMA_STS.7		
			Channel 0 frame end	DMA_IE.4	DMA_STS.8		
			Channel 1 frame end	DMA_IE.5	DMA_STS.9		
			Channel 2 frame end	DMA_IE.6	DMA_STS.10		
			Channel 3 frame end	DMA_IE.7	DMA_STS.11		

			Channel 0 data abort	DMA_IE.8	DMA_STS .12		
			Channel 1 data abort	DMA_IE.9	DMA_STS .13		
			Channel 2 data abort	DMA_IE.10	DMA_STS .14		
			Channel 3 data abort	DMA_IE.11	DMA_STS .15		
FLASH	0000009Ch	23	checksum error	FLASH_CTRL.2	FLASH_IN T.0		
ANA	000000A0h	24	manual ADC conversion done	ANA_INTEN.0	ANA_INT STS.0		
			auto ADC conversion done	ANA_INTEN.1	ANA_INT STS.1		
			COMP1 rising or falling	ANA_INTEN.2	ANA_INT STS.2	V	V
			COMP2 rising or falling	ANA_INTEN.3	ANA_INT STS.3	V	V
			VDDALARM rising or falling	ANA_INTEN.7	ANA_INT STS.7	V	V
			VDCIN rising or falling	ANA_INTEN.8	ANA_INT STS.8	V	V
			VDDLV rising or falling	ANA_INTEN.1 0	ANA_INT STS.10	V	V
			VDCINDROP is 0 and the entry of sleep or deep-sleep modes are detected	ANA_INTEN.1 1	ANA_INT STS.11	V	V
			ANA_REGx error	ANA_INTEN.1 2	ANA_INT STS.12	V	V
			TADC change over threshold	ANA_INTEN.1 3	ANA_INT STS.13	V	V

7.11. Working Model

The following diagram shows the power state machine of V94XX(A).

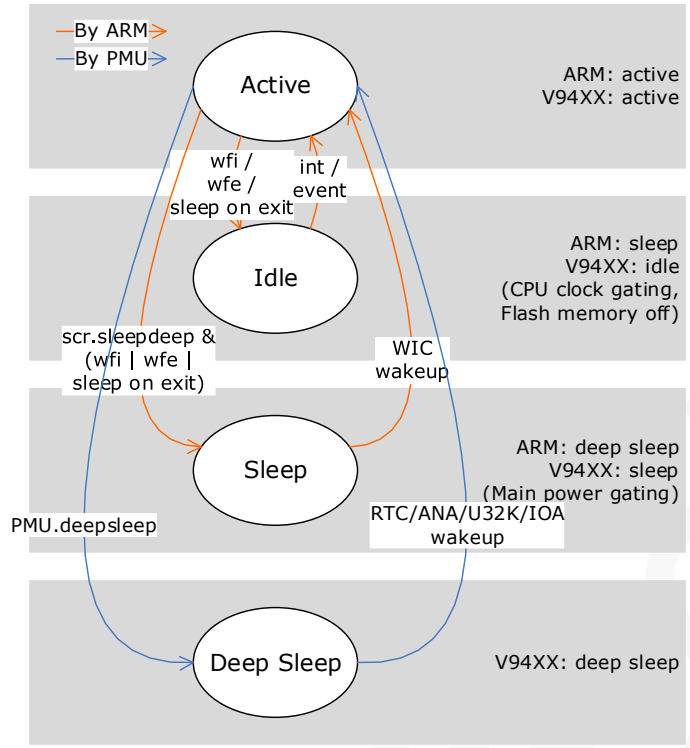


Figure 7-3 Power State Flow Chart of V94XX(A)

According to the diagram above, idle mode or sleep is controlled by CPU directly, and the programmer only needs to execute corresponded instruction (WFI or WFE) to enter these two modes. For deep sleep mode, PMU controller will handle the entry and exit of this mode and it will always return to active mode after wake-up. Corresponded wake-up source must be set before entry deep sleep mode, this part should be taken care by software programmer. The following shows the wake-up source under each mode.

Note: (1) It should be noted that MCU could enter sleep mode or deep sleep mode only when MODE=1. If MCU execute instruction for entry sleep mode when MODE=0, MCU will enter idle mode. Before MCU enter deep sleep mode, programmer should configure PDNS (ANA_CTRL bit6) and PDNS2 (ANA_CTRL bit24) firstly, or judge the state of VDCINDROP and VDDALRAM. For details, please refer to ANA_CTRL register.

(2) When MCU wake up from sleep mode, hardware will switch the system clock to the setting before entry sleep mode. For example, the system clock is PLLL before entry sleep mode, the hardware will switch the system clock to PLLL when wake up from sleep mode. When MCU wake up from deep sleep mode, the hardware will switch the system clock to RCH automatically. Before entry IDLE mode and wake up from IDLE mode, the hardware does not change the system clock automatically.

(3) User can't select RTCCLK as system clock before entry sleep mode. System clock source control by CLKSEL (MISC2_CTRL bit2:0).

(4) When wake up from sleep mode, PLLL lock time is 1ms, and PLLH lock time is 15μs.

Table 7-27 Wake-up Source under Each Mode

INT Number	Source	Wake up from		
		deep sleep	sleep	idle
Event	-	-	-	-
NMI	SRAM Parity Error	-	-	V
0	PMU (Ext Int)	V	V	V

1	RTC	V	V	V
2	UART 32K 0	V	V	V
3	UART 32K 1	V	V	V
4	I2C	-	-	V
5	-	-	-	V
6	UART0	-	-	V
7	UART1	-	-	V
8	UART2	-	-	V
9	-	-	-	V
10	UART4	-	-	V
11	UART5	-	-	V
12	ISO7816	-	-	V
13	-	-	-	-
14	TIMER0	-	-	V
15	TIMER1	-	-	V
16	TIMER2	-	-	V
17	TIMER3	-	-	V
18	PWM0	-	-	V
19	PWM1	-	-	V
20	PWM2	-	-	V
21	PWM3	-	-	V
22	DMA	-	-	V
23	FLASH	-	-	V
24	ANA	V	V	V
27	SPI	-	-	V

7.12. Application Note

7.12.1. External IO Wake-up

All 16 IOAs can wake-up the system from sleep or deep-sleep mode. In order to prevent some glitches on these signal to unexpected wake-up the system, a de-glitch circuit is embedded in V94XX(A). The following diagram shows an example of how this de-glitch circuit works. The de-glitch time will increase accordingly when the RTCCLK pre-scaler is set to a non-zero value. For example, when RTCCLK pre-scaler is set to 1/4, the de-glitch time will be increased to 122*4=488μs. The de-glitch time only affects the wake-up signal under sleep and deep-sleep mode.

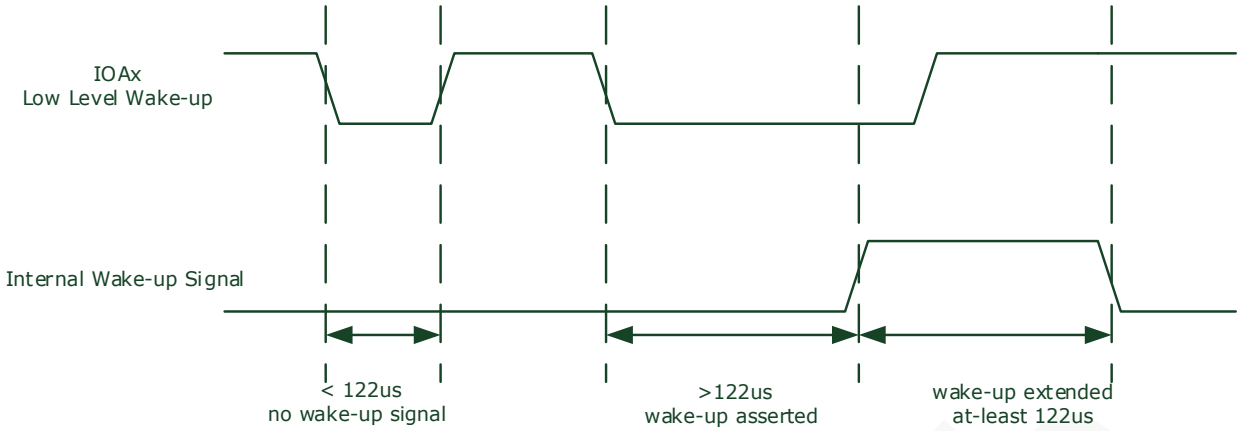
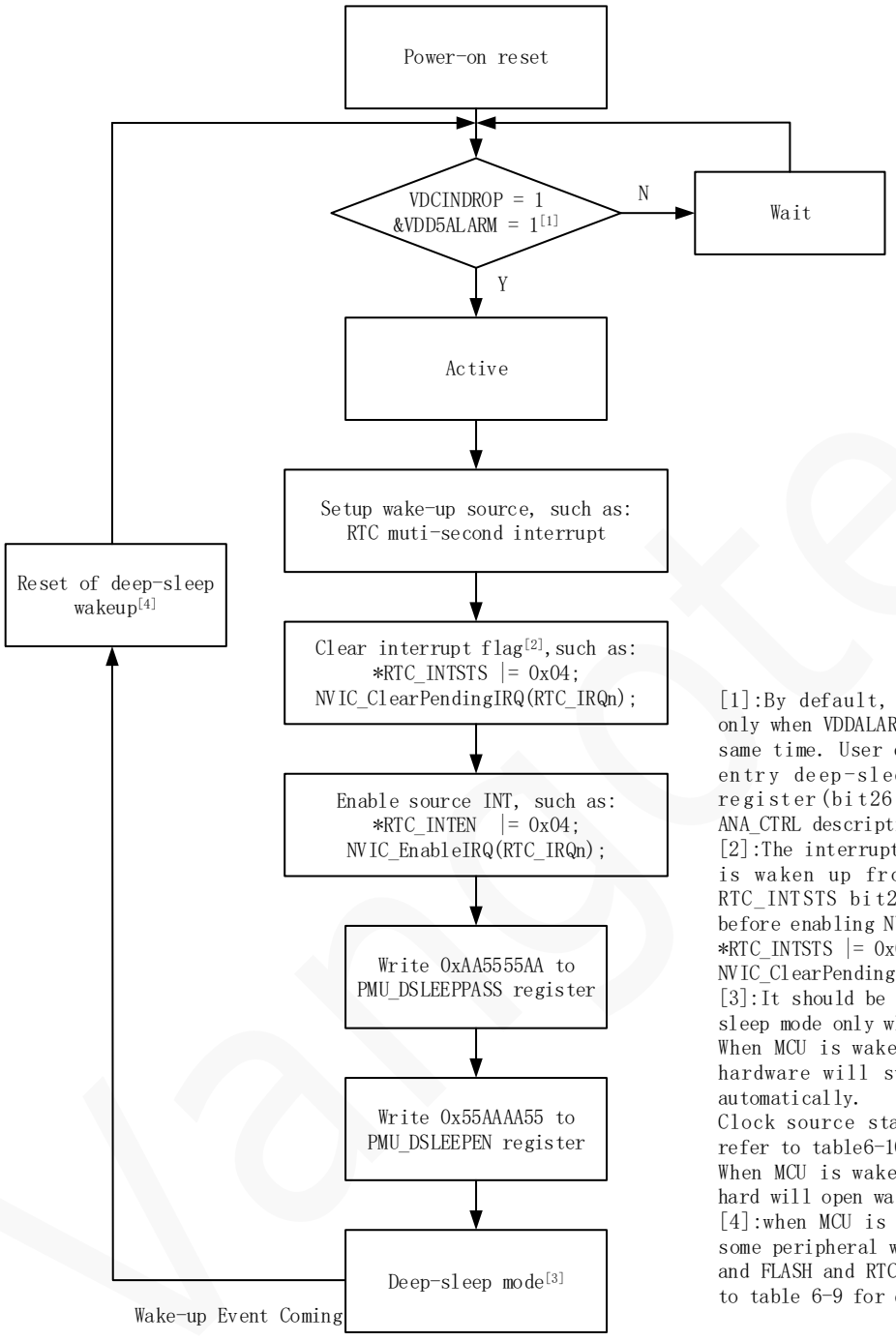


Figure 7-4 External Wake-up Example

7.12.2. Deep-sleep Entry Procedure

The following figure shows an example of deep-sleep mode entry procedure.

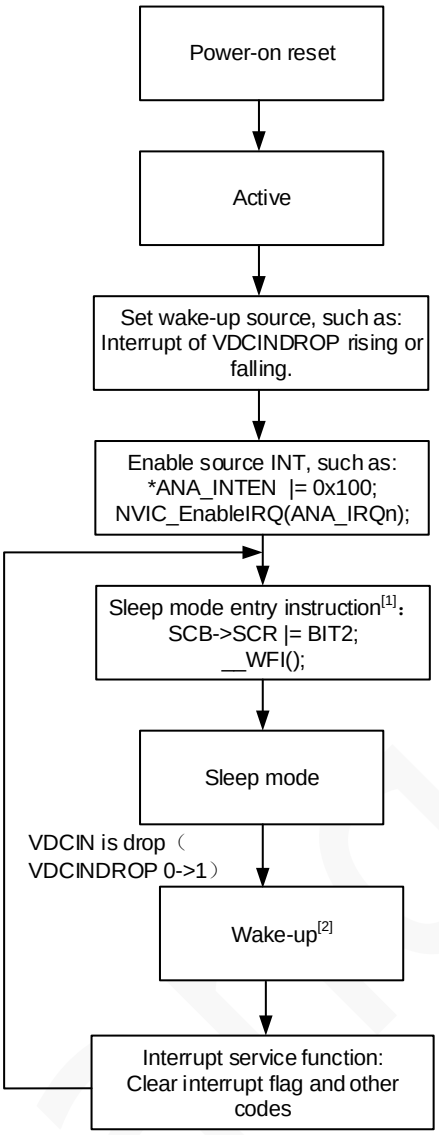


[1]:By default, MCU can entry deep-sleep mode only when VDDALARM and VDCINROP must be 1 at the same time. User can change the condition of MCU entry deep-sleep mode by setting ANA_CTRL register(bit26 and bit6). Please refer to ANA_CTRL description for details.
[2]:The interrupt flag will be set to 1 when MCU is waken up from deep-sleep mode, such as: RTC_INTSTS bit2. User should clear the flag before enabling NVIC interrupt again, such as:
*RTC_INTSTS |= 0x04;
NVIC_ClearPendingIRQ(RTC_IRQn);
[3]:It should be noted that MCU could enter deep-sleep mode only when MODE=1.
When MCU is waken up from deep sleep mode, the hardware will switch the system clock to RCH automatically.
Clock source state in different modes, please refer to table6-10 for details.
When MCU is waken up from deep-sleep mode, the hard will open watch dog automatically.
[4]:when MCU is waken up from deep-sleep mode, some peripheral will not be reset including SRAM and FLASH and RTC and WDT and so on, please refer to table 6-9 for details.

Figure 7-5 Deep-sleep Mode Entry Flow

7.12.3. Sleep Entry Procedure

The following figure shows an example of sleep mode entry procedure.



[1]:It should be noted that MCU could enter sleep mode only when MODE=1. If MCU executes instruction for entry sleep mode when MODE=0, MCU will entry IDLE mode.
[2]:When MCU is waken up from deep-sleep mode, some peripheral will be reset including UART , SPI , I2C and so on, but LCD , GPIO , ANA and so on will not be reset, please refer to table 6-9 for details.
When MCU is waken up from sleep mode, hardware will switch the system clock to the state of entry sleep mode. For example, the system clock is PLLL before entering sleep mode, the hardware will switch the system clock to PLLL when waking up from sleep mode.
The sate of clock source in different modes , please refer to table 6-10 for details.
When MCU is waken up from deep-sleep mode, the hard will open watch dog automatically.
Note: (1)If user enables RTC automatic temperature compensation, user should not select RCH as system clock before entering sleep mode. If user does not enable RTC automatic temperature compensation, user can select RCH as system clock before entering sleep mode. System clock source is controlled by CLKSEL(MISC2_CTRL bit2:0).
(2)User should not select RTCCLK as system clock before entering sleep mode. System clock source is controlled by CLKSEL(MISC2_CTRL bit2:0).

Figure 7-6 Sleep Mode Entry Flow

7.12.4. IDLE Entry Procedure

The following figure shows an example of idle mode entry procedure.

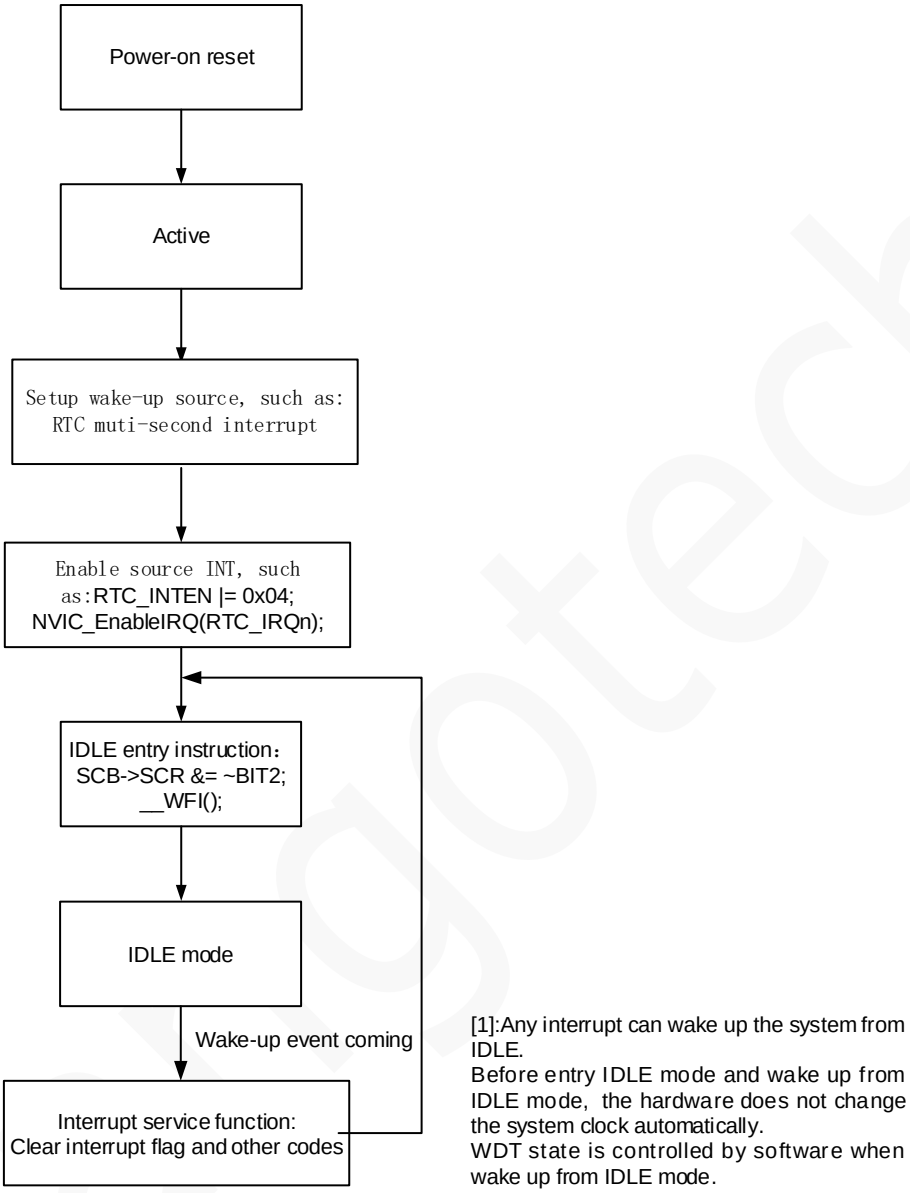


Figure 7-7 IDLE Mode Entry Flow

8.Clock Controller

8.1. Introduction

The settings in clock controller will be reset after wake-up from deep-sleep mode or system reset, programmer should restore the setting manually after wake-up from deep-sleep mode.

In the V94XX(A), there are four clock sources:

- The 32K RC oscillator circuit, to generate a 32.768K RC clock (32K RC). This circuit is running always. 32k RC can trimming from RCLTRIM [4:0] (ANA_REGB).
- The 32K crystal oscillator circuit, to generate a 32.768K XTAL clock (32K XTAL). This circuit is monitored by the 32K XTAL monitoring circuit that is sourced by 32K RC clock. When this oscillator circuit stops running, 32K RC clock will replace 32K XTAL, and the monitoring circuit will stimulate the crystal oscillator circuit until it runs again.
- The 6M RC oscillator circuit, to generate a 6.5536M RC clock (6M RC). This circuit can stop running by user register control. This circuit starts running from chip reset.
- The 6M XTAL oscillator circuit, to generate a 6.5536M XTAL clock (6M XTAL). This circuit can stop running by user register control.

In the V94XX(A), there are three clock domains:

- HCLK is generated by one of the 6.5536M XTAL\6.5536M RC\32.768K XTAL\32.768K RC or multiply of them. HCLK provides clock pulses for the CPU\FLASH\SRAM\DMA\GPIO\LCD\CRYPT.
- PCLK is divided from HCLK. PCLK provides clock pulses for the slow peripheral.
- RTCCLK provides clock pulses for the RTC\ WDT\ UART32K\LCD.

For different mode, the enable or disable of clock generated module will be controlled by hardware or software, the following tables shows the detail of clock status under each mode.

Table 8-1 Clock Source Enable or Disable in Different Modes

Clock Source	Power modes			
	Deep sleep	Sleep	IDLE	Active
6.5536M RC	OFF	OFF	Controlled by RCHPD	
6.5536M XTAL	OFF	OFF	Controlled by XOHPDN	
PLLH	OFF	OFF	Controlled by PLLHPDN	
PLLL	OFF	OFF	Controlled by PLLLPDN	
32K RC	ON	ON	ON	
32K XTAL	ON	ON	ON	

Clock Source	Wake up from different modes		
	Deep sleep	Sleep	IDLE
6.5536M RC	ON	Controlled by RCHPD	
6.5536M XTAL	OFF	Controlled by XOHPDN	
PLLH	OFF	Controlled by PLLHPDN	
PLLL	OFF	Controlled by PLLLPDN	
32K RC	ON	ON	
32K XTAL	ON	ON	

8.2. Block Diagram

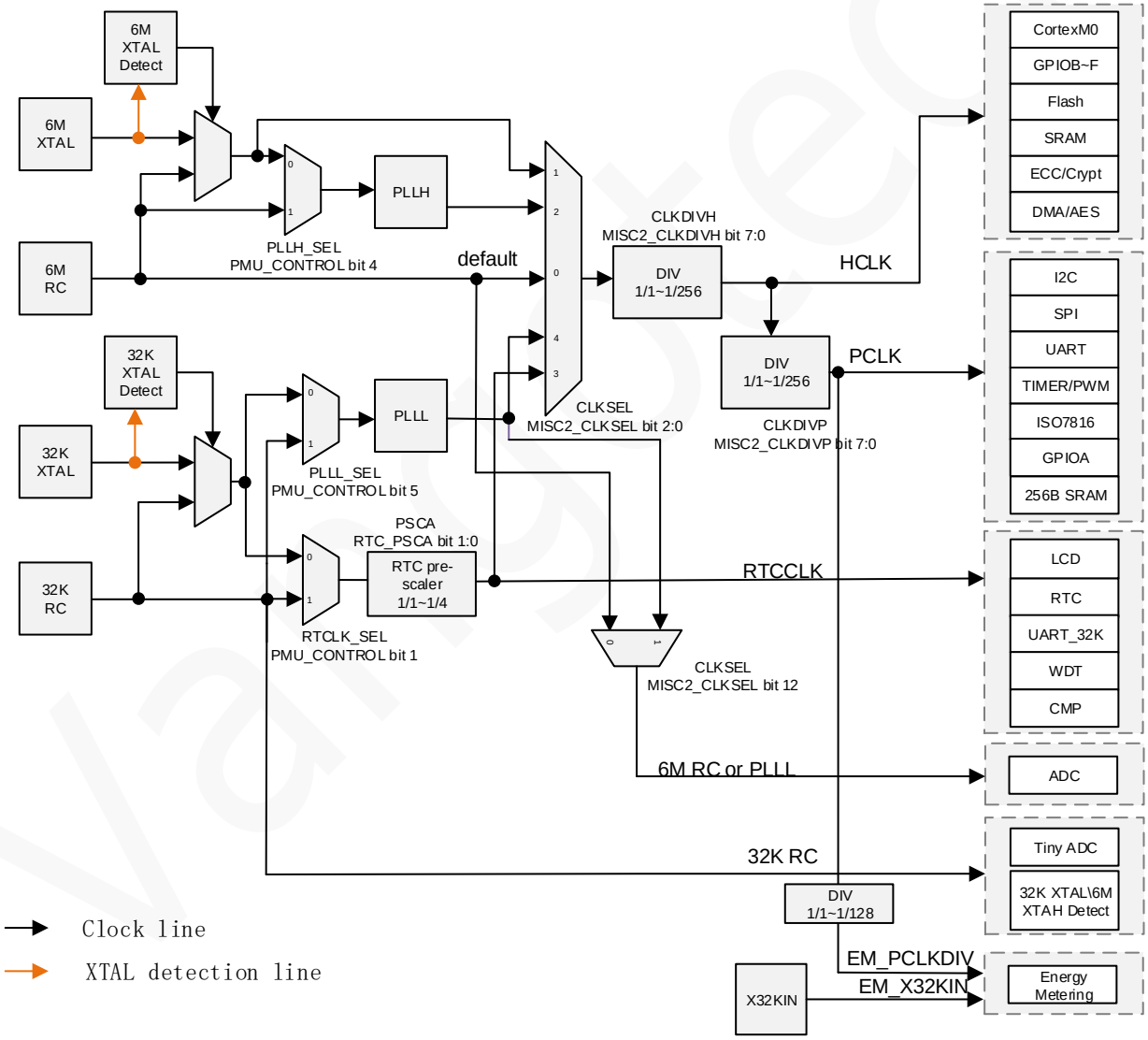


Figure 8-1 V94XX(A) Clock Block Diagram

8.3. Register Location

Table 8-2 Register Location of ANA Controller for CLOCK (ANA Base: 0x40014200)

Name	Type	Address	Description	Default
ANA_REG2	R/W	0x0008	Analog control register 2	0x00
ANA_REG3	R/W	0x000C	Analog control register 3	0x00
ANA_REG9	R/W	0x0024	Analog control register 9	0x00
ANA_REGB	R/W	0x002C	Analog control register 11	From FLASH
ANA_REGC	R/W	0x0030	Analog control register 12	From FLASH
ANA_CMPOUT	R	0x0054	Comparator result register	0x0030

Table 8-3 Register Location of the PMU Controller (PMU Base: 0x40014000)

Name	Type	Address	Description	Default
PMU_CONTROL	R/W	0x0008	PMU control register	0x0000
PMU_STS	R/C	0x000C	PMU Status register	0x0000074

Table 8-4 Register Location of MISC2 Controller (MISC2 Base: 0x40013E00)

Name	Type	Address	Description	Default
MISC2_CLKSEL	R/W	0x0004	Clock selection register	0x0
MISC2_CLKDIVH	R/W	0x0008	AHB clock divider control register	0x00
MISC2_CLKDIVP	R/W	0x000C	APB clock divider control register	0x01
MISC2_HCLKEN	R/W	0x0010	AHB clock enable control register	0x1FF
MISC2_PCLKEN	R/W	0x0014	APB clock enable control register	0xFFFFFFFF

8.4. Feature

--Clock control of each sub-module

--Clock divider of AHBCLK and APBCLK.

8.5. Register Definition

8.5.1. ANA_REG3 Register

Table 8-5 Description of ANA_REG3

Bit	Name	Function	Notes
3	ADCBGPPD*	ADCBGP power down control signal.	0: Power-up ADCBGP. 1: Power-down ADCBGP.
4	RCHPD	RCH (6.5536M RC) power down control signal.	0: Power-up RCH. 1: Power-down RCH.
5	PLLLPDN	PLLL (32768Hz input PLL) power up control signal.	0: Power-down PLLL. 1: Power-up PLLL.
6	PLLHPDN	PLLH (6.5536MHz input PLL) power up control signal.	0: Power-down PLLH. 1: Power-up PLLH.
7	XOHPDN	6.5536M crystal power up control signal.	0: Power-down XOH. 1: Power-up XOH.
Note*: RCH and PLL and ADC are related to ADCBGP, must power-up ADCBGP before power-up RCH			

or PLL or ADC. User can power down ADCBGP by set ADCBGPPD to 1 when ADCBGP was not used in program. User could not power down ADCBGP by set ADCBGPPD to 1 when ADCBGP was used in program, because the system has a protection function to ensure reliability. User can power down ADCBGP in sleep mode and deep-sleep mode whether ADCBGP is used or not.

8.5.2. ANA_REG4 Register

Table 8-6 Description of ANA_REG4

Bit	Name	Function	Notes
7:0		Reserved.	Default: 0x00, must be set to 0x01 by user.

8.5.3. ANA_REG9 Register

Table 8-7 Description of ANA_REG9

Bit	Name	Function	Notes
2:0	PLLLSEL[2:0]	Frequency selection of PLLL.	000: 26.2144MHz 001: 13.1072MHz 010: 6.5536MHz 011: 3.2768MHz 100: 1.6384MHz 101: 0.8192MHz 110: 0.4096MHz 111: 0.2048MHz
6:3	PLLHSEL[3:0]	Frequency selection of PLLH. The PLLH's frequency is the multiply of external XOH or internal RCH.	1000~1011: Reserved. 1100: 2 x Input clock 1101: 2.5 x Input clock 1110: 3 x Input clock 1111: 3.5 x Input clock 0000: 4 x Input clock 0001: 4.5 x Input clock 0010: 5 x Input clock 0011: 5.5 x Input clock 0100: 6 x Input clock 0101: 6.5 x Input clock 0110: 7 x Input clock 0111: 7.5 x Input clock

8.5.4. ANA_REGB Register

Table 8-8 Description of ANA_REGB

Bit	Name	Function	Notes
4:0	RCLTRIM[4:0]	Trimming of 32kHz RC.	00000~01111: increased by 4% for each step; 10000~11111: decreased by 4% for each step;

Note: Users must not modify the configuration of ANA_REGx(x=B~E), it can be loaded from FLASH automatically.

8.5.5. ANA_REGC Register

Table 8-9 Description of ANA_REGC

Bit	Name	Function	Notes
5:0	RCHTRIM[5:0]	Trimming of 6.5536MHz RC	000000~011111: increased by 1.25% for each step; 100000~111111: decreased by 1.25% for each step;
Note: Users must not modify the configuration of ANA_REGx(x=B~E), it can be loaded from FLASH automatically.			

8.5.6. ANA_CMPOUT Register

Table 8-10 Description of ANA_CMPOUT Register

Bit	Name	Type	Description	Default
1	LOCKL	R	PLLL lock status It takes about 1ms until PLLL locked. 0: PLLL is not lock. 1: PLLL is lock.	0x0
0	LOCKH	R	PLLH lock status It takes about 15μs until PLLH locked. 0: PLLH is not lock. 1: PLLH is lock.	0x0

8.5.7. PMU_CONTROL Register

Table 8-11 Description of PMU_CONTROL Register

Bit	Name	Type	Description	Default
5	PLLL_SEL	R/W	Low speed PLL input clock selection. 0: 32KXTAL 1: 32K RC	0x0
4	PLLH_SEL	R/W	High speed PLL input clock selection. 0: 6.5MHz RC 1: 6.5536MHz XTAL	0x0
3	INT_6M_EN	R/W	6.5536M XTAL absent interrupt enable register. This bit is used to control the interrupt signal output to CPU. When this bit is set to 1, if 6.5536M crystal is removed or broken, an interrupt will be issued to CPU.	0x0
2	INT_32K_EN	R/W	32K XTAL absent interrupt enable register. This bit is used to control the interrupt signal output to CPU. When this bit is set to 1, if 32K crystal is removed or broken, an interrupt will be issued to CPU. And if this event is	0x0

			happened during sleep, CPU will be waked up.	
1	RTCCLK_SEL	R/W	RTC Clock selection. 0: 32K XTAL 1: 32K RC	0x0

8.5.8. PMU_STS Register

Table 8-12 Description of PMU_STS Register

Bit	Name	Type	Description	Default
3	EXIST_6M	R	6.5536M XTAL exist status register. This bit represents 6.5536M XTAL is existed or absent. After 6.5536MHz XTAL (BIT7 of ANA_REG3 is configured as 1) is turned on, the state bit will refresh, otherwise it will remain in its previous state. 0: 6.5536M crystal is absent. 1: 6.5536M crystal is existed.	0x0
2	EXIST_32K	R	32K XTAL exist status register. This bit represents 32K XTAL is existed or absent. 0: 32K crystal is absent. 1: 32K crystal is existed.	0x1
1	INT_6M	R/C	This bit represents the 6.5536M crystal absent interrupt status. When this bit is set to 1, it means the 6.5536M crystal is removed or broken. When the EXIST_6M state goes from 1 to 0, the state position is 1. Write 1 to this bit can clear this flag to 0.	0x0
0	INT_32K	R/C	This bit represents the 32K crystal absent interrupt status. When this bit is set to 1, it means the 32K crystal is removed or broken. When the EXIST_32K state goes from 1 to 0, the state position is 1. Write 1 to this bit can clear this flag to 0.	0x0

8.5.9. MISC2_CLKSEL Register

Table 8-13 Description of MISC2_CLKSEL Register

Bit	Name	Type	Description	Default
31:3	-	-	Reserved.	0
2:0	CLKSEL	R/W	This register is used to control AHB clock source. 0: RCH (6.5MHz RC) 1: XOH (6.5536MHz XTAH). 2: PLLH. 3: RTCCLK (controlled by RTCCLK_SEL in PMU_CONTROL register). 4: PLLL. Before clock select to one of the clock source,	0x0

			programmer should enable the corresponded module first by setting PMU_CONTROL register.	

8.5.10. MISC2_CLKDIVH Register

Table 8-14 Description of MISC2_CLKDIVH Register

Bit	Name	Type	Description	Default
31:8	-	-	Reserved.	0
7:0	CLKDIVH	R/W	This register is used to control AHB clock divider. 0: Clock source divide by 1 1: Clock source divide by 2. 2: Clock source divide by 3. …. 255: Clock source divide by 256.	0x00

8.5.11. MISC2_CLKDIVP Register

Table 8-15 Description of MISC2_CLKDIVP Register

Bit	Name	Type	Description	Default
31:8	-	-	Reserved.	0
7:0	CLKDIVP	R/W	This register is used to control APB clock divider. 0: AHB clock divide by 1. 1: AHB clock divide by 2. 2: AHB clock divide by 3. …. 255: AHB clock divide by 256.	0x01

8.5.12. MISC2_HCLKEN Register

Table 8-16 Description of MISC2_HCLKEN Register

Bit	Name	Type	Description	Default
31:9	-	-	Reserved.	0
8:0	HCLKEN	R/W	This register is used to control clock enable of each AHB module. The corresponded module can be turned-off only when its function is not been used. Refer to Table 8-17 for detail about each module. 0: Disable. 1: Enable.	0x1FF

Table 8-17 HCLK clock enable of each module

Bit	Module	Note
0	--	
1	Arbiter & Bus Matrix	Shouldn’t off when CPU or DMA is active.
2	FLASH Controller	Shouldn’t off.

3	SRAM Controller	Shouldn't off.
4	DMA Controller	
5	GPIO Controller	
6	LCD Controller	
7	--	
8	CRYPT Controller	

8.5.13. MISC2_PCLKEN Register

Table 8-18 Description of MISC2_PCLKEN Register

Bit	Name	Type	Description	Default
31:0	PCLKEN	R/W	This register is used to control clock enable of each APB module. The corresponded module can be turned-off only when its function is not been used. Refer to Table 8-19 for detail about each module. 0: Disable. 1: Enable.	0xFFFFFFFF

Table 8-19 PCLK Clock Enable of Each Module

Bit	Module	Note
0	AHB2APB Bridge	Shouldn't off.
1	DMA Controller	
2	I2C	
3	Reserved.	
4	UART0	
5	UART1	
6	UART2	
7	-	
8	UART4	
9	UART5	
10	ISO7816	
11	Reserved.	
12	Timer	
13	MISC	
14	MISC2	
15	PMU	
16	RTC	
17	ANA	
18	U32K 0	
19	U32K 1	
20	Reserved.	
21	SPI	
31:22	Reserved.	

9.Analog Controller

9.1. Introduction

The Analog controller is used to control the analog function of V94XX(A). All the analog related control like ADC, comparator and other analog flag detection are controlled by this module. The analog controller is placed in always-on domain, so all the analog setting will be kept under deep-sleep mode.

9.2. Feature

-- Interrupt/wake-up signal generated for analog detect flag.

-- Comparator interrupt generation.

-- Comparator counter.

-- ADC manual and auto sample mode.

-- ADC interrupt generation.

9.3. Block Diagram

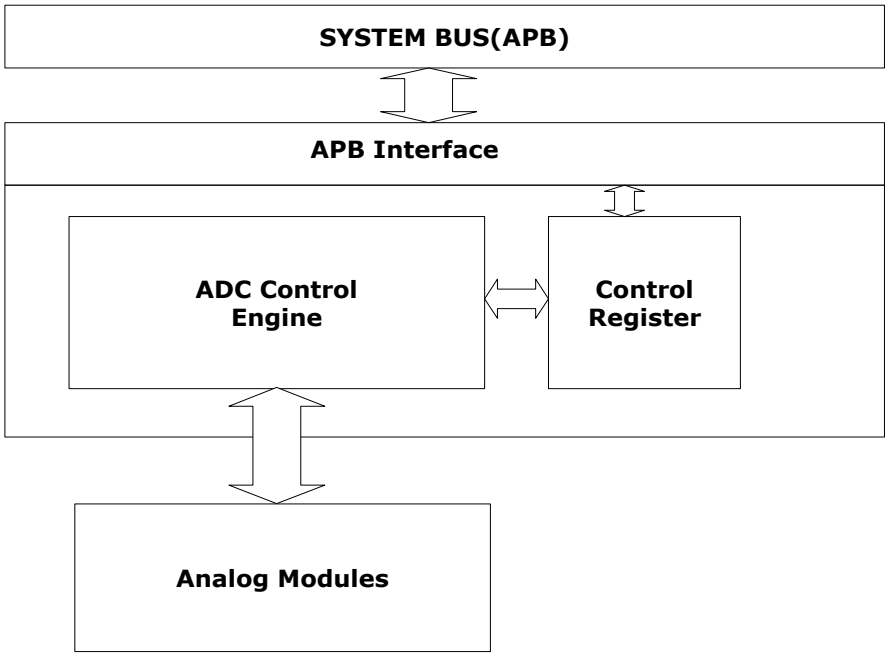


Figure 9-1 Functional Block Diagram of Analog Controller

9.4. Register Location

Table 9-1 ANA Registers Map

Register Name	Offset	Type	Reset Value	Description
ANA_REG0	0x0000	rw	0x0000_0000	Analog register 0
ANA_REG1	0x0004	rw	0x0000_0000	Analog register 1
ANA_REG2	0x0008	rw	0x0000_0000	Analog register 2
ANA_REG3	0x000C	rw	0x0000_0000	Analog register 3
ANA_REG4	0x0010	rw	0x0000_0000	Analog register 4
ANA_REG5	0x0014	rw	0x0000_0000	Analog register 5
ANA_REG6	0x0018	rw	0x0000_0000	Analog register 6
ANA_REG7	0x001C	rw	0x0000_0000	Analog register 7
ANA_REG8	0x0020	rw	0x0000_0000	Analog register 8
ANA_REG9	0x0024	rw	0x0000_0000	Analog register 9
ANA_REGA	0x0028	rw	0x0000_0000	Analog register 10
ANA_REGB	0x002C	rw	0x0000_0000	Analog register 11 (Load from Flash)
ANA_REGC	0x0030	rw	0x0000_0000	Analog register 12 (Load from Flash)
ANA_REGD	0x0034	rw	0x0000_0000	Analog register 13 (Load from Flash)
ANA_REGE	0x0038	rw	0x0000_0000	Analog register 14 (Load from Flash)
ANA_REGF	0x003C	rw	0x0000_0000	Analog register 15
ANA_CTRL	0x0050	rw	0x0000_0000	Analog control register
ANA_CMPOUT	0x0054	r	0x0000_0030	Comparator result register
ANA_INTSTS	0x0060	rc_w1	0x0000_0000	Analog interrupt status register
ANA_INTEN	0x0064	rw	0x0000_0000	Analog interrupt enable register
ANA_ADCCTRL	0x0068	rw	0x0000_0000	ADC control register
ANA_ADCDATAx[0..11,0x4]	0x0070	r	0x0000_0000	ADC channel x data register
ANA_CMPCNTx[1..2,0x4]	0x00B0	rc_w1	0x0000_0000	Comparator x counter
ANA_MISC	0x00B8	rw	0x0000_0000	Analog misc. control register

9.5. Register Definition

9.5.1. ANA_REGx Register

Table 9-2 Description of ANA_REGx

	Bit								
	7	6	5	4	3	2	1	0	Address
ANA_REG0	-	-	-		-		-		0x0000
ANA_REG1	-	-	GDE4	RESDIV	-				0x0004
ANA_REG2	-	-	REFSEL_CMP2	REFSEL_CMP1	CMP2_SEL[1:0]		CMP1_SEL[1:0]		0x0008
ANA_REG3	XOHPDN	PLLHPDN	PLLLPDN	RCHPD	ADCBGPPD	CMP2PDN	CMP1PDN	ADCPDN	0x000C
ANA_REG4	-		-		-	-	-		0x0010
ANA_REG5	-	-	-	-	IT_CMP2[1:0]		IT_CMP1[1:0]		0x0014
ANA_REG6	BAT2DISC	BAT1DISC	-	VLCD[3:0]				LCD_BMOD	0x0018
ANA_REG7	-	-	-	-	-	-	-	-	0x001C
ANA_REG8	-	VDDPVDSEL[2:0]			-		-		0x0020
ANA_REG9	PD_VDDDET	PLLHSEL[3:0]			PLLLSEL[2:0]				0x0024
ANA_REGA	PD_VDCINDET	-	-	-	-	-	-	-	0x0028
ANA_REGB		-	-	RCLTRIM[4:0]					0x002C

ANA_REGC	-	-	RCHTRIM[5:0]					0x0030
ANA_REGD	-							0x0034
ANA_REGE	-							0x0038
ANA_REGF	ADTREF3_SEL	ADTREF2_SEL	ADTREF1_SEL	SEL_ADT	PDN_ADT	VDDO_EN	-	0x003C

9.5.2. ANA_REG0 Register

Table 9-3 ANA_REG0 Register Description

Bit	Name	Type	Description
31:8	Rsvd	-	Reserved.
7:0	REG0_RSVD	rw	Reserved.

9.5.3. ANA_REG1 Register

Table 9-4 ANA_REG1 Register Description

Bit	Name	Type	Description
31:6	Rsvd	-	Reserved.
5	GDE4	rw	Enable cap division for M ADC's input signal 0: Disable 1: Enable 1/4 cap division
4	RESDIV	rw	Enable resistor division for M ADC's input signal 0: Disable 1: Enable 1/4 resistor division
3:0	Rsvd	-	Reserved.

9.5.4. ANA_REG2 Register

Table 9-5 ANA_REG2 Register Description

Bit	Name	Type	Description
31:6	Rsvd	-	Reserved.
5	REFSEL_CMP2	rw	REF selection of CMP2 0: LPREF 1: ADCREF
4	REFSEL_CMP1	rw	REF selection of CMP1 0: LPREF 1: ADCREF
3:2	CMP2_SEL	rw	Signal source selection of comparator B 00: CMP2_P to REF 01: CMP2_N to REF 1*: CMP2_P to CMP2_N
1:0	CMP1_SEL	rw	Signal source selection of comparator A 00: CMP1_P to REF 01: CMP1_N to REF 1*: CMP1_P to CMP1_N

9.5.5. ANA_REG3 Register

Table 9-6 ANA_REG3 Register Description

Bit	Name	Type	Description
31:8	Rsvd	-	Reserved.
7	XOHPDN	rw	6.5536M crystal power up control signal. : Power-down XOH 1: Power-up XOH
6	PLLHPDN	rw	PLLH (6.5536MHz input PLL) power up control signal. 0: Power-down PLLH 1: Power-up PLLH
5	PLLLPDN	rw	PLLL (32768Hz input PLL) power up control signal. 0: Power-down PLLL 1: Power-up PLLL
4	RCHPD	rw	RCH (6.5536M RC) power down control signal 0: Power-up RCH 1: Power-down RCH
3	ADCBGPPD	rw	ADCBGP power down control signal. 0: Power-up ADCBGP 1: Power-down ADCBGP
2	CMP2PDN	rw	CMP2 power up control signal 0: Power-down CMP2 1: Power-up CMP2
1	CMP1PDN	rw	CMP1 power up control signal 0: Power-down CMP1 1: Power-up CMP1
0	ADCPDN	rw	ADC power up control signal. ADC automatic conversion should be disabled before ADC is powered down. 0: Power-down ADC 1: Power-up ADC

ADCBGPPD Note: RCH and PLL and ADC are related to ADCBGP, must power-up ADCBGP before power-up RCH or PLL or ADC. User can power down ADCBGP by set ADCBGPPD to 1 when ADCBGP was not used in program. User could not power down ADCBGP by set ADCBGPPD to 1 when ADCBGP was used in program, because the system has a protection function to ensure reliability. User can power down ADCBGP in sleep mode and deep-sleep mode whether ADCBGP is used or not.

9.5.6. ANA_REG4 Register

Table 9-7 ANA_REG4 Register Description

Bit	Name	Type	Description
31:8	Rsvd	-	Reserved.
7:0	REG4_RSVD	rw	Reserved. Default: 0x00, must be set to 0x01 by user.

9.5.7. ANA_REG5 Register

Table 9-8 ANA_REG5 Register Description

Bit	Name	Type	Description
31:7	Rsvd	-	Reserved.
6	VDDLVDETPD	rw	Power down VDD low voltage detector. 0: Power-up VDDLV detector 1: Power-down detector
5:4	Rsvd	-	Reserved.
3:2	IT_CMP2	rw	Bias current selection of CMP2 00: 20nA 01: 100nA 1*: 500nA
1:0	IT_CMP1	rw	Bias current selection of CMP1 00: 20nA 01: 100nA 1*: 500nA

9.5.8. ANA_REG6 Register

Table 9-9 ANA_REG6 Register Description

Bit	Name	Type	Description
31:8	Rsvd	-	Reserved.
7	BAT2DISC	rw	Discharge the BAT2 battery. Discharge resistance is 1.7k, and the discharge current is VBAT2 / 1.7k. 1: enable 1.7k resistor from BAT2 to GND
6	BAT1DISC	rw	Discharge the BAT1 battery. Discharge resistance is 1.7k, and the discharge current is VBAT1 / 1.7k. 1: enable 1.7k resistor from BAT1 to GND
5	Rsvd	-	Reserved.
4:1	VLCD	rw	LCD driving voltage VLCD=0: default VLCD=0~5: adjust range =+60mV*VLCD VLCD=6~15: adjust range =-60mV*(VLCD-5)
0	LCD_BMODE	rw	LCD BIAS mode selection 0: 1/3 bias 1: 1/4 bias

9.5.9. ANA_REG7 Register

Table 9-10 ANA_REG7 Register Description

Bit	Name	Type	Description
31:8	Rsvd	-	Reserved.

7:0	REG7_RSVD	rw	Reserved. Default: 0x00, must be set to 0x00.

9.5.10. ANA_REG8 Register

Table 9-11 ANA_REG8 Register Description

Bit	Name	Type	Description
31:8	Rsvd	-	Reserved.
7	REG8_RSVD	rw	Reserved. Default: 0, must be set to 1.
6:4	VDDPVDSEL	rw	Voltage selection of VDD power detector, the setting in this register will affect the status of VDDALARM. 000: Reserved 001: Reserved 010: Reserved 011: 3.6V 100: 3.2V 101: 2.9V 110: 2.6V 111: 2.3V
3:0	Rsvd	-	Reserved.

9.5.11. ANA_REG9 Register

Table 9-12 ANA_REG9 Register Description

Bit	Name	Type	Description
31:8	Rsvd	-	Reserved.
7	PD_VDDDET	rw	Power down VDD input VDDALARM detector. This module powered by VDD. 0: Power up 1: Power down
6:3	PLLHSEL	rw	Frequency selection of PLLH. The PLLH's frequency is the multiply of external XOH or internal RCH. 1000~1011: Reserved. 1100: 2 x Input clock 1101: 2.5 x Input clock 1110: 3 x Input clock 1111: 3.5 x Input clock 0000: 4 x Input clock 0001: 4.5 x Input clock 0010: 5 x Input clock 0011: 5.5 x Input clock 0100: 6 x Input clock 0101: 6.5 x Input clock 0110: 7 x Input clock 0111: 7.5 x Input clock

2:0	PLLLSEL	rw	Frequency selection of PLLL 000: 26.2144 MHz 001: 13.1072 MHz 010: 6.5536 MHz 011: 3.2768 MHz 100: 1.6384 MHz 101: 0.8192 MHz 110: 0.4096 MHz 111: 0.2048 MHz

9.5.12. ANA_REGA Register

Table 9-13 ANA_REGA Register Description

Bit	Name	Type	Description
31:8	Rsvd	-	Reserved.
7	PD_VDCINDET	rw	PD VDCIN detector 0: Power up 1: Power down
6:0	REGA_RSVD	rw	Reserved. Default: 0x00, must be set to 0x0A.

9.5.13. ANA_REGB Register

Table 9-14 ANA_REGB Register Description

Bit	Name	Type	Description
31:8	Rsvd	-	Reserved.
7:5	LPREFTRIM	rw	Trimming of LPREF, which will affect DVCC1's output by same ratio 011: +9% 010: +6% 001: +3% 000: 0%
4:0	RCLTRIM	rw	Trimming of 32kHz RC. 00000~01111: increased by 4% for each step 10000~11111: decreased by 4% for each step

Note: Users must not modify the configuration of ANA_REGx(x=B~E), it can be loaded from FLASH automatically.

9.5.14. ANA_REGC Register

Table 9-15 ANA_REGC Register Description

Bit	Name	Type	Description
31:6	Rsvd	-	Reserved.
5:0	RCHTRIM	rw	Trimming of 6.5536MHz RC 000000~011111:increased by 1.25% for each step

			100000~111111:decreased by 1.25% for each step

Note: Users must not modify the configuration of ANA_REGx(x=B~E), it can be loaded from FLASH automatically.

9.5.15. ANA_REGD Register

Table 9-16 ANA_REGD Register Description

Bit	Name	Type	Description
31:8	Rsvd	-	Reserved.
7:0	REGD_RSVD	rw	Reserved.

Note: Users must not modify the configuration of ANA_REGx(x=B~E), it can be loaded from FLASH automatically.

9.5.16. ANA_REGE Register

Table 9-17 ANA_REGE Register Description

Bit	Name	Type	Description
31:8	Rsvd	-	Reserved.
7:0	REGE_RSVD	rw	Reserved.

Note: Users must not modify the configuration of ANA_REGx(x=B~E), it can be loaded from FLASH automatically.

9.5.17. ANA_REGF Register

Table 9-18 ANA_REGF Register Description

Bit	Name	Type	Description
31:8	Rsvd	-	Reserved.
7	ADTREF3_SEL	rw	REF3 of ADT selection 0: 2.7V 1: 2.5V
6	ADTREF2_SEL	rw	REF2 of ADT selection 0: 1.8V 1: 1.6V
5	ADTREF1_SEL	rw	REF1 of ADT selection 0: 0.9V 1: 0.7V
4	SEL_ADT	rw	Signal selection for ADT 0: Connect to IOE6 1: Connect to IOE7
3	PDN_ADT	rw	Power up Tiny ADC 0: Power down. 1: Power up
2	VDDO_EN	rw	Enable VDD_OUT pin to output VDD level.

			0: High resistance. 1: VDD_OUT pin output VDD level, and it can be used to drive small power module.
1:0		-	Reserved.

9.5.18. ANA_CTRL Register

Table 9-19 ANA_CTRL Register Description

Bit	Name	Type	Description
31:27	Rsvd	-	Reserved.
26	PDNS2	rw	This register is used to set the deep sleep behavior when VDDALARM is 0 (Still need to consider the PDNS setting). 0: Can't enter deep-sleep mode when VDDALARM is 0. When VDDALARM is 1, The system can enter deep-sleep mode. And system will wake-up from deep-sleep mode automatically as long as VDDALARM became 0. 1: Can enter deep-sleep mode no-matter which state VDDALARM is.
25:24	VDCINDEB	rw	VDCIN de-bounce control register. 0: No de-bounce. 1: 2 RTCCLK de-bounce. 2: 3 RTCCLK de-bounce. 3: 4 RTCCLK de-bounce. When de-bounce is enabled, the input signal is valid only when the signal isn't change in multi-cycles of RTCCLK clock. And, the response time of the wake-up and interrupt will be delayed until the signal is valid. This circuit can work under all mode including sleep and deep-sleep mode.
23:22	CMP2DEB	rw	Comparator 2 de-bounce control register. 0: No de-bounce. 1: 2 RTCCLK de-bounce. 2: 3 RTCCLK de-bounce. 3: 4 RTCCLK de-bounce. When de-bounce is enabled, the input signal is valid only when the signal isn't change in multi-cycles of RTCCLK clock. And, the response time of the wake-up and interrupt will be delayed until the signal is valid. This circuit can work under all mode including sleep and deep-sleep mode.
21:20	CMP1DEB	rw	Comparator 1 de-bounce control register. 0: No de-bounce. 1: 2 RTCCLK de-bounce. 2: 3 RTCCLK de-bounce. 3: 4 RTCCLK de-bounce. When de-bounce is enabled, the input signal is valid only when the signal isn't change in multi-cycles of RTCCLK clock. And, the response time of the wake-up and interrupt will be delayed until the signal is valid. This circuit can work under

			all mode including sleep and deep-sleep mode.
19:16	Rsvd	-	Reserved.
15:8	RCHTGT	rw	RCH auto calibration target register. This register is used to store the target value of RCH. When the target frequency is 6.5536MHz, user should fill 6553600/32768 = 200 to this register.
7	Rsvd	-	Reserved.
6	PDNS	rw	This register is used to set the deep sleep behavior when VDCINDROP is 0(Still need to consider the PDNS setting). 0: Can't enter deep-sleep mode when VDCINDROP is 0. When VDCINDROP is 1, The system can enter deep-sleep mode. And system will wake-up from deep-sleep mode automatically as long as VDCINDROP became 0. 1: Can enter deep-sleep mode no-matter which state VDCINDROP is.
5:4	Rsvd	-	Reserved.
3:2	COMP2_SEL	rw	This register is used to control the interrupt and wake-up signal generation of COMP2. 0: Off. 1: Rising edge of COMP2. 2: Falling edge of COMP2. 3: Change of COMP2.
1:0	COMP1_SEL	rw	This register is used to control the interrupt and wake-up signal generation of COMP1. 0: Off. 1: Rising edge of COMP1. 2: Falling edge of COMP1. 3: Change of COMP1.

9.5.19. ANA_CMPOUT Register

Table 9-20 ANA_CMPOUT Register Description

Bit	Name	Type	Description
31:16	Rsvd	-	Reserved.
15:14	TADCO	r	Tiny ADC output.
13:11	Rsvd	-	Reserved.
10	VDDLV	r	VDD low power status. And hysteresis voltage of VDDLV is 20mV~30mV. 0: VDD is higher than 2.5V. 1: VDD is lower than 2.5V.
9	Rsvd	-	Reserved.
8	VDCINDROP	r	VDCIN drop status 0: VDCIN is not drop (VDCIN higher than threshold). 1: VDCIN is drop (i.e. VDCIN lower than threshold).
7	VDDALARM	r	This bit shows the output of VDDALARM. 0: Voltage of VDD is higher than voltage setting by VDDPVDSEL.

			1: Voltage of VDD is lower than voltage setting by VDDPVDSEL.
6:4	Rsvd	-	Reserved.
3	COMP2	r	This bit shows the output of comparator 2.
2	COMP1	r	This bit shows the output of comparator 1.
1	LOCKL	r	PLLL lock status. It takes about 1ms until PLLL locked. 0: PLLL is not lock. 1: PLLL is lock.
0	LOCKH	r	PLLH lock status. It takes about 15μs until PLLH locked. 0: PLLH is not lock. 1: PLLH is lock.

9.5.20. ANA_INSTS Register

Table 9-21 ANA_INTSTS Register Description

Bit	Name	Type	Description
31:14	Rsvd	-	Reserved.
13	INTSTS13	rc_w1	TADC change over-threshold interrupt. This interrupt will be set when the TADC is rising or falling and the change value compare to previous cycle is larger than the threshold setting in the TADCTH in ANA_MISC register, this interrupt flag will be set. Read 0: No TADC over threshold interrupt. Read 1: TADC over threshold is happened. Write 0: No effect. Write 1: clear this bit.
12	INTSTS12	rc_w1	ANA_REGx error flag. This interrupt is used to detect the error status of ANA_REGx, an automatically check0sum and parity check is applied to ANA_REGx, when external noise cause by ESD or other problem affect the setting of ANA_REGx, this interrupt will be asserted and programmer can use this flag to determine if it is necessary to recover the setting in the ANA_REGx. Read 0: No ANA_REGx error interrupt. Read 1: ANA_REGx error is happened. Write 0: No effect. Write 1: clear this bit.
11	INTSTS11	rc_w1	Interrupt flag of sleep mode entry under VDCINDROP is 0(i.e. VDCIN higher than threshold), this interrupt will be generated when VDCINDROP is 0 and the entry of sleep or deep-sleep modes are detected. Programmer can enable this interrupt to force CPU wake-up from sleep or deep-sleep mode when VDCINDROP is 0. Read 0: No Sleep mode entry interrupt. Read 1: Sleep mode entry interrupt is happened. Write 0: No effect. Write 1: clear this bit.

10	INTSTS10	rc_w1	Interrupt flag of VDDLV (VDD low power status), this interrupt will be generated when VDDLV rising or falling. Read 0: No VDDLV interrupt. Read 1: VDDLV interrupt is happened. Write 0: No effect. Write 1: clear this bit.
9	Rsvd	-	Reserved.
8	INTSTS8	rc_w1	Interrupt flag of VDCINDROP (VDCIN status), this interrupt will be generated when VDCINDROP rising or falling. Read 0: No VDCINDROP interrupt. Read 1: VDCINDROP interrupt is happened. Write 0: No effect. Write 1: clear this bit.
7	INTSTS7	rc_w1	Interrupt flag of VDDALARM (VDD status), this interrupt will be generated when VDDALARM rising or falling. Read 0: No VDDALARM interrupt. Read 1: VDDALARM interrupt is happened. Write 0: No effect. Write 1: clear this bit.
6:4	Rsvd	-	Reserved.
3	INTSTS3	rc_w1	Interrupt flag of COMP2, the interrupt generate condition is controlled by COMP2_SEL. Read 0: No COMP2 interrupt. Read 1: COMP2 interrupt is happened. Write 0: No effect. Write 1: clear this bit.
2	INTSTS2	rc_w1	Interrupt flag of COMP1, the interrupt generate condition is controlled by COMP1_SEL. Read 0: No COMP1 interrupt. Read 1: COMP1 interrupt is happened. Write 0: No effect. Write 1: clear this bit.
1	INTSTS1	rc_w1	Interrupt flag of auto ADC conversion done. Read 0: Auto ADC conversion not complete. Read 1: Auto ADC conversion has done. Write 0: No effect. Write 1: clear this bit.
0	INTSTS0	rc_w1	Interrupt flag of manual ADC conversion done. Read 0: Manual ADC conversion not complete. Read 1: Manual ADC conversion has done. Write 0: No effect. Write 1: clear this bit.

9.5.21. ANA_INTEN Register

Table 9-22 ANA_INTEN Register Description

Bit	Name	Type	Description

31:14	Rsvd	-	Reserved.
13	INTEN13	rw	Interrupt and wake-up enable control of the change in TADC output value is over or equal to threshold. 0: Disable TADC interrupt and wake-up. 1: Enable TADC interrupt and wake-up.
12	INTEN12	rw	Interrupt and wake-up enable control of ANA_REGx error. 0: Disable ANA_REGx error interrupt and wake-up. 1: Enable ANA_REGx error interrupt and wake-up.
11	INTEN11	rw	Interrupt and wake-up enable control of sleep mode entry, when VDCINDROP is 0(i.e. VDCIN higher than threshold). Programmer can enable this interrupt to force CPU wake-up from sleep or deep-sleep mode when VDCINDROP is 0 and the entry of sleep or deep-sleep modes are detected. 0: Disable Sleep mode entry interrupt and wake-up. 1: Enable Sleep mode entry interrupt and wake-up.
10	INTEN10	rw	Interrupt and wake-up enable control of VDDLV. 0: Disable VDDLV interrupt and wake-up. 1: Enable VDDLV interrupt and wake-up.
9	Rsvd	-	Reserved.
8	INTEN8	rw	Interrupt and wake-up enable control of VDCINDROP. 0: Disable VDCINDROP interrupt and wake-up. 1: Enable VDCINDROP interrupt and wake-up.
7	INTEN7	rw	Interrupt and wake-up enable control of VDDALARM. 0: Disable VDDALARM interrupt and wake-up. 1: Enable VDDALARM interrupt and wake-up.
6:4	Rsvd	-	Reserved.
3	INTEN3	rw	Interrupt and wake-up enable control of COMP2. 0: Disable COMP2 interrupt and wake-up. 1: Enable COMP2 interrupt and wake-up.
2	INTEN2	rw	Interrupt and wake-up enable control of COMP1. 0: Disable COMP1 interrupt and wake-up. 1: Enable COMP1 interrupt and wake-up.
1	INTEN1	rw	Interrupt enable control of auto ADC conversion done. 0: Disable auto ADC conversion interrupt. 1: Enable auto ADC conversion interrupt.
0	INTEN0	rw	Interrupt enable control of manual ADC conversion done. 0: Disable manual ADC conversion interrupt. 1: Enable manual ADC conversion interrupt.

9.5.22. ANA_ADCCTRL Register

Table 9-23 ANA_ADCCTRL Register Description

Bit	Name	Type	Description
31	MTRIG	rw	Manual ADC trigger. Write 0: No effect. Write 1: Start a manual ADC conversion. Read 0: Current manual ADC conversion is done.

			Read 1: Current manual ADC conversion is ongoing.
30	Rsvd	-	Reserved.
29	CICAON	rw	CIC filter always on control register. 0: CIC filter will be disabled when no ADC sample process is ongoing. 1: CIC filter will be enabled for all the time.
28	CICINV	rw	CIC filter input inversion. 0: No invert CIC filter input. 1: Invert CIC filter input.
27	CICSCA	rw	CIC output scale-down selection. 0: No scale down CIC filter's output. 1: Scale down CIC filter's output to 1/2.
26:24	CICSKIP	rw	CIC output skip control register. This register is used to control how many samples will be skipped at the beginning of ADC sample. If CICAON is 1 and the ADC channel is not changed, the CIC output will not be skipped by the ADC controller, this can be used for high speed capture to single channel. 0: Skip first 4 samples. 1: Skip first 5 samples. 2: Skip first 6 samples. 3: Skip first 7 samples. 4: No skip any sample. 5: Skip first 1 sample. 6: Skip first 2 samples. 7: Skip first 3 samples.
23:22	DSRSEL	rw	CIC down sampling rate control register. The higher down-sampling rate, the higher output data stability, and lower sampling rate. 0: 1/512 down-sampling rate. 1: 1/256 down-sampling rate. 2: 1/128 down-sampling rate. 3: 1/64 down-sampling rate.
21	AMODE	rw	Auto ADC mode control. 0: Capture single channel specified by ACH. 1: Capture multiple channels (0~11 channels) at one time.
20	MMODE	rw	Manual ADC mode control. 0: Capture single channel specified by MCH. 1: Capture multiple channels (0~11 channels) at one time.
19	Rsvd	-	Reserved.
18:16	AEN	rw	Auto ADC conversion enable control register. 0: Auto ADC conversion is off. 4: Auto ADC will be triggered by timer 0's overflow. 5: Auto ADC will be triggered by timer 1's overflow. 6: Auto ADC will be triggered by timer 2's overflow. 7: Auto ADC will be triggered by timer 3's overflow.
15:13	Rsvd	-	Reserved.
12	CLKSEL	rw	ADC clock source selection.

			0: 6.5M RCH 1: PLLL
11:8	CLKDIV	rw	The ADC clock source is internal 6.5M RCH or PLLL. The typical ADC main clock is 1.6384MHz, if ADC clock source is 6.5M RCH, CLKDIV is calculated such as: CLKDIV=6.5536/1.6384-1=3.
7:4	ACH	rw	Auto ADC channel control. 0: Auto ADC capture ADC channel 0. 1: Auto ADC capture ADC channel 1. …. 11: Auto ADC capture ADC channel 11. 12~15: Reserved. This register is valid only when AMODE is 0.
3:0	MCH	rw	Manual ADC channel control. 0: Manual ADC capture ADC channel 0. 1: Manual ADC capture ADC channel 1. …. 11: Auto ADC capture ADC channel 11. 12~15: Reserved. This register is valid only when MMODE is 0.

9.5.23. ANA_ADCDATAx Register

Table 9-24 ANA_ADCDATAx Register Description

Bit	Name	Type	Description
31:16	Rsvd	-	Reserved.
15:0	ADCDATAx	r	The result of ADC conversion will be stored in these registers. DATA0: Store conversion result of ADC channel 0. DATA1: Store conversion result of ADC channel 1. … DATA11: Store conversion result of ADC channel 11. For single channel conversion (MMODE is 0 or AMODE is 0), only the channel specified by MCH or ACH will be updated. For multi-channels conversion (MMODE is 1 or AMODE is 1), DATA0~DATA11 will be updated.

9.5.24. ANA_CMPCNTx Register

Table 9-25 ANA_CMPCNTx Register Description

Bit	Name	Type	Description
31:0	CNTx	rc_w1	This register stores the happen times of comparator x according to the setting in COMPx_SEL. For example, when COMPx_SEL is set to 1, then this counter will increase 1 when the COMPx is rising. This register can be cleared by writing 0 to this register, but this operation is valid only when

			corresponded CMPPDNx is set to 1 (when the corresponded comparator is enabled).

9.5.25. ANA_MISC Register

Table 9-26 ANA_MISC Register Description

Bit	Name	Type	Description
31:6	Rsvd	-	Reserved.
5:4	TADCTH	rw	TADC threshold setting. This register controls the threshold of TADC's interrupt. The TADC is using internal 32K RC as clock source to sample external signal, when TADC's interrupt is enable and the difference of two continuous cycles is larger than TADCTH, the INTSTS13 will be set and an interrupt will be asserted.
3:0	Rsvd	-	Reserved.

10. ADC Controller

10.1. Introduction

One second-order Σ-ΔADC is designed in 12 channels of the V94XX(A) for analog-to-digital conversion, and their full measurement scale is 0~1.2V if no voltage division. After set voltage division, when main power supply is 3.3V, the measurement scale is 0~3.6V. The ADC can be used to measure the ground, temperature, BAT1, BAT2 voltage and external voltage signals. The clock source is 6.5536M RC or PLLL. The ADC controller is placed in always-on domain, so all the ADC setting will be kept under deep-sleep mode.

10.2. Feature

-- ADC manual and auto sample mode.

-- ADC interrupt generation.

-- Support 12 channel full scan function.

10.3. Block Diagram

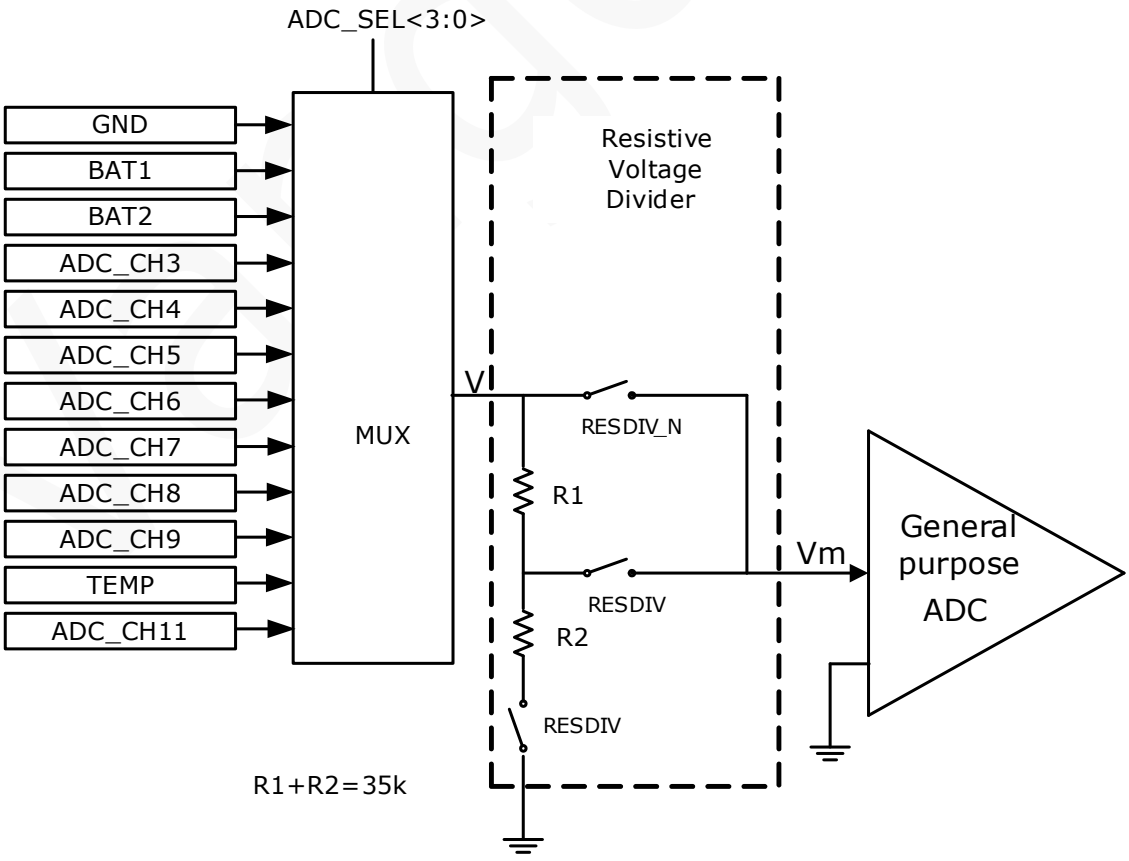


Figure 10-1 ADC Architecture

10.4. Register Location

Table 10-1 Register Location of ANA Controller for ADC (ANA Base: 0x40014200)

Name	Type	Address	Description	Default
ANA_REG0	R/W	0x0000	Analog register 0	0x00
ANA_REG1	R/W	0x0004	Analog register 1	0x00
ANA_REG3	R/W	0x000C	Analog register 3	0x00
ANA_INTSTS	R/C	0x0060	Analog interrupt status register	0x0000
ANA_INTEN	R/W	0x0064	Analog interrupt enable register	0x0000
ANA_ADCCTRL	R/W	0x0068	ADC control register	0x00000000
ANA_ADCDATA0	R	0x0070	ADC channel 0 data register	--
ANA_ADCDATA1	R	0x0074	ADC channel 1 data register	--
ANA_ADCDATA2	R	0x0078	ADC channel 2 data register	--
ANA_ADCDATA3	R	0x007C	ADC channel 3 data register	--
ANA_ADCDATA4	R	0x0080	ADC channel 4 data register	--
ANA_ADCDATA5	R	0x0084	ADC channel 5 data register	--
ANA_ADCDATA6	R	0x0088	ADC channel 6 data register	--
ANA_ADCDATA7	R	0x008C	ADC channel 7 data register	--
ANA_ADCDATA8	R	0x0090	ADC channel 8 data register	--
ANA_ADCDATA9	R	0x0094	ADC channel 9 data register	--
ANA_ADCDATAA	R	0x0098	ADC channel 10 data register	--
ANA_ADCDATAB	R	0x009C	ADC channel 11 data register	--

10.5. Register Definition

10.5.1. ANA_REG1 Register

Table 10-2 Description of each bit in ANA_REG1 of ADC

Bit	Name	Function	Notes
3:0		Reserved.	0
4	RESDIV	Enable resistor division for ADC's input signal	0: Disable 1: Enable 1/4 resistor division
5	GDE4	Enable cap division for ADC's input signal	0: Disable 1: Enable 1/4 cap division
7:6		Reserved.	0

10.5.2. ANA_REG3 Register

Table 10-3 Description of each bit in ANA_REG3 of ADC

Bit	Name	Function	Notes
0	ADCPDN	ADC power up control signal. ADC automatic conversion should be disabled before ADC is powered down.	0: Power-down ADC 1: Power-up ADC
3	ADCBGPPD*	ADCBGP power down control signal.	0: Power-up ADCBGP 1: Power-down ADCBGP
4	RCHPD	RCH (6.5536M RC) power down control signal	0: Power-up RCH 1: Power-down RCH
Note*: RCH and PLL and ADC are related to ADCBGP, must power-up ADCBGP before power-up RCH or PLL or ADC. User can power down ADCBGP by set ADCBGPPD to 1 when ADCBGP was not used in program. User could not power down ADCBGP by set ADCBGPPD to 1 when ADCBGP was used in program, because the system has a protection function to ensure reliability. User can power down ADCBGP in sleep mode and deep-sleep mode whether ADCBGP is used or not.			

10.5.3. ANA_INSTS Register

Table 10-4 Description of ANA_INTSTS Register for ADC

Bit	Name	Type	Description	Default
1	INTSTS1	R/C	Interrupt flag of auto ADC conversion done. Read 0: Auto ADC conversion not complete. Read 1: Auto ADC conversion has done. Write 0: No effect. Write 1: clear this bit.	0x0
0	INTSTS0	R/C	Interrupt flag of manual ADC conversion done. Read 0: Manual ADC conversion not complete. Read 1: Manual ADC conversion has done. Write 0: No effect. Write 1: clear this bit.	0x0

10.5.4. ANA_INTEN Register

Table 10-5 Description of ANA_INTEN Register for ADC

Bit	Name	Type	Description	Default
1	INTEN1	R/W	Interrupt enable control of auto ADC conversion done. 0: Disable auto ADC conversion interrupt. 1: Enable auto ADC conversion interrupt.	0x0
0	INTEN0	R/W	Interrupt enable control of manual ADC conversion done. 0: Disable manual ADC conversion interrupt. 1: Enable manual ADC conversion interrupt.	0x0

10.5.5. ANA_ADCCTRL Register

Table 10-6 Description of ANA_ADCCTRL Register

Bit	Name	Type	Description	Default
31	MTRIG	R/W	Manual ADC trigger. Write 0: No effect. Write 1: Start a manual ADC conversion. Read 0: Current manual ADC conversion is done. Read 1: Current manual ADC conversion is ongoing.	0x0
30	-	-	Reserved.	0
29	CICAON	R/W	CIC filter always on control register. 0: CIC filter will be disabled when no ADC sample process is ongoing. 1: CIC filter will be enabled for all the time.	0x0
28	CICINV	R/W	CIC filter input inversion. 0: No invert CIC filter input. 1: Invert CIC filter input.	0x0
27	CICSCA	R/W	CIC output scale-down selection. 0: No scale down CIC filter's output. 1: Scale down CIC filter's output to 1/2.	0x0
26:24	CICSKIP	R/W	CIC output skip control register. This register is used to control how many samples will be skipped at the beginning of ADC sample. If CICAON is 1 and the ADC channel is not changed, the CIC output will not be skipped by the ADC controller, this can be used for high speed capture to single channel. 0: Skip first 4 samples. 1: Skip first 5 samples. 2: Skip first 6 samples. 3: Skip first 7 samples. 4: No skip any sample. 5: Skip first 1 sample. 6: Skip first 2 samples. 7: Skip first 3 samples.	0x0
23:22	DSRSEL	R/W	CIC down sampling rate control register. The higher down-sampling rate, the higher output data stability, and lower sampling rate. 0: 1/512 down-sampling rate. 1: 1/256 down-sampling rate. 2: 1/128 down-sampling rate. 3: 1/64 down-sampling rate.	0x0
21	AMODE	R/W	Auto ADC mode control. 0: Capture single channel specified by ACH. 1: Capture multiple channels (0~11 channels) at one time.	0x0
20	MMODE	R/W	Manual ADC mode control. 0: Capture single channel specified by MCH. 1: Capture multiple channels (0~11 channels) at one time.	0x0
19			Reserved.	0

18:16	AEN	R/W	Auto ADC conversion enable control register. 0: Auto ADC conversion is off. 4: Auto ADC will be triggered by timer 0's overflow. 5: Auto ADC will be triggered by timer 1's overflow. 6: Auto ADC will be triggered by timer 2's overflow. 7: Auto ADC will be triggered by timer 3's overflow. Others: Reserved.	0x0
15:13			Reserved.	0
12	CLKSEL	R/W	ADC clock source selection. 0: 6.5M RCH 1: PLLL	0x0
11:8	CLKDIV	R/W	The ADC clock source is internal 6.5M RCH or PLLL. The typical ADC main clock is 1.6384MHz, if ADC clock source is 6.5M RCH, CLKDIV is calculated such as: CLKDIV=6.5536/1.6384-1=3.	0x0
7:4	ACH	R/W	Auto ADC channel control. 0: Auto ADC capture ADC channel 0. 1: Auto ADC capture ADC channel 1. …. 11: Auto ADC capture ADC channel 11. 12~15: Reserved. This register is valid only when AMODE is 0. The ADC sampling channels show as the following table.	0x0
3:0	MCH	R/W	Manual ADC channel control. 0: Manual ADC capture ADC channel 0. 1: Manual ADC capture ADC channel 1. …. 11: Auto ADC capture ADC channel 11. 12~15: Reserved. This register is valid only when MMODE is 0. The ADC sampling channels show as the following table.	0x0

Table 10-7 The ADC Sampling Channels

Bit	Name	value
7:4	ACH	0000: GND; 0001: BAT1 0010: BAT2; 0011: ADC_CH3 0100: ADC_CH4; 0101: ADC_CH5 0110: ADC_CH6; 0111: ADC_CH7 1000: ADC_CH8; 1001: ADC_CH9 1010: TEMP; 1011: ADC_CH11
3:0	MCH	

		1100~1111: Reserved.

10.5.6. ANA_ADCDATAx Register

Table 10-8 Description of ANA_ADCDATAx Register

Bit	Name	Type	Description	Default
31:16	-	-	Reserved.	0
15:0	ADCDATAx	R	The result of ADC conversion will be stored in these registers. DATA0: Store conversion result of ADC channel 0. DATA1: Store conversion result of ADC channel 1. … DATA11: Store conversion result of ADC channel 11. For single channel conversion (MMODE is 0 or AMODE is 0), only the channel specified by MCH or ACH will be updated. For multi-channels conversion (MMODE is 1 or AMODE is 1), DATA0~DATA11 will be updated.	0x--

10.6. Measuring Battery Voltage and External Voltage

In the V94XX(A), ADC can be used to measure external voltage signals by ADC_CHx, and can be used to measure BAT1/BAT2 signals.

ADC channel mode: single channel; multi-channel.

ADC trigger mode: auto triggered by timer; manual trigger.

Divider mode: no divider; resistive divider; capacitive divider. Resistance voltage divider has extra power consumption. Because there are 35kΩ resistors in the internal resistive divider network, this network consumes power:

$$P = U_D \times I_D = V \times \frac{V}{R_1 + R_2} = \frac{V^2}{35000}$$ Equation 10-1

The voltage of ordinary channels (ADC_CHx): channel 3, 4, 5, 6, 7, 8, 9 and 11.

The voltage of BAT1 channels: channel 1.

The voltage of BAT2 channels: channel 2.

User needs to check whether a and b (A and B) parameters of storage area used to store ADC coefficients are legal. If so, the data of the storage area is used for calculation; if not, the ADC coefficient is used for calculation with fixed parameters. The calculation formula is shown in Table 4-2 Info Information Register, voltage measuring range and formula. A and b (a and b) of ADC coefficients are shown in Table 4-2 Info Information Register.

Table 10-9 Voltage measurement range and formula

Power	Channel	Divider	Signal	Formula

		Mode	range (V)	
3.3V	ADC_CHx	No divider	-0.2~1.2	If a and b parameters of ADC are valid, $V_{DC} = a1 \div 100000000 * X + b1 \div 100000000$ else $V_{DC}=0.00003680*X+0.00205011$
		Resistive	-0.2~3.6	If a and b parameters of ADC are valid, $V_{DC} = a2 \div 100000000 * X + b2 \div 100000000$ else $V_{DC}=0.00016425*X+0.03739179$
		Capacitive	-0.2~3.6	If a and b parameters of ADC are valid, $V_{DC} = a3 \div 100000000 * X + b3 \div 100000000$ else $V_{DC}=0.00014051*X-0.00023322$
	BAT1 channels	Resistive	2.5~4.8	If a and b parameters of ADC are valid, $V_{DC} = a4 \div 100000000 * X + b4 \div 100000000$ else $V_{DC}=0.00015392*X+0.06667986+OffsetBatR\div1000$
		Capacitive	2.5~4.6	If a and b parameters of ADC are valid, $V_{DC} = a5 \div 100000000 * X + b5 \div 100000000$ else $V_{DC}=0.00014107*X-0.00699515+OffsetBatC\div1000$
	BAT2 channels	Resistive	0.7~4.8	If a and b parameters of ADC are valid, $V_{DC} = a6 \div 100000000 * X + b6 \div 100000000$ else $V_{DC}=0.00015392*X+0.06667986+OffsetBatR\div1000$
		Capacitive	0.7~4.6	If a and b parameters of ADC are valid, $V_{DC} = a7 \div 100000000 * X + b7 \div 100000000$ else $V_{DC}=0.00014107*X-0.00699515+OffsetBatC\div1000$

In the above equations,

$$X = ADC\_DATAx \qquad \text{Equation 10-2}$$

Where:

ADC_DATAx is the content of bytes located at addresses (0x40014270+4x), x is channel 0~11.

10.7. Measuring Temperature

When the ADC channel you choose is TEMPERATURE (CH10), you should not set capacitive division. The temperature measurement range is over -40~+85°C.

It is recommended to measure temperature following steps:

1. Set ADC to start working.

   Users must set ADC CLK to 1.6384 MHz, and set DSRSEL to 1/512 down-sampling rate, with no voltage division or resistor division, then start ADC conversion.

2. Wait for read 1 from ANAINSTS (0x40014260)(ANAINTSTS0(bit 0)/ANAINSTS1(bit 1) in auto/manual mode), and then read the register ADC_DATAA (0x40014298).

3. Calibrate temperature T: (in unit of 8.8 format °C). The format of T is 16-bit signed value, including 8 bits integer and 8 bits fraction signed value. The actual temperature is equal to T/256.0. For example, 0x1880 means 24.5 °C.

$$T = ((P0 * ((X * X) >> 16)) + P1 * X + P2) >> 8$$ Equation 10-3

where X is the reading of register ADC_DATAA(in hexadecimal);

P0 is the content of bytes located at addresses 0x40D00(16bit);

P1 is the content of bytes located at addresses 0x40D02(16bit);

P2 is calculated by the following equation:

$$P2 = P2' + (Tr - Tm) * 256$$ Equation 9-4

where P2' is the content of bytes located at addresses 0x40D04(32bit);

Tr is the content of bytes located at addresses 0x40D70(32bit);

Tm is the content of bytes located at addresses 0x40D74(32bit).

Note:

To enhance ADC data quality in the channel 10 for the temperature sensor, four-sample moving average is implemented. The four buffers used to average are first-in first-out queues, which are reset to zero by DPOR. Every time a user makes an ADC conversion, the hardware writes a data to the buffer, and calculates the average value of the data of the four buffers inside, and puts it in the register of ADC_DATAA. Therefore, in order to get the exact temperature value of a certain temperature, users need to convert ADC four times continuously and take the last ADC_DATAA register data as ADC data.

11. Comparator Controller

11.1. Introduction

The V94XX(A) integrates two comparators to compare the analog signals. Three patterns can be selected as input sources:

- Positive signal input on pin CMP_P and negative signal input on pin CMP_N;
- Positive signal input on pin CMP_P and negative signal from ADCREF or LPREF;
- Positive signal input on pin CMP_N and negative signal from ADCREF or LPREF.

Each comparator have hysteresis voltage of 20mV.

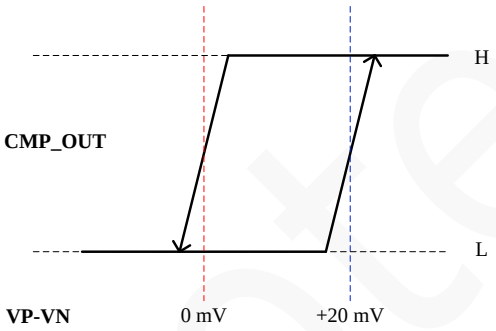


Figure 11-1 hysteresis Window of CMP Controller

11.2. Feature

-- Interrupt/wake-up signal generated for analog detect flag.

-- Comparator interrupt generation.

-- Comparator counter.

11.3. Block Diagram

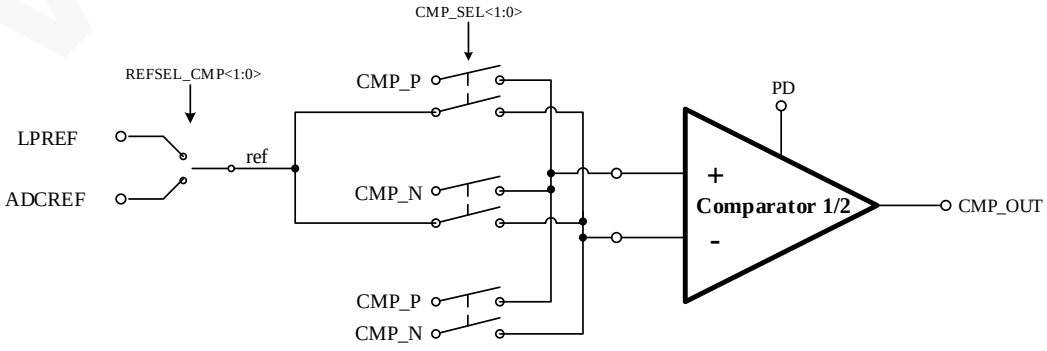


Figure 11-2 Functional Block Diagram of CMP Controller

11.4. Register Location

Table 11-1 Register Location of ANA Controller for CMP (ANA Base: 0x40014200)

Name	Type	Address	Description	Default
ANA_REG2	R/W	0x0008	Analog register 2	0x00
ANA_REG3	R/W	0x000C	Analog register 3	0x00
ANA_REG5	R/W	0x0014	Analog register 5	0x00
ANA_CTRL	R/W	0x0050	Analog control register	0x0000000
ANA_CMPOUT	R	0x0054	Comparator result register	0x0030
ANA_INTSTS	R/C	0x0060	Analog interrupt status register	0x0000
ANA_INTEN	R/W	0x0064	Analog interrupt enable register	0x0000
ANA_CMPCNT1	R/C	0x00B0	Comparator 1 counter	0x00000000
ANA_CMPCNT2	R/C	0x00B4	Comparator 2 counter	0x00000000

11.5. Register Definition

11.5.1. ANA_REG2 Register

Table 11-2 Description of each bit in ANA_REG2 for CMP

Bit	Name	Function	Notes
1:0	CMP1_SEL[1:0]	Signal source selection of comparator 1	00 CMP1_P to REF 01: CMP1_N to REF 1*: CMP1_P to CMP1_N
3:2	CMP2_SEL[1:0]	Signal source selection of comparator 2	00: CMP2_P to REF 01: CMP2_N to REF 1*: CMP2_P to CMP2_N
4	REFSEL_CMP1	REF selection of CMP1	0: LPREF 1: ADCREF
5	REFSEL_CMP2	REF selection of CMP2	0: LPREF 1: ADCREF

11.5.2. ANA_REG3 Register

Table 11-3 Description of each bit in ANA_REG3 for CMP

Bit	Name	Function	Notes
1	CMP1PDN	CMP1 power up control signal	0: Power-down CMP1 1: Power-up CMP1
2	CMP2PDN	CMP2 power up control signal	0: Power-down CMP2 1: Power-up CMP2
3	ADCBGPPD*	ADCBGP power down control signal.	0: Power-up ADCBGP 1: Power-down ADCBGP
Note*: RCH and PLL and ADC are related to ADCBGP, You must power-up ADCBGP before you			

power-up RCH or PLL or ADC. User can power down ADCBGP by set ADCBGPPD to 1 when ADCBGP was not used in program. User could not power down ADCBGP by set ADCBGPPD to 1 when ADCBGP was used in program, because the system has a protection function to ensure reliability. User can power down ADCBGP in sleep mode and deep-sleep mode whether ADCBGP is used or not.

11.5.3. ANA_REG5 Register

Table 11-4 Description of each bit in ANA_REG5 for CMP

Bit	Name	Function	Notes
1:0	IT_CMP1[1:0]	Bias current selection of CMP1	00: 20nA; 01: 100nA; 1*: 500nA;
3:2	IT_CMP2[1:0]	Bias current selection of CMP2	00: 20nA; 01: 100nA; 1*: 500nA;
Note: The smaller the CMP bias current, the lower the power consumption and the longer the propagation delay time; the higher the CMP bias current, the higher the power consumption and the shorter the propagation delay time.			

11.5.4. ANA_CTRL Register

Table 11-5 Description of ANA_CTRL Register for CMP

Bit	Name	Type	Description	Default
23:22	CMP2DEB	R/W	Comparator 2 de-bounce control register. 0: No de-bounce. 1: 2 RTCCLK de-bounce. 2: 3 RTCCLK de-bounce. 3: 4 RTCCLK de-bounce. When de-bounce is enabled, the input signal is valid only when the signal isn't change in multi-cycles of RTCCLK clock. And, the response time of the wake-up and interrupt will be delayed until the signal is valid. This circuit can work under all mode including sleep and deep-sleep mode.	0x0
21:20	CMP1DEB	R/W	Comparator 1 de-bounce control register. 0: No de-bounce. 1: 2 RTCCLK de-bounce. 2: 3 RTCCLK de-bounce. 3: 4 RTCCLK de-bounce. When de-bounce is enabled, the input signal is valid only when the signal isn't change in multi-cycles of RTCCLK clock. And, the response time of the wake-up and interrupt will be delayed until the signal is valid. This circuit can work under all mode including sleep and deep-sleep mode.	0x0
19:18			Reserved.	0

3:2	COMP2_SEL	R/W	This register is used to control the interrupt and wake-up signal generation of COMP2. 0: Off 1: Rising edge of COMP2. 2: Falling edge of COMP2. 3: Change of COMP2.	0x0
1:0	COMP1_SEL	R/W	This register is used to control the interrupt and wake-up signal generation of COMP1. 0: Off 1: Rising edge of COMP1. 2: Falling edge of COMP1. 3: Change of COMP1.	0x0

11.5.5. ANA_CMPOUT Register

Table 11-6 Description of ANA_CMPOUT Register for CMP

Bit	Name	Type	Description	Default
3	COMP2	R	This bit shows the output of comparator 2.	0x0
2	COMP1	R	This bit shows the output of comparator 1.	0x0

11.5.6. ANA_INSTS Register

Table 11-7 Description of ANA_INTSTS Register for CMP

Bit	Name	Type	Description	Default
3	INTSTS3	R/C	Interrupt flag of COMP2, the interrupt generate condition is controlled by COMP2_SEL. Read 0: No COMP2 interrupt. Read 1: COMP2 interrupt is happened. Write 0: No effect. Write 1: Clear this bit.	0x0
2	INTSTS2	R/C	Interrupt flag of COMP1, the interrupt generate condition is controlled by COMP1_SEL. Read 0: No COMP1 interrupt. Read 1: COMP1 interrupt is happened. Write 0: No effect. Write 1: Clear this bit.	0x0

11.5.7. ANA_INTEN Register

Table 11-8 Description of ANA_INTEN Register for CMP

Bit	Name	Type	Description	Default
3	INTEN3	R/W	Interrupt and wake-up enable control of COMP2. 0: Disable COMP2 interrupt and wake-up. 1: Enable COMP2 interrupt and wake-up.	0x0
2	INTEN2	R/W	Interrupt and wake-up enable control of COMP1.	0x0

			0: Disable COMP1 interrupt and wake-up. 1: Enable COMP1 interrupt and wake-up.	

11.5.8. ANA_CMPCNTx Register

Table 11-9 Description of ANA_CMPCNTx Register

Bit	Name	Type	Description	Default
31:0	CNTx	R/C	This register store the happen times of comparator x according to the setting in COMPx_SEL. For example, when COMPx_SEL is set to 1, then this counter will increase 1 when the COMPx is rising. This register can be cleared by writing 0 to this register, but this operation is valid only when corresponded CMPPDNx is set to 1 (when the corresponded comparator is enabled).	0x0000000

12. Tiny ADC Controller

12.1. Introduction

The Tiny ADC (2 BIT ADC) controller is used to control the Tiny ADC function of V94XX(A). TinyADC is powered by VDD. TinyADC controller is placed in always-on domain, so all the tiny ADC setting will be kept under deep-sleep mode.

12.2. Feature

-- TinyADC interrupt generation.

12.3. Block Diagram

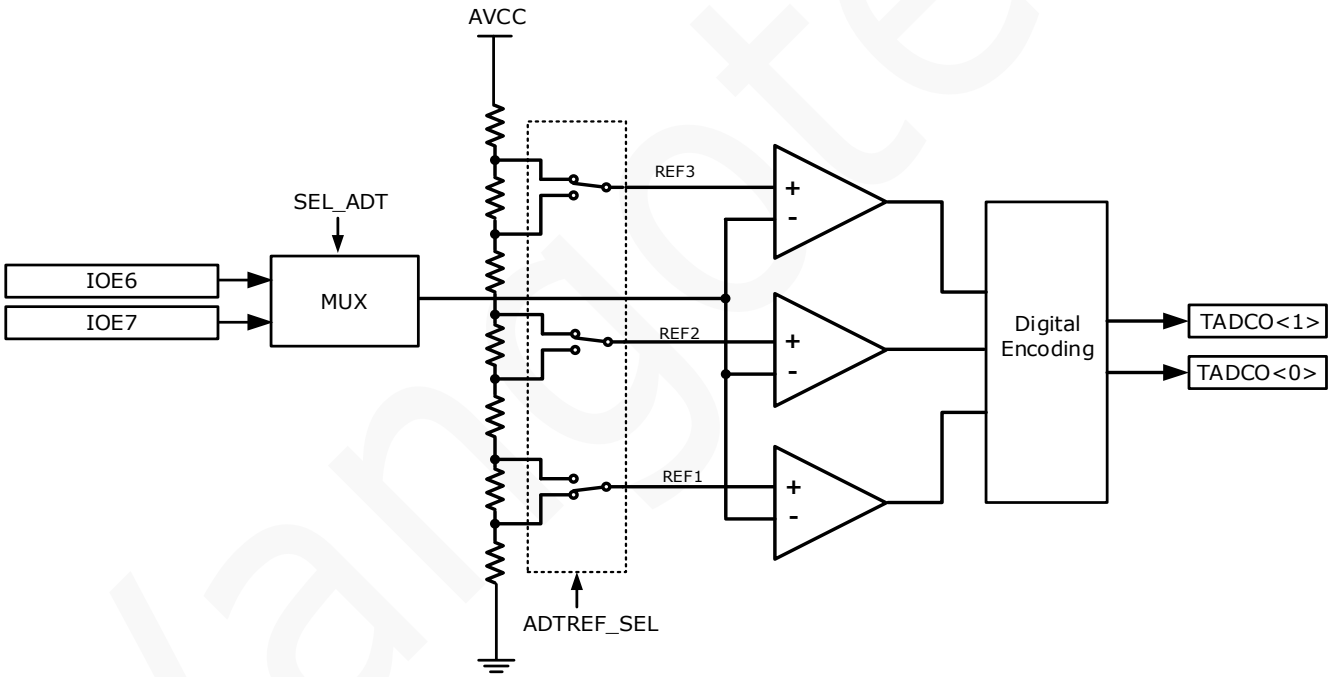


Figure 12-1 Functional Block Diagram of Analog Controller

12.4. Register Location

Table 12-1 Register Location of ANA Controller for TADC(ANA Base: 0x40014200)

Name	Type	Address	Description	Default
ANA_REGF	R/W	0x003C	Analog control register 15	0x00
ANA_CMPOUT	R	0x0054	Comparator result register	0x0030
ANA_INTSTS	R/C	0x0060	Analog interrupt status register	0x0000
ANA_INTEN	R/W	0x0064	Analog interrupt enable register	0x0000
ANA_MISC	R/W	0x00B8	Analog misc. control register	0x00

12.5. Register Definition

12.5.1. ANA_REGF Register

Table 12-2 Description of each bit in ANA_REGF for TADC

Bit	Name	Function	Notes
3	PDN_ADT	Power up Tiny ADC	0: Power down. 1: Power up
4	SEL_ADT	Signal selection for TADC	0: Connect to IOE6 1: Connect to IOE7
5	ADTREF1_SEL	REF1 of TADC selection	0: 0.9V 1: 0.7V
6	ADTREF2_SEL	REF2 of TADC selection	0: 1.8V 1: 1.6V
7	ADTREF3_SEL	REF3 of TADC selection	0: 2.7V 1: 2.5V

12.5.2. ANA_CMPOUT Register

Table 12-3 Description of ANA_CMPOUT Register for TADC

Bit	Name	Type	Description	Default
15:14	TADCO	R	Tiny ADC output. For example, if all the ADTREFx_SEL set to 0, TADCO value as follows. When signal <0.9V, TADCO =0, When signal >0.9V && <1.8V, TADCO =1, When signal >1.8V && <2.7V, TADCO =2, When signal >2.7V, TADCO =3.	-

12.5.3. ANA_INSTS Register

Table 12-4 Description of ANA_INTSTS Register for TADC

Bit	Name	Type	Description	Default
31:14	-	-	Reserved.	0
13	INTSTS13	R/C	TADC change over-threshold interrupt. This interrupt will be set when the TADC is rising or falling and the change value compare to previous cycle is larger than or equal to the threshold setting in the TADCTH in ANA_MISC register, this interrupt flag will be set. Read 0: No TADC over threshold interrupt. Read 1: TADC over threshold is happened. Write 0: No effect. Write 1: Clear this bit.	0x0

12.5.4. ANA_INTEN Register

Table 12-5 Description of ANA_INTEN Register for TADC

Bit	Name	Type	Description	Default
31:14	-	-	Reserved.	0
13	INTEN13	R/W	Interrupt and wake-up enable control of TADC change over or equal to threshold. 0: Disable TADC interrupt and wake-up. 1: Enable TADC interrupt and wake-up.	0x0

12.5.5. ANA_MISC Register

Table 12-6 Description of ANA_MISC Register

Bit	Name	Type	Description	Default
31:6	-	-	Reserved.	0
5:4	TADCTH*	R/W	TADC threshold setting. This register controls the threshold of TADC's interrupt. The TADC is using internal 32K RC as clock source to sample external signal, when TADC's interrupt is enable and the difference of two continuous cycles is larger than or equal to TADCTH, the INTSTS13 will be set and an interrupt will be asserted.	0x0
3:0	-	-	Reserved.	0

Note*: Bit3:0 of ANA_MISC register should be set 0 all the time.

13. PMU_WDT Unit

13.1. Introduction

In the V94XX(A), the embedded 16-bit watchdog timer (WDT) counting pulses of the 32kHz RTCCLK clock.
When the program gets stuck somewhere, the timer overflows and reset the system to cause the program start from the beginning. WDT's reset level is the same as POR reset, it can provide chip's internal reset.

13.2. Features

--WDT counting period:2s\1s\0.5s\0.25s.

--Password protection to avoid close WDT in un-expected event.

13.3. WDT State in Different Modes

For different mode, the enable or disable of WDT module will be controlled by hardware or software, the following table shows the detail of WDT status under each mode when MODE (PMU_STS register bit24) is 1. If MODE (PMU_STS register bit24) is 0, WDT is invalid in all modes.

Table 13-1 WDT Enable or Disable in Different Modes (MODE=1)

WDT	**Power modes**			
	Deep sleep	**Sleep**	**IDLE**	**Active**
State	ON(WDTEN = 1) OFF(WDTEN = 0)	ON(WDTEN = 1) OFF(WDTEN = 0)	ON(WDTEN = 1) OFF(WDTEN = 0)	ON(WDTEN = 1) OFF(WDTEN = 0)
WDT	**Wake up from different modes**			
	Deep sleep		**Sleep**	**IDLE**
State	ON		ON	ON(WDTEN = 1) OFF(WDTEN = 0)

13.4. Register Location

Table 13-2 Register Location of the PMU_WDT Controller (PMU Base: 0x40014000)

Name	**Type**	**Address**	**Description**	**Default**
PMU_WDTPASS	R/W	0x0040	Watch dog timing unlock register	0x00000000
PMU_WDTEN	R/W	0x0044	Watch dog timer enable register	0x1
PMU_WDTCLR	W	0x0048	Watch dog timer clear register	0x0000

13.5. Register Definitions

13.5.1. PMU_WDTPASS Register

Table 13-3 PMU_WDTPASS Register Description

Bit	Name	Type	Description
31:1	Rsvd	-	Reserved.
0	UNLOCK	r	This bit indicates the watch dog timer enable register has been unlocked and is ready to change the watch dog enable control register. To set this bit to 1, programmer should write 0xAA5555AA to this register. This bit will be cleared immediately after any register write to any PMU control register, including ICE write, so programmer should set the PMU_WDTEN immediately after the UNLOCK bit is set to 1, otherwise the UNLOCK procedure should start again.

13.5.2. PMU_WDTEN Register

Table 13-4 PMU_WDTEN Register Description

Bit	Name	Type	Description
31:4	Rsvd	-	Reserved.
3:2	WDTSEL	rw	This register is used to control the WDT counting period. 0: 2 secs 1: 1 sec 2: 0.5 secs 3: 0.25 secs To change the value of this register, UNLOCK bit of PMU_WDTPASS should be set to 1 first.
1	Rsvd	-	Reserved.
0	WDTEN	rw	This bit indicates the watch dog timer is enable. To change the value of this register, UNLOCK bit of PMU_WDTPASS should be set to 1 first.

13.5.3. PMU_WDTCLR Register

Table 13-5 PMU_WDTCLR Register Description

Bit	Name	Type	Description
31:16	Rsvd	-	Reserved.
15:0	WDTCNT	rc_w1	This register shows the current counter value of wat dog timer. When this timer count to limit value set by WDTSEL, the WDT will issue a system reset. So programmer should clear this timer in a regulator time to avoid WDT reset. To clear this timer programmer should write 0x55AAAA55 to this register. During debug mode, this register will be cleared

			to 0 automatically and no WDT reset will be issued under the debug mode.

14. RTC Controller

14.1. Introduction

The RTC controller is used to control time calculation and RTC calibration function. The time calculation function can realize the year, month, week, day, hour, minute, second automatically calculation function and the leap year detection. RTC correction function can automatically correct RTC by software in the background which can detect temperature and adjust one second clock period to compensate the clock shift caused by temperature variation. There are also multi-second, multi-minutes, and multi-hours auto wake-up timer embedded in the RTC engine.

14.2. Feature

--BCD format Time Calculation from second to year.

--Automatically leap year detection.

--Support 32768 frequency compensation.

--Programmable multiple wake-up source.

--Initialize calibration engine for manufactory.

--RTC clock scaling for lower power consumption under sleep/deep-sleep mode.

14.3. Block Diagram

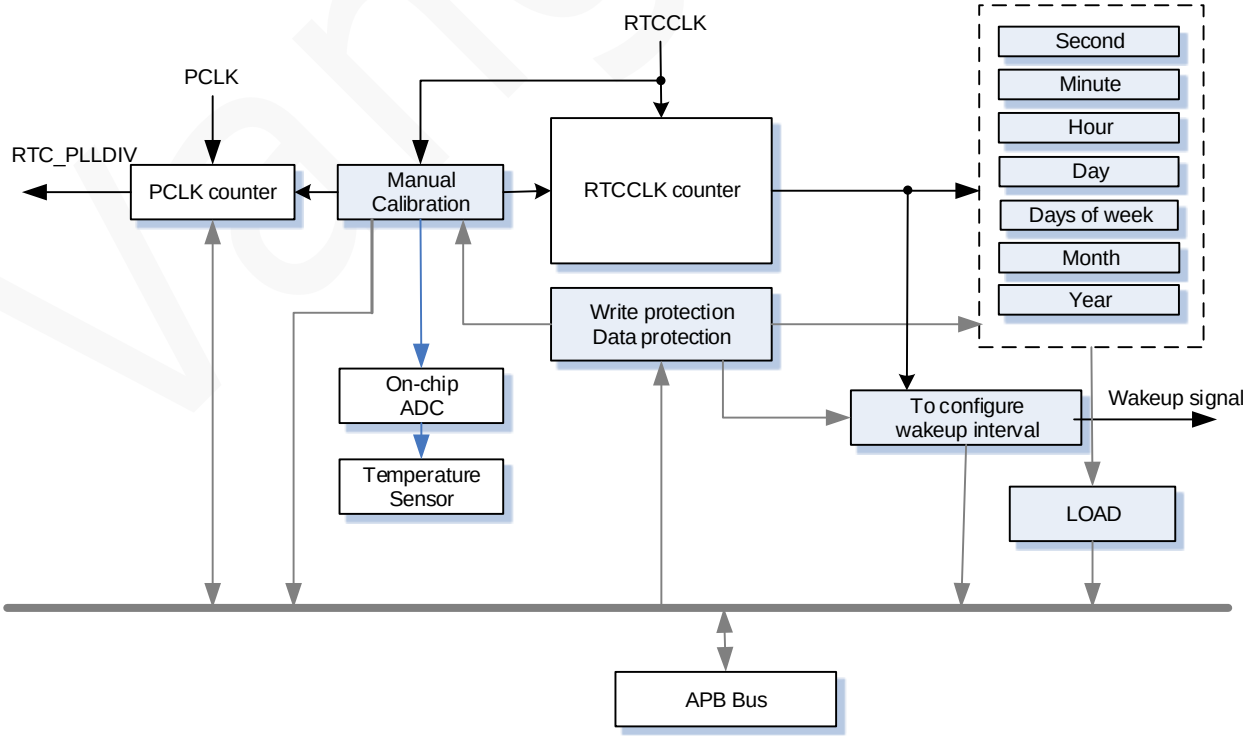


Figure 14-1 Functional Block Diagram of RTC Controller

14.4. Reading and Writing of RTC Register

14.4.1. Writing of RTC

In the V94XX(A), some RTC registers are protected by write protection, including RTC timing registers and RTC calibration registers and so on. For details, please refer to the table 13-1.

The MCU must write of these registers following steps as:

1. User must wait until BSY (bit1 of register RTC_CE) is 0, to ensure the state of RTC is idle;
2. Writing 0x5AA55AA5 to the register RTC_PWD to enable the RTC_CE port's access;
3. Writing 0xA55AA55B to the register RTC_CE to enable writing of write protection registers.
4. Configuring write protection registers. RTC_SEC ~ RTC_YEAR register should be configured together;
5. Writing 0x5AA55AA5 to the register RTC_PWD to enable the RTC_CE port's access;
6. Writing 0xA55AA55A to the register RTC_CE to clear CE (bit0 of register RTC_CE) flag, and BSY (bit1 of register RTC_CE) flag will be set immediately after the CE is cleared from 1 to 0. After CE is cleared to 0, the contents of write protection registers update to RTC core will be start. The update procedure take around 3 32K period, which is around 100us.
7. User must wait until BSY (bit1 of register RTC_CE) cleared to 0 automatically after sixth step configuration, to ensure RTC update is done.

The MCU can write a register that without write protection directly.

14.4.2. Reading of RTC

RTC timing registers are protected from reading. For details, please refer to the Table 14-2.

To read the timing registers, the MCU must read these registers following steps as:

1. User must wait until BSY (bit1 of register RTC_CE) is 0, to ensure the state of RTC is idle;
2. The MCU must read register RTC_LOAD firstly, BSY (bit1 of register RTC_CE) will be set immediately when RTC_LOAD port is read by MCU. BSY will cleared automatically after the read procedure is done, the read procedure take around 3 32K period, which is around 100 μS;
3. After the read procedure of RTC_LOAD is done, the current timed will be latched and programmer can read data from RTC_SEC ~ RTC_YEAR register.

The MCU can read a register that without read protection directly.

14.5. Register Write Reading Protection

"Writing Protection" means the register can write only when CE set 1. When CE clear 0, the value will br updated to RTC register. "Reading Protection" means after RTC_LOAD reading operation happened and BSY clear 0, these register values will be updated.

Table 14-1 RTC Register Protection

Name	Write Protection	Read Protection
RTC_SEC	V	V
RTC_MIN	V	V
RTC_HOUR	V	V
RTC_DAY	V	V
RTC_WEEK	V	V
RTC_MON	V	V
RTC_YEAR	V	V
RTC_WKUSEC	V	
RTC_WKUMIN	V	
RTC_WKUHOUR	V	
RTC_WKUCNT	V	
RTC_CAL	V	
RTC_DIV		
RTC_CTL		
RTC_PWD		
RTC_CE		
RTC_LOAD		
RTC_INTSTS		
RTC_INTEN		
RTC_PSCA	V	
RTC_ACTI	V	
RTC_ACF200	V	
RTC_ACP0	V	
RTC_ACP1	V	
RTC_ACP2	V	
RTC_ACP3		
RTC_ACP4	V	
RTC_ACP5	V	
RTC_ACP6	V	
RTC_ACP7	V	
RTC_ACK1	V	
RTC_ACK2	V	
RTC_ACK3	V	
RTC_ACK4	V	
RTC_ACK5	V	
RTC_WKUCNTR		
RTC_ACKTEMP	V	

14.6. Register Location

The following table shows the register location of each register. The column "Write Protect means the register can only be written when CE is set to 1, and will be updated to RTC core only when CE is cleared

to 0. The column "Read protect" means the value in these register will be updated only when RTC_LOAD port is read and BSY bit is cleared to 0.

Table 14-2 RTC Registers Map

Register Name	Offset	Type	Reset Value	Description
RTC_SEC	0x0000	rw	0x0000_0000	RTC second register
RTC_MIN	0x0004	rw	0x0000_0000	RTC minute register
RTC_HOUR	0x0008	rw	0x0000_0000	RTC hour register
RTC_DAY	0x000C	rw	0x0000_0000	RTC day register
RTC_WEEK	0x0010	rw	0x0000_0000	RTC week-day register
RTC_MON	0x0014	rw	0x0000_0000	RTC month register
RTC_YEAR	0x0018	rw	0x0000_0000	RTC year register
RTC_WKUSEC	0x0020	rw	0x0000_0000	RTC wake-up second register
RTC_WKUMIN	0x0024	rw	0x0000_0000	RTC wake-up minute register
RTC_WKUHOUR	0x0028	rw	0x0000_0000	RTC wake-up hour register
RTC_WKUCNT	0x002C	rw	0x0000_0000	RTC wake-up counter register
RTC_CAL	0x0030	rw	0x0000_0000	RTC calibration register
RTC_DIV	0x0034	rw	0x0000_0000	RTC PLL divider register
RTC_CTL	0x0038	rw	0x0000_0000	RTC PLL divider control register
RTC_PWD	0x0044	rw	0x0000_0000	RTC password control register
RTC_CE	0x0048	rw	0x0000_0000	RTC write enable control register
RTC_LOAD	0x004C	rw	0x0000_0000	RTC read enable control register
RTC_INTSTS	0x0050	rw	0x0000_0000	RTC interrupt status control register
RTC_INTEN	0x0054	rw	0x0000_0000	RTC interrupt enable control register
RTC_PSCA	0x0058	rw	0x0000_0000	RTC clock pre-scaler control register
RTC_ACTI	0x0084	rw	0x0000_1800	RTC center temperature control register
RTC_ACF200	0x0088	rw	0x0064_0000	RTC 200*frequency control register
RTC_ACPx[0..7,0x4]	0x0090	rw	0x0000_0000	RTC parameter x control register
RTC_ACKx[1..5,0x4]	0x00B0	rw	0x0000_0000	RTC parameter k x control register
RTC_WKUCNTR	0x00CC	r	0x0000_0000	This register is used to represent the current WKUCNT value
RTC_ACKTEMP	0x00D0	rw	0x3C28_00EC	RTC k temperature section control register

14.7. Register Definition

14.7.1. RTC_SEC/MIN/DAY/WEEK/MONTH/YEAR Register

The time register is following the BCD encode, where the bit 7~4 is represent the 10's digit and bit 3~0 is for 1's digit. The value in these register can be set only when CE is high, and it will be update to RTC core only when the CE is cleared from 1 to 0. To read current time, programmer should process a read operation to RTC_LOAD register, and wait until the BSY bit is cleared. Otherwise, the register value will be invalid.

Table 14-3 Description of RTC_SEC/MIN/DAY/WEEK/MONTH/YEAR Register

Register		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x0000	RTC_SEC, 0~59	-	S40	S20	S10	S8	S4	S2	S1
0x0004	RTC_MIN, 0~59	-	M40	M20	M10	M8	M4	M2	M1
0x0008	RTC_HOUR,0~23	-	-	H20	H10	H8	H4	H2	H1
0x000C	RTC_DAY, 1~31	-	-	D20	D10	D8	D4	D2	D1
0x0010	RTC_WEEK, 0~6	-	-	-	-	-	W4	W2	W1
0x0014	RTC_MON, 1~12	-	-	-	Mo10	Mo8	Mo4	Mo2	Mo1
0x0018	RTC_YEAR, 00~99	Y80	Y40	Y20	Y10	Y8	Y4	Y2	Y1
Default		X	X	X	X	X	X	X	X
"week" can only be set by user, RTC will not detect automatically. After initialize setting, RTC will increase the week count automatically. For example, when user set 2010/1/1 as Friday, RTC will detect 2010/01/02 as Saturday. W4/W2/W1:000, Sunday; 001, Monday; 010, Tuesday; 011, Wednesday; 100, Thursday; 101, Friday; 110, Saturday. System can only set the last two digit of year, for example, when setting year 2010, RTC_YEAR should be set as 0b00010000.									

14.7.2. RTC_SEC Register

Table 14-4 RTC_SEC Register Description

Bit	Name	Type	Description
31:7	Rsvd	-	Reserved.
6:0	SEC	rw	RTC second register

14.7.3. RTC_MIN Register

Table 14-5 RTC_MIN Register Description

Bit	Name	Type	Description
31:7	Rsvd	-	Reserved.
6:0	MIN	rw	RTC minute register

14.7.4. RTC_HOUR Register

Table 14-6 RTC_HOUR Register Description

Bit	Name	Type	Description
31:6	Rsvd	-	Reserved.
5:0	HOUR	rw	RTC hour register

14.7.5. RTC_DAY Register

Table 14-7 RTC_DAY Register Description

Bit	Name	Type	Description
31:6	Rsvd	-	Reserved.
5:0	DAY	rw	RTC day register

14.7.6. RTC_WEEK Register

Table 14-8 RTC_WEEK Register Description

Bit	Name	Type	Description
31:3	Rsvd	-	Reserved.
2:0	WEEK	rw	RTC week register

14.7.7. RTC_MON Register

Table 14-9 RTC_MON Register Description

Bit	Name	Type	Description
31:5	Rsvd	-	Reserved.
4:0	MON	rw	RTC mon register

14.7.8. RTC_YEAR Register

Table 14-10 RTC_YEAR Register Description

Bit	Name	Type	Description
31:8	Rsvd	-	Reserved.
7:0	YEAR	rw	RTC year register

14.7.9. RTC_WKUSEC Register

Table 14-11 RTC_WKUSEC Register Description

Bit	Name	Type	Description
31:6	Rsvd	-	Reserved.
5:0	WKUSEC	rw	This register is used to control the multi-second wake-up function. The wake-up period is (WKUSEC + 1)*1 second. When the INTEN[2] is 1 and the internal wake-up second count is reach the target value, the INTSTS[2] will be set to 1 and wake-up signal will be asserted to PMU controller. For the first interrupt generated by WKUSEC, it may have < 1 sec error if the new WKUSEC number is not equal to current WKUSEC number. If the new WKUSEC is equal to current WKUSEC, the first interrupt time may have 0~(WKUSEC +1) variation. To avoid this problem, set an alternative value (like 0) to this register and update it with RTC_CE operation. Then set the correct value to it.

14.7.10. RTC_WKUMIN Register

Table 14-12 RTC_WKUMIN Register Description

Bit	Name	Type	Description
31:6	Rsvd	-	Reserved.
5:0	WKUMIN	rw	This register is used to control the multi-minute wake-up function. The wake-up period is (WKUMIN + 1)*1 minute. When the INTEN[3] is 1 and the internal wake-up minute count is reach the target value, the INTSTS[3] will be set to 1 and wake-up signal will be asserted to PMU controller. For the first interrupt generated by WKUMIN, it may have < 1 minute error if the new WKUMIN number is not equal to current WKUMIN number. If the new WKUMIN is equal to current WKUMIN, the first interrupt time may have 0~(WKUMIN +1) variation. To avoid this problem, set an alternative value (like 0) to this register and update it with RTC_CE operation. Then set the correct value to it.

14.7.11. RTC_WKUHOUR Register

Table 14-13 RTC_WKUHOUR Register Description

Bit	Name	Type	Description
31:5	Rsvd	-	Reserved.
4:0	WKUHOUR	rw	This register is used to control the multi-hour wake-up function. The wake-up period is (WKUHOUR + 1)*1 hour. When the INTEN[4] is 1 and the internal wake-up hour count is reach the target value, the INTSTS[4] will be set to 1 and wake-up signal will be asserted to PMU controller. For the first interrupt generated by WKUHOUR, it may have < 1 hour error if the new WKUHOUR number is not equal to current WKUHOUR number. If the new WKUHOUR is equal to current WKUHOUR, the first interrupt time may have 0~(WKUHOUR +1) variation. To avoid this problem, set an alternative value (like 0) to this register and update it with RTC_CE operation. Then set the correct value to it.

14.7.12. RTC_WKUCNT Register

Table 14-14 RTC_WKUCNT Register Description

Bit	Name	Type	Description
31:26	Rsvd	-	Reserved.
25:24	CNTSEL	rw	This is register is used to set the counter clock of WKUCNT. When PSCA is 0.

			0: Counter clock is 32768Hz 1: Counter clock is 2048Hz. 2: Counter clock is 512Hz 3: Counter clock is 128Hz When PSCA is 1. 0: Counter clock is 8192Hz 1: Counter clock is 2048Hz. 2: Counter clock is 512Hz 3: Counter clock is 128Hz
23:0	WKUCNT	rw	This register is used to control the 32K counter wake-up function. The wake-up period is (WKUCNT + 1)*Counter Clock Cycle. The counter clock is controlled by CNTSEL. When the INTEN[6] is 1 and the internal wake-up count is reach the target value, the INTSTS[6] will be set to 1 and wake-up signal will be asserted to PMU controller.

14.7.13. RTC_CAL Register

Table 14-15 RTC_CAL Register Description

Bit	Name	Type	Description
31:14	Rsvd	-	Reserved.
13:0	CAL	rw	RTC 32768 calibration register, this register is a 14 bits signed value. The RTC engine will do calibration for every 30 seconds, the internal counter will count 32768 times during 1~29 second. At the 30 second, it will count [32768-(CAL-1)] for a second, so it can let the average 1 second pulse in 30 seconds become an accurate 1 second pulse. The PPM resolution of the CAL register is 1.02ppm, and the adjustable range is ±8332.3ppm (±12 minutes/day). When RTC is corrected manually, the value of this register needs to be updated manually.

14.7.14. RTC_DIV Register

Table 14-16 RTC_DIV Register Description

Bit	Name	Type	Description
31:26	Rsvd	-	Reserved.
25:0	RTCDIV	rw	This register is used to generate divider output. The output frequency is PCLK/(2*(RTCDIV+1)). When RTC is corrected manually, the value of this register needs to be updated manually.

14.7.15. RTC_CTL Register

Table 14-17 RTC_CTL Register Description

Bit	Name	Type	Description
31:3	Rsvd	-	Reserved.
2	RTCPLLOE	rw	RTC_PLLDIV Divider output enable, this register is used to control the RTC_PLLDIV output. 0: Disable RTC_PLLDIV output. 1: Enable RTC_PLLDIV output. The RTC_PLLDIV output is at IOA[3] or IOA[7], the PMU_IOASEL bit 3 or 7 should also be set to 1 when RTC_PLLDIV output is enabled.
1:0	Rsvd	-	Reserved.

14.7.16. RTC_PWD Register

Table 14-18 RTC_PWD Register Description

Bit	Name	Type	Description
31:1	Rsvd	-	Reserved.
0	PWDEN	r	This register is used to protect the RTC_CE port's access. Before access the RTC_CE, programmer should write 0x5AA55AA5 to this port, and the PWDEN will be set to 1. This bit will be cleared automatically after any write to RTC_CE port. Which means programmer should write to this port again before next access to RTC_CE port.

14.7.17. RTC_CE Register

Table 14-19 RTC_CE Register Description

Bit	Name	Type	Description
31:2	Rsvd	-	Reserved.
1	BSY	r	This flag is used to indicate the RTC update procedure or RTC read procedure is ongoing. This bit will be set immediately after the CE is cleared from 1 to 0 or when RTC_LOAD port is read by CPU. This bit will be cleared automatically after the read or write procedure is done. Programmer can poll this bit to know if the RTC update is done or not. The update or read procedure take around 3 32K period, which is around 100 μS.

0	CE	r	This register is used to unlock the access to RTC register. This register can be only when PWDEN is set to 1 and 0xA55AA55B is written to this register. After this bit is set to 1, the RTC register can be programmed, but the actual update to RTC core will be start after this bit is cleared to 0. To clear this bit, the PWDEN should be set to 1 and 0xA55AA55A should be written to this register.

14.7.18. RTC_LOAD Register

Table 14-20 RTC_LOAD Register Description

Bit	Name	Type	Description
31:0	LOAD	rw	This register is used to let RTC engine read data from RTC core. When programmer read from this port, the current time will be latched and programmer can read data from RTC_SEC ~ RTC_YEAR register. The read procedure will takes 3 RTCCLK cycles, programmer can check the BSY bit to know if the procedure is done. The read data from this port is invalid.

14.7.19. RTC_INTSTS Register

Table 14-21 RTC_INTSTS Register Description

Bit	Name	Type	Description
31:9	Rsvd	-	Reserved.
8	INTSTS8	rc_w1	Interrupt status 8, this interrupt will be set when an illegal write to CE register is happened.The illegal write means the BSY bit is still 1 but CE is set to 1 again or RTC_LOAD port is read again. Write 1 to clear this bit.
7	Rsvd	-	Reserved.
6	INTSTS6	rc_w1	Interrupt status 6, this interrupt will be set when 32K counter interrupt period set by WKUCNT is reach. Write 1 to clear this bit.
5	INTSTS5	rc_w1	Interrupt status 5, this interrupt will be set when mid-night (00:00) is reach. Write 1 to clear this bit.
4	INTSTS4	rc_w1	Interrupt status 4, this interrupt will be set when multi-hour interrupt period set by WKUHOUR is reach. Write 1 to clear this bit.
3	INTSTS3	rc_w1	Interrupt status 3, this interrupt will be set when multi-minute interrupt period set by WKUMIN is reach. Write 1 to clear this bit.
2	INTSTS2	rc_w1	Interrupt status 2, this interrupt will be set when multi-second interrupt period set by WKUSEC is reach. Write 1 to clear this bit.
1	INTSTS1	rc_w1	Interrupt status 1, this interrupt will be set when illegal time format is written into RTC core. Write 1 to clear this bit.

0	Rsvd	-	Reserved.

14.7.20. RTC_INTEN Register

Table 14-22 RTC_INTEN Register Description

Bit	Name	Type	Description
31:9	Rsvd	-	Reserved.
8	INTEN8	rw	Interrupt enable 8, when this bit is 1 and INTSTS8 is set, and interrupt will be asserted to CPU.
7	Rsvd	-	Reserved.
6	INTEN6	rw	Interrupt enable 6, when this bit is 1, the INTSTS6 interrupt will be asserted to CPU and wake-up signal will be asserted to PMU controller.
5	INTEN5	rw	Interrupt enable 5, when this bit is 1, the INTSTS5 interrupt will be asserted to CPU and wake-up signal will be asserted to PMU controller.
4	INTEN4	rw	Interrupt enable 4, when this bit is 1, the INTSTS3 interrupt will be asserted to CPU and wake-up signal will be asserted to PMU controller.
3	INTEN3	rw	Interrupt enable 3, when this bit is 1, the INTSTS3 interrupt will be asserted to CPU and wake-up signal will be asserted to PMU controller.
2	INTEN2	rw	Interrupt enable 2, when this bit is 1, the INTSTS2 interrupt will be asserted to CPU and wake-up signal will be asserted to PMU controller.
1	INTEN1	rw	Interrupt enable 1, when this bit is 1, the INTSTS1 interrupt will be asserted to CPU and wake-up signal will be asserted to PMU controller.
0	Rsvd	-	Reserved.

14.7.21. RTC_PSCA Register

Table 14-23 RTC_PSCA Register Description

Bit	Name	Type	Description
31:2	Rsvd	-	Reserved.
1:0	PSCA	rw	This register is used to control the RTCCLK pre-scaler. When slow down the RTCCLK, it can significantly reduce the power under sleep or deep-sleep mode. 0: No pre-scaler, RTC clock is 32768 Hz. 1: 1/4 pre-scaler, RTC clock is 8192 Hz. 2~3: Reserved. When this register is set, all modules which is using RTCCLK will be affected. The RTC time counter and LCD frame rate will be automatically adjusted by hardware, so no need to modify the setting. But the RTC_WKUCNT's input clock will be changed, so programmer should modify the corresponded

			setting. And the UART 32K baud rate register need to be re-calculated according to new RTCCLK speed.

14.7.22. RTC_ACTI Register

Table 14-24 RTC_ACTI Register Description

Bit	Name	Type	Description
31:16	Rsvd	-	Reserved.
15:0	ACTI	rw	This register is used to store the Ti value which is used as the center temperature during calibration. This register is 8 bits integer and 8 bits fraction value. This register can be updated only when CE is 1. For example, 0x1880 means 24.5 degree (24.5*256=6272=0x1880), 0xE780 means -24.5 degree(~0x1880+1=0xE780).

14.7.23. RTC_ACF200 Register

Table 14-25 RTC_ACF200 Register Description

Bit	Name	Type	Description
31:26	Rsvd	-	Reserved.
25:0	F200	rw	This register is used to store the current PCLK speed value which is used for the calculation of PLLDIV value. This register is 26 bits integer. For example, when current PCLK speed is 6.5536MHz, then programmer should fill 6553600/2 = 0x320000 into this register. At the same time, the P6 should also be changed according to the following equation. P6 = 0.0004096 * F200. This register can be updated only when CE is 1.

14.7.24. RTC_ACPx Register

Table 14-26 RTC_ACPx Register Description

Bit	Name	Type	Description
31:0	P0~P7	rw	Only P2 is 32 bits signed value, other P0~P7 is 16 bits signed value. P3 is read only and will be updated automatically according to calculated temperature. These registers can be updated only when CE is 1. The P0~P7 (exclude P3) will be updated automatically when power-up or wake-up from deep-sleep mode. Please refer to FLASH control section for detail.

14.7.25. RTC_ACKx Register

Table 14-27 RTC_ACKx Register Description

Bit	Name	Type	Description
31:16	Rsvd	-	Reserved.
15:0	K1~K5	rw	The K1~K5 registers are 16 bits signed register. Hardware will auto select a suitable Kx according to calculated temperature T and update to RTC_ACP3 register. K1: T< KTEMP1. K2: KTEMP1≤T< KTEMP2. K3: KTEMP2≤T< KTEMP3. K4: KTEMP3≤T< KTEMP4. K5: T≥KTEMP4. These registers can be updated only when CE is 1.

14.7.26. RTC_ACKTEMP Register

Table 14-28 RTC_ACKTEMP Register Description

Bit	Name	Type	Description
31:24	KTEMP4	rw	This register is used to control the section 4 temperature. This is a signed 8 bits value. This register can be updated only when CE is 1.
23:16	KTEMP3	rw	This register is used to control the section 3 temperature. This is a signed 8 bits value. This register can be updated only when CE is 1.
15:8	KTEMP2	rw	This register is used to control the section 2 temperature. This is a signed 8 bits value. This register can be updated only when CE is 1.
7:0	KTEMP1	rw	This register is used to control the section 1 temperature. This is a signed 8 bits value. This register can be updated only when CE is 1.

14.7.27. RTC_WKUCNTR Register

Table 14-29 RTC_WKUCNTR Register Description

Bit	Name	Type	Description
31:24	Rsvd	-	Reserved.
23:0	WKUCNTR	r	This register is used to represent the current WKUCNT value. WKUCNTR increases from 0 to WKUCNT. Accumulating from 0, after reaching the WKUCNT setting value, continue to accumulate from 0 again.

14.8. Info information register（Related to RTC-Cal）

The RTC calibration data is stored in Info Sector 4 (0x40800). The address 0x40800 ~ 0x409FF data is written by special download tool (offline download and RTC calibration). Other data is written before leaving factory. The following table shows the details of this information.

Info Sector data can only be read and cannot be written. All information has a backup. The first data in the form is expressed in 1, and second copies in 2. Each data has a checksum data. Checksum algorithm: add up each data, and reverse the result.

Table 14-30 Info Information Register (Related to RTC-Cal)

Address	Sign	Data	Description
0x00040800	P4	RTC normal temperature offset 1	Load low 16 bits to RTC_ACP4 register, such as 0. unit(0.1ppm),
0x00040804		Check sum 1	INV(SUM(0x40800,0x40800))
0x00040808	P4	RTC normal temperature offset 2	Load low 16 bits to RTC_ACP4 register, such as 0. unit(0.1ppm),
0x0004080C		Check sum 2	INV(SUM(0x40808,0x40808))
0x00040810	K1	Crystal secondary calibration coefficient K1 1	Load to RTC_ACK1 register. K1 is calculated as follows: K1=B1/1000000*65536, B1 is the segment factor of crystal oscillator' quadratic curve. For example, the value of K1 is 20827.
0x00040814	K2	Crystal secondary calibration coefficient K2 1	Load to RTC_ACK2 register. K2 is calculated as follows: K2=B2/1000000*65536, B2 is the segment factor of crystal oscillator' quadratic curve. For example, the value of K2 is 21496.
0x00040818	K3	Crystal secondary calibration coefficient K3 1	Load to RTC_ACK3 register. K3 is calculated as follows: K3=B3/1000000*65536, B3 is the segment factor of crystal oscillator' quadratic curve. For example, the value of K3 is 22020.
0x0004081C	K4	Crystal secondary calibration coefficient K4 1	Load to RTC_ACK4 register. K4 is calculated as follows: K4=B4/1000000*65536, B4 is the segment factor of crystal oscillator' quadratic curve. For example, the value of K4 is 24517.
0x00040820	K5	Crystal secondary calibration coefficient K5 1	Load to RTC_ACK5 register. K5 is calculated as follows: K5=B5/1000000*65536, B5 is the segment factor of crystal oscillator' quadratic curve. For example, the value of K5 is 25257.
0x00040824		Check sum 1	INV(SUM(0x40810, 0x40820))
0x00040828	K1	Crystal secondary calibration coefficient K1 2	Load to RTC_ACK1 register. K1 is calculated as follows: K1=B1/1000000*65536, B1 is the segment factor of crystal oscillator' quadratic curve. For example, the value of K1 is 20827.
0x0004082C	K2	Crystal secondary calibration coefficient K2 2	Load to RTC_ACK2 register. K2 is calculated as follows: K2=B2/1000000*65536, B2 is the segment factor of crystal oscillator' quadratic curve. For example, the value of K2 is 21496.
0x00040830	K3	Crystal secondary calibration coefficient K3 2	Load to RTC_ACK3 register. K3 is calculated as follows: K3=B3/1000000*65536, B3 is the segment factor of crystal oscillator' quadratic curve. For example, the value of K3 is 22020.
0x00040834	K4	Crystal secondary calibration coefficient K4 2	Load to RTC_ACK4 register. K4 is calculated as follows: K4=B4/1000000*65536, B4 is the segment factor of crystal oscillator' quadratic

			curve. For example, the value of K4 is 24517.
0x00040838	K5	Crystal secondary calibration coefficient K5 2	Load to RTC_ACK5 register. K5 is calculated as follows: K5=B5/1000000*65536, B5 is the segment factor of crystal oscillator' quadratic curve. For example, the value of K5 is 25257.
0x0004083C		Check sum 2	INV(SUM(0x40828, 0x40838))
0x00040840	ACTI	Fixed point temperature of crystal 1	Load to RTC_ACTI register, such as 0x1800
0x00040844		Check sum 1	INV(SUM(0x40840,0x40840))
0x00040848	ACTI	Fixed point temperature of crystal 2	Load to RTC_ACTI register, such as 0x1800
0x0004084C		Check sum 2	INV(SUM(0x40848,0x40848))
0x00040850	KTEMPx(x=4~1)	Temperature section division settings 1	Load to RTC_ACKTEMP register, such as 0x3C2800EC
0x00040854		Check sum 1	INV(SUM(0x40850,0x40850))
0x00040858	KTEMPx(x=4~1)	Temperature section division settings 2	Load to RTC_ACKTEMP register, such as 0x3C2800EC
0x0004085C		Check sum 2	INV(SUM(0x40858,0x40858))
0x00040D00	P1/P0	RTC_ACP1/0 set 1	Load the high 16 bits to RTC_ACP1 register, such as 1060; Load the low 16 bits to RTC_ACP0, such as -214.
0x00040D04	P2'	RTC_ACP2 set 1	The value in this register is recorded as P2', such as -19746971. According to the formula P2=P2'+(Tr-Tm)*256 to calculate P2, and load P2 to RTC_ACP2 register.
0x00040D08	P5	RTC_ACP5 set 1	Load the high 16 bits to RTC_ACP5 register, such as 6444, and the low 16 bits be abandon.
0x00040D0C	P7/P6'	RTC_ACP 7/6 set 1	Load the high 16 bits to RTC_ACP7 register, such as 0; Load the low 16 bits to P6' register, such as 1342. According to the formula: P6=a*P6' to calculate P6, where a=PCLK/6553600.
0x00040D10		Check Sum set 1	INV(SUM(0x40DE0, 0x40DEC))
0x00040D14	P1/P0	RTC_ACP1/0 set 2	Load the high 16 bits to RTC_ACP1 register, such as 1060; Load the low 16 bits to RTC_ACP0, such as -214.
0x00040D18	P2'	RTC_ACP2 set 2	The value in this register is recorded as P2', such as -19746971. According to the formula P2=P2'+(Tr-Tm)*256 to calculate P2, and load P2 to RTC_ACP2 register.
0x00040D1C	P5	RTC_ACP5 set 2	Load the high 16 bits to RTC_ACP5 register, such as 6444, and the low 16 bits be abandon.
0x00040D20	P7/P6'	RTC_ACP 7/6 set 2	Load the high 16 bits to RTC_ACP7 register, such as 0; Load the low 16 bits to P6' register, such as 1342. According to the formula: P6=a*P6' to calculate

			P6, where a=PCLK/6553600.
0x00040D24		Check Sum set 2	INV(SUM(0x40DF4, 0x40E00))
0x00040D70	Tr	Real Temperature 1 (from tmp275)	According to the formula P2=P2'+(Tr-Tm)*256 to calculate P2, and load P2 to RTC_ACP2 register.
0x00040D74	Tm	Measure Temperature 1 (from ADC)	
0x00040D78		Temp Check sum 1	INV(SUM(0x40D70, 0x40D74))
0x00040D7C	Tr	Real Temperature 2 (from tmp275)	According to the formula P2=P2'+(Tr-Tm)*256 to calculate P2, and load P2 to RTC_ACP2 register.
0x00040D80	Tm	Measure Temperature 2 (from ADC)	
0x00040D84		Temp Check sum 2	INV(SUM(0x40D7C, 0x40D80))

14.9. Application Note

14.9.1. Temperature Calibration

User can calculate temperature T according to the following formula, and T is 256 times larger than the actual temperature.

$$T = \left(\left(P0 * \left(\left(X * X\right) >> 16\right)\right) + P1 * X + P2\right) >> 8$$

Where X is ADC sampling data, and X is 16 bits complement.

The P0~P2 is the value in RTC_ACP0~RTC_ACP2 registers, and P0~P2 is used to doing the temperature calibration.

The actual temperature is calculated as following.

$$T' = T / 256$$

14.9.2. Frequency Error Calibration

（1） User can calculate the frequency error of the chip as follows:

$$Delta = \left(P3 * \left(\left(T - Ti\right)^2 >> 16\right)\right) >> 16 + P4$$

Where *Delta* is the error rate in 0.1ppm unit of frequency deviation of 32768.

T = Actual temperature of the chip.

Ti= Setting value in RTC_ACTI register, which is the center temperature of the crystal during RTC calibration.

P4= The crystal deviation in normal temperature.

P3 is the K coefficient of the crystal for the current temperature. When RTC manual temperature compensation, users need to manually match Kx (x = 1 ~ 5) according to the calculated temperature T, and carry out frequency correction according to Kx. There is no need to store values to RTC_ ACP3

register.

（2） User can calculate the frequency correction value as follows:

$$RTC\_CAL = (Delta * P5) >> 16$$

P5 is the value in RTC_ACP5 register, or user can calculate *P5* as follows:

$P5 = 65536 / 10 / (1 / 30 / 32768 / \text{RTCCLK prescaler})$, and $(1 / 30 / 32768 / \text{RTCCLK prescaler})$ is PPM resolution of the RTC_CAL register.

（3） User can calculate the PLL frequency division to output second pulse as follows:

$$RTC\_DIV = PCLK / 2 - (Delta * P6) >> 12 - 1$$

Where *P6* is the value in RTC_ACP6 register, or user can calculate *P6* as follows:

$$P6 = PCLK * 2.048 * 10^{-4}$$

14.9.3. RTC Manual Temperature Compensation

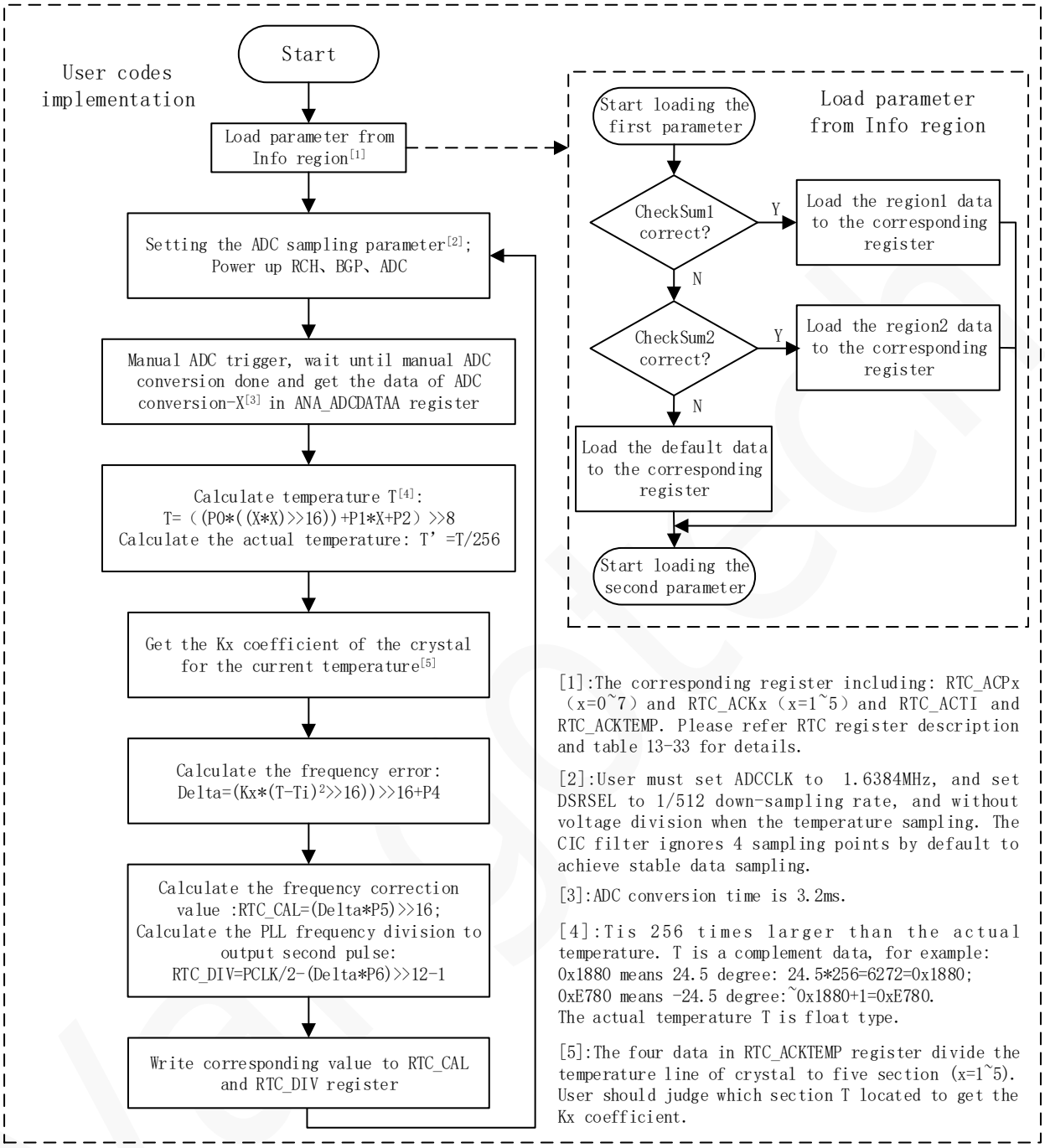


Figure 14-2 RTC Manual Temperature Compensation Flow Chart

15. FLASH Controller

15.1. Introduction

The FLASH controller is used to controller the read/write program of embedded FLASH. It supports byte/half-word/word program and sector/chip erase. Programmable timing can be controlled by 1USCYCLE in MISC controller. It will automatically gate the external master access when FLASH is not ready, and always provide correct data with correct access timing. The setting in FLASH controller will be reset after wake-up from sleep or deep-sleep mode, programmer should restore the setting manually after wake-up from these two states.

15.2. Feature

--Support byte/half-word/word programming.

--Support sector/chip erase.

--Support standby mode. When MCU does not access flash, flash automatically enters standby mode. Any access to flash will wake the flash from standby with a wake-up time of 0.

--Support deep-standby mode. When MCU enters sleep mode or deep-standby mode, flash automatically enters deep-standby mode. At the same time, support the manual access to the deep-standby mode by configuration of flash FLASH_DSTB register. Any access to flash will cause flash to wake up from deep-standby with a wake-up time of 10*1ustick.

--Support automatically gate external master when FLASH is not ready.

--Support Info sector read.

--Support FLASH configuration register read/write.

--Programmable program speed.

--Support background checksum function and interrupt.

15.3. Block Diagram

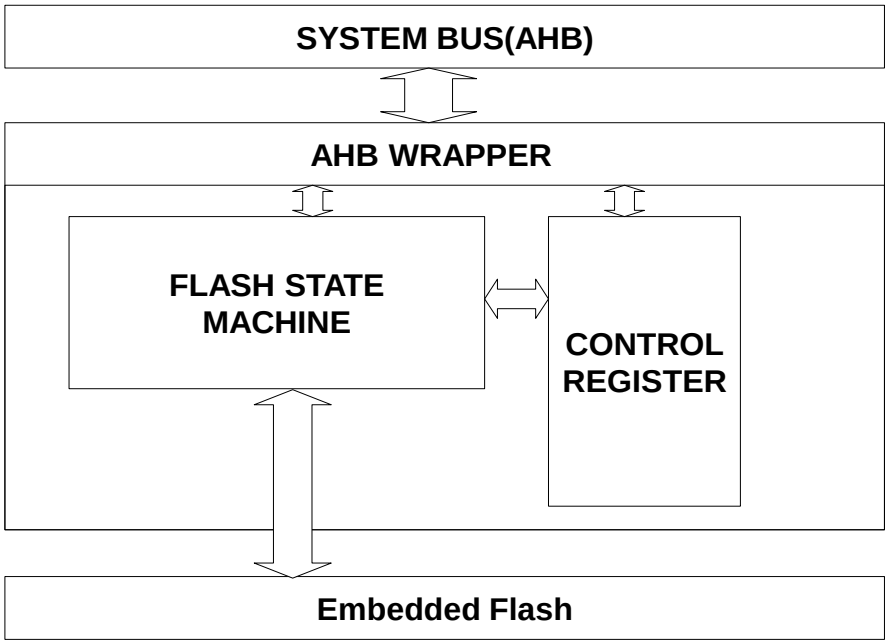


Figure 15-1 Functional Block Diagram of FLASH Controller

15.4. Register Location

Table 15-1 FLASH Registers Map

Register Name	Offset	Type	Reset Value	Description
FLASH_STS	0x00BC	r	0x0000_0000	FLASH programming status register
FLASH_INT	0x00CC	rc_w1	0x0000_0000	FLASH Checksum interrupt status
FLASH_CSSADDR	0x00D0	rw	0x0000_0000	FLASH Checksum start address
FLASH_CSEADDR	0x00D4	rw	0x0003_FFFC	FLASH Checksum end address
FLASH_CSVALUE	0x00D8	r	0x0000_0000	FLASH Checksum value register
FLASH_CSCVALUE	0x00DC	rw	0x0000_0000	FLASH Checksum compare value register
FLASH_PASS	0x00E0	rw	0x0000_0000	FLASH password register
FLASH_CTRL	0x00E4	rw	0x0000_0000	FLASH control register
FLASH_PGADDR	0x00E8	rw	0x0000_0000	FLASH program address register
FLASH_PGDATA	0x00EC	rw	0x0000_0000	FLASH program word data register
FLASH_SERASE	0x00F4	rw	0x0000_0000	FLASH sector erase control register
FLASH_CERASE	0x00F8	rw	0x0000_0000	FLASH chip erase control register
FLASH_DSTB	0x00FC	rw	0x0000_0000	FLASH deep standby control register

Table 15-2 Register Location of MISC2 Controller for FLASH (MISC2 Base: 0x40013E00)

Name	Type	Address	Description	Default
MISC2_FLASHWC	R/W	0x0000	FLASH wait cycle register	0x2100

15.5. Register Definition

15.5.1. FLASH_PASS Register

Table 15-3 FLASH_PASS Register Description

Bit	Name	Type	Description
31:1	Rsvd	-	Reserved.
0	UNLOCK	r	The UNLOCK bit is used to indicate the FLASH program has been unlocked or not. To set this bit, programmer should write 0x55AAAA55 to this register. This bit will be kept high until programmer write any other value to this register. If the UNLOCK bit is 0, all FLASH program or erase or write configuration action will be disabled.

15.5.2. FLASH_CTRL Register

Table 15-4 FLASH_CTRL Register Description

Bit	Name	Type	Description
31:4	Rsvd	-	Reserved.
2	CSINTEN	rw	This register is used to control the interrupt enable of checksum error. 0: Disable checksum error interrupt. 1: Enable checksum error interrupt.
1:0	CSMODE	rw	This register is used to control the checksum mode. 0: Disable checksum function. 1: Always-on checksum mode 2: Checksum start at overflow of timer 2. 3: Checksum start at rising edge of RTC second pulse.

15.5.3. FLASH_PGADDR Register

Table 15-5 FLASH_PGADDR Register Description

Bit	Name	Type	Description
31:18	Rsvd	-	Reserved.
17:0	PGADDR	rw	This register is used to control the program address before doing program. This is byte address of FLASH IP, please refer to table 14-6 for detail about address under each mode. This address will increment automatically when a successful program is done.

Table 15-6 Description of PGADDR and Write Data Port under Different Mode

Mode	PGADDR[17:2]	PGADDR[1:0]	Write Data Port
Normal Word Program	0x0000~0xFFFF	0	FLASH_PGDATA
Normal Byte Program	0x0000~0xFFFF	0	FLASH_PGB0

		1	FLASH_PGB1
		2	FLASH_PGB2
		3	FLASH_PGB3
Normal Half-Word Program	0x0000~0xFFFF	0	FLASH_PGHW0
		2	FLASH_PGHW1
Sector Erase	0x0000~0xFFFF	0	FLASH_SERASE

15.5.4. FLASH_PGDATA Register

Table 15-7 FLASH_PGDATA Register Description

Bit	Name	Type	Description
31:0	PGDATA	rw	This register is used to control the program data. When UNLOCK is 1, write to this register will trigger a 4 bytes program automatically. Any access to FLASH IP during this period will be gated until the program is done. A two 32 bits FIFO is inside the FLASH controller, so programmer can do continuous program without interrupt. But if programmer needs to access FLASH IP, like execute program, during this period the FLASH program speed will become slower since more setup time is required for FLASH IP. It is suggested to put your programming program in SRAM, then the maximum program speed can be achieved. It is a must to do word write to this register to trigger a 4 bytes program, byte or half-word write will result-in single byte or two-bytes program.

15.5.5. FLASH_PGBx Register

Table 15-8 Description of FLASH_PGBx Register

Bit	Name	Type	Description	Default
7:0	PGBx	R/W	This register is used to control the program data. When UNLOCK is 1, write to this register will trigger one-byte program automatically. Any access to FLASH IP during this period will be gated until the program is done. A two 8 bits FIFO is inside the FLASH controller, so programmer can do continuous program without interrupt. But if programmer needs to access FLASH IP, like execute program, during this period the FLASH program speed will become slower since more setup time is required for FLASH IP. It is suggested to put your programming program in SRAM, then the maximum program speed can be achieved. It is a must to do byte write to this register to trigger a single byte program, word or half-word write will result-in 4 bytes or two-bytes program.	

15.5.6. FLASH_PGHWx Register

Table 15-9 Description of FLASH_PGHWx Register

Bit	Name	Type	Description	Default
15:0	PGHWx	R/W	This register is used to control the program data. When UNLOCK is 1, write to this register will trigger a 2 bytes program automatically. Any access to FLASH IP during this period will be gated until the program is done. A two 16 bits FIFO is inside the FLASH controller, so programmer can do continuous program without interrupt. But if programmer needs to access FLASH IP, like execute program, during this period the FLASH program speed will become slower since more setup time is required for FLASH IP. It is suggested to put your programming program in SRAM, then the maximum program speed can be achieved. It is a must to do half-word write to this register to trigger a 2 bytes program, byte or word write will result-in single byte or 4-bytes program.	

15.5.7. FLASH_SERASE Register

Table 15-10 FLASH_SERASE Register Description

Bit	Name	Type	Description
31:1	Rsvd	-	Reserved.
0	SERASE	r	This bit is used to indicate if the sector erase is ongoing or not. This bit can be set when UNLOCK is 1 and programmer write 0xAA5555AA to this register, and it will be cleared automatically after the sector erase is done. The address of sector erase is controlled by PGADDR[17:2]. The sector erase time is 4000* 1us tick. One sector is 512 byte.

15.5.8. FLASH_CERASE Register

Table 15-11 FLASH_CERASE Register Description

Bit	Name	Type	Description
31:1	Rsvd	-	Reserved.
0	CERASE	r	This bit is used to indicate if the chip erase is ongoing or not. This bit can be set when UNLOCK is 1 and programmer write 0xAA5555AA to this register, and it will be cleared automatically after the chip erase is done. The chip erase time is 30000* 1us tick.

15.5.9. FLASH_DSTB Register

Table 15-12 FLASH_DSTB Register Description

Bit	Name	Type	Description
31:1	Rsvd	-	Reserved.
0	DSTB	r	This bit is used to indicate if the FLASH IP is entering deep standby. This bit can be set when UNLOCK is 1 and programmer write 0xAA5555AA to this register, and it will be cleared automatically after the FLASH IP wake-up from deep-standby mode. The deep standby mode can exit by any access to FLASH IP, but a 10 μS tick is required for the FLASH IP to back to normal state. During this period, the any access to FLASH will be gated until FLASH is ready.

15.5.10. FLASH_INT Register

Table 15-13 FLASH_INT Register Description

Bit	Name	Type	Description
31:1	Rsvd	-	Reserved.
0	CSERR	rc_w1	Checksum error status bit. This flag is used to indicate the previous checksum operation has error, which means compare fail from CSVALUE to CSCVALUE. When CSINTEN is 1, an interrupt will be asserted to CPU. Write 1 to clear this flag.

15.5.11. FLASH_CSSADDR Register

Table 15-14 FLASH_CSSADDR Register Description

Bit	Name	Type	Description
31:18	Rsvd	-	Reserved.
17:0	CSSADDR	rw	Checksum start address register. This register is used to control the start address of checksum. The value in this register is byte address, but the LSB 2 bits are always 0.

15.5.12. FLASH_CSEADDR Register

Table 15-15 FLASH_CSEADDR Register Description

Bit	Name	Type	Description
31:18	Rsvd	-	Reserved.
17:0	CSEADDR	rw	Checksum end address register. This register is used to control the end address of checksum. The value in this register is byte address, but the LSB 2 bits are always 0. The checksum range is (CSSADDR =< ADDR =< CSSADDR).

15.5.13. FLASH_CSVALUE Register

Table 15-16 FLASH_CSVALUE Register Description

Bit	Name	Type	Description
31:0	CSVALUE	r	Checksum latched value register. This register is used to represent the checksum result of previous checksum operation.

15.5.14. FLASH_CSCVALUE Register

Table 15-17 FLASH_CSCVALUE Register Description

Bit	Name	Type	Description
31:0	CSCVALUE	rw	Checksum compare value register. This register is used to store the expected checksum result. When the checksum is done but the calculated checksum value doesn't match CSCVALUE, the CSERR flag will be set. Calculating method of checksum compare value: accumulate all the values in this range (CSSADDR =< ADDR=< CSEADDR). The cumulative result is valid for 32 bits of data.

15.5.15. FLASH_STS Register

Table 15-18 FLASH_STS Register Description

Bit	Name	Type	Description
31:5	Rsvd	-	Reserved.
4:0	STS	r	FLASH controller status register. 1: FLASH operation is done. Others: FLASH controller is in busy state or idle state. Programmer can poll this register to ensure all FLASH operation is done before disabling the FLASH_PASS register.

15.5.16. MISC2_FLASHWC Register

Table 15-19 Description of MISC2_FLASHWC Register

Bit	Name	Type	Description	Default
31:14	-		Reserved.	0
13:8	1USCYCLE	R/W	This register is used for FLASH controller to calculate 1ustick from AHB clock 1ustick = (AHB clock period)*(1USCYCLE+1) This setting is related to the wake-up time of FLASH, and the programming time of FLASH. FLASH wake-up time =1ustick *10. It must meet 1ustick >=1 μs. For example, the clock frequency of AHB is 26.2144MHz. In order to ensure the minimum wake-up time, 1USCYCLE should be set to 26. So, the	0x21

			wake-up time of FLASH is 27 / 26214400 * 10, which is about 10 μs. For example, the clock frequency of AHB is 32.768KHz. In order to ensure the minimum wake-up time, 1USCYCLE should be set to 0. So, the wake-up time of FLASH is 1 / 32768 * 10, which is about 305 μs.	
7:0	-		Reserved.	0

16. GPIO Controller

16.1. Introduction

There total 75 IOs in V94XX(A) and 14 IOs (GPIOA) are controlled by PMU controller with wake-up function. Other IOs (GPIOB~GPIOF) are controlled by GPIO controller which will lose its state at deep sleep mode, but keep their state at sleep mode, programmer should restore the setting manually after wake-up from deep-sleep mode.

16.2. Feature

--Each IO can be input or output mode.

--Each IO can be open drain mode.

--All pins have no pull-up and pull-down.

--GPIOA can wake up Sleep mode and Deep-sleep mode.

16.3. Block Diagram

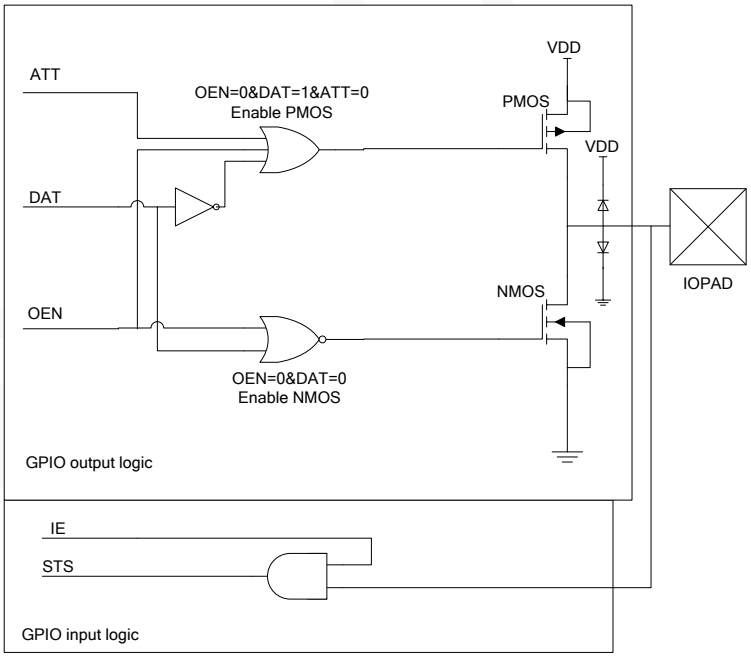


Figure 16-1 Functional Block Diagram of GPIO Controller

16.4. GPIOA Register Location

Table 16-1 Register Location of the PMU_IOA Controller for GPIO(PMU Base: 0x40014000)

Name	Type	Address	Description	Default
PMU_IOAOEN	R/W	0x0010	IOA output enable register	0xFFFF

PMU_IOAIE	R/W	0x0014	IOA input enable register	0xFFFF
PMU_IOADAT	R/W	0x0018	IOA data register	0x0000
PMU_IOAATT	R/W	0x001C	IOA attribute register	0x0000
PMU_IOAWKUEN	R/W	0x0020	IOA wake-up enable register	0x00000000
PMU_IOASTS	R	0x0024	IOA input status register	--
PMU_IOAINTSTS	R/C	0x0028	IOA interrupt status register	0x0000
PMU_IOASEL	R/W	0x0038	IOA special function select register	0x0000
PMU_IOANODEG	R/W	0x0050	IOA no-deglitch control register.	0x0000

16.5. GPIOA Register Definition

16.5.1. PMU_IOAOEN Register

Table 16-2 Description of PMU_IOAOEN Register

Bit	Name	Type	Description	Default
31:16	-	-	Reserved.	0
15:0	IOAOEN	R/W	Each bit controls the IOA's output enable signal, referred to Table 16-6 for detail of IO state. 0: Enable IO's output function. 1: Disable IO's output function.	0xFFFF

16.5.2. PMU_IOAIE Register

Table 16-3 Description of PMU_IOAIE Register

Bit	Name	Type	Description	Default
31:16			Reserved.	0
15:0	IOAIE	R/W	Each bit controls the IOA's input enable signal, referred to Table 16-6 for detail of IO state. 0: Disable IO's input function. 1: Enable IO's input function.	0xFFFF

16.5.3. PMU_IOADAT Register

Table 16-4 Description of PMU_IOADAT Register

Bit	Name	Type	Description	Default
31:16			Reserved.	0
15:0	IOADAT	R/W	Each bit controls the IOA's output data and pull low/high function, referred to Table 16-6 for detail of IO state.	0x0000

16.5.4. PMU_IOAATT Register

Table 16-5 Description of PMU_IOAATT Register

Bit	Name	Type	Description	Default
31:16			Reserved.	0
15:0	IOAATT	R/W	Each bit controls the IOA's attribute, referred to Table 16-6 for detail of IO state. When an IO is set to output mode (GPIO or special function), this bit is used to control the CMOS or open drain mode of the IO pad. 0: CMOS mode. 1: Open drain mode (disable PMOS output).	0x0000

Table 16-6 IO Status under Different Kind of Setting

IOx Setting			IO Status
IOxOEN	IOxDAT	IOxATT	
1	0	0	Disable output function.
1	1	0	Disable output function.
1	0	1	Disable output function.
1	1	1	Disable output function.
0	0	0	Output low
0	1	0	Output high
0	0	1	Open drain output low.
0	1	1	Open drain pull-high

16.5.5. PMU_IOAWKUEN Register

Table 16-7 Description of PMU_IOAWKUEN Register

Bit	Name	Type	Description	Default
31:0	IOAWKUEN	R/W	Every 2 bits control the IOA's wake up or interrupt enable function. Bit [1:0]: IOA0WKUEN[1:0] Bit [3:2]: IOA1WKUEN[1:0] …… Bit [31:30]: IOA15WKUEN[1:0] Refer to Table 16-8 for detail of each wake-up mode.	0x00000000

Table 16-8 Description of each IO wake-up mode

IOAyWKUEN[1:0]	IOAyDAT	Wake-up Event
0	X	Disable wake-up function
1	0	Rising edge
	1	Falling Edge
2	0	High Level
	1	Low level
3	X	Rising or falling edge

Which y=0 ... 15, indicating an IO port.

For rising edge or falling edge wake-up source, since the H/W will use the final latch IO status before entering sleep or deep-sleep mode, so the programmer needs to wait until the IO status change back to normal state. For example, when rising edge mode is chosen, the programmer should wait until the IO

status back to low state to ensure the rising edge can be detected correctly. For high level or low level source, IO have no debounce in normal interrupt or wake up from sleep or deep sleep mode, but IO have four RTCCLK clock cycles debounce When CPU wake up from sleep or deep sleep mode.

16.5.6. PMU_IOASTS Register

Table 16-9 Description of PMU_IOASTS Register

Bit	Name	Type	Description	Default
31:16	-	-	Reserved.	0
15:0	IOASTS	R	Each bit represents the current IOA's input data value.	

16.5.7. PMU_IOAINTSTS Register

Table 16-10 Description of PMU_IOAINTSTS Register

Bit	Name	Type	Description	Default
31:16	-	-	Reserved.	0
15:0	IOAINTSTS	R/C	Each bit represents the IOA's interrupt status. The corresponded bit will be set to 1 when corresponded wake-up event is detected. This register can be clear to 0 by writing corresponded bit to 1.	0x0000

16.5.8. PMU_IOASEL Register

Table 16-11 Description of PMU_IOASEL Register

Bit	Name	Type	Description	Default
31:8	-	-	Reserved.	0
7	IOA_SEL7	R/W	IOA7 special function select register. 0: GPIO 1: Special function 1 (RTC_PLLDIV).	0x0
6	IOA_SEL6	R/W	IOA6 special function select register. 0: GPIO 1: Special function 2 (CMP2_O).	0x0
5:4	-	-	Reserved.	0
3	IOA_SEL3	R/W	IOA3 special function select register. 0: GPIO 1: Special function 1 (RTC_PLLDIV).	0x0
2:0	-	-	Reserved.	0

16.5.9. PMU_IOANODEG Register

Table 16-12 Description of PMU_IOANODEG Register

Bit	Name	Type	Description	Default
31:16	-	-	Reserved.	0
15:0	IOANODEG	R/W	Each bit control if the IOA wake-up signal will go through	0x0000

			de-glitch circuit or not. If set this bit to 1, the corresponded IOA wake-up signal will not go through de-glitch circuit which can have a faster wake-up time. This bit affect the edge wake-up signal under sleep and deep-sleep mode. 0: IOA wake-up signal will go through de-glitch circuit. 1: IOA wake-up signal will not go through de-glitch circuit.	

16.6. GPIOB-F Register Location

Table 16-13 GPIO Registers Map

Register Name	Offset	Type	Reset Value	Description
GPIO_OEN	0x0000	rw	0x0000_FFFF	GPIO output enable register
GPIO_IE	0x0004	rw	0x0000_FFFF	GPIO input enable register
GPIO_DAT	0x0008	rw	0x0000_0000	GPIO output data register
GPIO_ATT	0x000C	rw	0x0000_0000	GPIO attribute register
GPIO_STS	0x0010	r	0x0000_0000	GPIO input status register

16.7. GPIOB-F Register Definition

16.7.1. GPIO_OEN Register

Table 16-14 GPIO_OEN Register Description

Bit	Name	Type	Description
31:16	Rsvd	-	Reserved.
15:0	OENx	rw	Each bit controls the output enable signal of pin x. About the details of IO bit, please refer to 错误!未找到引用源。. 0: enable IO output 1: diable IO outuput

16.7.2. GPIO_IE Register

Table 16-15 GPIO_IE Register Description

Bit	Name	Type	Description
31:16	Rsvd	-	Reserved.
15:0	IEx	rw	Each bit controls the input enable signal of pin x. About the details of IO status, please refer to 错误!未找到引用源。. 0: disable IO input 1: enable IO input

Note*: The bit6 & bit7 of GPIOE port should be set to 1.

16.7.3. GPIO_DAT Register

Table 16-16 GPIO_DAT Register Description

Bit	Name	Type	Description
31:16	Rsvd	-	Reserved.
15:0	DATx	rw	Each bit controls output data and pull-high/pull-down function. The details of IO bit, please refer to 错误!未找到引用源。.

16.7.4. GPIO_ATT Register

Table 16-17 GPIO_ATT Register Description

Bit	Name	Type	Description
31:16	Rsvd	-	Reserved.
15:0	ATTx	rw	Each bit in the register is used to control the corresponding IO attribute. 0: CMOS output 1: open-drain output When an IO is configured as the special function, such as UART or SPI, user can configure the corresponding ATT to 1, and let it become open-drain mode via the external output high.

16.7.5. GPIO_STS Register

Table 16-18 GPIO_STS Register Description

Bit	Name	Type	Description
31:16	Rsvd	-	Reserved.
15:0	STSx	r	Each bit shows the current pin x input data. It must enable input, then can read the external level status.

16.8. GPIOAF Register Address

Table 16-19 GPIOAF Registers Map

Register Name	Offset	Type	Reset Value	Description
GPIOAF_PBSEL	0x0000	rw	0x0000_0000	GPIOAF port B special function select register
GPIOAF_PESEL	0x000C	rw	0x0000_0000	GPIOAF port E special function select register
GPIOAF_MISC	0x0020	rw	0x0000_0000	GPIOAF misc control register

16.9. GPIOAF Register Definition

16.9.1. GPIOAF_PBSEL Register

Table 16-20 GPIOAF_PBSEL Register Description

Bit	Name	Type	Description
31:7	Rsvd	-	Reserved.
6	SEL6	rw	IOB6 special function select register 0: GPIO or special function 1/2. 1: Special function 3 (RTCCLK output) when special function 1/2 is not enabled.
5:3	Rsvd	-	Reserved.
2	SEL2	rw	IOB2 special function select register 0: GPIO or special function 1/2. 1: Special function 3 (PLLL output) when special function 1/2 is not enabled.
1	SEL1	rw	IOB1 special function select register 0: GPIO or special function 1/2. 1: Special function 3 (PLLH divider output) when special function 1/2 is not enabled.
0	Rsvd	-	Reserved.

16.9.2. GPIOAF_PESEL Register

Table 16-21 GPIOAF_PESEL Register Description

Bit	Name	Type	Description
31:8	Rsvd	-	Reserved.
7	SEL7	rw	IOE7 special function select register 0: GPIO or high resistance 1: Special function 1 (CMP1_O)
6:0	Rsvd	-	Reserved.

16.9.3. GPIOAF_MISC Register

Table 16-22 GPIOAF_MISC Register Description

Bit	Name	Type	Description
31:6	Rsvd	-	Reserved.
5	I2CIOC	rw	The register is used to control IOB and IOC for I^2C function. 0: I^2C function with IOB13~IOB14 1: I^2C function with IOC4~IOC5
4:3	Rsvd	-	Reserved.
2:0	PLLHDIV	rw	When IOB1 is selected as the special function 3, the register

			is used to control PLLH output division ratio. 0: /1 1: /2 2: /4 3: /8 4: /16 Other: reserved

16.10. Special Function of IO

16.10.1. Special Function of IOA

The following table shows the special function of IOA, the special function will be turn-on when corresponded module is enabled.

Table 16-23 Special Function of IOA

IO	Special Function 1	Special Function 2	Special Function 3	Special Function 4
IOA0	SWCLK (When MODE is 0)		LCDSEG54	
IOA1	SWDIO (When MODE is 0)		LCDSEG53	
IOA3	RTC_PLLDIV		LCDSEG51	
IOA4			LCDSEG66	CMP2_P
IOA5			LCDSEG67	CMP2_N
IOA6	CMP2_O		LCDSEG68	
IOA7	RTC_PLLDIV		LCDSEG69	
IOA8			LCDSEG50	ADC_CH3
IOA9			LCDSEG49	ADC_CH4
IOA11			LCDSEG47	ADC_CH6
IOA12	UART RX0		LCDSEG71	
IOA13	UART RX1	ISO7816_IO	LCDSEG73	
IOA14	UART RX2		LCDSEG13	
IOA15			LCDSEG15	

16.10.2. Special Function of IOB

The following table shows the special function of IOB, the special function will be turn-on when corresponded module is enabled. But when special function is LCD COM/SEG or ADC or CMP or X6_5M or VDCIN, programmer should disable GPIO input and disable GPIO output manually and disable other special function on this GPIO to ensure the correctness of these special functions.

Table 16-24 Special function of IOB

IO	Special Function 1	Special Function 2	Special Function 3	Special Function 4
IOB0	UART RX4	PWM0		LCDSEG43
IOB1	UART RX5		PLLH divider	LCDSEG45

IOB2	UART TX0		PLLL	LCDSEG70
IOB3	UART TX1	ISO7816_CLK		LCDSEG72
IOB4	UART TX2			LCDSEG12
IOB6	UART TX4	PWM1	RTCCLK	LCDSEG44
IOB7	UART TX5			LCDSEG46
IOB9				LCDSEG36
IOB13	I2CSCL (I2CIOC=0)	PWM2		LCDSEG40
IOB14	I2CSDA (I2CIOC=0)	PWM3		LCDSEG41
IOB15	TIMER EXT CLK			LCDSEG42

16.10.3. Special Function of IOC

The following table shows the special function of IOC, the special function will be turn-on when corresponded module is enabled. But when special function is LCD COM/SEG or ADC or CMP or X6_5M or VDCIN, programmer should disable GPIO input and disable GPIO output manually and disable other special function on this GPIO to ensure the correctness of these special functions.

Table 16-25 Special function of IOC

IO	Special Function 1	Special Function 2	Special Function 3
IOC0	SPICSN		LCDSEG16
IOC1	SPICLK		LCDSEG17
IOC2	SPIMISO		LCDSEG18
IOC3	SPIMOSI		LCDSEG19
IOC4		I2CSCL (I2CIOC=1)	LCDSEG20
IOC5		I2CSDA (I2CIOC=1)	LCDSEG21
IOC6			LCDSEG22
IOC7			LCDSEG23
IOC8			LCDSEG24
IOC9			LCDSEG25
IOC10			LCDSEG26
IOC11			LCDSEG27
IOC12			LCDSEG28
IOC13			LCDSEG29
IOC14			LCDSEG30
IOC15			LCDSEG31

16.10.4. Special Function of IOD

The following table shows the special function of IOD, the special function will be turn-on when corresponded module is enabled. But when special function is LCD COM/SEG or ADC or CMP or X6_5M or VDCIN, programmer should disable GPIO input and disable GPIO output manually and disable other special function on this GPIO to ensure the correctness of these special functions.

Table 16-26 Special function of IOD

IO	Special Function 1	Special Function 2
IOD0	LCDCOM0	

IOD1	LCDCOM1	
IOD2	LCDCOM2	
IOD3	LCDCOM3	
IOD4	LCDCOM4	LCDSEG0
IOD5	LCDCOM5	LCDSEG1
IOD6	LCDCOM6	LCDSEG2
IOD7	LCDCOM7	LCDSEG3
IOD8	LCDSEG4	
IOD9	LCDSEG5	
IOD10	LCDSEG6	
IOD12	LCDSEG8	
IOD13	LCDSEG9	
IOD14	LCDSEG10	
IOD15	LCDSEG11	

16.10.5. Special Function of IOE

The following table shows the special function of IOE, the special function will be turn-on when corresponded module is enabled. But when special function is LCD COM/SEG or ADC or CMP or X6_5M or VDCIN, programmer should disable GPIO input and disable GPIO output manually and disable other special function on this GPIO to ensure the correctness of these special functions.

Table 16-27 Special function of IOE

IO	Special Function 1	Special Function 2	Special Function 3
IOE0		LCDSEG74	
IOE1		LCDSEG75	
IOE2		LCDSEG76	
IOE3		LCDSEG77	
IOE4		LCDSEG63	ADC_CH7
IOE5		LCDSEG62	ADC_CH8
IOE6		LCDSEG61	ADC_CH9, Tiny ADC 0
IOE7	CMP1_O	LCDSEG60	ADC_CH11, Tiny ADC 1
IOE8		LCDSEG59	CMP1_P
IOE9			CMP1_N
IOE10		LCDSEG32	
IOE11		LCDSEG33	
IOE13		LCDSEG55	
IOE14		LCDSEG56	

16.10.6. Special Function of IOF

The following table shows the special function of IOF, the special function will be turn-on when corresponded module is enabled. But when special function is LCD COM/SEG or ADC or CMP or X6_5M or VDCIN, programmer should disable GPIO input and disable GPIO output manually and disable other special function on this GPIO to ensure the correctness of these special functions.

Table 16-28 Special function of IOF

IO	Special Function 1
IOF0	X6_5MI
IOF1	X6_5MO

17. DMA Controller

17.1. Introduction

The DMA controller is used to transfer data from memory to memory or transfer data from memory to IO or from IO to memory. The DMA controller is also integrated with an AHB to APB bridge, so when DMA is doing APB transfer, the AHB performance will not be affected by slow peripheral. There are total 4 channels integrated in V94XX(A) and each channel's priority is round-robin. The setting in DMA controller will be reset after wake-up from sleep or deep-sleep mode, programmer should restore the setting manually after wake-up from these two states.

17.2. Feature

--Memory to Memory Transfer

--Memory to IO Transfer

--IO to Memory Transfer

--Software mode or Hardware DMA request mode.

--Support Fix, Package Round or Frame Round Address mode

--Support Package/Frame/Data-abort IRQ generation.

--Support detection of data abort on bus.

--Integrated with AHB to APB Bridge.

--Support AES 128/192/256 encode/decode

17.3. Block Diagram

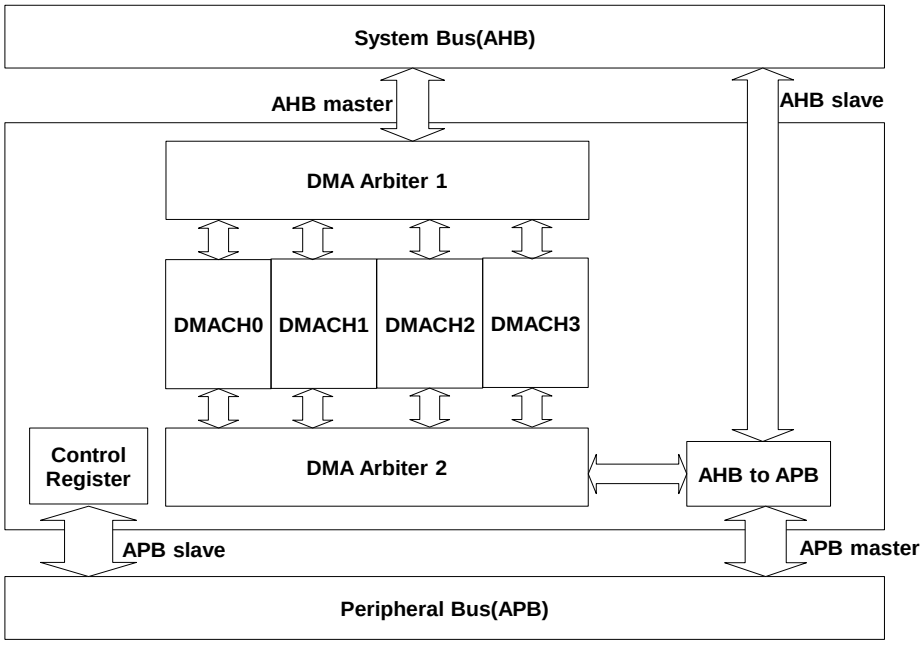


Figure 17-1 Functional Block Diagram of DMA Controller

17.4. Register Location

Table 17-1 DMA Registers Map

Register Name	Offset	Type	Reset Value	Description
DMA_IE	0x0000	rw	0x0000_0000	DMA interrupt enable register
DMA_STS	0x0004	rw	0x0000_0000	DMA status register
DMA_CxCTL[0..3,0x10]	0x0010	rw	0x0000_0000	DMA channel x control register
DMA_CxSRC[0..3,0x10]	0x0014	rw	0x0000_0000	DMA channel x source register
DMA_CxDST[0..3,0x10]	0x0018	rw	0x0000_0000	DMA channel x destination register
DMA_CxLEN[0..3,0x10]	0x001C	r	0x0000_0000	DMA channel x transfer length register
DMA_AESCTL	0x0050	rw	0x0000_0000	DMA AES control register
DMA_AESKEYx[0..7,0x4]	0x0060	rw	0x0000_0000	DMA AES key x register

17.5. Register Definition

17.5.1. DMA_IE Register

Table 17-2 DMA_IE Register Description

Bit	Name	Type	Description
31:12	Rsvd	-	Reserved.
11	C3DAIE	rw	Channel 3 data abort interrupt enable 0: Disable

			1: Enable
10	C2DAIE	rw	Channel 2 data abort interrupt enable 0: Disable 1: Enable
9	C1DAIE	rw	Channel 1 data abort interrupt enable 0: Disable 1: Enable
8	C0DAIE	rw	Channel 0 data abort interrupt enable 0: Disable 1: Enable
7	C3FEIE	rw	Channel 3 frame end interrupt enable 0: Disable 1: Enable
6	C2FEIE	rw	Channel 2 frame end interrupt enable 0: Disable 1: Enable
5	C1FEIE	rw	Channel 1 frame end interrupt enable 0: Disable 1: Enable
4	C0FEIE	rw	Channel 0 frame end interrupt enable 0: Disable 1: Enable
3	C3PEIE	rw	Channel 3 package end interrupt enable 0: Disable 1: Enable
2	C2PEIE	rw	Channel 2 package end interrupt enable 0: Disable 1: Enable
1	C1PEIE	rw	Channel 1 package end interrupt enable 0: Disable 1: Enable
0	C0PEIE	rw	Channel 0 package end interrupt enable 0: Disable 1: Enable

17.5.2. DMA_STS Register

Table 17-3 DMA_STS Register Description

Bit	Name	Type	Description
31:16	Rsvd	-	Reserved.
15	C3DA	rc_w1	Channel 3 data abort interrupt flag, write 1 to clear this flag.
14	C2DA	rc_w1	Channel 2 data abort interrupt flag, write 1 to clear this flag.
13	C1DA	rc_w1	Channel 1 data abort interrupt flag, write 1 to clear this flag.
12	C0DA	rc_w1	Channel 0 data abort interrupt flag, write 1 to clear this flag.
11	C3FE	rc_w1	Channel 3 frame end interrupt flag, write 1 to clear this flag.
10	C2FE	rc_w1	Channel 2 frame end interrupt flag, write 1 to clear this flag.
9	C1FE	rc_w1	Channel 1 frame end interrupt flag, write 1 to clear this flag.

8	C0FE	rc_w1	Channel 0 frame end interrupt flag, write 1 to clear this flag.
7	C3PE	rc_w1	Channel 3 package end interrupt flag, write 1 to clear this flag.
6	C2PE	rc_w1	Channel 2 package end interrupt flag, write 1 to clear this flag.
5	C1PE	rc_w1	Channel 1 package end interrupt flag, write 1 to clear this flag.
4	C0PE	rc_w1	Channel 0 package end interrupt flag, write 1 to clear this flag.
3	C3BUSY	r	DMA channel 3 busy register 0: Idle 1: Busy
2	C2BUSY	r	DMA channel 2 busy register. 0: Idle 1: Busy
1	C1BUSY	r	DMA channel 1 busy register. 0: Idle 1: Busy
0	C0BUSY	r	DMA channel 0 busy register. 0: Idle 1: Busy

17.5.3. DMA_CxCTL Register

Table 17-4 shows the bit assignment of DMA_CxCTL register, the data in this register will be latched into DMA channel after the transfer is start, so any modification to this register won't affect the on-going DMA transfer. Only STOP bit can stop the DMA transfer immediately.

Table 17-4 DMA_CxCTL Register Description

Bit	Name	Type	Description
31:24	FLEN	rw	Package number register, actual transfer package number is (FLEN + 1). Total length is (FLEN + 1) * (PLEN + 1).
23:16	PLEN	rw	Package length register, actual transfer package length is (PLEN + 1). Total length is (FLEN + 1) * (PLEN + 1).
15	STOP	rw	Force stop DMA transfer, write 1 to this bit will force the DMA channel back to idle state, programmer should clear this bit to 0 if another DMA transfer need to be assigned into the same channel. 0: Normal mode. 1: Force stop DMA transfer.
14	AESEN	rw	Enable AES encrypt/decrypt function of DMA channel. Only DMA channel 3 supports AES function. When AES function is enabled, the SIZE should be set to 32 bits mode and SMODE and TMODE should be set to 1 or 2. And package size should be multiply of 4. 0: Disable. 1: Enable.

13	CONT	rw	Continuous mode, DMA transfer will not stop until STOP bit is set to 1. Every time DMA complete all package and frame transfer, it will start from beginning and do the transfer continuously. 0: Discontinuous mode. 1: Continuous mode.
12	TMODE	rw	Transfer mode selection register. 0: One DMA request only transfers one single data. 1: One DMA request transfers one package data.
11:7	DMASEL	rw	DMA request source selection. Please refer to Table 16-5 of detail about each DMA
6:5	DMODE	rw	Destination address mode. 0: Fix. 1: Incremental but rounded at package end. 2: Incremental but rounded at frame end. 3: Reserved.
4:3	SMODE	rw	Source address mode. 0: Fix. 1: Incremental but rounded at package end. 2: Incremental but rounded at frame end. 3: Reserved.
2:1	SIZE	rw	Transfer size mode. 0: Byte (8 bits). 1: Half-word (16 bits) 2: Word (32 bits) 3: Reserved.
0	EN	rw	DMA channel enable register. 0: Disable DMA channel (no effect when CONT is 1) 1: Enable DMA channel. This bit will be cleared automatically by hardware when a DMA transfer is done at CONT is 0.

Table 17-5 DMA Source Selection

DMASEL	Source	DMASEL	Source	DMASEL	Source	DMASEL	Source
0	Software	8	-	16	-	24	UART 32K 0
1	-	9	-	17	-	25	UART 32K 1
2	UART0 TX	10	UART4 TX	18	TIMER 0	26	CMP1
3	UART0 RX	11	UART4 RX	19	TIMER 1	27	CMP2
4	UART1 TX	12	UART5 TX	20	TIMER 2	28	-
5	UART1 RX	13	UART5 RX	21	TIMER 3	29	-
6	UART2 TX	14	ISO7816 TX	22	-	30	SPI TX
7	UART2 RX	15	ISO7816 RX	23	-	31	SPI RX

17.5.4. DMA_CxSRC Register

Table 17-6 DMA_CxSRC Register Description

Bit	Name	Type	Description
31:0	SRC	rw	DMA source address register. When SIZE in DMA_CxCTL is 1, then this register must be half-word aligned. When SIZE in DMA_CxCTL is 2, then this register must be word aligned. When the SRC is set to 0x4001xxxx, then it will be switch to IO read automatically.

17.5.5. DMA_CxDST Register

Table 17-7 DMA_CxDST Register Description

Bit	Name	Type	Description
31:0	DST	rw	DMA destination address register. When SIZE in DMA_CxCTL is 1, then this register must be half-word aligned. When SIZE in DMA_CxCTL is 2, then this register must be word aligned. When the DST is set to 0x4001xxxx, then it will be switch to IO write automatically.

17.5.6. DMA_CxLEN Register

Table 17-8 DMA_CxLEN Register Description

Bit	Name	Type	Description
31:16	Rsvd	-	Reserved.
15:8	CFLEN	r	Current transferred package number. The total length of DMA transmission is CFLEN * (PLEN +1) + CPLEN. After all packages are transferred, it will be automatically cleared.
7:0	CPLEN	r	Current transferred package length. The total length of DMA transmission is CFLEN * (PLEN +1) + CPLEN. After all packages are transferred, it will be automatically cleared.

17.5.7. DMA_AESCTL Register

Table 17-9 DMA_AESCTL Register Description

Bit	Name	Type	Description
31:4	Rsvd	-	Reserved.
3:2	MODE	rw	AES mode selection register. 0: AES128 1: AES192 2: AES256 3: Reserved.
1	Rsvd	-	Reserved.
0	ENC	rw	AES encode/decode selection register. 0: Decode 1: Encode

17.5.8. DMA_AESKEYx Register

Table 17-10 DMA_AESKEYx Register Description

Bit	Name	Type	Description
31:0	KEYx	rw	AES KEY register. KEY0: bit 31~0 KEY1: bit 63~32 KEY2: bit 95~64 KEY3: bit 127~96 KEY4: bit 159~128 KEY5: bit 191~160 KEY6: bit 223~192 KEY7: bit 255~224. When mode is AES128, only bit 127~0 is used. When mode is AES192, only bit 191~0 is used. When mode is AES256, bit 255~0 is used.

18. UART Controller

18.1. Introduction

The UART controller is used to transmit/receive data via UART protocol. There are total 5 UART controller in V94XX(A), each UART controller can be program individually and has its own interrupt to CPU. The UART controller can support 8 bits transfer without parity or 9 bits transfer with even or odd parity. One data buffer and one shift register is used for transmit engine, and another set of data buffer and shift register are used for receive engine. The setting in UART controller will be reset after wake-up from sleep or deep-sleep mode, programmer should restore the setting manually after wake-up from these two states. The baud rate range of UART is 300~819200bps.

18.2. Feature

--Programmable baud rate generator

--8 bits or 9 bits with odd/even parity transfer.

--Parity error detection.

--Transmit/Receive interrupt flag.

--Transmit/Receive overrun interrupt flag.

18.3. Block Diagram

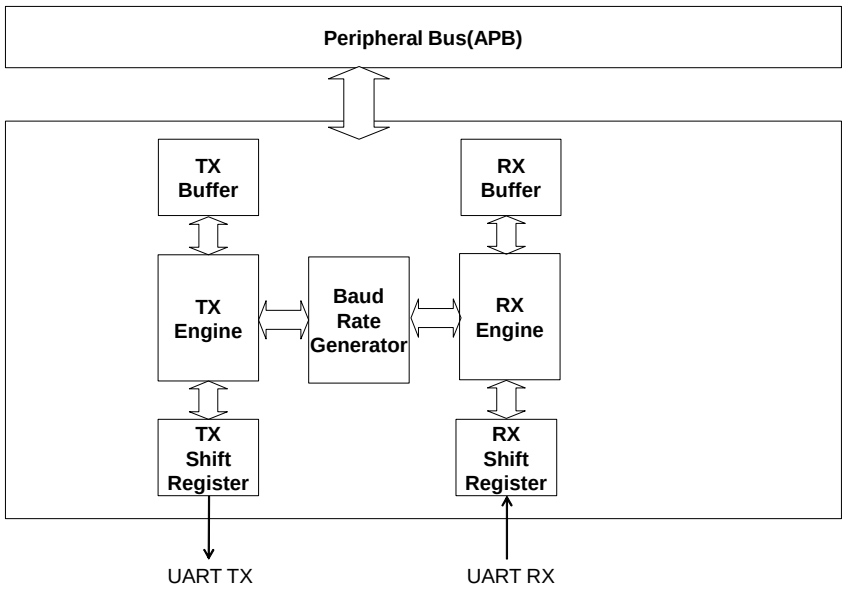


Figure 18-1 Functional Block Diagram of UART Controller

18.4. Register Location

Table 18-1 UART Registers Map

Register Name	Offset	Type	Reset Value	Description
UART_DATA	0x0000	rw	0x0000_0000	UART data register
UART_STATE	0x0004	rc_w1	0x0000_0000	UART status register
UART_CTRL	0x0008	rw	0x0000_0000	UART control register
UART_INTSTS	0x000C	rc_w1	0x0000_0000	UART interrupt status register
UART_BAUDDIV	0x0010	rw	0x0000_0000	UART baud rate divide register
UART_CTRL2	0x0014	rw	0x0000_0000	UART control register 2

Table 18-2 Register Location of MISC Controller for UART(MISC Base: 0x40013000)

Name	Type	Address	Description	Default
MISC_IREN	R/W	0x000C	IR enable control register	0x00
MISC_DUTYL	R/W	0x0010	IR Duty low pulse control register	0x0000
MISC_DUTYH	R/W	0x0014	IR Duty high pulse control register	0x0000

18.5. Register Definition

18.5.1. UART_DATA Register

Table 18-3 UART_DATA Register Description

Bit	Name	Type	Description
31:8	Rsvd	-	Reserved.
7:0	DATA	rw	Read: Receive data Write: Transmit data

18.5.2. UART_STATE Register

Table 18-4 UART_STATE Register Description

Bit	Name	Type	Description
31:7	Rsvd	-	Reserved.
6	RXPSTS	r	Receive parity data flag. This flag show the parity bit of last receive data.
5	TXDONE	rc_w1	Transmit done flag. This flag will be set when a single byte data is transmitted. The bit will be cleared when programmer write 1 to this bit or write 1 to TXDONEIF bit in UARTx_INTSTS register.
4	RXPE	rc_w1	Receive parity error flag. This flag will be set when receive data's parity does not meet expectation. The bit will be cleared when programmer write 1 to this bit or write 1 to RXPEIF bit in UARTx_INTSTS register.

3	RXOV	rc_w1	Receive buffer overrun flag. This flag will be set when RXFULL is 1 and another new data is received from RX engine. The bit will be cleared when programmer write 1 to this bit or write 1 to RXOVIF bit in UARTx_INTSTS register.
2	TXOV	rc_w1	Transmit buffer overrun flag. This flag will be set when TXFULL is 1 and another new data is written into UARTx_DATA register. The bit will be cleared when programmer write 1 to this bit or write 1 to TXOVIF bit in UARTx_INTSTS register.
1	RXFULL	r	Receive buffer full register. 0: Receive buffer is empty. 1: Receive buffer is full. This flag will be set when a data is receive from the UART RX engine, and will be cleared to 0 when programmer read the data from UARTx_DATA register.
0	Rsvd	-	Reserved.

18.5.3. UART_CTRL Register

Table 18-5 UART_CTRL Register Description

Bit	Name	Type	Description
31:9	Rsvd	-	Reserved.
8	TXDONEIE	rw	Transmit done interrupt enable register.
7	RXPEIE	rw	Receive parity error interrupt enable register.
6	Rsvd	-	Reserved.
5	RXOVIE	rw	Receive overrun interrupt enable register.
4	TXOVIE	rw	Transmit overrun interrupt enable register.
3	RXIE	rw	Receive interrupt enable register.
2	Rsvd	-	Reserved.
1	RXEN	rw	Receive engine enable register.
0	TXEN	rw	Transmit engine enable register.

18.5.4. UART_INTSTS Register

Table 18-6 UART_INTSTS Register Description

Bit	Name	Type	Description
31:6	Rsvd	-	Reserved.
5	TXDONEIF	rc_w1	Transmit done flag. This flag will be set when a single byte is transmitted and TXDONEIE is 1. The bit will be cleared when programmer write 1 to this bit or write 1 to TXDONE bit in UARTx_STATE register.
4	RXPEIF	rc_w1	Receive parity error flag. This flag will be set when receive data's parity does not meet expectation and RXPEIEis1.The bit will be cleared when programmer write 1 to this bit or write 1 to RXPE bit in UARTx_STATE register.
3	RXOVIF	rc_w1	Receive buffer overrun flag. This flag will be set when

			RXOVIE is 1 and RXFULL is 1 and another new data is received from RX engine. The bit will be cleared when programmer write 1 to this bit or write 1 to RXOV bit in UARTx_STATE register.
2	TXOVIF	rc_w1	Transmit buffer overrun flag. This flag will be set when TXOVIE is 1 and TXFULL is 1 and another new data is written into UARTx_DATA register. The bit will be cleared when programmer write 1 to this bit or write 1 to TXOV bit in UARTx_STATE register.
1	RXIF	rc_w1	Receive interrupt flag. This bit will be set when a data is received and put in UARTx_DATA register. This bit will be cleared when write 1 to this register.
0	Rsvd	-	Reserved.

18.5.5. UART_BAUDDIV Register

Table 18-7 UART_BAUDDIV Register Description

Bit	Name	Type	Description
31:20	Rsvd	-	Reserved.
19:0	BAUDDIV	rw	Baud rate divider register, this register must be set before enable UART engine. BAUDDIV = APBCLK/Baud-rate. For example, when APBCLK = 6.5536MHz and baud-rate is 9600, fill 6553600/9600 = 682 in this register.

18.5.6. UART_CTRL2 Register

Table 18-8 UART_CTRL2 Register Description

Bit	Name	Type	Description
31:4	Rsvd	-	Reserved.
3:2	PMODE	rw	Parity mode control register, this register is valid only when MODE is set to 1. 0: Even parity. 1: Odd parity. 2: Always 0 at parity bit. 3: Always 1 at parity bit.
1	MODE	rw	UART mode control register. 0: 1+8+1 mode. 1: 1+8+1+1 mode, the parity bit is controlled by PMODE register.
0	MSB	rw	LSB/MSB transmit order control register. 0: LSB transmit first. 1: MSB transmit first.

18.5.7. MISC_IREN Register

Table 18-9 Description of MISC_IREN Register

Bit	Name	Type	Description	Default
31:6	-	-	Reserved.	0
5:0	IREN	R/W	IR enable control register. Each bit in this register corresponded to 1 UART TX channel. When IREN[x] is set to 1, it means UART TX[x] will be modulated with IR pulse to output.	0x00

18.5.8. MISC_DUTYL Register

Table 18-10 Description of MISC_DUTYL Register

Bit	Name	Type	Description	Default
31:16			Reserved.	0
15:0	DUTYL	R/W	IR low pulse width control register. The low pulse width will be (DUTYL + 1)*APBCLK period.	0x0000

18.5.9. MISC_DUTYH Register

Table 18-11 Description of MISC_DUTYH Register

Bit	Name	Type	Description	Default
31:16	-	-	Reserved.	0
15:0	DUTYH	R/W	IR high pulse width control register. The high pulse width will be (DUTYH + 1)*APBCLK period.	0x0000

19. UART 32K Controller

19.1. Introduction

The UART 32K controller is used to receive data via UART protocol. There are two individual UART 32K controllers in V94XX(A), which can select input from UART rx0 ~ rx2. UART 32K controller is designed to operate at 32K crystal frequency, so it can work under sleep or deep sleep mode. The typical baud rate is 9600. The UART 32K controller can support 8 bits transfer without parity or 9 bits transfer with even or odd parity. One data buffer and one shift register is used for receive engine. The baud rate range of UART 32K is 300~9600bps.

19.2. Feature

--Operated under sleep or deep-sleep mode.

--Wake-up capability under sleep or deep-sleep mode.

--Programmable Baud rate generator

--8 bits or 9 bits with odd/even parity transfer.

--Parity error detection.

--Receive interrupt flag.

--Receive parity error flag.

--Receive overrun interrupt flag.

19.3. Block Diagram

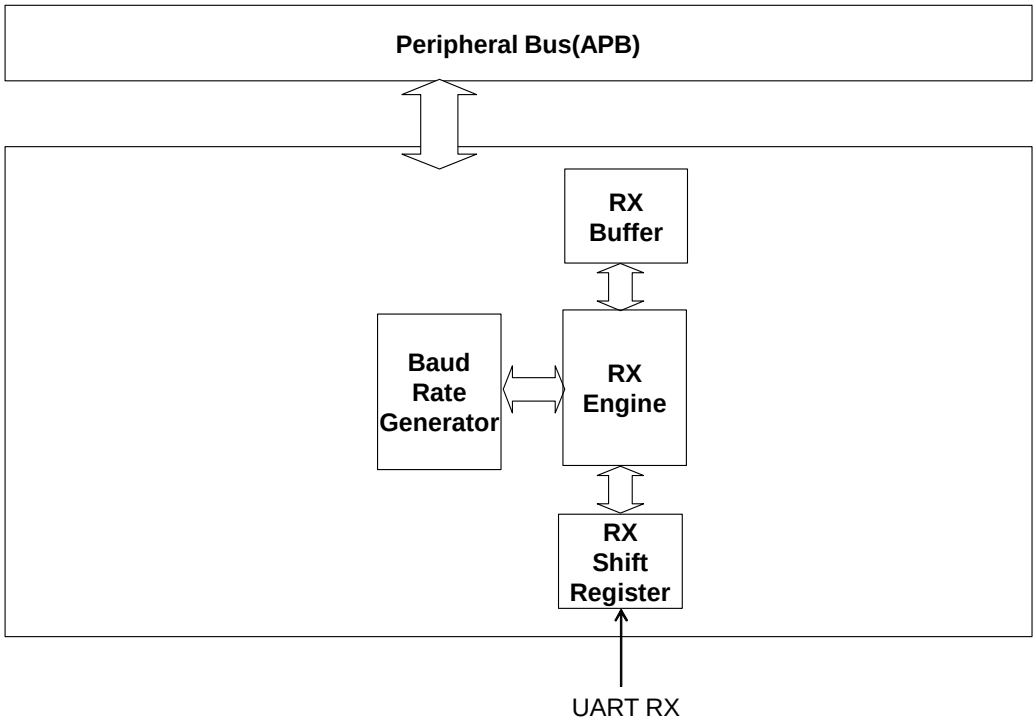


Figure 19-1 Functional Block Diagram of UART 32K Controller

19.4. Register Location

Table 19-1 U32K Registers Map

Register Name	Offset	Type	Reset Value	Description
U32K_CTRL0	0x0000	rw	0x0000_0000	UART 32K control register 0
U32K_CTRL1	0x0004	rw	0x0000_0000	UART 32K control register 1
U32K_PHASE	0x0008	rw	0x0000_4B00	UART 32K baud rate control register
U32K_DATA	0x000C	r	0x0000_0000	UART 32K receive data buffer
U32K_STS	0x0010	rc_w1	0x0000_0000	UART 32K interrupt status register

19.5. Register Definition

19.5.1. U32K_CTRL0 Register

Table 19-2 U32K_CTRL0 Register Description

Bit	Name	Type	Description
31:9	Rsvd	-	Reserved.
8	WKUMODE	rw	Wake-up mode control register. This register is valid when

			RXIE = 1. 0: Wake-up when a package is received no matter parity or stop bit is correct or not. 1: Wake-up only when parity bit and stop bit is correct.
7:6	DEBSEL	rw	De-bounce control register 0: No de-bounce. 1: 2 RTCCLK clocks de-bounce. 2: 3 RTCCLK clocks de-bounce. 3: 4 RTCCLK clocks de-bounce. This register is used when the UART bus is dirty, enable the de-bounce function can reduce the noise on the receive data. But a too large de-bounce cycles may result in loss of receive data.
5:4	PMODE	rw	Parity mode control register, this register is valid only when MODE is set to 1. 0: Even parity. 1: Odd parity. 2: Always 0 at parity bit. 3: Always 1 at parity bit.
3	MODE	rw	UART mode control register. 0: 1+8+1 mode. 1: 1+8+1+1 mode, the parity bit is controlled by PMODE register.
2	MSB	rw	UART receive order control register. 0: LSB receive first. 1: MSB receive first.
1	ACOFF	rw	Auto-calibration off control register. In order to correct receive UART data under RTCCLK clock, there is a hardware auto calibration mechanism inside the controller. By default, this mode is turned on, programmer can set 1 to this bit to turn off this function. 0: Enable auto-calibration. 1: Disable auto-calibration.
0	EN	rw	UART32K controller enable register. When this bit is set to 1, the UART32K controller will start to receive data after two 32768 Hz clock cycles. So use must set correct parameter and control register before set this register to 1. 0: Disable. 1: Enable.

19.5.2. U32K_CTRL1 Register

Table 19-3 U32K_CTRL1 Register Description

Bit	Name	Type	Description
31:6	Rsvd	-	Reserved.
5:4	RXSEL	rw	Receive data select register. 0: From UART RX0 (IOA12).

			1: From UART RX1 (IOA13). 2: From UART RX2 (IOA14). 3: Reserved
3	Rsvd	-	Reserved.
2	RXOVIE	rw	Receive overrun interrupt/wake-up enable register.
1	RXPEIE	rw	Receive parity error interrupt/wake-up enable register.
0	RXIE	rw	Receive interrupt/wake-up enable register. When enabled, when WKUMODE is 0, it will wake up as long as it receives serial data; when WKUMODE is 1, it will wake up only when parity and stop bits are correct.

19.5.3. U32K_PHASE Register

Table 19-4 U32K_PHASE Register Description

Bit	Name	Type	Description
31:16	Rsvd	-	Reserved.
15:0	PHASE	rw	Baud rate divider register, this register must be set before enable UART 32K engine. PHASE = 65536*Baud-rate/32768. For example, when baud-rate is 9600, fill 65536*9600/32768 = 19200 in this register. The maximum baud rate which UART 32K can support is 9600. When PSCA in RTC_PSCA register is not 0, the value in this register should be calculated by the divided RTCCLK frequency.

19.5.4. U32K_DATA Register

Table 19-5 U32K_DATA Register Description

Bit	Name	Type	Description
31:8	Rsvd	-	Reserved.
7:0	DATA	r	Read: Receive data.

19.5.5. U32K_STS Register

Table 19-6 U32K_STS Register Description

Bit	Name	Type	Description
31:3	Rsvd	-	Reserved.
2	RXOV	rc_w1	Receive buffer overrun flag. This flag will be set when receive FIFO is full and another new data is received from RX engine. The bit will be cleared when programmer write 1 to this bit.
1	RXPE	rc_w1	Receive parity error flag. This flag will be set when receive data's parity does not meet expectation. The bit will be cleared when programmer write 1 to this bit.
0	RXIF	rc_w1	Receive interrupt flag, this bit will be set when a data is

			received and put in U32K_DATA register. This bit will be cleared when write 1 to this register.

20. ISO7816 Controller

20.1. Introduction

The ISO7816 controller is an enhanced UART protocol which is able to do half-duplex communication on the 2 wires bus. One ISO7816 controller is in V94XX(A), ISO7816 controller can be program individually and has its own interrupt to CPU. A clock divider is also included inside the IP which is capable to generate a 1~5MHz clock for ISO7816 device. The setting in ISO7816 controller will be reset after wake-up from sleep or deep-sleep mode, programmer should restore the setting manually after wake-up from these two states.

20.2. Feature

--Programmable Baud rate generator

--Support automatically retry.

--Support half-duplex transmit/receive.

--Support clock divider.

20.3. Block Diagram

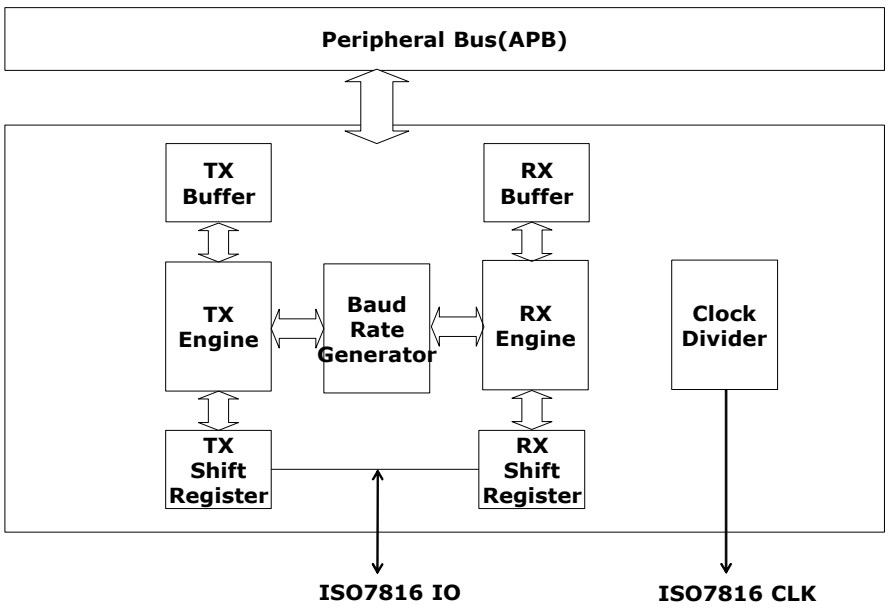


Figure 20-1 Functional Block Diagram of ISO7816 Controller

20.4. Register Location

Table 20-1 ISO7816 Registers Map

Register Name	Offset	Type	Reset Value	Description
ISO7816_BAUDDIVL	0x0004	rw	0x0000_0000	ISO7816 baud-rate low byte register
ISO7816_BAUDDIVH	0x0008	rw	0x0000_0000	ISO7816 baud-rate high byte register
ISO7816_DATA	0x000C	rw	0x0000_0000	ISO7816 data register
ISO7816_INFO	0x0010	rc_w1	0x0000_0000	ISO7816 information register
ISO7816_CFG	0x0014	rw	0x0000_0000	ISO7816 control register
ISO7816_CLK	0x0018	rw	0x0000_0000	ISO7816 clock divider control register

20.5. Register Definition

20.5.1. ISO7816_BAUDDIVL Register

Table 20-2 ISO7816_BAUDDIVL Register Description

Bit	Name	Type	Description
31:8	Rsvd	-	Reserved.
7:0	BAUDDIVL	rw	Low byte of baud-rate divider.

20.5.2. ISO7816_BAUDDIVH Register

Table 20-3 ISO7816_BAUDDIVH Register Description

Bit	Name	Type	Description
31:8	Rsvd	-	Reserved.
7:0	BAUDDIVH	rw	High byte of baud-rate divider. The baud-rate counter is count from BAUDDIV to 0xFFFF, so the setting should be. BAUDDIV = 0x10000 – (APBCLK/Baud-rate). For example, when APBCLK is 6.5536MHz and baud-rate is 9600, then 0x10000-(6553600/9600) = 0xFD56 should be written into this register.

20.5.3. ISO7816_DATA Register

Table 20-4 ISO7816_DATA Register Description

Bit	Name	Type	Description
31:8	Rsvd	-	Reserved.
7:0	DATA	rw	Read: Receive data, when receive data is not read by programmer and another data has been received, the OVIF flag will be set. Write: Transmit data, a write to this port will trigger a transmit event on the ISO7816 bus.

20.5.4. ISO7816_INFO Register

Table 20-5 ISO7816_INFO Register Description

Bit	Name	Type	Description
31:8	Rsvd	-	Reserved.
7	OVIF	rc_w1	Receive overflow flag. This bit will be set when a data is received by not been read by CPU but another receive data is coming in. This bit can be cleared by write 1 to this flag.
6	SDIF	rc_w1	Transmit interrupt flag. This bit will set when a byte has been transmitted and ACK has been received. This bit will be set no matter the received ACK is 0 or 1. This bit can be cleared by write 1 to this flag.
5	RCIF	rc_w1	Receive interrupt flag. This bit will set when a byte has been received and ACK has been transmitted. This bit can be cleared by write 1 to this flag.
4	LSB	rw	MSB/LSB transmit/receive order control register. 0: Transmit MSB first. 1: Transmit LSB first.
3	SDERR	rc_w1	When the received ACK is 0 during transmit mode, this bit will be set to 1. This bit can be clear by write 1 to this bit.
2	RCERR	rc_w1	When received data have check sum error, this bit will be set to 1. This bit can be clear by write 1 to this bit.
1	CHKSUM	rw	The transmitted or received data's check sum bit. This bit can be read/write by CPU, by the original message will be lost.
0	RCACK	rw	The received ACK at the end of transmit. This bit can be read/write by CPU, by the original message will be lost.

20.5.5. ISO7816_CFG Register

Table 20-6 ISO7816_CFG Register Description

Bit	Name	Type	Description
31:8	Rsvd	-	Reserved.
7	OVIE	rw	Receive overrun interrupt enable register.
6	SDIE	rw	Transmit interrupt enable register.
5	RCIE	rw	Receive interrupt enable register.
4	ACKLEN	rw	ACK low period when receive an error data. 0: 1 bit 1: 2 bits.
3	AUTOSD	rw	Automatic re-transmit when receive ACK is 0. 0: Disable automatic re-transmit mode. 1: Enable automatic re-transmit mode.
2	AUTORC	rw	Automatic response ACK as 0 when receive an error data to let transmitter re-send the data. 0: Disable automatic re-receive mode.

			1: Enable automatic re-receive mode.
1	CHKP	rw	Parity mode control register. 0: Even parity 1: Odd parity.
0	EN	rw	ISO7816 enable register. 0: Disable ISO7816 function. 1: Enable ISO7816 function.

20.5.6. ISO7816_CLK Register

Table 20-7 ISO7816_CLK Register Description

Bit	Name	Type	Description
31:8	Rsvd	-	Reserved.
7	CLKEN	rw	ISO7816 clock output enable. 0: Disable clock output. 1: Enable clock output.
6:0	CLKDIV	rw	The ISO7816 clock divider ratio. 0: APBCLK/1 1: APBCLK /2 2: APBCLK /3 … 127: APBCLK /128

In ISO7816's protocol, the re-transmit should be less or equal to 3 times, this part should be take care by software to disable the auto transmit or receive function after two times of failure retry.

The following table shows the ISO7816's package format.

Table 20-8 Package format of ISO7816

bit	0	1~8	9	10	11	12	0	…
Transmit Direction	Transmitter→Receiver			Receiver→Transmitter		--	Transmitter→Receiver	
Definition	Start bit	Data	Parity bit	ACK*		Wait	Start bit	…
Value	0	MSB→LSB	P	ACK*		1	0	…
TX	0	MSB→LSB	P	1			0	…
RX	1	1	1	ACK*		1	1	…
Description	10 bits data			3 bits guarding time			Next Frame	

*If ACK is 0, then the RX will be reset from 1 to 0 at the middle of 10^{th} bit, and set to 1 at 11^{th} or 12^{th} bit, which is controlled by ACKLEN in ISO7816_CFG.

The transmit package contains totally 10 bits including a start bit and 8 bits data and 1 parity bit. And then in a 3 bits guarding time, the receiver will check the parity correctness response 1 or 2 bits ACK to transmitter. At bit 12, both transmitter and receiver should be kept at high state before next package is ready to be transmitted.

21. Timer/PWM Controller

21.1. Introduction

There are in total 8 timers in V94XX(A). Four of them are general purpose 32 bits timer. Another 4 timers are 16 bits timers with PWM function. Each timer can generate interrupt to CM0. Each PWM can output 3 outputs with different output waveform. The setting in timer/PWM controller will be reset after wake-up from sleep or deep-sleep mode, programmer should restore the setting manually after wake-up from these two states.

21.2. Feature

--4 32 bits general purpose count timer

--4 16 bits PWM timer.

--Each PWM timer can have at most 3 outputs.

--8 output modes.

21.3. Block Diagram

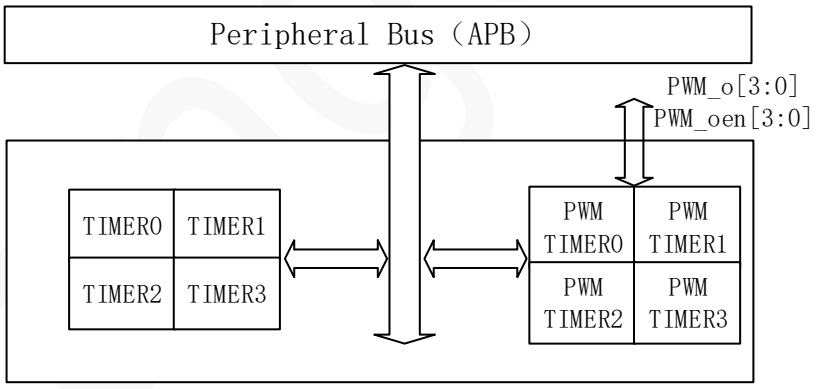


Figure 21-1 Functional Block Diagram of TIMER Controller

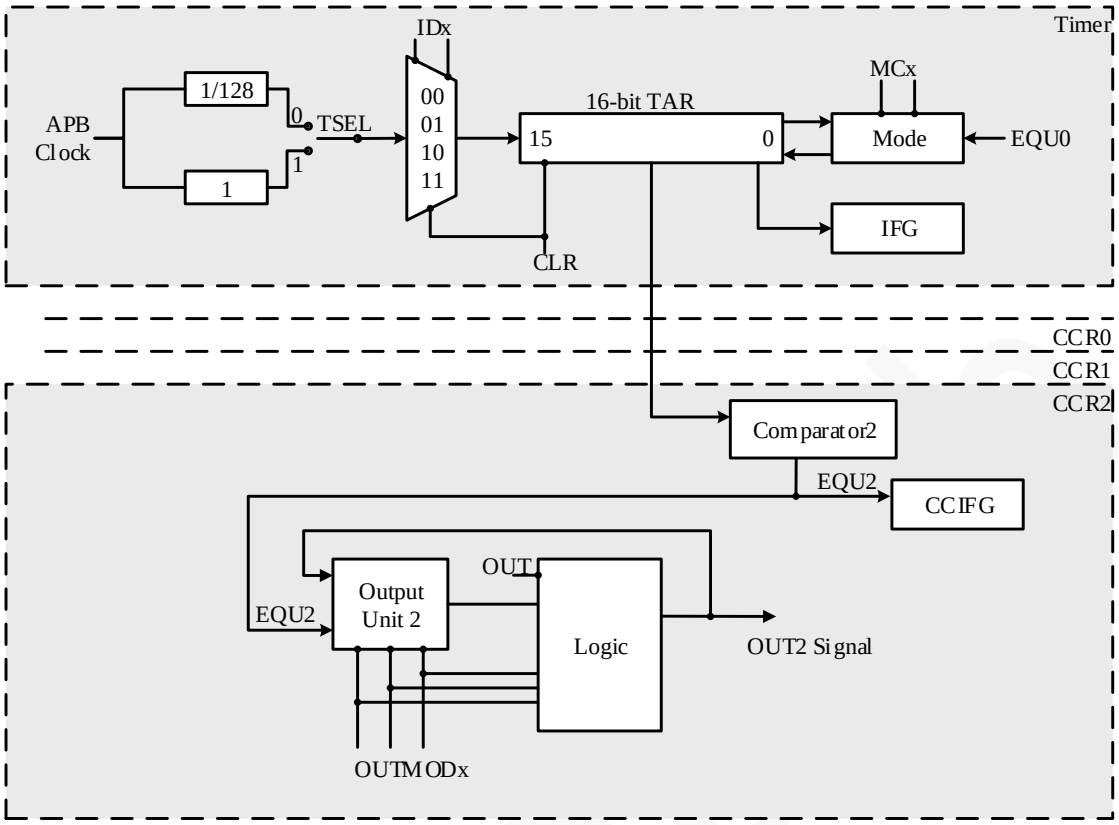


Figure 21-2 Functional Block Diagram of PWM TIMER Controller

21.4. 32-bit Timer Register Location

Table 21-1 TMR Registers Map

Register Name	Offset	Type	Reset Value	Description
TMR_CTRL	0x0000	rw	0x0000_0000	Timer control register
TMR_VALUE	0x0004	rw	0x0000_0000	Timer current count register
TMR_RELOAD	0x0008	rw	0x0000_0000	Timer reload register
TMR_INT	0x000C	rc_w1	0x0000_0000	Timer interrupt status register

21.5. 32-bit Timer Register Definition

21.5.1. TMR_CTRL Register

Table 21-2 TMR_CTRL Register Description

Bit	Name	Type	Description
31:4	Rsvd	-	Reserved.
3	INTEN	rw	Timer x interrupt enable register.
2	EXTCLK	rw	Select ext_clk (IOB15) as clock source. The ext_clk's rising

			edge will be used as internal down counter's enable signal. Every time when the ext_clk is rising, the internal counter will decrease by 1. Under this mode, the frequency of ext_clk should be lower than PLCK/6.
1	EXTEN	rw	When the ext_clk (IOB15) is logic 1, the internal down counter will be decreased by 1 with the speed of PCLK. A two clocks sync logic will be applied on the ext_clk to avoid the glitch on the ext_clk. When both the EXTCLK and EXTEN bits are enabled, the EXTCLK bit has higher priority.
0	EN	rw	Timer x enable control register.

21.5.2. TMR_VALUE Register

Table 21-3 TMR_VALUE Register Description

Bit	Name	Type	Description
31:0	VALUE	rw	Timer x current value register.

21.5.3. TMR_RELOAD Register

Table 21-4 TMR_RELOAD Register Description

Bit	Name	Type	Description
31:0	RELOAD	rw	Timer x reload value register. A write to this register sets the current value. Every time when the timer down count to 0, the value in this register will be reloaded into the counter and start to down count again. At the same time, the INT bit will be set to 1. The RELOAD of the timer can be calculated by the following equation. RELOAD = Period * APBCLK - 1.

21.5.4. TMR_INT Register

Table 21-5 TMR_INT Register Description

Bit	Name	Type	Description
31:1	Rsvd	-	Reserved.
0	INT	rc_w1	Timer x interrupt status register, write 1 to clear this bit. When the internal down counter timer reach 0, this bit will be set to 1.

21.6. 16-bit PWM Register Location

Table 21-6 PWM Registers Map

Register Name	Offset	Type	Reset Value	Description
PWM_CTL	0x0000	rw	0x0000_0000	PWM Timer control register

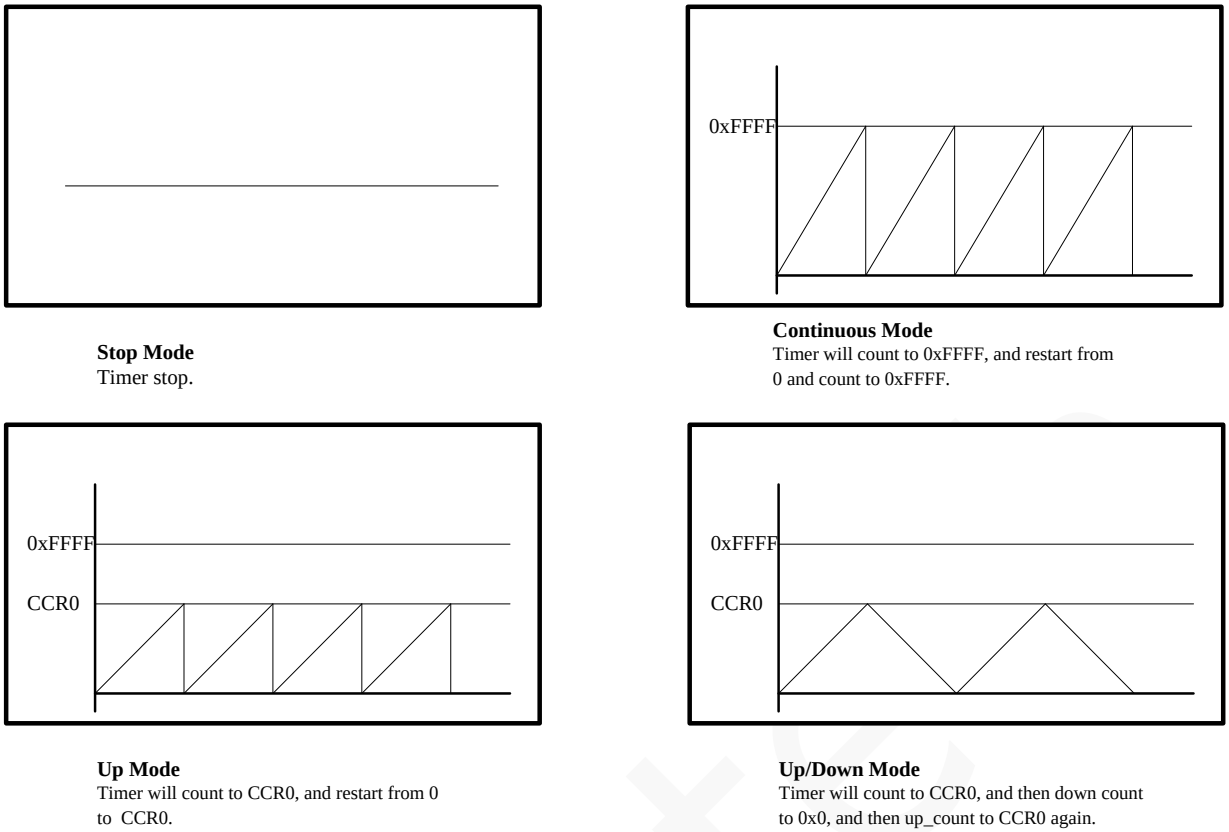
PWM_TAR	0x0004	r	0x0000_0000	PWM Timer current count register
PWM_CCTLx[0..2,0x4]	0x0008	rw	0x0000_0000	PWM Timer compare control register x
PWM_CCRx[0..2,0x4]	0x0014	rw	0x0000_0000	PWM Timer compare data register x

21.7. 16-bit PWM Register Definition

21.7.1. PWM_CTL Register

Table 21-7 PWM_CTL Register Description

Bit	Name	Type	Description
31:8	Rsvd	-	Reserved.
7:6	ID	rw	PWM timer Input clock divider control. 0: Input clock divide by 2 1: Input clock divide by 4 2: Input clock divide by 8 3: Input clock divide by 16
5:4	MC	rw	PWM Timer mode control 0: Timer stop. 1: Up-count mode: timer will count to CCR0 and restart from 0. 2: Continuous mode: timer will count to 0xFFFF and start from 0. 3: Up/Down mode: timer will count to CCR0 and then decrease to 0. Refer to figure 2 for each mode.
3	TSEL	rw	Clock source selection 0: APB Clock/128. 1: APB Clock.
2	CLR	rw	TAR clear register, when this bit is set to 1, the TAR will be clear to 0. This bit will be cleared to 0 automatically after TAR is cleared.
1	IE	rw	PWM Timer interrupt enable register.
0	IFG	rc_w1	PWM Timer interrupt status flag, write 1 to clear this flag to 0. Up mode: Set when counter change from CCR0 to 0. Continuous mode: Set when counter change from 0xFFFF to 0. Up-Down mode: Set when counter change from 0x0001 to 0.



Stop Mode
Timer stop.

Continuous Mode
Timer will count to 0xFFFF, and restart from 0 and count to 0xFFFF.

Up Mode
Timer will count to CCR0, and restart from 0 to CCR0.

Up/Down Mode
Timer will count to CCR0, and then down count to 0x0, and then up_count to CCR0 again.

Figure 21-3 Mode description of PWM TIMER Controller

When MC is set to a non-zero value, the timer will start to work. Under up mode or up/down mode, if PWMx_CCR0 is set to 0, then timer x will stop counting. The timer will start to count again if a non-zero value is written to PWMx_CCR0.

Under up-mode, if the CCR0 is changed during the operation time and new CCR value is larger than current count value, then the timer will count to the new CCR0 then return to 0. And if the new CCR0 is smaller than current count value, the timer will count one tick and reset to 0 to start again.

Under up-down mode and the timer is under up-count process, if the CCR0 is changed during the operation time and new CCR value is larger than current count value, then the timer will count to the new CCR0 then down count to 0. And if the new CCR0 is smaller than current count value, the timer will count one tick and start to down count to 0. Under up-down mode and the timer is under down-count process, if the CCR0 is changed during the operation time, then the timer will continuously complete the down count process.

Under continuous mode, user can set the output frequency depends on the dynamic setting of CCR0~CCR2. The following diagram shows an example of this application.

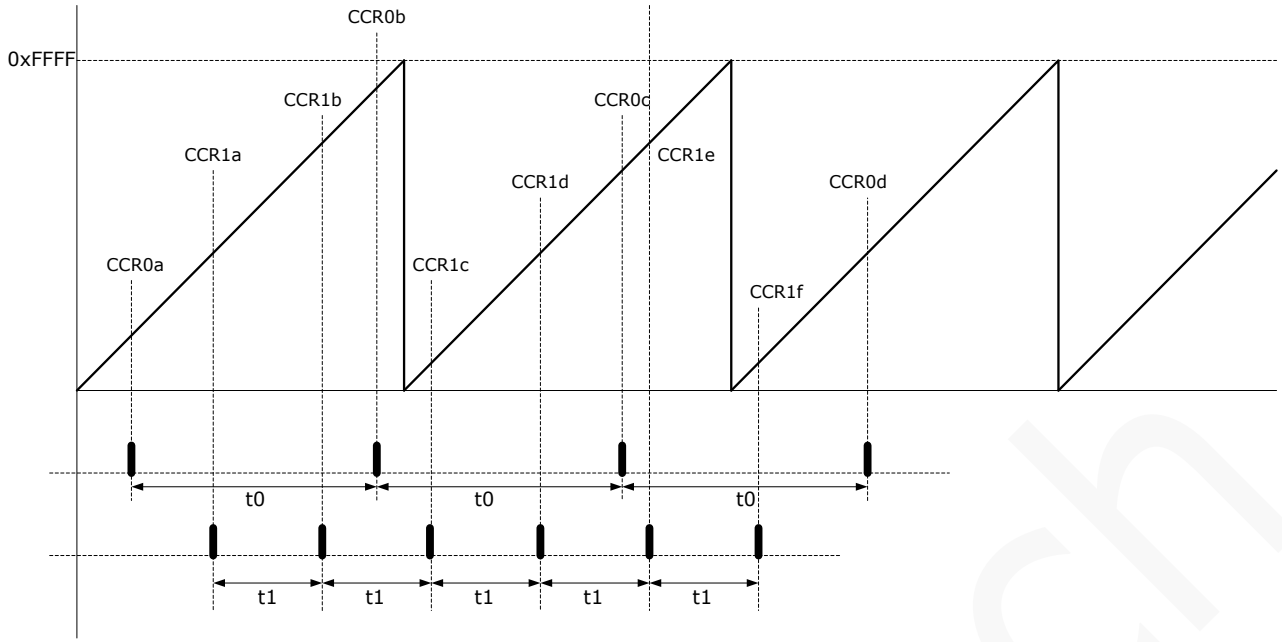


Figure 21-4 Example of Continuous Mode

In the above diagram, CCR0a or CCR1a is the CCR0 or CCR1 at Ta0 or Ta1, CCR0b or CCR1b is the CCR0 or CCR1 at Tb0 or Tb1. (Tb0=Ta0+t0, Tb1=Ta1+t1)

The above diagram shows that under continuous mode, user can use CCIFG (bit 0 of CCTLx) and CCIE (bit 4 of CCTLx) to generate a regulator interrupt by setting CCR0a and CCR1a to assert interrupt when TAR=CCR0a or TAR=CCR1a. And when TAR=CCR0b or TAR=CCR1b, it can generate another interrupt with different period. The t0 and t1 can be totally independent, so at most user can set 3 totally independent interrupt with one single PWM timer. Under this mode, the IFG flag will be set when the timer count from 0xFFFF to 0x0.

21.7.2. PWM_TAR Register

Table 21-8 PWM_TAR Register Description

Bit	Name	Type	Description
31:0	TAR	r	PWM Timer0 real time counting register

21.7.3. PWM_CCTLx Register

Table 21-9 PWM_CCTLx Register Description

Bit	Name	Type	Description
31:10	Rsvd	-	Reserved.
9	OUTEN	rw	OUTx output enable control register. 0: OUTx output disable 1: OUTx output enable
8	Rsvd	-	Reserved.
7:5	OUTMOD	rw	Output mode selection. 0: Constant mode, OUTx output the value of OUT bit. 1: Set mode, OUTx will be set to 1 when TAR=CCRx

			(x=0~2). 2: Toggle/Reset mode, OUTx will be toggled when TAR=CCRx (x=1~2), and will be reset to 0 when TAR=CCR0. This mode can't be used on OUT0. 3: Set/Reset mode, OUTx will be set to 1 when TAR=CCRx (x=1~2), and will be reset to 0 when TAR=CCR0. This mode can't be used on OUT0. 4: Toggle mode, OUTx will be toggled when TAR=CCRx (x=0~2). 5: Reset mode, OUTx will be reset to 0 when TAR=CCRx (x=0~2). 6: Toggle/set mode, OUTx will be toggled when TAR=CCRx (x=1~2), and will be set to 1 when TAR=CCR0. This mode can't be used on OUT0. 7: Reset/set mode, OUTx will be reset to 0 when TAR=CCRx (x=1~2), and will be set to 1 when TAR=CCR0. This mode can't be used on OUT0.
4	CCIE	rw	Compare interrupt enable register.
3	Rsvd	-	Reserved.
2	OUT	rw	This bit is used to control the output value of OUTx when OUTMOD is set to 0.
1	Rsvd	-	Reserved.
0	CCIFG	rc_w1	Under compare mode, this bit will be set when TAR=CCRx. This bit can be cleared only when write 1 to this bit.

The following figure shows the PWM output under up-mode.

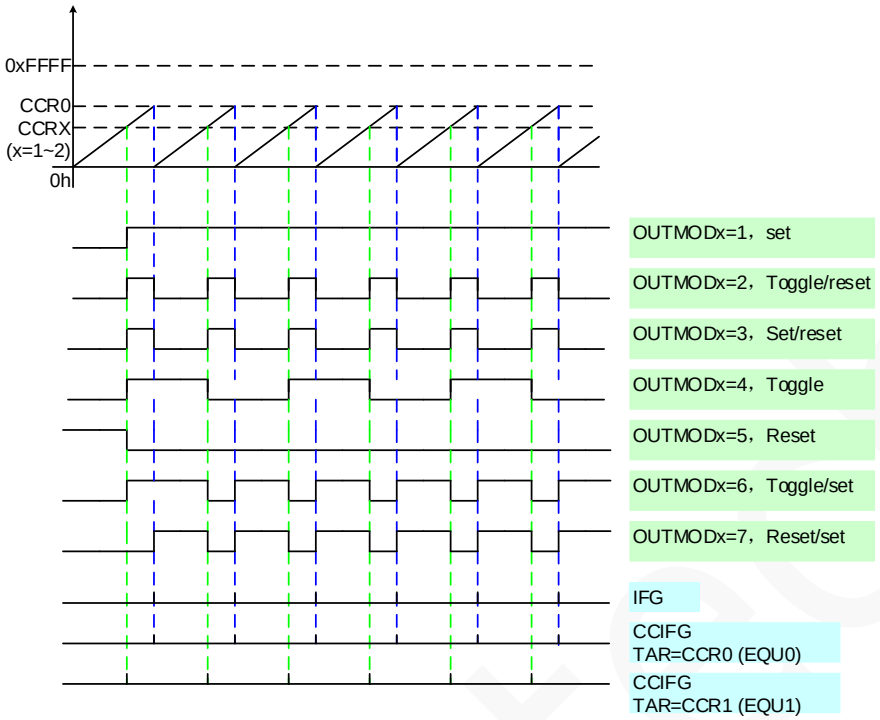


Figure 21-5 PWM Output under Up-count Mode

The following figure shows the PWM output under continuous-mode.

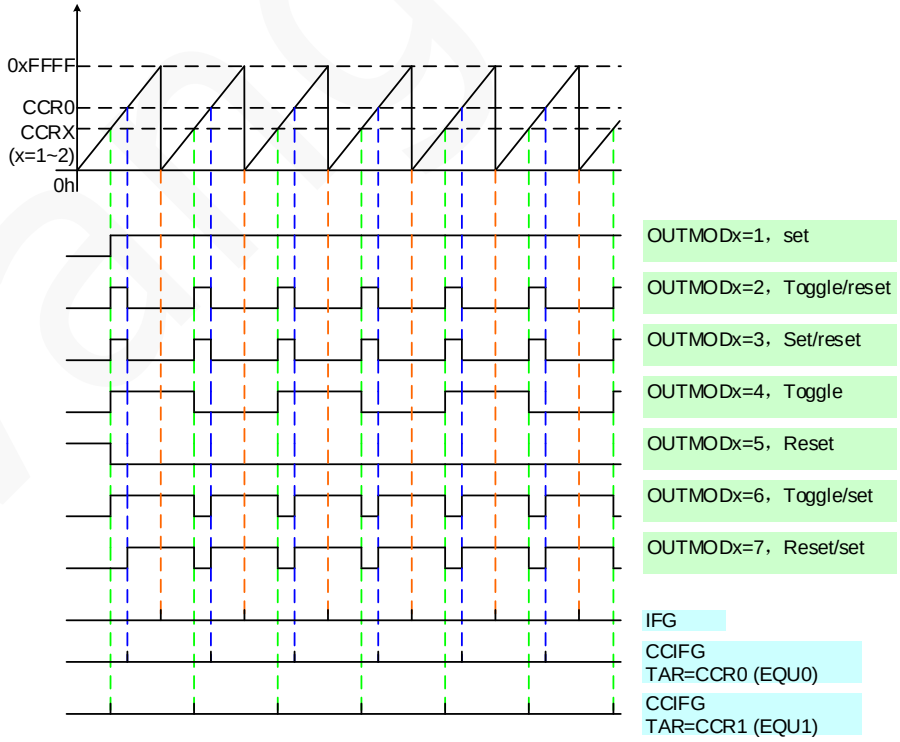


Figure 21-6 PWM Output under Continuous Mode

The following figure shows the PWM output under up/down count mode.

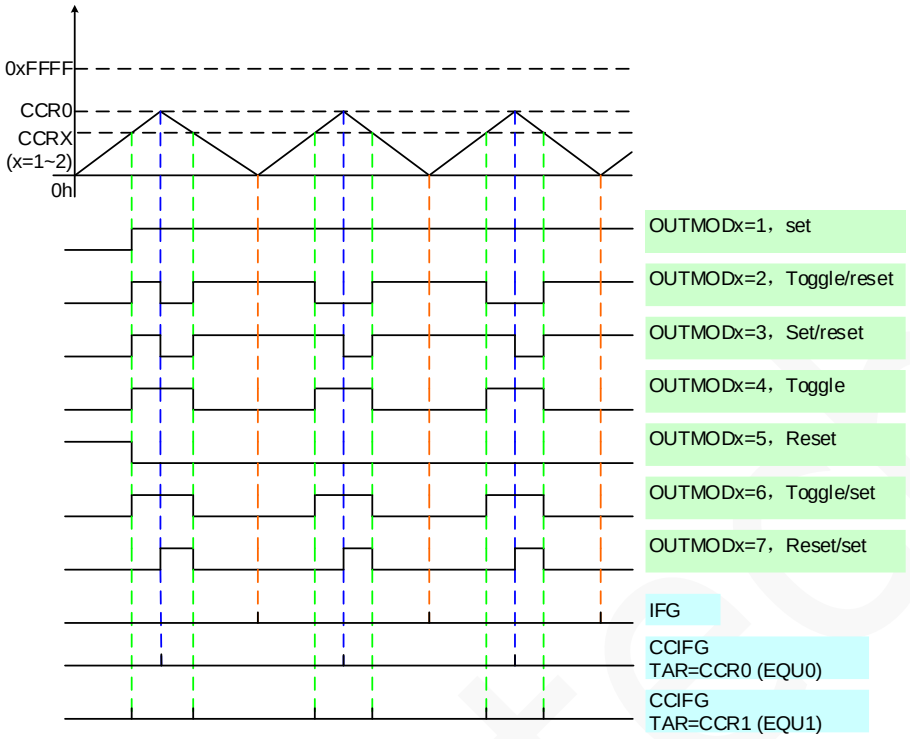


Figure 21-7 PWM Output under Up/down Count Mode

21.7.4. PWM_CCRx Register

Table 21-10 PWM_CCRx Register Description

Bit	Name	Type	Description
31:16	Rsvd	-	Reserved.
15:0	CCRx	rw	Compare data register. This register is used to compare with TAR to generate PWM output.

21.8. PWMMUX Register Location

Table 21-11 PWMMUX Registers Map

Register Name	Offset	Type	Reset Value	Description
PWMMUX_OSEL	0x0000	rw	0x0000_DB51	PWM output selection register

21.9. PWMMUX Register Definition

21.9.1. PWMMUX_OSEL Register

Table 21-12 PWMMUX_OSEL Register Description

Bit	Name	Type	Description
31:16	Rsvd	-	Reserved.
15:12	O_SEL3	rw	External output PWM3 output selection register. Same definition as O_SEL0
11:8	O_SEL2	rw	External output PWM2 output selection register. Same definition as O_SEL0
7:4	O_SEL1	rw	External output PWM1 output selection register. Same definition as O_SEL0
3:0	O_SEL0	rw	External output PWM0 output selection register. 0: From PWM0's OUT0 1: From PWM0's OUT1 2: From PWM0's OUT2 4: From PWM1's OUT0 5: From PWM1's OUT1 6: From PWM1's OUT2 8: From PWM2's OUT0 9: From PWM2's OUT1 10: From PWM2's OUT2 12: From PWM3's OUT0 13: From PWM3's OUT1 14: From PWM3's OUT2 Others: Reserved.

22. LCD Controller

22.1. Introduction

The LCD controller is used to display content on the LCD panel. The LCD controller supports 4 COMs or 6 COMs and 8 COMs mode, and maximum 65 segments. There are two frame buffers inside the LCD controller, which support automatically switch function. The setting in GPIO controller will be reset after wake-up from deep-sleep mode, programmer should restore the setting manually after wake-up from deep-sleep mode.

22.2. Feature

--Support 4, 6 or 8 COMs mode.

--Support maximum 4 COMs×65 SEGs, 6 COMs×63 SEGs or 8 COMs×61 SEGs.

--Support 1/3 Bias or 1/4 Bias modes

--Bias voltage generated by an individual 3.3V LDO, and can be adjusted from 3.6V-2.7V with resolution of 60mV/LSB

--An internal resistor ladder to generate the LCD waveform voltages--LCD scan frequency generated by the RTCCLK clock

--Two frame buffers which support automatically switch function.

--Adjustable frame rate.

22.3. Block Diagram

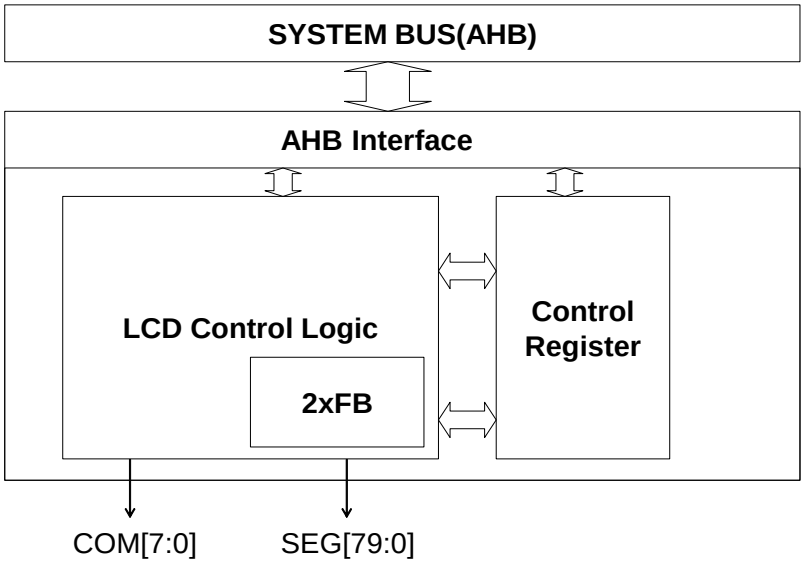


Figure 22-1 Functional Block Diagram of LCD Controller

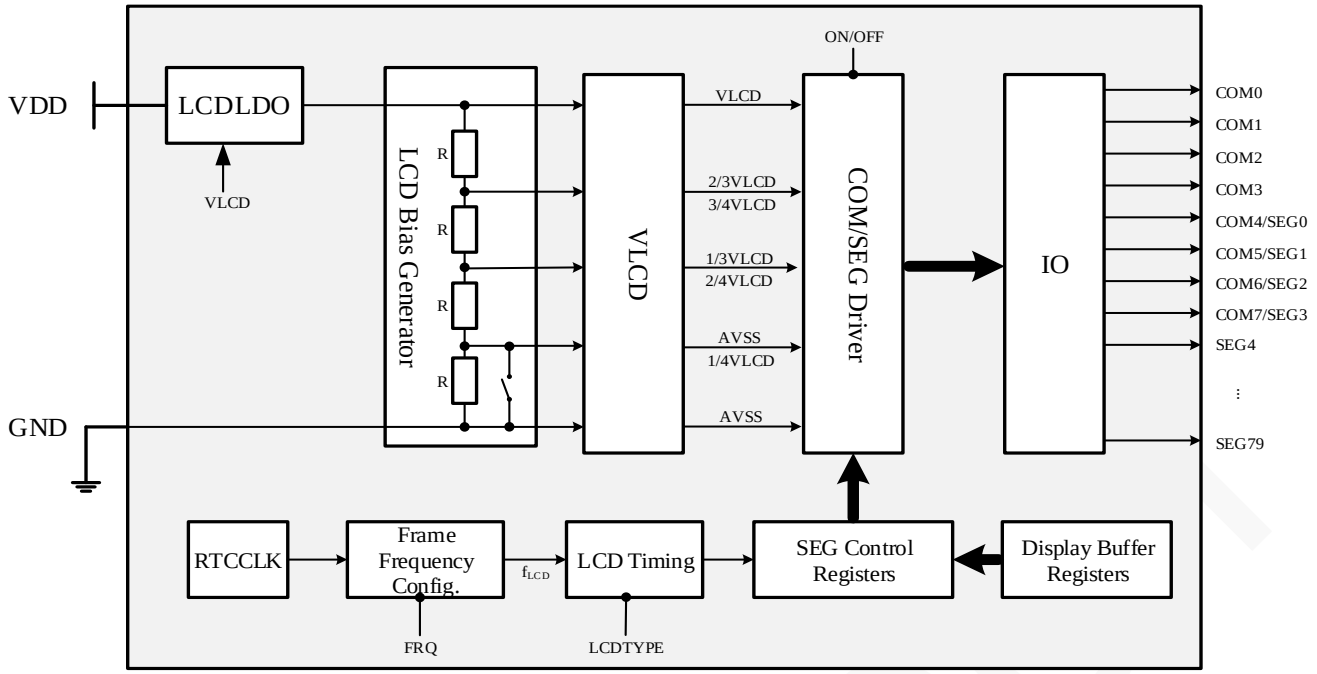


Figure 22-2 LCD Controller Structure Diagram

22.4. LCD Timing

In the V94XX(A), the CLK, sourced by the 32.768 kHz RTCCLK clock, provides the LCD driver with clock pulse for timing generation. Generally, the crystal oscillator keeps on running until it is powered off, so the LCD driver keeps on working even in Sleep (not Deep Sleep) state unless CLK is disabled. When the crystal stops running anomaly when power is still on, the internal RC clock will become the replacement of the XTAL clock to source the LCD driver until the crystal is stimulated to run again.

The CLK frequency is divided to generate frame frequency for the waveform. The MCU can configure bit[1:0] of LCD_CTRL to select the appropriate frame frequency. By default it is 64Hz.

22.5. LCD Waveform Voltage

In the V94XX(A), the bias voltage of LCD driver is generated by an individual 3.3V LDO, and an internal resistor ladder is designed to generate LCD waveform voltage (VLCD). Users can adjust the waveform voltage via bits VLCD[3:0](bit[4:1] of ANA_REG6).

22.6. LCD Operating Current

Users can adjust the resistance value of each resistor in the resistor ladder of the bias voltage generation circuits via bits DRV[1:0] (bit[3:2] of LCD_CTRL) to adjust the current through the circuits to change the lightness of the display panel. By default, the resistance value is 300 kΩ.

22.7. LCD Drive Waveform

There are 4 resistors in series in the bias voltage generation circuit, which can be configured to work in 1/3 bias mode or 1/4 bias mode. Users can configure bit LCD_BMOD (bit0 of ANA_REG6) to disable or enable one resistor in the bias voltage generation circuit to enable the LCD driver to work in 1/3 bias mode or 1/4 bias mode.

When an LCD panel of 1/4 duty 1/3 bias is applied, the LCD drive waveform is depicted in the following figure.

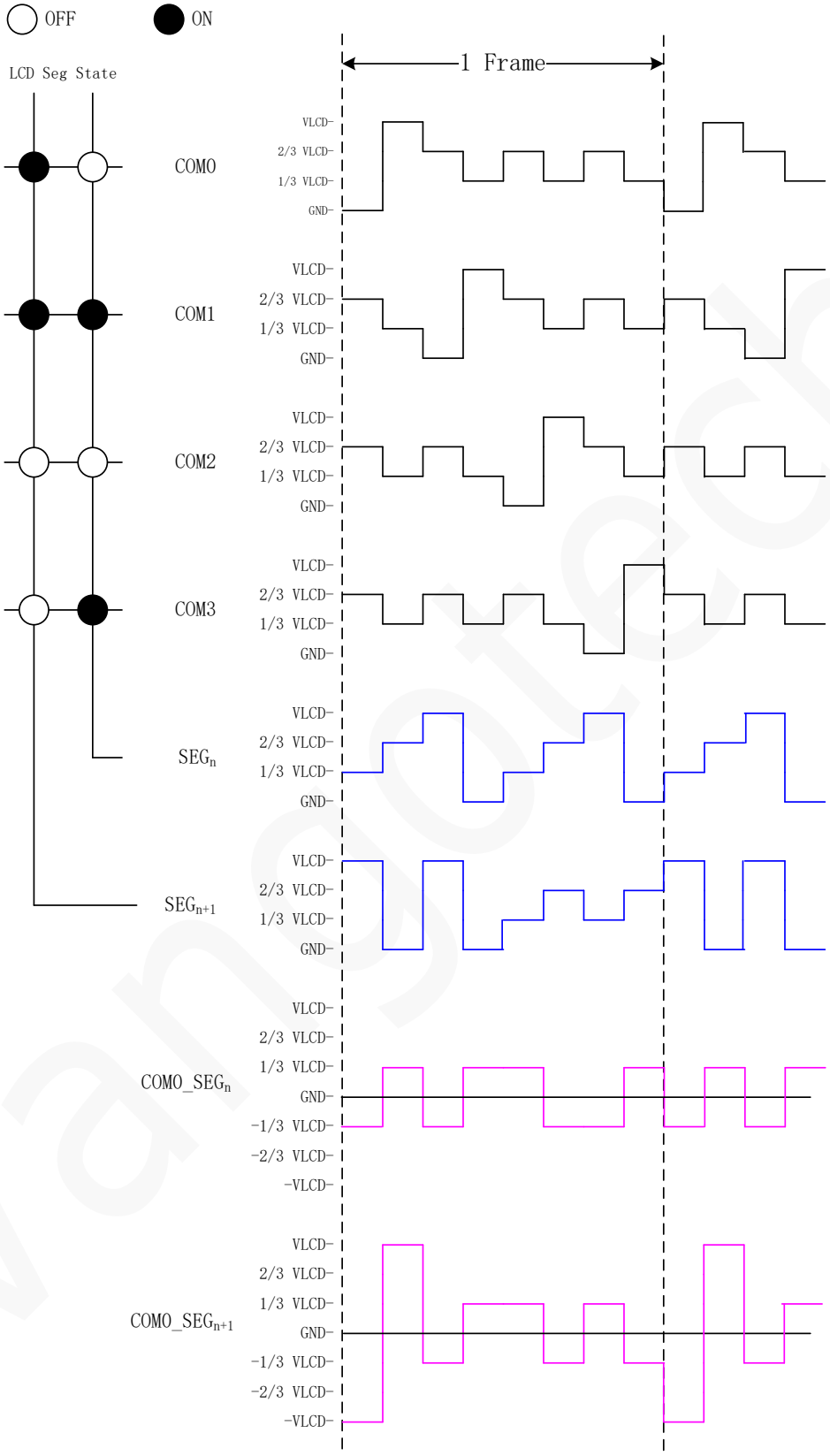


Figure 22-3 LCD Drive Waveform of 1/4 Duty and 1/3 Bias

When LCD panel of 1/6 duty and 1/3 bias is applied, the LCD drive waveform is depicted in the following figure.

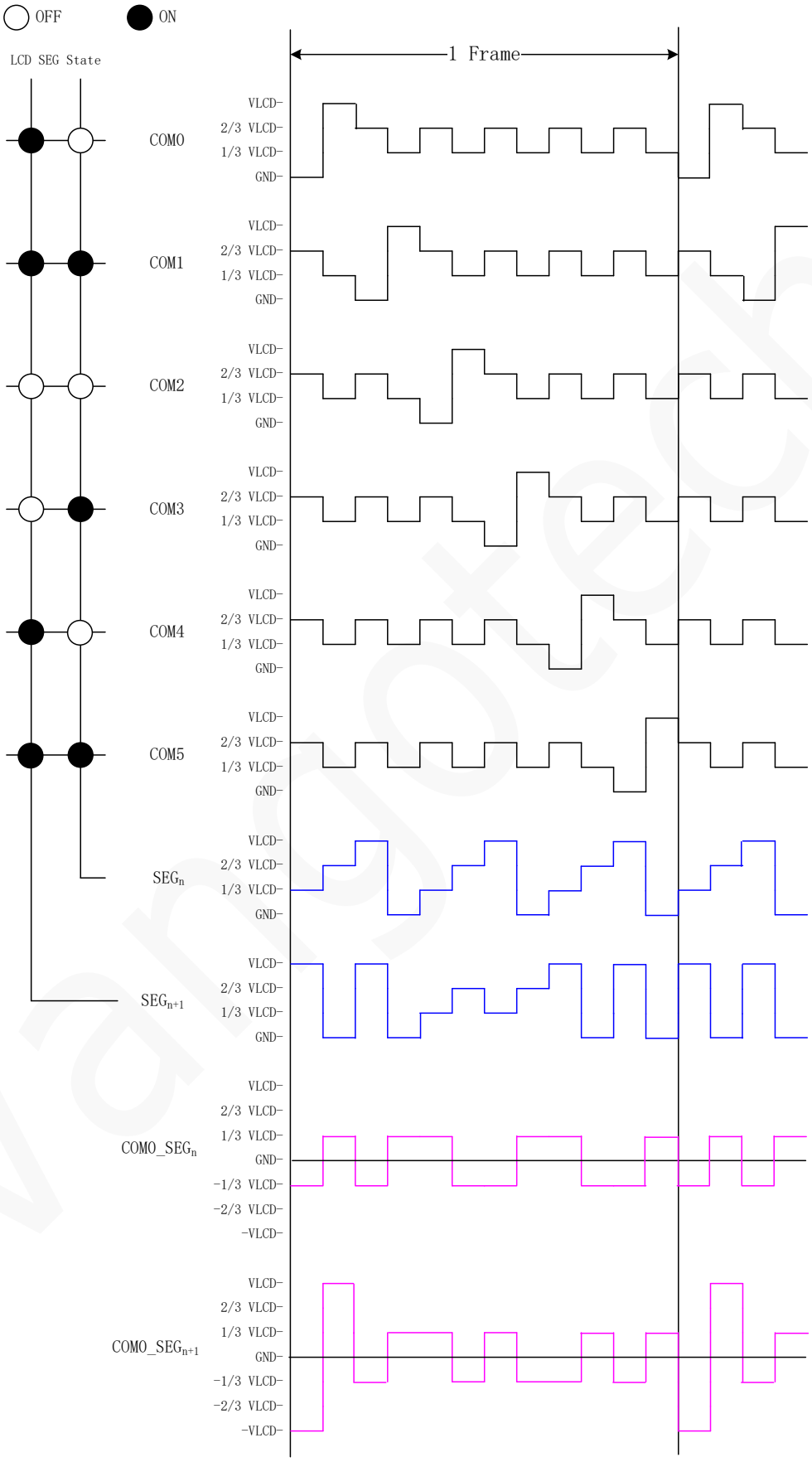


Figure 22-4 LCD Drive Waveform of 1/6 Duty and 1/3 Bias

When an LCD panel of 1/8 duty and 1/3 bias is applied, the LCD drive waveform is depicted in the following figures.

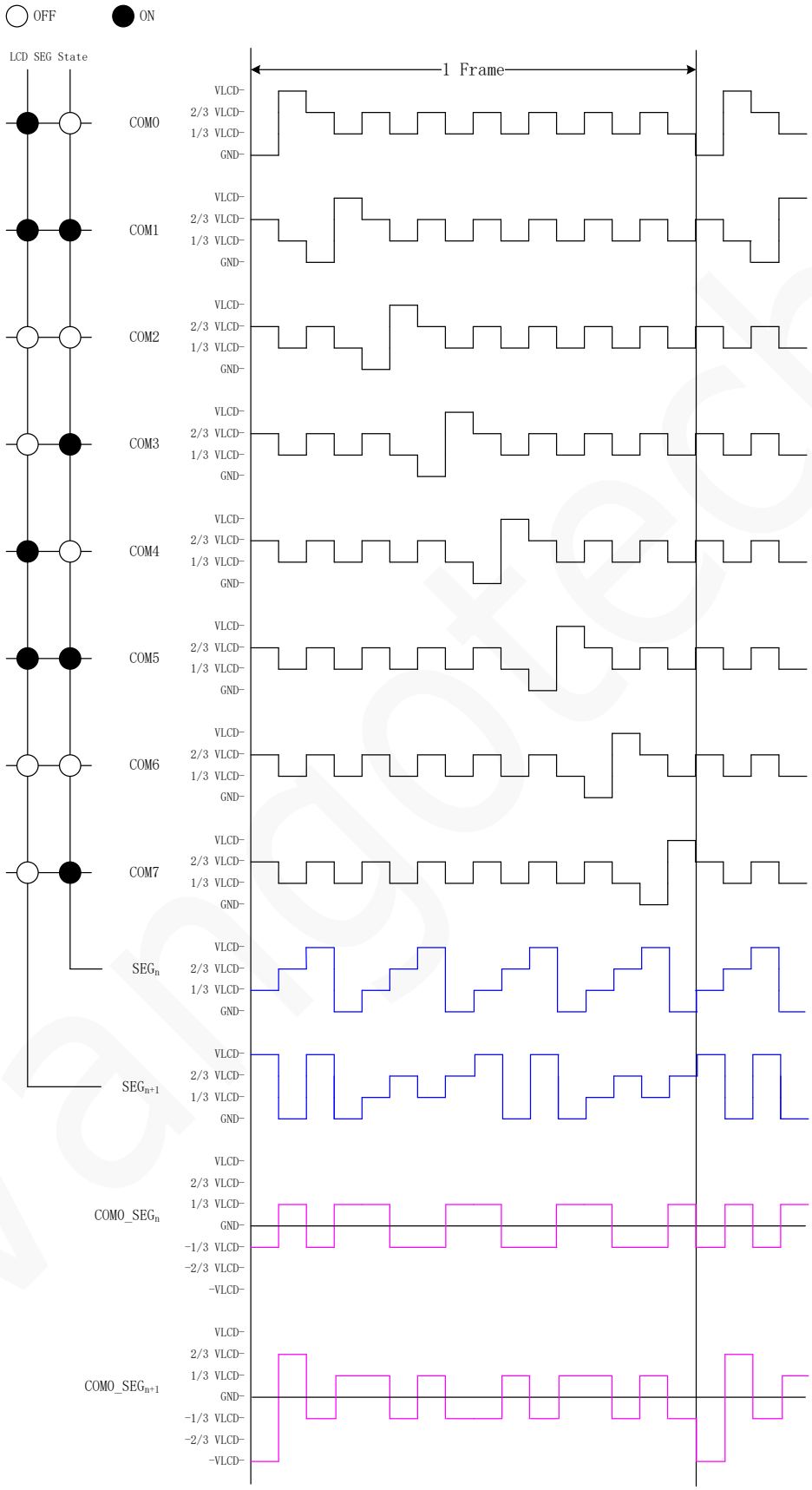


Figure 22-5 LCD Drive Waveform of 1/8 Duty and 1/3 Bias

When an LCD panel of 1/8 duty and 1/4 bias is applied, the LCD drive waveform is depicted in the following figures.

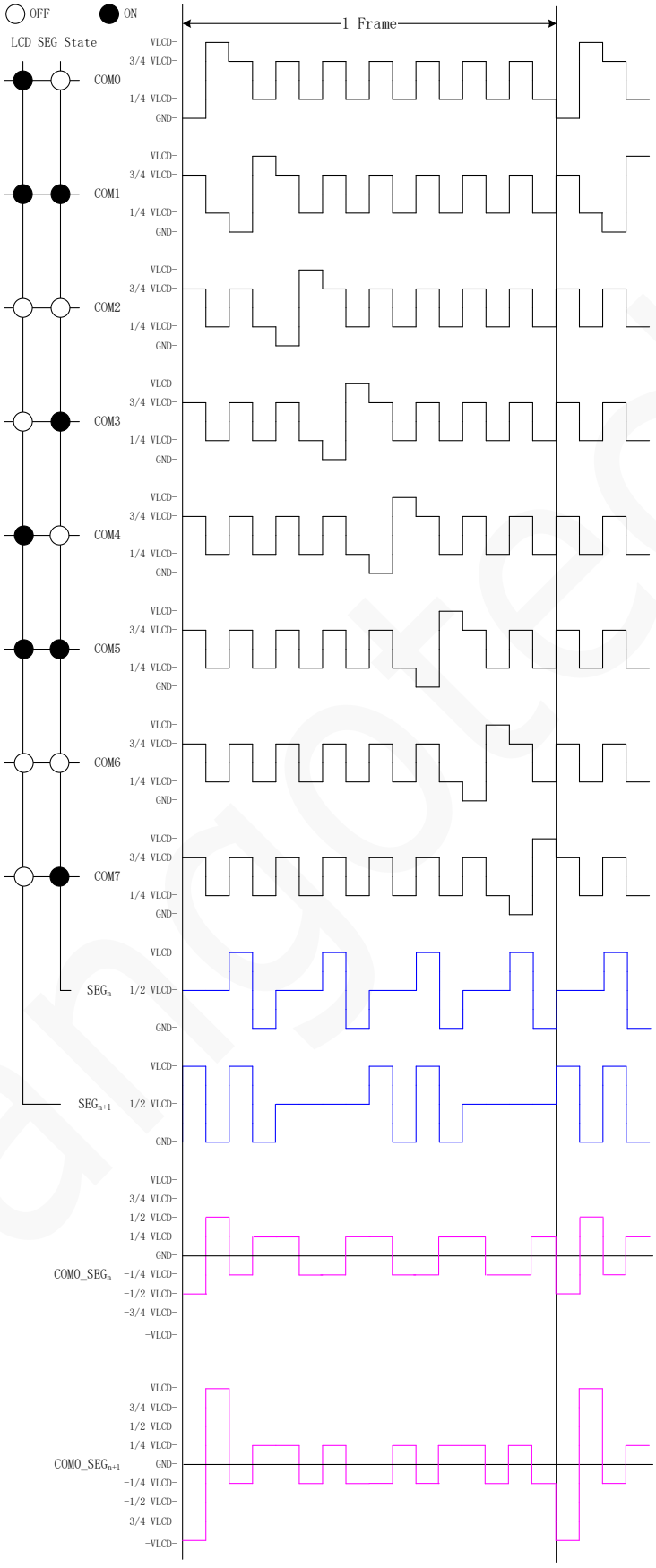


Figure 22-6 LCD Drive Waveform of 1/8 Duty and 1/4 Bias

22.8. Register Location

Table 22-1 Register Location of ANA Controller for LCD (ANA Base: 0x40014200)

Name	Type	Address	Description	Default
ANA_REG6	R/W	0x0018	Analog control register 6	0x00

Table 22-2 LCD Registers Map

Register Name	Offset	Type	Reset Value	Description
LCD_FBx[0..39,0x4]	0x0000	rw	0x0000_0000	LCD Frame buffer x register
LCD_CTRL	0x0100	rw	0x0000_0000	LCD control register
LCD_CTRL2	0x0104	rw	0x0000_0000	LCD control register 2
LCD_SEGCTRL0	0x0108	rw	0x0000_0000	LCD segment enable control register 0
LCD_SEGCTRL1	0x010C	rw	0x0000_0000	LCD segment enable control register 1
LCD_SEGCTRL2	0x0110	rw	0x0000_0000	LCD segment enable control register 2

22.9. Register Definition

22.9.1. LCD_FBx Register

Table 22-3 LCD_FBx Register Description

Bit	Name	Type	Description
31:0	DATAx	rw	Each bit represents a data in the display array; see Table 3~6 for detail of data arrangement under different mode. These registers can do byte read or write, so programmer can use CPU or DMA to fill these registers.

The LCD_FB00~LCD_FB13 is frame buffer A.

The LCD_FB14~LCD_FB27 is frame buffer B.

The following tables show only for frame buffer A, if FBMODE is select to 1, the frame buffer B has the same data layout as frame buffer A.

Table 22-4 Data arrangement of LCD_FBx

Register	Data bit			
	31:24	23:16	15:8	7:0
LCD_FB00	COM[7:0] of SEG3	COM[7:0] of SEG2	COM[7:0] of SEG1	COM[7:0] of SEG0
LCD_FB01	COM[7:0] of SEG7	COM[7:0] of SEG6	COM[7:0] of SEG5	COM[7:0] of SEG4
…..				
LCD_FB13	COM[7:0] of SEG79	COM[7:0] of SEG78	COM[7:0] of SEG77	COM[7:0] of SEG76

When 4 or 6 COMs mode is selected, the high bit of COM will be discarded, so the data format is the same as 8 COMs mode.

22.9.2. LCD_CTRL Register

Table 22-5 LCD_CTRL Register Description

Bit	Name	Type	Description
31:8	Rsvd	-	Reserved.
7	EN	rw	LCD controller enable register. 0: Disable 1: Enable
6	Rsvd	-	Reserved.
5:4	TYPE	rw	LCD type control register. 0: 4 COM mode 1: 6 COM mode 2: 8 COM mode 3: Reserved.
3:2	DRV	rw	LCD driving resistance control register. 0: 300 kohm 1: 600 kohm 2: 150 kohm 3: 200 kohm
1:0	FRQ	rw	LCD scan frequency 0: 64Hz 1: 128 Hz 2: 256Hz 3: 512Hz The scan frequency here means the scan speed of each COM, so if total COM is 4, then the overall frame rate will be this value divided by 4.

Note: If user want to switch COM type, user should disable LCD controller (bit7 of LCD_CTRL register) firstly, and then wait for a delay to ensure the current frame transmission is completed. The delay is calculated according to the current frame rate (bit7 and bit1:0 of LCD_CTRL register). For example, the current LCD scan frequency is 64Hz, and user want switch 4 COM to 6 COM, the delay is calculated as following: T_{Delay}=1/(64/4)=62.5ms

22.9.3. LCD_CTRL2 Register

Table 22-6 LCD_CTRL2 Register Description

Bit	Name	Type	Description
31:16	Rsvd	-	Reserved.
15:8	SWPR	rw	Frame buffer switch period. The switch period is calculated by the following equation. 0.5 sec * (SWPR + 1).
7:6	FBMODE	rw	LCD frame buffer switch mode control register. 0: Always show frame buffer A. 1: Switch between frame buffer A and frame buffer B. 2: Switch between frame buffer A and blank. 3: Reserved.

5	Rsvd	-	Reserved.
4	BKFILL	rw	Fill value at blank period. This register is used to control the filling value during blank period.
3:0	Rsvd	-	Reserved.

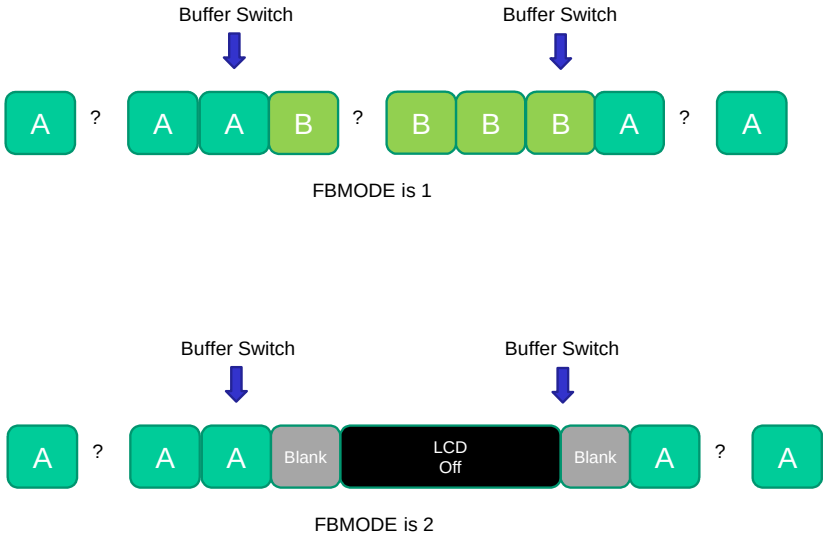


Figure 22-7 Frame buffer operation mode under different FBMODE

22.9.4. LCD_SEGCTRL0 Register

Table 22-7 LCD_SEGCTRL0 Register Description

Bit	Name	Type	Description
31:0	SEGCTRL	rw	Each bit control the SEG0~SEG31's LCD signal enable. Bit 0: SEG 0's enable control. Bit 1: SEG 1's enable control. …. Bit 31: SEG 31's enable control. 0: Disable SEG's output. 1: Enable SEG's output.

22.9.5. LCD_SEGCTRL1 Register

Table 22-8 LCD_SEGCTRL1 Register Description

Bit	Name	Type	Description
31:0	SEGCTRL	rw	Each bit control the SEG32~SEG63's LCD signal enable. Bit 0: SEG 32's enable control. Bit 1: SEG 33's enable control. …. Bit 31: SEG 63's enable control. 0: Disable SEG's output.

			1: Enable SEG's output.

22.9.6. LCD_SEGCTRL2 Register

Table 22-9 LCD_SEGCTRL2 Register Description

Bit	Name	Type	Description
31:16	Rsvd	-	Reserved.
15:0	SEGCTRL	rw	Each bit control the SEG64~SEG79's LCD signal enable. Bit 0: SEG 64's enable control. Bit 1: SEG 65's enable control. …. Bit 15: SEG 79's enable control. 0: Disable SEG's output. 1: Enable SEG's output.

22.9.7. ANA_REG6 Register

Table 22-10 Description of each bit in ANA_REG6

Bit	Name	Function	Notes
0	LCD_BMODE	LCD BIAS mode selection	0: 1/3 bias; 1: 1/4 bias.
4:1	VLCD[3:0]	LCD driving voltage	When VLCD=0:default When VLCD=0~5: adjust range =+60mV*VLCD When VLCD=6~15: adjust range =-60mV* (VLCD-5)

For Each COM and SEG, before enable the corresponding pin's LCD function, programmer should disable corresponding IO input and output function manually, and disable all special function of the corresponding IO to ensure LCD function work correctly.

23. SPI Controller

23.1. Introduction

One independent Serial Peripheral Interface (SPI) controller is built in V94XX(A) to facilitate communicating with other devices and components. The setting in SPI controller will be reset after wake-up from sleep or deep-sleep mode, programmer should restore the setting manually after wake-up from these two states. The SPICLK range supported by SPI host mode is APBCLK /2/4/8/16/32/64/128. The maximum SPICLK clock supported by SPI slave mode is APBCLK /2.

23.2. Features

--Support both master and slave mode.

--Support single byte and consecutive bytes transferring.

--Support receive overrun error indication

--Support transmitting / receiving interrupt request

--Programmable phase and polarity of master clock

--Selectable data sampling time (end or middle of clock period)

--Programmable master SCK clock frequency: APB Clock / 2, / 4, /8, /16, /32, /64, /128

--Built-in 8-depth 8-bits FIFO in both transmit and receive direction, the interrupt level of these two FIFOs is both programmable.

23.3. Block Diagram

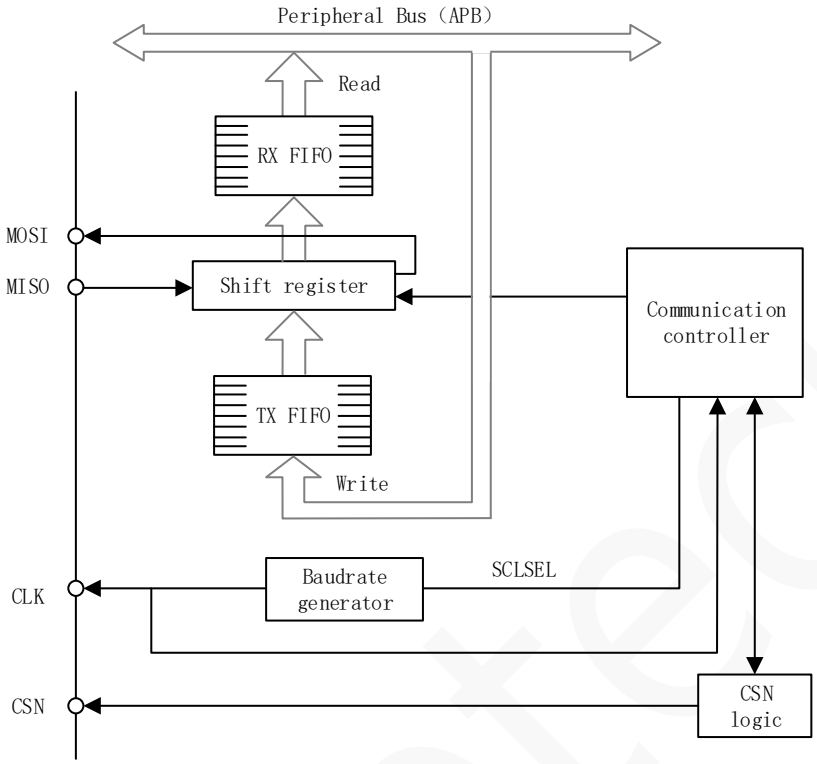


Figure 23-1 Functional Block Diagram of SPI Controller

Usually, the SPI is connected to the external device by 4 pins.

MOSI: The output pin in master mode/the input pin in slave mode. In general, MOSI is used to send data in master mode and receive data in slave mode.

MISO: The input pin in master mode/the output pin in slave mode. In general, MISO is used to receive data in master mode and send data in slave mode.

CLK: SPI serial clock pin, and controlled by master.

CSN: Slave chip select pin, According to the setting of SPI and CSN, CSN can be used as following:

--Select a slave to communication.

--Synchronous data frame.

Note: The maximum SPICLK clock supported by SPI slave mode is 1/2 APBCLK.

23.4. Register Location

Table 23-1 SPI Registers Map

Register Name	Offset	Type	Reset Value	Description
SPI_CTRL	0x0000	rw	0x0000_0000	SPI Control Register
SPI_TXSTS	0x0004	rw	0x0000_8200	SPI Transmit Status Register
SPI_TXDAT	0x0008	rw	0x0000_0000	SPI Transmit FIFO register

SPI_RXSTS	0x000C	rw	0x0000_0000	SPI Receive Status Register
SPI_RXDAT	0x0010	r	0x0000_0000	SPI Receive FIFO Register
SPI_MISC	0x0014	rw	0x0000_0003	SPI Misc. Control Register

23.5. Register Definition

23.5.1. SPI_CTRL Register

The SPI_CTRL register is used to control the SPI controller's behavior.

Table 23-2 SPI_CTRL Register Description

Bit	Name	Type	Description
31:16	Rsvd	-	Reserved.
15	SPIEN	rw	SPI enable For SPI engine, if this bit is set to 1, IOC[3:0] becomes SPI interface. 0: Disabled 1: Enabled
14:12	Rsvd	-	Reserved.
11	SPIRST	w	SPI Soft Reset. If this bit is written by "1", the state machine of SPI controller and FIFO pointer will return to the original value. 0: No effect 1: Reset SPI Controller
10	CSGPIO	rw	SPI CS pin is controlled by GPIO or H/W. For Master mode. 0: SPI CS pin control by SPI H/W. 1: SPI CS pin control by GPIO setting. For Slave mode. 0: SPI CS pin is controlled by external master. 1: SPI CS pin is connected to logic 0.
9	SWAP	rw	SPI MISO/MOSI swap control register. 0: No swap MISO/MOSI 1: Swap MISO/MOSI.
8	MOD	rw	SPI Mode Selection register 0: Master mode 1: Slave mode
7:6	Rsvd	-	Reserved.
5	SCKPHA	rw	SPI clock phase, refer to timing scheme on following section.
4	SCKPOL	rw	SPI clock polarity, refer to timing scheme on following section.
3	Rsvd	-	Reserved.
2:0	SCKSEL	rw	Master mode clock selection 000: APBCLK / 2 001: APBCLK / 4 010: APBCLK / 8

			011: APBCLK / 16 100: APBCLK / 32 101: APBCLK / 64 110: APBCLK / 128 111: Reserved.

23.5.2. SPI_TXSTS Register

The SPI_TXSTS register is used to control the SPI transmit FIFO and related interrupt.

Table 23-3 SPI_TXSTS Register Description

Bit	Name	Type	Description
31:16	Rsvd	-	Reserved.
15	SPITXIF	rc_w1	SPI Transmit Interrupt flag. This bit is set to "1" by hardware when the transmit FIFO level is lower than the value set by the user. When SMART is set in SPI_MISC register, the bit will be cleared as long as the transmit FIFO level is high than interrupt level, else you should write "1" to this control bit to clear this flag. Read 0: Not Occurred Read 1: Occurred Write 0: No effect Write 1: Clear the flag
14	SPITXIEN	rw	SPI Transmit Interrupt Enable If this bit is set to "1", and SPI interrupt (when 8-bit TX FIFO level in lower then interrupt level) occurs, hardware will issue an interrupt to CPU. If this bit is cleared to "0", this interrupt will be masked. 0: Disabled 1: Enabled
13:10	Rsvd	-	Reserved.
9	TXEMPTY	r	Transmit FIFO empty register. This bit will be set by hardware when the transmit FIFO is empty. And will be clear by hardware when the transmit FIFO is not empty. 0: Not Empty 1: Empty
8	TXFUR	r	Transmit FIFO under run register This will be set when transmit FIFO is empty and more data is requested by external SPI master, this bit will be set only at SPI slave mode. This bit will be cleared when programmer write 1 to SPITXIF flag.
7	Rsvd	-	Reserved.
6:4	TXFLEV	rw	Transmit FIFO interrupt level register. This register is used to indicated how much bytes is stored in transmit FIFO when issued interrupt. The lower value is set,

			the lower interrupt penalty you have. Since you can write more data in one interrupt. FIFO Full Interrupt issue timing 000: data no. in FIFO <1, 8 write is allowed. 001: data no. in FIFO <2, 7 write is allowed. 010: data no. in FIFO <3, 6 write is allowed. 011: data no. in FIFO <4, 5 write is allowed. 100: data no. in FIFO <5, 4 write is allowed. 101: data no. in FIFO <6, 3 write is allowed. 110: data no. in FIFO <7, 2 write is allowed. 111: data no. in FIFO <8, 1 write is allowed.
3	Rsvd	-	Reserved.
2:0	TXFFLAG	r	Transmit FIFO Data Level. The register is used to indicate how much data is still in the FIFO. 0000: No data in FIFO or 8 bytes in FIFO. 0001: 1 byte in FIFO. 0010: 2 bytes in FIFO. 0011: 3 bytes in FIFO. 0100: 4 bytes in FIFO. 0101: 5 bytes in FIFO. 0110: 6 bytes in FIFO. 0111: 7 bytes in FIFO.

23.5.3. SPI_TXDAT Register

The SPI_TXDAT register is used to write data to transmit FIFO of SPI engine and shift out to external master or slave.

Table 23-4 SPI_TXDAT Register Description

Bit	Name	Type	Description
31:8	Rsvd	-	Reserved.
7:0	SPITXD	w	Write data to SPI Transmit FIFO.

23.5.4. SPI_RXSTS Register

The SPI_RXSTS register is used to control the SPI receive FIFO and related interrupt. Table 18-5 shows the bit assignment of SPI_RXSTS register.

Table 23-5 SPI_RXSTS Register Description

Bit	Name	Type	Description
31:16	Rsvd	-	Reserved.
15	SPIRXIF	rc_w1	SPI Receive Interrupt flag. This bit is set to "1" by hardware when the receive FIFO level is higher than the value set by the user. When SMART is set in SPI_MISC register, the bit will be cleared as long as the receive FIFO level is lower than interrupt level, else you

			should write "1" to this control bit to clear this flag. Read 0: Not Occurred Read 1: Occurred Write 0: No effect Write 1: Clear the flag
14	SPIRXIEN	rw	SPI Receive Interrupt Enable. If this bit is set to "1", and SPI interrupt (when 8-bit RX FIFO level in higher than interrupt level) occurs, hardware will issue an interrupt to CPU. If this bit is cleared to "0", this interrupt will be masked. 0: Disabled 1: Enabled
13:10	Rsvd	-	Reserved.
9	RXFULL	r	Receive FIFO full register. This bit will be set by hardware when the receive FIFO is full. And will be clear by hardware when the receive FIFO is not full. 0: Not Full 1: Full
8	RXFOV	r	Receive FIFO over run register. This will be set when receive FIFO is full and more data is receive on the SPI data bus. This bit will be cleared when write 1 to SPIRXIF.
7	Rsvd	-	Reserved.
6:4	RXFLEV	rw	Receive FIFO interrupt level register. This register is used to indicated how much bytes is stored in receive FIFO when issued interrupt. The larger value is set, the lower interrupt penalty you have. Since you can read more data in one interrupt. FIFO Full Interrupt issue timing. 000: data no. in FIFO >= 1, 1 read is allowed. 001: data no. in FIFO >= 2, 2 read is allowed. 010: data no. in FIFO >= 3, 3 read is allowed. 011: data no. in FIFO >= 4, 4 read is allowed. 100: data no. in FIFO >= 5, 5 read is allowed. 101: data no. in FIFO >= 6, 6 read is allowed. 110: data no. in FIFO >= 7, 7 read is allowed. 111: data no. in FIFO >= 8, 8 read is allowed.
3	Rsvd	-	Reserved.
2:0	RXFFLAG	r	Receive FIFO Data Level The register is used to indicate how much data is still in the FIFO. 0000: No data in FIFO or 8 bytes in FIFO 0001: 1 byte in FIFO 0010: 2 bytes in FIFO 0011: 3 bytes in FIFO 0100: 4 bytes in FIFO 0101: 5 bytes in FIFO

			0110: 6 bytes in FIFO 0111: 7 bytes in FIFO

23.5.5. SPI_RXDAT Register

The SPI_RXDAT register is used to read data from receive FIFO of SPI engine.

Table 23-6 SPI_RXDAT Register Description

Bit	Name	Type	Description
31:8	Rsvd	-	Reserved.
7:0	SPIRXD	r	Read data from SPI Receive FIFO.

23.5.6. SPI_MISC Register

The SPI_MISC register is used to control misc. features of SPI engine.

Table 23-7 SPI_MISC Register Description

Bit	Name	Type	Description
31:10	Rsvd	-	Reserved.
9	OVER	rw	SPI FIFO Over Write Mode This register is used to control the data will be overwrite or skipped when TX/RX FIFO is full. 0: The further write to the full FIFO will be skipped. 1: The further write to the full FIFO will overwrite the last written data in the FIFO.
8	SMART	rw	SPI FIFO SMART Mode Register When this bit is set to "1", programmer don't need to clear the transmit/receive interrupt flag when the FIFO status is reach, programmer only needs write-to/read-from transmit/receive FIFO and let the FIFO level lower/higher than the interrupt level, and the interrupt flag will clear automatically. When DMA mode is selected, this bit must be set to 1 to ensure the DMA operation correctly. 0: Normal Interrupt Clear 1: Smart Interrupt Clear
7:5	Rsvd	-	Reserved.
4	BSY	r	SPI Controller Busy Flag This bit is used to indicate if the SPI controller is busy or not. 0: Idle 1: Busy
3	RFF	r	Receive FIFO Full Flag This bit is used to indicate if the SPI controller is real full or not. If the receive FIFO is full, that means any data read from SPI bus can't be written into the FIFO, and the RFOV bit will be set in this situation. 0: Receive FIFO not full 1: Receive FIFO full.

2	RNE	r	Receive FIFO Not Empty Flag This bit is used to indicated if there is any data currently in the receive FIFO. 0: Receive FIFO is empty 1: Receive FIFO is not empty
1	TNF	r	Transmit FIFO Not Full Flag. This bit is used to indicated if there is any empty slots in the transmit FIFO. 0: Transmit FIFO is full, you can't write any more data into it. 1: Transmit FIFO is not full.
0	TFE	r	Transmit FIFO Empty Flag This bit is used to indicated if the transmit FIFO is empty or not. 0: Transmit FIFO is not empty. 1: Transmit FIFO is empty.

23.6. Application Note

23.6.1. Master Mode

When in master mode, the shifting clock (SPICLK) is generated by V94XX(A). There are two control bits to control the clock phase and polarity. The transmission starts immediately from a register writes to the SPI_TXDAT register. As long as there is data in the FIFO, the transmission will start automatically when one byte is transferred.

The SPI shifts the data from MSB to LSB through the SDO pin. The 8-bit data is shifted out after 8 SCK cycles. At the same time, the data is also shifted in through slave device SDI pin. When the transmit FIFO level is lower than the interrupt trigger level, the SPITXIF flag bit will be set; besides, a SPI interrupt will be generated if the SPITXIEN bit is set. When the receive FIFO level is higher than the interrupt trigger level, the SPIRXIF flag bit will be set; besides, a SPI interrupt will be generated if the SPIRXIEN bit is set. Programmer can read SPI data from SPI_RXDAT register.

The following diagram depicts the timing scheme on SPI master mode for different operation types (polarity control bit equals "1" or "0", phase control bit equals "1" or "0", and sample strobe control bit equals "1" or "0").

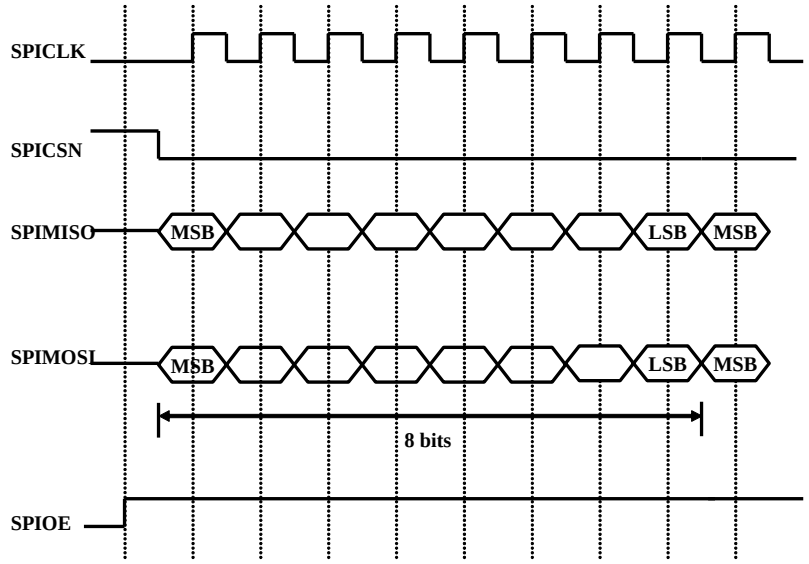


Figure 23-2Master Mode, SPO = 0, SPH=0

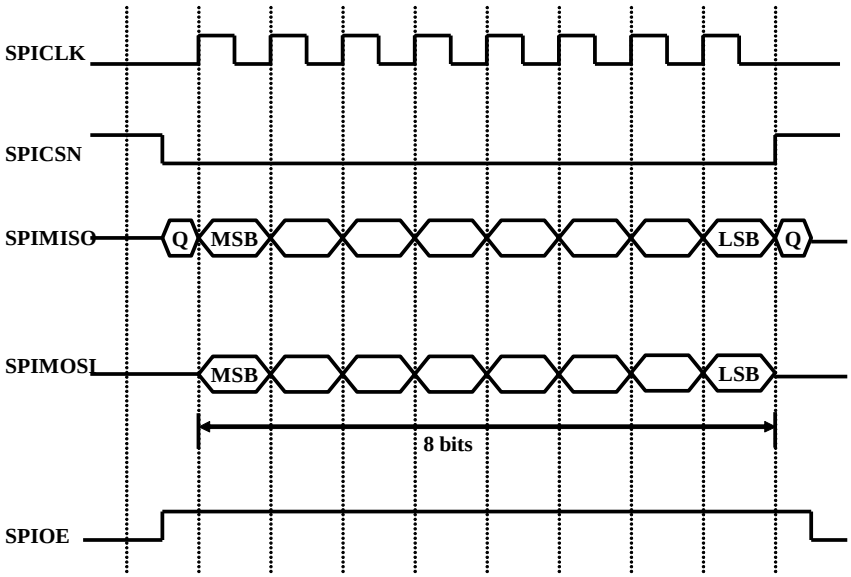


Figure 23-3 Master Mode, SPO = 0, SPH=1

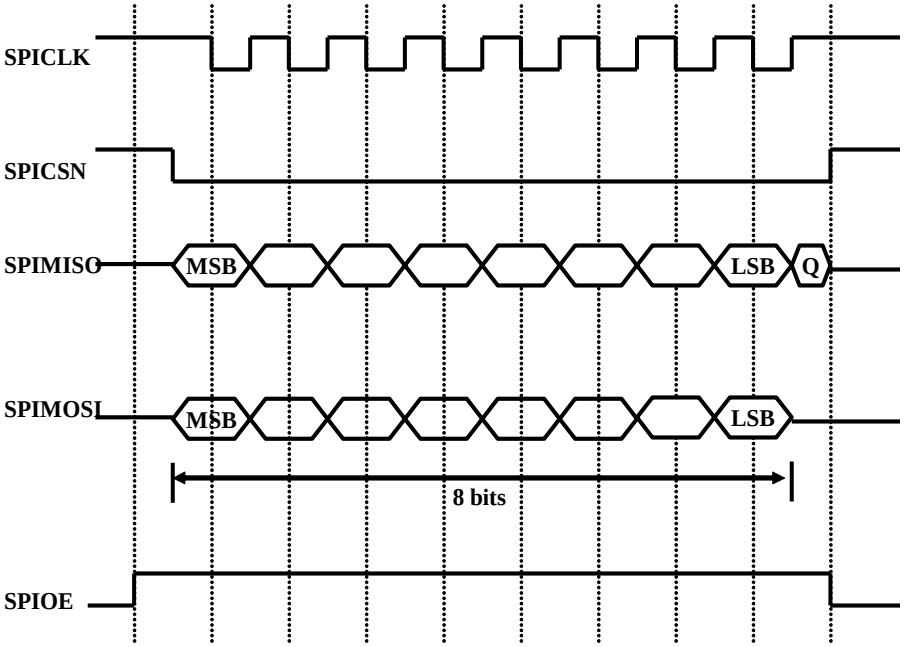


Figure 23-4 Master Mode, SPO = 1, SPH=0

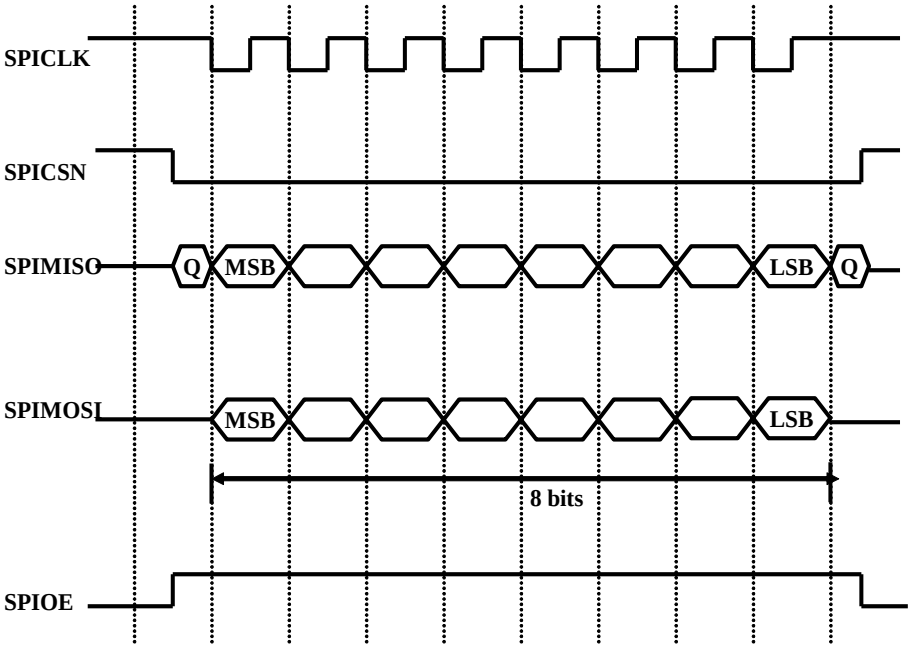


Figure 23-5 Master Mode, SPO = 1, SPH=1

23.6.2. Salve Mode

During SPI salve mode, the SPICLK and SPICSN is generated by the external master. The SPI slave mode is supported only for SPO=0 and SPH=0. The same SPI_TXDAT and SPI_RXDAT registers are used for data transmit and receive. The maximum allowed SPICLK during SPI slave mode is 1/2 APBCLK. And DMA transfer is recommended when the receive clock is fast.

23.6.3. Consecutive Bytes Transfer

Consecutive bytes transfer is available in master and slave modes. In transmission, software is able to send the data consecutively as long as the TNF bit is 1. In reception, software will check for overrun error to monitor if there is any missing data due to the polling rate is too low.

24. I2C Controller

24.1. Introduction

The I2C subcomponent is the I2C Bus Controller which provides an interface that meets the Philips I2C bus specification and supports all transfer modes from and to the I2C bus. The I2C bus uses two wires to transfer information between devices connected to the bus: "scl" (serial clock line) and "sda" (serial data line). The I2C logic handles bytes transfer autonomously. It also keeps track of serial transfers, and a status register reflects the status of the I2C Bus Controller and the I2C bus. The setting in I2C controller will be reset after wake-up from sleep or deep-sleep mode, programmer should restore the setting manually after wake-up from these two states. The I2C Bus supports fSCL = 1MHz (period: 1us) and can be realized by setting the overflow frequency of timer 3.

24.2. Feature

--Master transmit/receive mode supported.

--Slave transmit/receive mode supported.

--Detection of bus arbitration fail.

--Interrupt generation.

--Programmable ACK generation.

--Programmable clock speed in master mode.

--Input de-bounce circuit.

24.3. Block Diagram

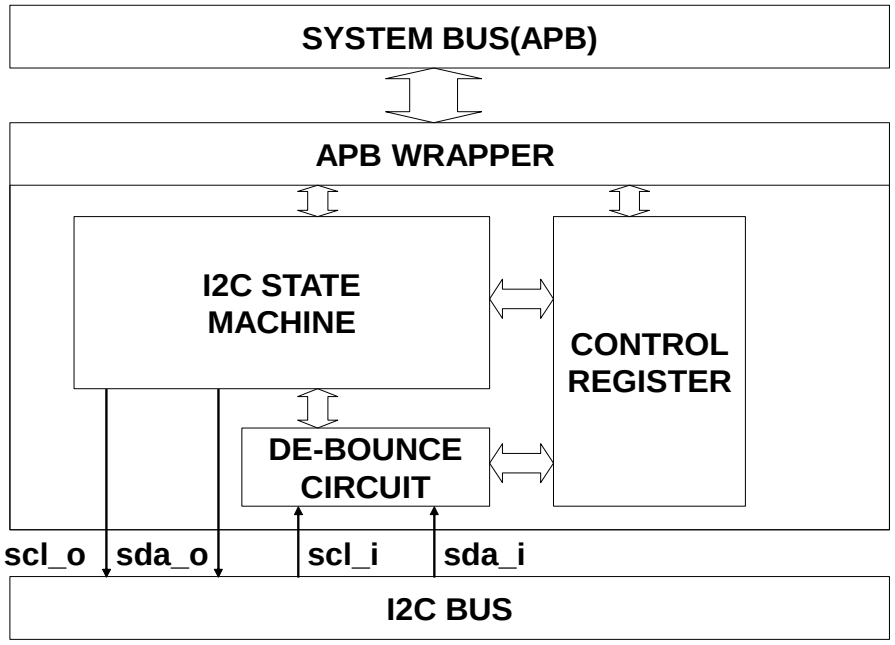


Figure 24-1 Functional Block Diagram of I2C Controller

24.4. Register Location

Table 24-1 I2C Registers Map

Register Name	Offset	Type	Reset Value	Description
I2C_DATA	0x0000	rw	0x0000_0000	I2C data register
I2C_ADDR	0x0004	rw	0x0000_0000	I2C address register
I2C_CTRL	0x0008	rw	0x0000_0000	I2C control/status register
I2C_STS	0x000C	r	0x0000_00F8	I2C status register
I2C_CTRL2	0x0018	rw	0x0000_0000	I2C interrupt enable register

24.5. Register Definition

24.5.1. I2C_DATA Register

Table 24-2 I2C_DATA Register Description

Bit	Name	Type	Description
31:8	Rsvd	-	Reserved.
7:0	DATA	rw	The I2C_DATA register contains a byte to be transmitted through I2C bus or a byte which has just been received through I2C bus. The CPU can read from and write to this 8-bit register while it is not in the process of byte shifting. The I2C_DATA register is not shadowed or double buffered so the

			user should only read I2C_DATA when an I2C interrupt occurs.

24.5.2. I2C_ADDR Register

Table 24-3 I2C_ADDR Register Description

Bit	Name	Type	Description
31:8	Rsvd	-	Reserved.
7:1	SLA	rw	Own I2C slave address (7 bit)
0	GC	rw	General Call Address Acknowledge If this bit is set, the general call address is recognized; otherwise it is ignored.

24.5.3. I2C_CTRL Register

Table 24-4 I2C_CTRL Register Description

Bit	Name	Type	Description
31:8	Rsvd	-	Reserved.
7	CR2	rw	Clock rate bit 2
6	EN	rw	I2C enable bit When EN='0' the "sdao" and "sclo" outputs are set to 1, that drives the output pads of the chip in high impedance, and "sdai" and "scli" input signals are ignored. When EN='1' I2C component is enabled and corresponded GPIO will be set to I2C function automatically.
5	STA	rw	START Flag When STA='1', the I2C component checks the I2C bus status and if the bus is free a START condition is generated.
4	STO	rw	STOP Flag When STO='1' and I2C interface is in master mode, a STOP condition is transmitted to the I2C bus.
3	SI	rc_w1	Serial Interrupt Flag The "SI" is set by hardware when one of 25 out of 26 possible I2C states is entered. The only state that does not set the "SI" is state F8h, which indicates that no relevant state information is available. The "SI" flag must be cleared by software. In order to clear the "SI" bit, '0' must be written to this bit. Writing a '1' to "SI" bit does not change value of the "SI". When an interrupt is occurred, clear SI means the trigger of next action, so all the necessary control register or data must be set before SI is cleared.
2	AA	rw	Assert Acknowledge Flag When AA='1', an "acknowledge" will be returned when: - the "own slave address" has been received - the general call address has been received while GC bit in i2caddr register was set

			- a data byte has been received while I2C was in master receiver mode - a data byte has been received while I2C was in slave receiver mode When AA='0', an "not acknowledge" will be returned when: - a data byte has been received while I2C was in master receiver mode - a data byte has been received while I2C was in slave receiver mode
1	CR1	rw	Clock rate bit 1
0	CR0	rw	Clock rate bit 0

Table 24-5 shows the SCL clock frequency at master mode under different CR2~CR0 setting.

Table 24-5 SCL clock speed setting

CR2	CR1	CR0	SCL Frequency (KHz)				Clock Divided by
			PCLK = 6.5536 MHz	PCLK = 13.1072 MHz	PCLK = 19.6608 MHz	PCLK = 26.2144 MHz	
0	0	0	25.6	51.2	76.8	102.4	256
0	0	1	29.2	58.4	87.6	116.8	224
0	1	0	34.1	68.2	102.3	136.4	192
0	1	1	40.9	81.9	122.9	163.8	160
1	0	0	6.8	13.7	20.5	27.3	960
1	0	1	54.6	109.2	163.8	218.4	120
1	1	0	109.2	218.4	327.7	436.9	60
1	1	1	TIMER3's overflow frequency divide by 8				

24.5.4. I2C_STS Register

Table 24-6 I2C_STS Register Description

Bit	Name	Type	Description
31:8	Rsvd	-	Reserved.
7:3	STS	r	I2C Status Code.
2:0	Rsvd	-	Reserved.

Table 24-7~Table 24-11 shows the status code under different kind of I2C modes.

Table 24-7 I2C Status in Master Transmitter Mode

STS	Status of I2C	Application Software Response					Next Action taken by I2C hardware
		Read/Write I2C_DATA	To I2C_CTRL				
			STA	STO	SI	AA	
0x08	A START condition has been transmitted.	Write SLA+W*	X	0	0	X	SLA+W will be transmitted ACK will be received
0x10	A repeated START condition has been transmitted.	Write SLA+W	X	0	0	X	SLA+W will be transmitted ACK will be received
		Write	X	0	0	X	SLA+R will be transmitted

		SLA+R*					I2C will be switched to master receive mode
0x18	SLA+W has been transmitted. ACK has been received.	Write data byte	0	0	0	X	Data byte will be transmitted. ACK will be received
		no action	1	0	0	X	Repeated START will be transmitted.
		no action	0	1	0	X	STOP condition will be transmitted. STO flag will be reset
		no action	1	1	0	X	STOP condition followed by a START condition will be transmitted. STO flag will be reset
0x20	SLA+W has been transmitted. NACK has been received.	Write data byte	0	0	0	X	Data byte will be transmitted. ACK will be received
		no action	1	0	0	X	Repeated START will be transmitted.
		no action	0	1	0	X	STOP condition will be transmitted. STO flag will be reset
		no action	1	1	0	X	STOP condition followed by a START condition will be transmitted. STO flag will be reset
0x28	Data byte in i2cdat has been transmitted. ACK has been received.	Write data byte	0	0	0	X	Data byte will be transmitted. ACK bit will be received
		no action	1	0	0	X	Repeated START will be transmitted.
		no action	0	1	0	X	STOP condition will be transmitted. STO flag will be reset.
		no action	1	1	0	X	STOP condition followed by a START condition will be transmitted. STO flag will be reset.
0x30	Data byte in i2cdat has been transmitted. NACK has been received.	Write data byte *	0	0	0	X	Data byte will be transmitted. ACK will be received.
		no action	1	0	0	X	Repeated START will be transmitted.
		no action	0	1	0	X	STOP condition will be transmitted. STO flag will be reset.
		no action	1	1	0	X	STOP condition followed by a START condition will be

							transmitted. STO flag will be reset.

*: SLA+W: Slave address [7:1] and write bit as bit 0, write bit is 0.

*: SLA+R: Slave address [7:1] and read bit as bit 0, read bit is 1.

Table 24-8 I2C Status in Master Receiver Mode

STS	Status of I2C	Application Software Response					Next Action taken by I2C hardware
		Read/Write I2C_DATA	To I2C_CTRL				
			STA	STO	SI	AA	
0x08	A START condition has been transmitted	Write SLA+R	X	0	0	X	SLA+R will be transmitted. ACK will be received
0x10	A repeated START condition has been transmitted.	Write SLA+R	X	0	0	X	SLA+R will be transmitted. ACK will be received
		Write SLA+W	X	0	0	X	SLA+W will be transmitted. I2C will be switched to master transmit mode
0x40	SLA+R has been transmitted. ACK has been received.	no action	0	0	0	0	Data byte will be received. not ACK will be returned
		no action	0	0	0	1	Data byte will be received. ACK will be returned
0x48	SLA+R has been transmitted. Not ACK has been received.	no action	1	0	0	X	Repeated START condition will be transmitted
		no action	0	1	0	X	STOP condition will be transmitted. STO flag will be reset
		no action	1	1	0	X	STOP condition followed by a START condition will be transmitted. STO flag will be reset
0x50	Data byte has been received. ACK has been returned.	Read data byte	0	0	0	0	Data byte will be received. not ACK will be returned
		Read data byte	0	0	0	1	Data byte will be received. ACK will be returned
0x58	Data byte has been received. Not ACK has been returned.	Read data byte	1	0	0	X	Repeated START condition will be transmitted
		Read data byte	0	1	0	X	STOP condition will be transmitted. STO flag will be reset
		Read data byte	1	1	0	X	STOP condition followed by a START condition will be transmitted. STO flag will be reset

Table 24-9 I2C Status in Slave Receiver Mode

STS	Status of I2C	Application Software Response		Next Action taken by I2C hardware
		Read/Write	To I2C_CTRL	

		I2C_DATA	STA	STO	SI	AA	
0x60	Own SLA+W has been received. ACK has been returned.	no action	X	0	0	0	Data byte will be received and not ACK will be returned.
		no action	X	0	0	1	Data byte will be received and ACK will be returned.
0x68	Arbitration lost in SLA+R/W as master. Own SLA+W has been received, ACK returned.	no action	X	0	0	0	Data byte will be received and not ACK will be returned.
		no action	X	0	0	1	Data byte will be received and ACK will be returned.
0x70	General call address (00H) has been received. ACK has been returned.	no action	X	0	0	0	Data byte will be received and not ACK will be returned.
		no action	X	0	0	1	Data byte will be received and ACK will be returned.
0x78	Arbitration lost in SLA+R/W as master. General call address has been received, ACK returned.	no action	X	0	0	0	Data byte will be received and not ACK will be returned.
		no action	X	0	0	1	Data byte will be received and ACK will be returned.
0x80	Previously addressed with own SLV address. DATA has been received. ACK returned.	Read data byte	X	0	0	0	Data byte will be received and not ACK will be returned.
		Read data byte	X	0	0	1	Data byte will be received and ACK will be returned.
0x88	Previously addressed with own SLA. DATA byte has been received. Not ACK returned.	Read data byte	0	0	0	0	Switched to not addressed SLV mode. No recognition of own SLA or general call address.
		Read data byte	0	0	0	1	Switched to not addressed SLV mode. Own SLA or general call address will be recognized.
		Read data byte	1	0	0	0	Switched to not addressed SLV mode. No recognition of own SLA or general call address. START condition will be transmitted when the bus becomes free.
		Read data byte	1	0	0	1	Switched to not addressed SLV mode. Own SLA or general call address will be recognized. START condition will be transmitted when the bus becomes free.
0x90	Previously addressed with general call	Read data byte	X	0	0	0	Data byte will be received and not ACK will be

	address. DATA has been received. ACK returned.						returned.
		Read data byte	X	0	0	1	Data byte will be received and ACK will be returned.
0x98	Previously addressed with general call address. DATA has been received. Not ACK returned.	Read data byte	0	0	0	0	Switched to not addressed SLV mode. No recognition of own SLA or general call address
		Read data byte	0	0	0	1	Switched to not addressed SLV mode. Own SLA or general call address will be recognized.
		Read data byte	1	0	0	0	Switched to not addressed SLV mode; no recognition of own SLA or general call address. START condition will be transmitted when the bus becomes free.
		Read data byte	1	0	0	1	Switched to not addressed SLV mode. Own SLA or general call address will be recognized. START condition will be transmitted when the bus becomes free
0xA0	A STOP condition or repeated START condition has been received while still addressed as slave receive or slave transmit mode.	no action	0	0	0	0	Switched to not addressed SLV mode. No recognition of own SLA or general call address.
		no action	0	0	0	1	Switched to not addressed slave mode. Own SLA or general call address will be recognized.
		no action	1	0	0	0	Switched to not addressed SLV mode. No recognition of own SLA or general call address. START condition will be transmitted when the bus becomes free
		no action	1	0	0	1	Switched to not addressed SLV mode. Own SLA or general call address will be recognized. START condition will be transmitted when the bus becomes free.

Table 24-10 I2C Status in Slave Transmitter Mode

STS	Status of I2C	Application Software Response					Next Action taken by I2C hardware
		Read/Write I2C_DATA	To I2C_CTRL				
			STA	STO	SI	AA	

0xA8	Own SLA+R has been received. ACK has been returned.	Write data byte	X	0	0	0	Last data byte will be transmitted and ACK will be received.
		Write data byte	X	0	0	1	Data byte will be transmitted. ACK will be received.
0xB0	Arbitration lost in SLA+R/W as master. Own SLA+R has been received. ACK has been returned.	Write data byte	X	0	0	0	Last data byte will be transmitted and ACK will be received.
		Write data byte	X	0	0	1	Data byte will be transmitted. ACK will be received.
0xB8	Data byte has been transmitted. ACK has been received.	Write data byte	X	0	0	0	Last data byte will be transmitted and ACK will be received.
		Write data byte	X	0	0	1	Data byte will be transmitted; ACK will be received.
0xC0	Data byte has been transmitted. NACK has been received.	no action	0	0	0	0	Switched to not addressed SLV mode. No recognition of own SLA or general call address.
		no action	0	0	0	1	Switched to not addressed SLV mode. Own SLA or general call address will be recognized.
		no action	1	0	0	0	Switched to not addressed SLV mode. No recognition of own SLA or general call address. START condition will be transmitted when the bus becomes free.
		no action	1	0	0	1	Switched to not addressed SLV mode. Own SLA or general call address will be recognized. START condition will be transmitted when the bus becomes free.
0xC8	Last data byte has been transmitted. ACK has been received.	no action	0	0	0	0	Switched to not addressed SLV mode. No recognition of own SLA or general call address.
		no action	0	0	0	1	Switched to not addressed SLV mode. Own SLA or general call address will be recognized.
		no action	1	0	0	0	Switched to not addressed SLV mode. No recognition of

							own SLA or general call address. START condition will be transmitted when the bus becomes free.
		no action	1	0	0	1	Switched to not addressed SLV mode. Own SLA or general call address will be recognized. START condition will be transmitted when the bus becomes free.

Table 24-11 I2C Misc. Status

STS	Status of I2C	Application Software Response					Next Action taken by I2C hardware
		Read/Write I2C_DATA	To I2C_CTRL				
			STA	STO	SI	AA	
0x38	Arbitration lost	No action	0	0	0	X	I2C bus will be released; A start condition will be transmitted.
		No action	1	0	0	X	when the bus becomes free (enter to a master mode)
0xF8	No relevant state information available; si=0	No action	X	X	X	X	Wait or proceed current transfer
0x00	Bus error during MST or selected slave modes	No action	0	1	0	X	Only the internal hardware is affected in the MST or addressed SLV modes. In all cases, the bus is released and I2C is switched to the not addressed SLV mode. Sto flag is reset.

24.5.5. I2C_CTRL2 Register

Table 24-12 I2C_CTRL2 Register Description

Bit	Name	Type	Description
31:1	Rsvd	-	Reserved.
0	INTEN	rw	Interrupt enable control of I2C controller. 0: Disable. 1: Enable.

24.6. Application Notes

24.6.1. I2C Bus Protocol: Start/Stop Generation

A Start condition can transfer a one-byte serial data over the SDA line, and a stop condition can terminate the data transfer. A stop condition is a Low-to-High transition of the SDA line while SCL is high. Start

and Stop conditions are always generated by the master. The I2C-bus is busy when a Start condition is generated. A few clocks after a Stop condition, the IIC-bus will be free, again.

When a master initiates a Start condition, it should send a slave address to notify the slave device. The one byte of address field consists of a 7-bit address and a 1-bit transfer direction indicator (that is, write or read). If bit 8 is 0, it indicates a write operation (transmit operation); if bit 8 is 1, it indicates a request for data read (receive operation).

The master will finish the transfer operation by transmitting a Stop condition. If the master wants to continue the data transmission to the bus, it should generate another Start condition as well as a slave address. In this way, the read/write operation can be performed in various formats.

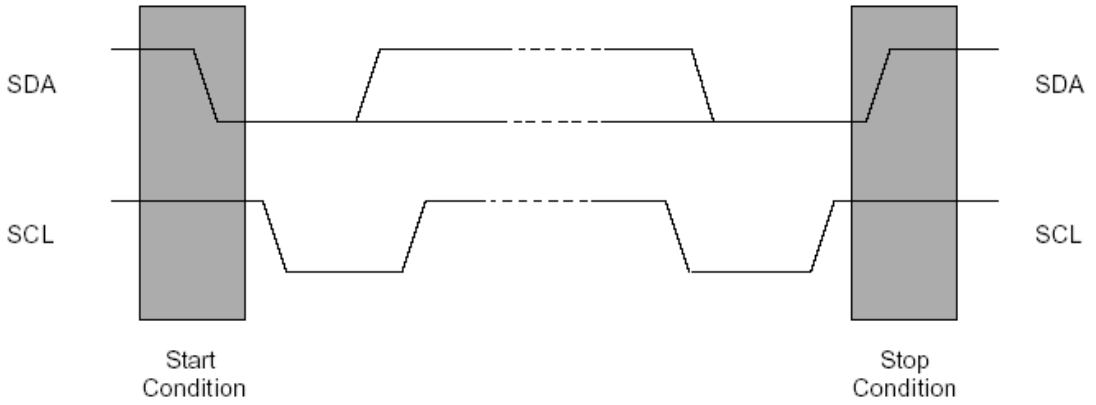


Figure 24-2 Start and Stop Conditions

24.6.2. Data Transfer Format

Every byte placed on the SDA line should be eight bits in length. The number of bytes which can be transmitted per transfer is unlimited. The first byte following a Start condition should have the address field. The address field can be transmitted by the master when the IIC-bus is operating in master mode. Each byte should be followed by an acknowledgement (ACK) bit. The MSB bit of the serial data and addresses are always sent first.

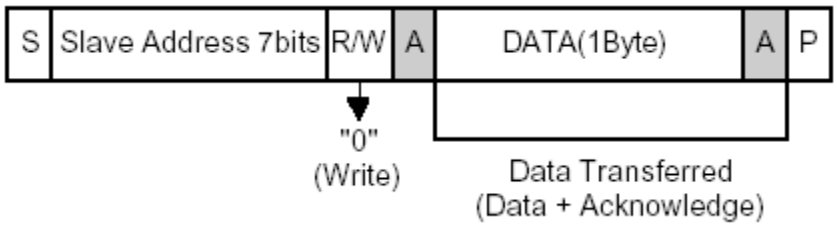


Figure 24-3 Write Mode with 7-bits Address

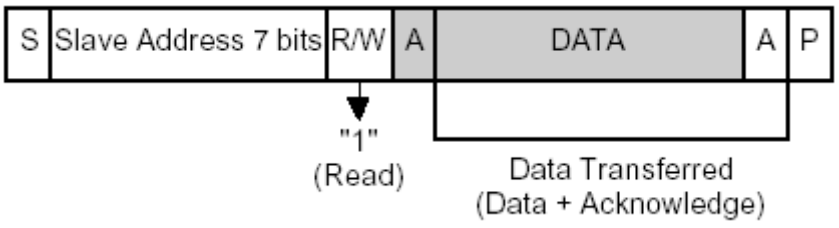


Figure 24-4 Read Mode with 7-bits Address

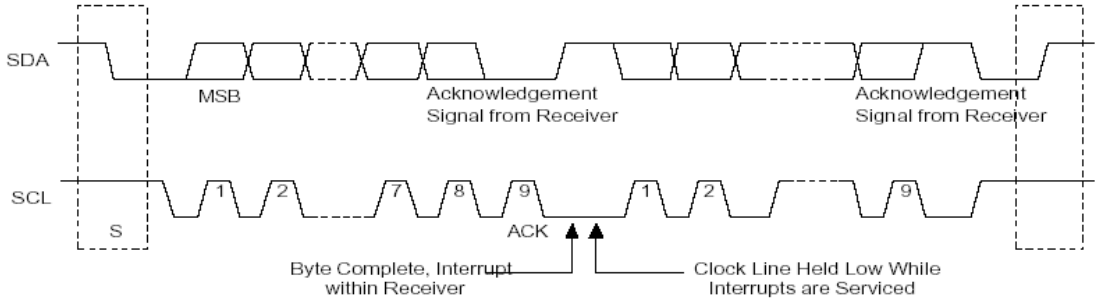


Figure 24-5 Data Transfer on The I2C bus

24.6.3. ACK Signal Transmission

To finish a one-byte transfer operation completely, the receiver should send an ACK bit to the transmitter. The ACK pulse should occur at the ninth clock of the SCL line. Eight clocks are required for the one-byte data transfer. The master should generate the clock pulse required to transmit the ACK bit.

The transmitter should release the SDA line by making the SDA line High when the ACK clock pulse is received. The receiver should also drive the SDA line Low during the ACK clock pulse so that the SDA is Low during the High period of the ninth SCL pulse.

The ACK bit transmit function can be enabled or disabled by software (AA). However, the ACK pulse on the ninth clock of SCL is required to complete a one-byte data transfer operation.

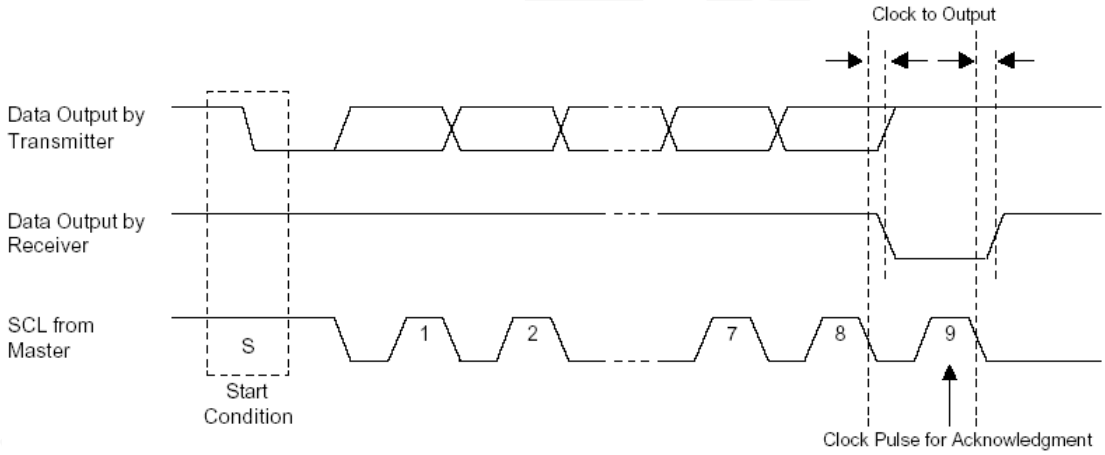


Figure 24-6 Acknowledge on The I2C bus

24.6.4. Read-Write Operation

In the transmitter mode, after the data is transferred, the I2C-bus interface will wait until pending interrupt is cleared. Until the interrupt is cleared, the SCL line will be held low. After the interrupt is cleared, the SCL line will be released. After the CPU receives the interrupt request, it should write a new data into I2C_DATA before clear the pending interrupt.

In the receive mode, after a data is received, the I2C-bus interface will wait until pending interrupt is cleared. Until the pending interrupt is cleared, the SCL line will be held low. After the pending interrupt is cleared, the SCL line will be released. After the CPU receives the interrupt request, it should read the data from I2C_DATA before clear the pending interrupt.

Bus Arbitration Procedures

Arbitration takes place on the SDA line to prevent the contention on the bus between two masters. If a master with a SDA High level detects another master with a SDA active Low level, it will not initiate a data transfer because the current level on the bus does not correspond to its own. The arbitration procedure will be extended until the SDA line turns high.

However when the masters simultaneously lower the SDA line, each master should evaluate whether or not the mastership is allocated to itself. For the purpose of evaluation, each master should detect the address bits. While each master generates the slaver address, it should also detect the address bit on the SDA line because the

Lowering of SDA line is stronger than maintaining High on the line. For example, one master generates a Low as first address bit, while the other master is maintaining High. In this case, both masters will detect Low on the bus because Low is stronger than high even if first master is trying to maintain high on the line. When this happens, low (as the first bit of address) -generating master will get the mastership and high (as the first bit of address) - generating master should withdraw the mastership. If both masters generate Low as the first bit of address, there should be an arbitration for second address bit, again. This arbitration will continue to the end of last address bit.

Abort Condition

If a slave receiver can't acknowledge the confirmation of the slave address, it should hold the level of the SDA line High. In this case, the master should generate a Stop condition and abort the transfer.

If a master receiver is involved in the aborted transfer, it should signal the end of the slave transmit operation by canceling the generation of an ACK after the last data byte received from the slave. The slave transmitter should then release the SDA to allow a master to generate a Stop condition.

24.6.5. Interface Timing

The following diagram shows the interface connection of I2C bus.

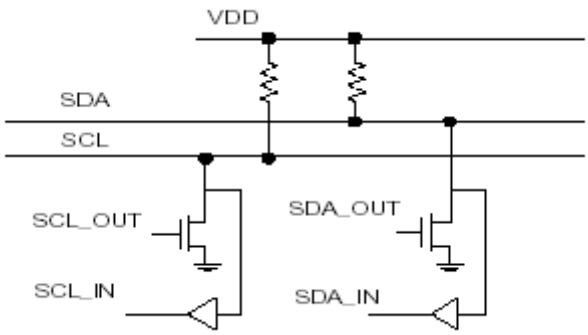


Figure 24-7 I2C Bus Connection Example

To control the frequency of the serial clock (SCL), programmer can use CR2~CR0 in the I2C_CTRL register.

The I2C Bus supports fSCL = 1MHz (period: 1us).

— Rise Time of the SCL and SDA: f_{SCL}= 100kHz: 1000ns；f_{SCL}= 400kHz: 300ns

— Fall Time of the SCL and SDA: f_{SCL}= 100kHz: 300ns；f_{SCL}= 400kHz: 300ns

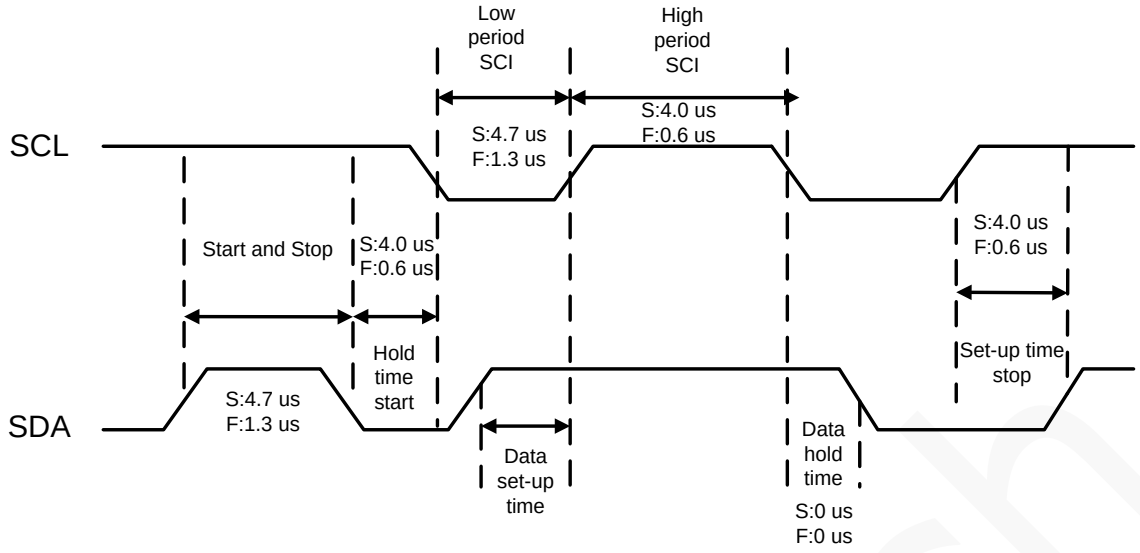


Figure 24-8 Timing on the SCL and SDA

Table 24-13 I2C AC Characteristics

Time	I2C – master mode (CR<7)		I2C – master mode (CR=7)	
$t_{HD:STA}$	scl/4	min(15 clk)	scl/4	(2 bclk)
t_{LOW}	scl/2	min(30 clk)	scl/2	(4 bclk)
t_{HIGH}	scl/2	min(30 clk)	scl/2	(4 bclk)
$t_{SU:STA}$	scl/4	min(15 clk)	scl/2 – if (scl/4<7 clk)	
			scl/4 – others	
$t_{HD:DAT}$	6*clk	(6 clk)	6*clk	(6 clk)
$t_{SU:DAT}$	1*clk (-for first bit)*	(1 clk)	1*clk (-for first bit)*	(1 clk)
	scl/2 - 6*clk	min(24 clk)	scl/2 - 6*clk	min(1clk)
$t_{SU:STO}$	scl/4 + 7*clk	min(22 clk)	min(bclk +9)	
t_{BUF}	(¾ scl)+9*clk	min(54 clk)	min (¾ scl)	

*- is a case when write to data register is close to the scl rising edge of the first bit data byte.

clk: APB clock period

bclk: Timer 3's overflow period

scl: I2C clock period

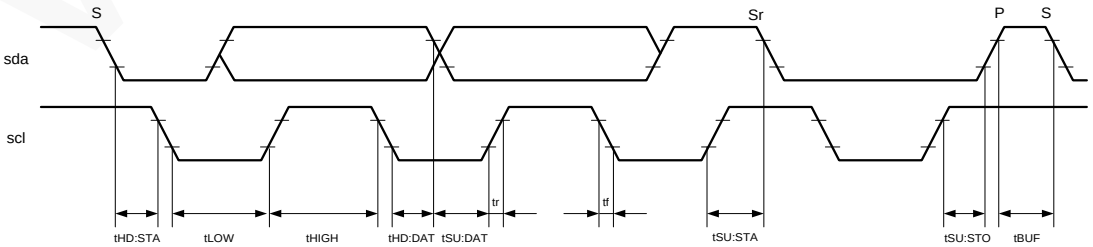


Figure 24-9 AC Timing of I2C Controller

24.6.6. The Resolution for SDA Pin Lock-Status

In the process of I2C communication, when the chip is reset (software reset, WDT reset, external reset), it may cause the I2C data line (SDA is locked in low level) is stuck LOW, the master should send nine clock pulses. The device that held the bus LOW should release it within those nine clocks. If I2C is not stuck LOW in the current time, the nine clock pulses add by user will not affect I2C usage.

24.7. Firmware Flow

24.7.1. Master Transmit Mode

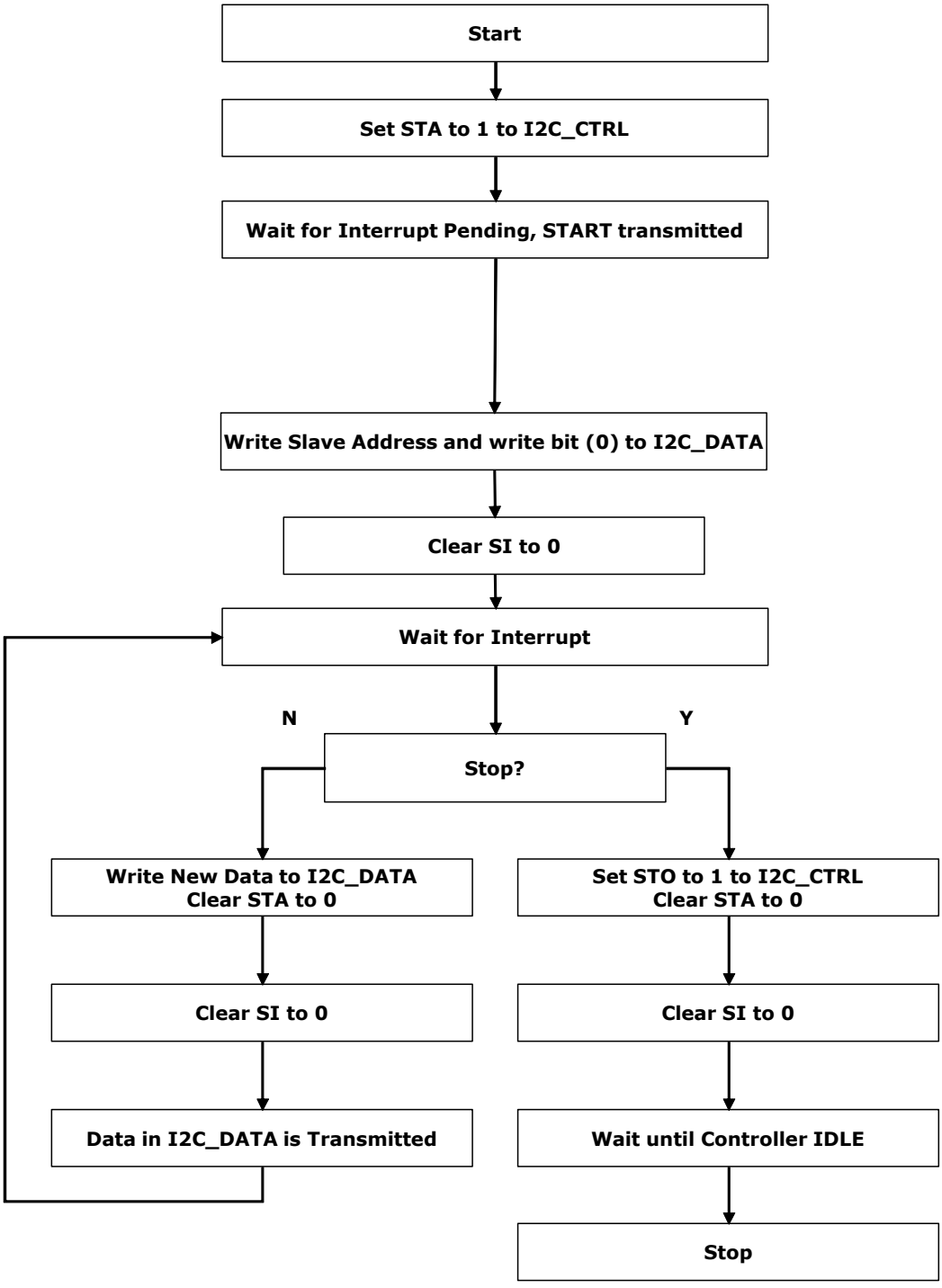


Figure 24-10 Operations for Master Transmitter Mode

24.7.2. Master Receive Mode

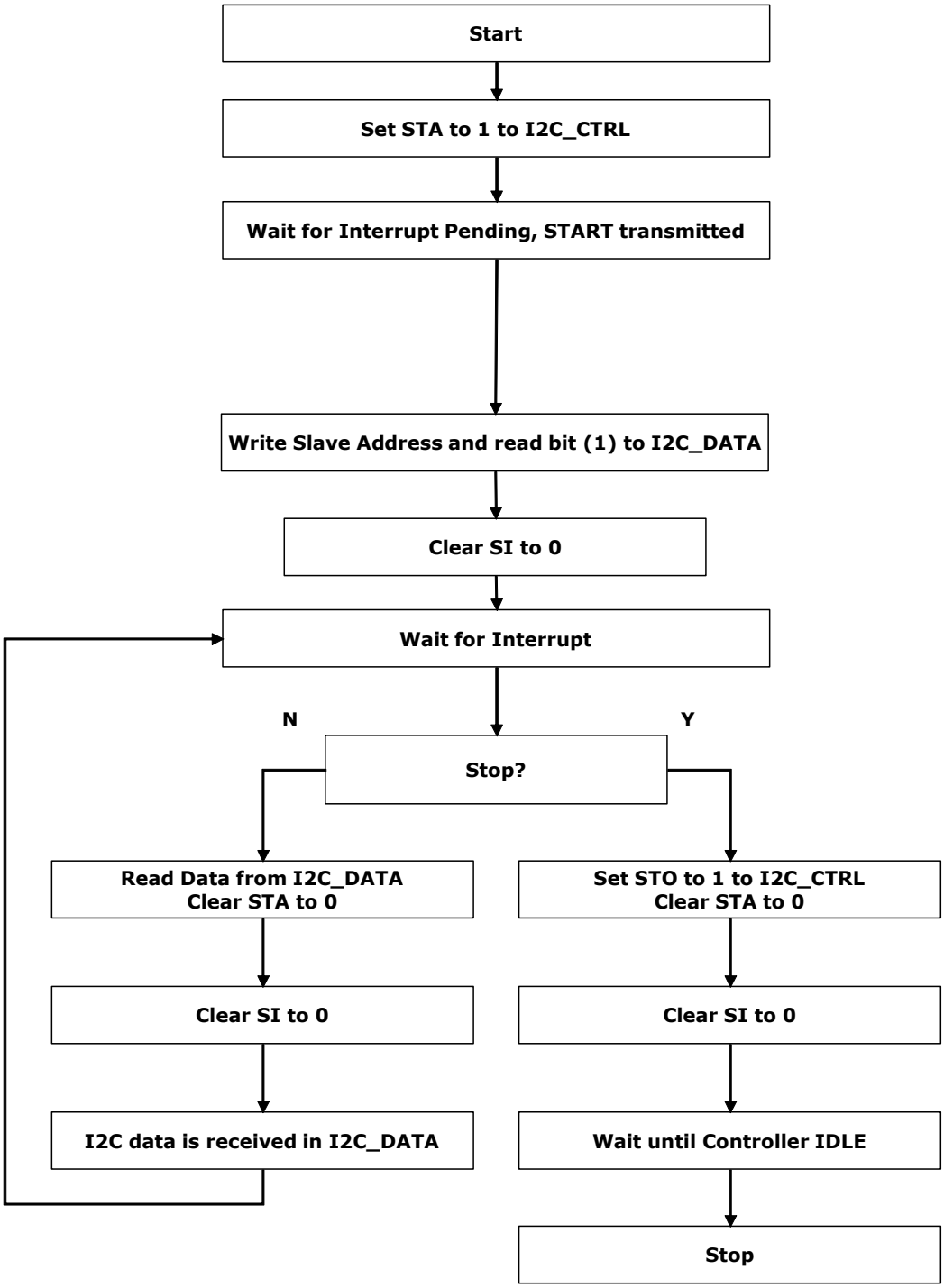


Figure 24-11 Operations for Master Receiver Mode

24.7.3. Slave Transmit Mode

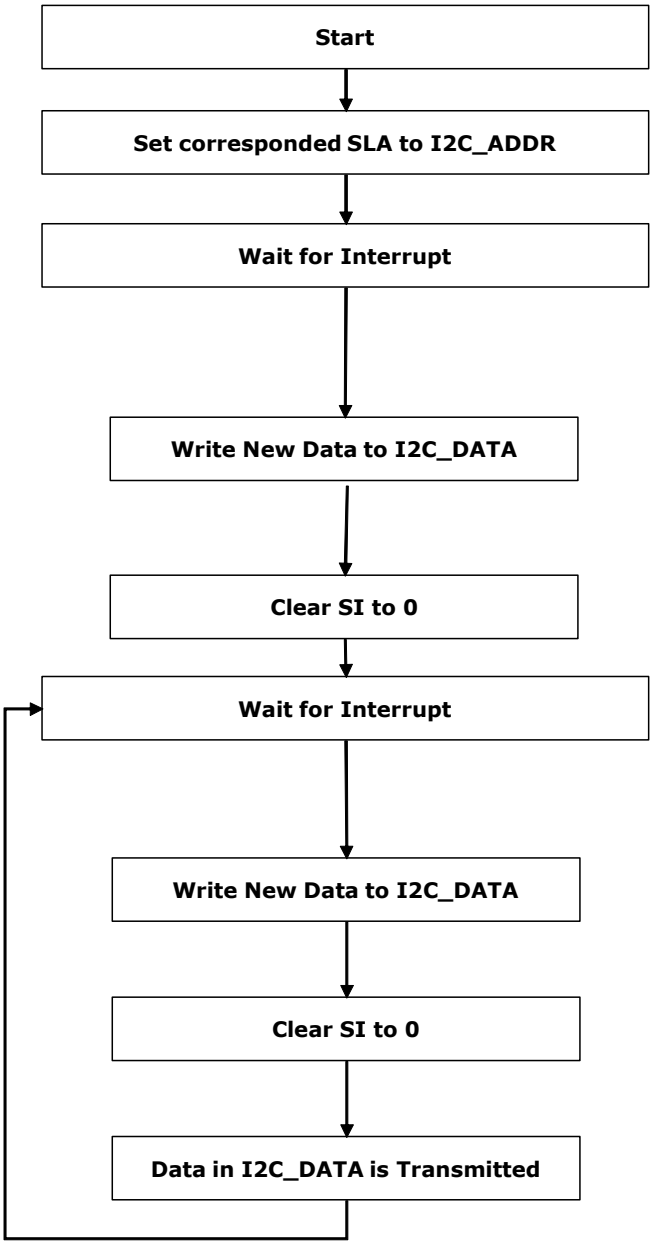


Figure 24-12 Operations for Slave Transmitter Mode

24.7.4. Slave Receive Mode

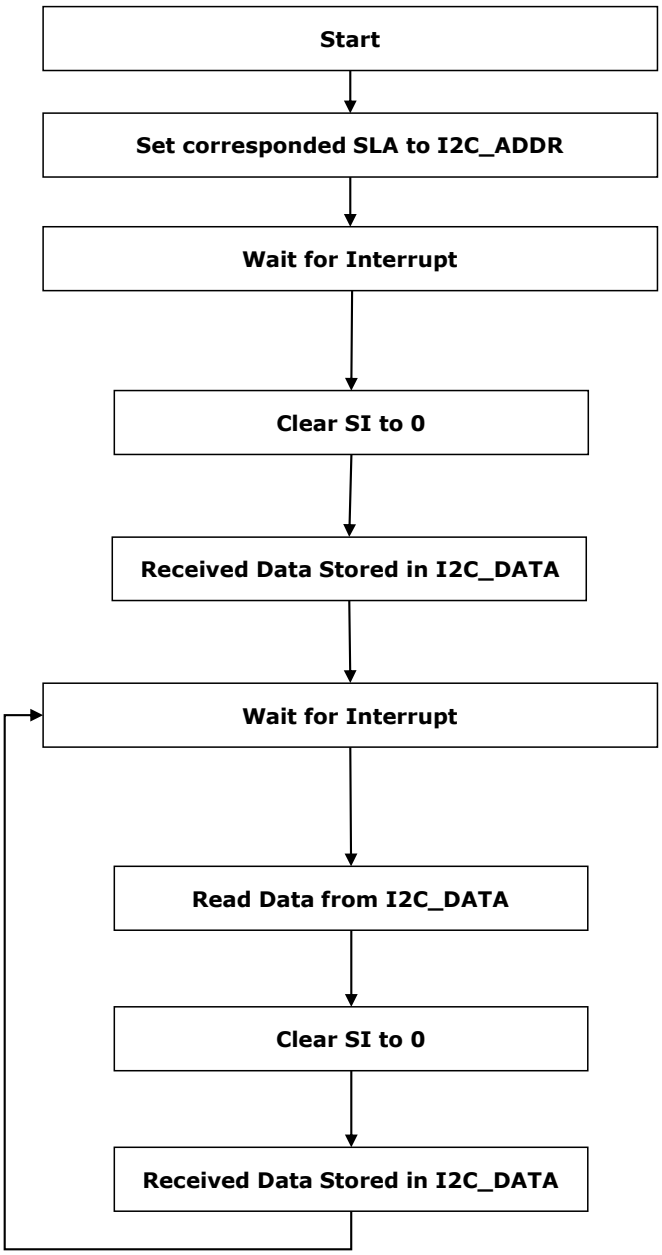


Figure 24-13 Operations for Slave Receiver Mode

25. MISC Controller

25.1. Introduction

The MISC controller is used to control some special function of V94XX(A). There are two MISC controllers inside V94XX(A), one is in core domain (MISC controller) which will be power-off during sleep and deep-sleep mode. The setting in MISC controller will be reset after wake-up from sleep or deep-sleep mode, programmer should restore the setting manually after wake-up from these two states. Another one (MISC2 controller) is in retention domain which will be power-off at deep-sleep mode. The setting in MISC2 controller will be reset after wake-up from deep-sleep mode, programmer should restore the setting manually after wake-up from deep-sleep mode.

25.2. Feature

--Clock control of each sub-module

--Clock divider of AHBCLK and APBCLK.

--FLASH program tick control

--IR duty control.

--SRAM parity check interrupt control.

25.3. Block Diagram

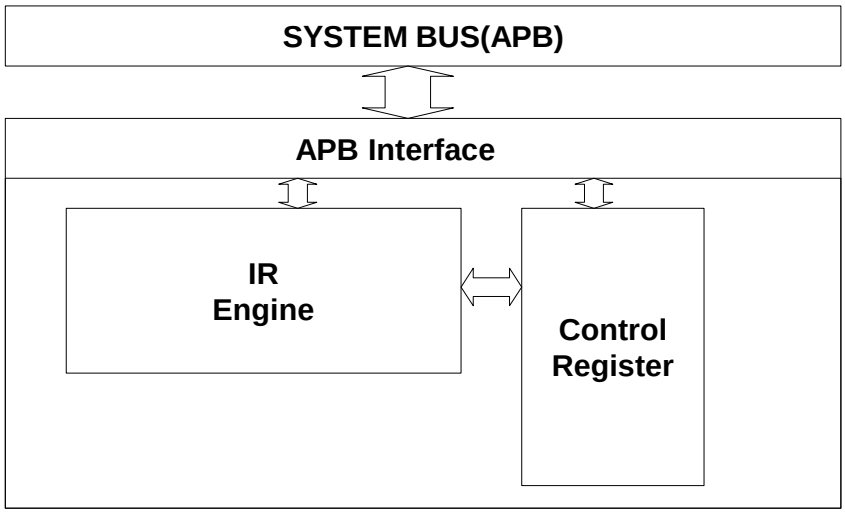


Figure 25-1 Functional Block Diagram of MISC Controller

25.4. MISC Register Location

Table 25-1 MISC Registers Map

Register Name	Offset	Type	Reset Value	Description
MISC_SRAMINT	0x0000	rc_w1	0x0000_0000	SRAM Parity Error Interrupt.
MISC_SRAMINIT	0x0004	rw	0x0000_0001	SRAM initialize register
MISC_PARERR	0x0008	r	0x0000_0000	SRAM Parity Error address register
MISC_IREN	0x000C	rw	0x0000_0000	IR enable control register
MISC_DUTYL	0x0010	rw	0x0000_0000	IR Duty low pulse control register
MISC_DUTYH	0x0014	rw	0x0000_0000	IR Duty high pulse control register
MISC_IRQLAT	0x0018	rw	0x0000_0000	Cortex-M0 IRQ latency control register
MISC_HIADDR	0x0020	r	0x0000_0000	AHB invalid access address
MISC_PIADDR	0x0024	r	0x0000_0000	APB invalid access address

25.5. MISC Register Definition

25.5.1. MISC_SRAMINT Register

Table 25-2 MISC_SRAMINT Register Description

Bit	Name	Type	Description
31:5	Rsvd	-	Reserved.
4	LOCKUP	rc_w1	This bit indicates the CM0 lockup has happened. Write 1 to clear this flag.
3	PIAC	rc_w1	This bit indicates that an invalid address access on APB bus is occurred. At the same time, the failure address is latched into MISC_PIADDR. The invalid APB address means not in the region of 0x40010000 ~ 0x40017FFF. If PIACIE is 1, then a NMI will be issued to CM0. Write 1 to clear this flag.
2	HIAC	rc_w1	This bit indicates that an invalid address access on AHB bus is occurred. At the same time, the failure address is latched into MISC_HIADDR. The invalid AHB address means not in the region of FLASH or SRAM or IO. If HIACIE is 1, then a NMI will be issued to CM0. Write 1 to clear this flag.
1	Rsvd	-	Reserved.
0	PERR	rc_w1	This bit indicates that a SRAM parity error is happened during the SRAM read process. If PERRIE is 1, then a NMI will be issued to CM0. Write 1 to clear this flag.

25.5.2. MISC_SRAMINIT Register

Table 25-3 MISC_SRAMINIT Register Description

Bit	Name	Type	Description
31:8	Rsvd	-	Reserved.
7	LOCKIE	rw	CM0 lockup NMI enable register.
6	PIACIE	rw	APB invalid address access NMI enable register.
5	HIACIE	rw	AHB invalid address access NMI enable register.
4:3	Rsvd	-	Reserved.

2	INIT	rw	SRAM initialize register, set this register to 1 will initialize the SRAM with all zero value with correct parity. This bit will be clear to 0 automatically, during the initialize time, it is not allowed for access of any master on the bus (CPU or DMA), wrong data maybe get during this period.
1	PERRIE	rw	SRAM parity error NMI enable register.
0	PEN	rw	Parity check enable register. When this bit is 1, all the write access to internal SRAM will also write the parity information into additional parity buffer. When doing SRAM read, automatically parity check will be done and generate the parity error interrupt when parity check fail. By default, this function is turned on, so no need special effort on the software side. But if CPU or DMA access some un-initialize region, parity may happen because the parity information didn't exist in those non-initialize area. At this moment, programmer can use INIT bit to do SRAM initialize automatically.

25.5.3. MISC_PARERR Register

Table 25-4 MISC_PARERR Register Description

Bit	Name	Type	Description
31:12	Rsvd	-	Reserved.
11:0	PEADDR	r	Parity error address. This register store the information of parity error address, when PE NMI is happened, programmer can check this register to know which SRAM address has defect bit. SRAM parity error address =0x20000000+4* PEADDR.

25.5.4. MISC_IREN Register

Table 25-5 MISC_IREN Register Description

Bit	Name	Type	Description
31:6	Rsvd	-	Reserved.
5:0	IREN	rw	IR enable control register. Each bit in this register corresponded to 1 UART TX channel. When IREN[x] is set to 1, it means UART TX[x] will be modulated with IR pulse to output.

25.5.5. MISC_DUTYL Register

Table 25-6 MISC_DUTYL Register Description

Bit	Name	Type	Description
31:16	Rsvd	-	Reserved.
15:0	DUTYL	rw	IR low pulse width control register. The low pulse width will

			be (DUTYL + 1)*APBCLK period.

25.5.6. MISC_DUTYH Register

Table 25-7 MISC_DUTYH Register Description

Bit	Name	Type	Description
31:16	Rsvd	-	Reserved.
15:0	DUTYH	rw	IR high pulse width control register. The high pulse width will be (DUTYH + 1)*APBCLK period.

25.5.7. MISC_IRQLAT Register

Table 25-8 MISC_IRQLAT Register Description

Bit	Name	Type	Description
31:10	Rsvd	-	Reserved.
9	NOHARDFAULT	rw	This register is used to disable the hard fault generation to CPU. 0: Enable hard fault generation when bus error is happened. 1: Disable hard fault generation when bus error is happened, the HIAL hard-fault is not able to be disabled by this bit. When CM0 detect hard fault is happened, it will jump to the hard fault service routine. After it complete the hard fault service, it will jump back to normal code and execute the same instruction again. So if the hard fault happens again, it will stop in this loop and never come out. This register is used for CPU to temporary disable the hard fault generation.
8	LOCKRESET	rw	This register is used to control if the lockup will issue a system reset. 0: Disable reset generation of CM0 lockup. 1: Enable reset generation of CM0 lockup.
7:0	IRQLAT	rw	This register is used to control the Cortex-M0 IRQ latency. The Cortex-M0 processor supports zero jitter interrupt latency for zero wait-state memory. IRQLAT specifies the minimum number of cycles between an interrupt that becomes pended in the NVIC, and the vector fetch for that interrupt being issued on the AHB-Lite interface. If this bus is set to 0, interrupts are taken as quickly as possible. For zero jitter in a zero wait state memory system, set this bus to at least a decimal value of 13. For non-zero wait state memory, zero jitter can be achieved with a higher value on IRQLAT.

25.5.8. MISC_HIADDR Register

Table 25-9 MISC_HIADDR Register Description

Bit	Name	Type	Description

31:0	HIADDR	r	AHB bus error address. The register is stored the error address information for acessing AHB bus. When error happened, user can access the error address via the register located AHB bus. The error address= HIADDR

25.5.9. MISC_PIADDR Register

Table 25-10 MISC_PIADDR Register Description

Bit	Name	Type	Description
31:0	PIADDR	r	APB bus error address. The register is stored the error address information for acessing APB bus. When error happened, user can access the error address via the register located APB bus. The error address= 0x40000000 + PIADDR

25.6. MISC2 Register Location

Table 25-11 MISC2 Registers Map

Register Name	Offset	Type	Reset Value	Description
MISC2_FLASHWC	0x0000	rw	0x0000_2100	FLASH wait cycle register.
MISC2_CLKSEL	0x0004	rw	0x0000_0000	Clock selection register.
MISC2_CLKDIVH	0x0008	rw	0x0000_0000	AHB clock divider control register
MISC2_CLKDIVP	0x000C	rw	0x0000_0001	APB clock divider control register
MISC2_HCLKEN	0x0010	rw	0x0000_01FF	AHB clock enable control register
MISC2_PCLKEN	0x0014	rw	0xFFFF_FFFF	APB clock enable control register

25.7. MISC2 Register Definition

25.7.1. MISC2_FLASHWC Register

Table 25-12 MISC2_FLASHWC Register Description

Bit	Name	Type	Description
31:14	Rsvd	-	Reserved.
13:8	1USCYCLE	rw	This register is used for FLASH controller to calculate 1ustick from AHB clock 1ustick = (AHB clock period)*(1USCYCLE+1) This setting is related to the wake-up time of FLASH, and the programming time of FLASH. FLASH wake-up time =1ustick *10. It must meet 1ustick >=1 μs. For example, the clock frequency of AHB is 26.2144MHz. In order to ensure the minimum wake-up time, 1USCYCLE should be set to 26. So, the wake-up time of FLASH is 27 / 26214400 * 10, which is about 10 μs.

			For example, the clock frequency of AHB is 32.768KHz. In order to ensure the minimum wake-up time, 1USCYCLE should be set to 0. So, the wake-up time of FLASH is 1 / 32768 * 10, which is about 305 μs.
7:0	Rsvd	-	Reserved.

25.7.2. MISC2_CLKSEL Register

Table 25-13 MISC2_CLKSEL Register Description

Bit	Name	Type	Description
31:3	Rsvd	-	Reserved.
2:0	CLKSEL	rw	This register is used to control AHB clock source. 0: RCH (6.5MHz RC) 1: XOH (6.5536MHz XTAH). 2: PLLH. 3: RTCCLK (controlled by RTCCLK_SEL in PMU_CONTROL register). 4: PLLL. Before clock select to one of the clock source, programmer should enable the corresponded module first by setting PMU_CONTROL register.

25.7.3. MISC2_CLKDIVH Register

Table 25-14 MISC2_CLKDIVH Register Description

Bit	Name	Type	Description
31:8	Rsvd	-	Reserved.
7:0	CLKDIVH	rw	This register is used to control AHB clock divider. 0: Clock source divide by 1 1: Clock source divide by 2. 2: Clock source divide by 3. …. 255: Clock source divide by 256.

25.7.4. MISC2_CLKDIVP Register

Table 25-15 MISC2_CLKDIVP Register Description

Bit	Name	Type	Description
31:8	Rsvd	-	Reserved.
7:0	CLKDIVP	rw	This register is used to control APB clock divider. 0: AHB clock divide by 1. 1: AHB clock divide by 2. 2: AHB clock divide by 3. …. 255: AHB clock divide by 256.

25.7.5. MISC2_HCLKEN Register

Table 25-16 MISC2_HCLKEN Register Description

Bit	Name	Type	Description
31:9	Rsvd	-	Reserved.
8:0	HCLKEN	rw	This register is used to control clock enable of each AHB module. The corresponded module can be turned-off only when its function is not been used. Refer to Table 25-17 for detail about each module. 0: Disable. 1: Enable.

Table 25-17 HCLK Clock Enable of Each Module

Bit	Module	Note
0	--	
1	Arbiter & Bus Matrix	Shouldn't off when CPU or DMA is active.
2	FLASH Controller	Shouldn't off
3	SRAM Controller	Shouldn't off
4	DMA Controller	
5	GPIO Controller	
6	LCD Controller	
7	--	
8	CRYPT Controller	

25.7.6. MISC2_PCLKEN Register

Table 25-18 MISC2_PCLKEN Register Description

Bit	Name	Type	Description
31:0	PCLKEN	rw	This register is used to control clock enable of each APB module. The corresponded module can be turned-off only when its function is not been used. Refer to Table 25-19 for detail about each module. 0: Disable. 1: Enable.

Table 25-19 PCLK clock Enable of Each Module

Bit	Module	Note
0	AHB2APB Bridge	Shouldn't off when CPU or DMA is access APB peripheral.
1	DMA Controller	
2	I2C	
3	Reserved	

4	UART0	
5	UART1	
6	UART2	
7	Reserved	
8	UART4	
9	UART5	
10	ISO7816	
11	Reserved	
12	Timer	
13	MISC	
14	MISC2	
15	PMU	
16	RTC	
17	ANA	
18	U32K 0	
19	U32K 1	
20	Reserved	
21	SPI	
31:22	Reserved	

26. CRYPT Controller

26.1. Introduction

The CRYPT controller is used to accelerate the ECC's sign and verify process speed. The major feature of CRYPT controller is the VLI (variable length integer) multiply, add, sub, and shift. It can achieve overall about 4 times faster than pure software process. Every encryption algorithm use VLI can use this hardware to accelerate the process speed. The CRYPT controller can access internal SRAM directly without affect the M0's access, it can also generate the carry or borrow bit automatically.

26.2. Feature

--Support VLI from 32 bits to 512 bits.

--VLI multiplier.

--VLI add and carry bit generation.

--VLI substrate and borrow bit generation.

--VLI right shift 1 bit.

--Internal SRAM direct access.

26.3. Block Diagram

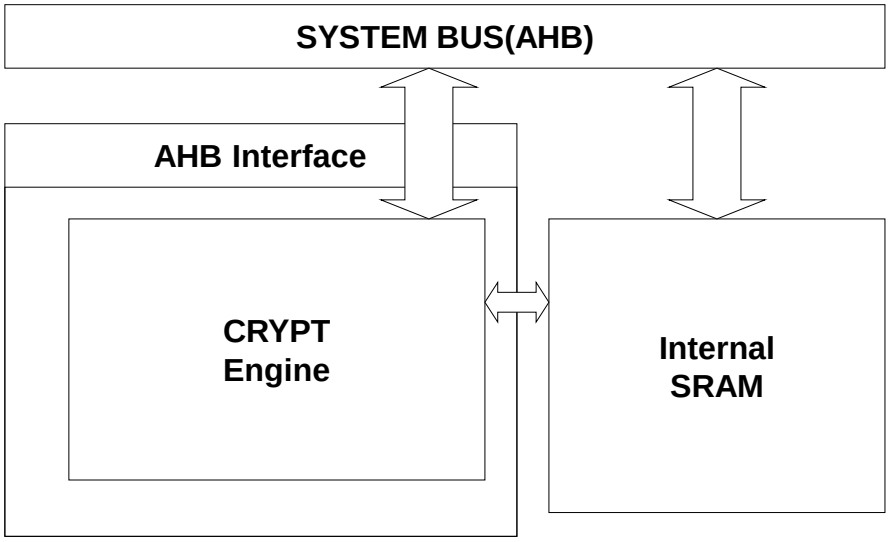


Figure 26-1Functional Block Diagram of CRYPT Controller

26.4. Register Location

Table 26-1 CRYPT Registers Map

Register Name	Offset	Type	Reset Value	Description
CRYPT_CTRL	0x0000	rw	0x0000_0000	CRYPT control register
CRYPT_PTRA	0x0004	rw	0x0000_0000	CRYPT pointer A
CRYPT_PTRB	0x0008	rw	0x0000_0000	CRYPT pointer B
CRYPT_PTRO	0x000C	rw	0x0000_0000	CRYPT pointer O
CRYPT_CARRY	0x0010	r	0x0000_0000	CRYPT carry/borrow bit register

26.5. Register Definition

26.5.1. CRYPT_CTRL Register

Table 26-2 CRYPT_CTRL Register Description

Bit	Name	Type	Description
31:16	Rsvd	-	Reserved.
15	NOSTOP	rw	This register is used to control if the CPU will be stop by CRYPT engine when the CRYPT engine is busy and CPU read or write CRYPT engine register. 0: Stop CPU when CRYPT engine is busy. 1: No stop CPU when CRYPT engine is busy. This register only affect the behavior when CPU access the CRYPT register, if CPU didn't access the crypt register, this bit has no effect.
14:12	Rsvd	-	Reserved.
11:8	LENGTH	rw	This bit is used to control the VLI length of current operation. Programmer can set this register together with write 1 to ACT bit, but should not change this register when ACT is 1. 0: 32 bits VLI 1: 64 bits VLI 2: 96 bits VLI …… 15: 512 bits VLI
7	Rsvd	-	Reserved.
6:4	MODE	rw	This register controls the operation mode of crypt engine. Programmer can set this register together with write 1 to ACT bit, but should not change this register when ACT is 1. 0: Multiply mode, *PTRO = *PTRA x *PTRB 1: Add mode, *PTRO = *PTRA + *PTRB 2: Sub mode, *PTRO = *PTRA - *PTRB 3: RSHIFT1 mode, *PTRO = (*PTRA>>1) 4~7: Reserved.
3:1	Rsvd	-	Reserved.

0	ACT	rw	Write 1 to this bit will start an operation specified in the MODE register. And this bit will be cleared automatically after the operation is done. Write 0 to this bit has no effect.

26.5.2. CRYPT_PTRA Register

Table 26-3 CRYPT_PTRA Register Description

Bit	Name	Type	Description
31:15	Rsvd	-	Reserved.
14:0	PTRA	rw	This is the PTRA register of CRYPT controller. The value here defines an address in the SRAM (byte unit). The data in this address will be read out to do the CRYPT calculation. Since the CRYPT control only support 32 bits process, the PTRA[1:0] should be 0 for all the time.

26.5.3. CRYPT_PTRB Register

Table 26-4 CRYPT_PTRB Register Description

Bit	Name	Type	Description
31:15	Rsvd	-	Reserved.
14:0	PTRB	rw	This is the PTRB register of CRYPT controller. The value here defines an address in the SRAM (byte unit). The data in this address will be read out to do the CRYPT calculation. Since the CRYPT control only support 32 bits process, the PTRB[1:0] should be 0 for all the time.

26.5.4. CRYPT_PTRO Register

Table 26-5 CRYPT_PTRO Register Description

Bit	Name	Type	Description
31:15	Rsvd	-	Reserved.
14:0	PTRO	rw	This is the PTRO register of CRYPT controller. The value here defines an address in the SRAM (byte unit). The CRYPT engine will write calculation result into this address. Since the CRYPT control only support 32 bits process, the PTRO[1:0] should be 0 for all the time.

26.5.5. CRYPT_CARRY Register

Table 26-6 CRYPT_CARRY Register Description

Bit	Name	Type	Description
31:1	Rsvd	-	Reserved.
0	CARRY	r	This bit represent the carry bit after add operation is done. The bit represent borrow bit after sub operation is done.

			Programmer can read this register immediately after the ACT bit is clear to 0.

26.6. Application Note

26.6.1. Data Format

The VLI is a positive integer with 32~512 bits. So all the operations here are unsigned processes. The following table shows the data sequence in the SRAM.

Address	Data
PTR + 0	VLI[31:0]
PTR + 4	VLI[63:32]
PTR + 8	VLI[95:64]
PTR + 12	VLI[127:96]
……	……
PTR + 60	VLI[511:480]

When different kind of LENGTH mode is selected, only the selected range of VLI will be used as input data. The following table shows the valid VLI bits under different LENGTH setting.

LENGTH	Data
0	VLI[31:0]
1	VLI[63:0]
2	VLI[95:0]
3	VLI[127:0]
……	……
15	VLI[511:0]

26.6.2. Operation Detail

For each operation, they will have different behavior on many ways, like the process cycles and the output width. The following tables shows detail of each mode.

	MULT	ADD	SUB	RSHIFT1
Operation	*PTRO = *PTRA x *PTRB	*PTRO = *PTRA + *PTRB	*PTRO = *PTRA - *PTRB	*PTRO = (*PTRA>>1)
Output length	2*input length	input length	input length	input length
CARRY bit	X	0: Output not overflow. 1: Output overflow	0: *PTRA > *PTRB 1: *PTRA < *PTRB	X
LENGTH	**Operation Cycles**			
0	8	6	6	6
1	17	8	8	8
2	32	12	12	10
3	53	14	14	12
4	80	18	18	14
5	113	20	20	16

6	152	24	24	18
7	197	26	26	20
8	248	30	30	22
9	305	32	32	24
10	368	36	36	26
11	437	38	38	28
12	512	42	42	30
13	593	44	44	32
14	680	48	48	34
15	773	50	50	36

By default, during the operation cycle, if the CPU accesses any of the register of CRYPT engine, the CPU will be halted until the operation is done. This is to prevent the configuration change during the operation. So if there is any high priority task in the system, it may block until the CPU is released by CRYPT engine. Set NOSTOP bit in the CRYPT_CTRL register to prevent this kind of situation. Under this condition, programmer should take care not to change the CRYPT configuration during the operation busy time.

Since the CRYPT only supports operations in the SRAM, when one of the input is not in the SRAM (ex. In FLASH or ROM), it is necessary to copy it into SRAM before do any operation.

27. Debug Features

V94XX(A) uses the Cortex-M0 core, which contains the hardware debug module.

27.1. Feature

The Cortex-M0 processor supports a number of useful debug features:

--Halting, resuming, and single stepping of program execution

--Access to processor core registers and special registers

--Hardware breakpoints (up to four comparators)

--Software breakpoints (BKPT instruction)

--Data watch points (up to two comparators)

--On-the-fly memory access (system memory can be accessed without stopping the processor)

--PC sampling for basic profiling

--Support of serial wire debug (SWD) protocol

27.2. SWD Port

Table 27-1 Special Function of SW Port

MODE	Function 1	Function 2
Debug (PIN MODE is L)	SWCLK	SWDIO
Normal (PIN MODE is H)	LCDSEG54/IOA0	LCDSEG53/IOA1

28. Cortex-M0 Core Brief Description

The ARM Cortex-M0 processor is designed to meet the needs of modern ultra-low-power microcontroller units (MCUs) and mixed-signal devices. The ARM Cortex-M0 processor is as small as an 8-bit or 16-bit processor, but it is a full 32-bit processor that incorporates advanced technologies with many compelling benefits over 8-bit or 16-bit devices. The ARM Cortex-M0 processor can achieve high Energy Efficiency and Code Density.

28.1. CMSIS Function Specification

Table 28-1 CMSIS Function

function	specification
void NVIC_EnableIRQ(IRQn_Type IRQn);	Enable an interrupt. This function does not apply to system exceptions.
void NVIC_DisableIRQ(IRQn_Type IRQn);	Disable an interrupt. This function does not apply to system exceptions.
void VIC_SetPendingIRQ(IRQn_Type IRQn);	Set the pending status of an interrupt. This function does not apply to system exceptions.
void NVIC_ClearPendingIRQ(IRQn_Type IRQn);	Clear the pending status of an interrupt. This function does not apply to system exceptions.
uint32_t NVIC_GetPendingIRQ(IRQn_Type IRQn);	Obtain the interrupt pending status of an interrupt. This function does not apply to system exceptions.
void NVIC_SetPriority(IRQn_Type IRQn,uint32_t priority);	Set up the priority level of an interrupt or system exception. The priority level value is automatically shifted to the implemented bits in the priority level register.
uint32_t NVIC_GetPriority(IRQn_TypeIRQn);	Obtain the priority level of an interrupt or system exception. The priority level is automatically shifted to remove unimplemented bits in the priority level values.
void __enable_irq(void);	Clear PRIMASK. Enable interrupts and system exceptions.
void __disable_irq(void);	Set PRIMASK. Disable all interrupts including system exceptions (apart from hard fault and NMI).
uint32_t SysTick_Config(uint32_t ticks);	Initialize and start the SysTick counter and its interrupt; this function programs the SysTick to generate SysTick except ionfor every “ticks” number of core clock cycles.
void NVIC_SystemReset(void);	M0-soft reset.
SCB->SCR |= SCB_SCR_SLEEPDEEP_Msk; void __WFI(void);	Wait for interrupt (enter sleep mode).
SCB->SCR &= (uint32_t)~((uint32_t)SCB_SCR_SLEEPDEEP_Msk);	Wait for interrupt (enter idle mode).

void __WFI(void);	

29. Electric Energy Metering

The V94XX(A) contains an electric energy metering module which supports the total-wave and fundamental-wave of various modes and supports various power grids to monitor events. Furthermore, the waveform data can be transmitted via Px by SPI protocol, or storage locally through the waveform buffer.

Note: All register read/write accesses of the electric energy metering module need to be realized by calling the function library provided by the company.

29.1. Metering Features

- 3 independent oversampling Σ/Δ ADCs: one of the ADC (channel A) can measure voltage, the other ADC with multifunction measure current or temperature etc.
- Highly Metering Accurate:
  - Supports the requirements of IEC 62053-21:2020/ IEC 62053-22:2020 and IEC 62053-23:2020.
  - Less than 0.1% error in active energy metering over a dynamic range of 5000:1
  - Less than 0.2% error in reactive energy metering over a dynamic range of 5000:1
  - Less than 0.5% error in current/voltage RMS over a dynamic range of 5000:1.
- Supports various measurements:
  - DC components of voltage and current signal
  - Total /fundamental instantaneous/average current/voltage RMS
  - Total instantaneous/average active /reactive/apparent power
  - 10 or 12 cycles of total RMS
  - Fundamental instantaneous/average active /reactive/apparent power
  - active/reactive energy, active/reactive/apparent power, Irms, constant value, and fundamental wave are selectable
  - Line frequency and phase
- DC signals measurement
- Software calibration
- Accelerating calibration when weak current is applied.

- Supports detection for over-current, over-voltage, under-current, under-voltage, voltage dip, and voltage swell
- Supports waveform buffer and waveform output
- Current input: current shunt resistor, CT, Hall cell, and TMR supportive

29.2. Functional Block Diagram

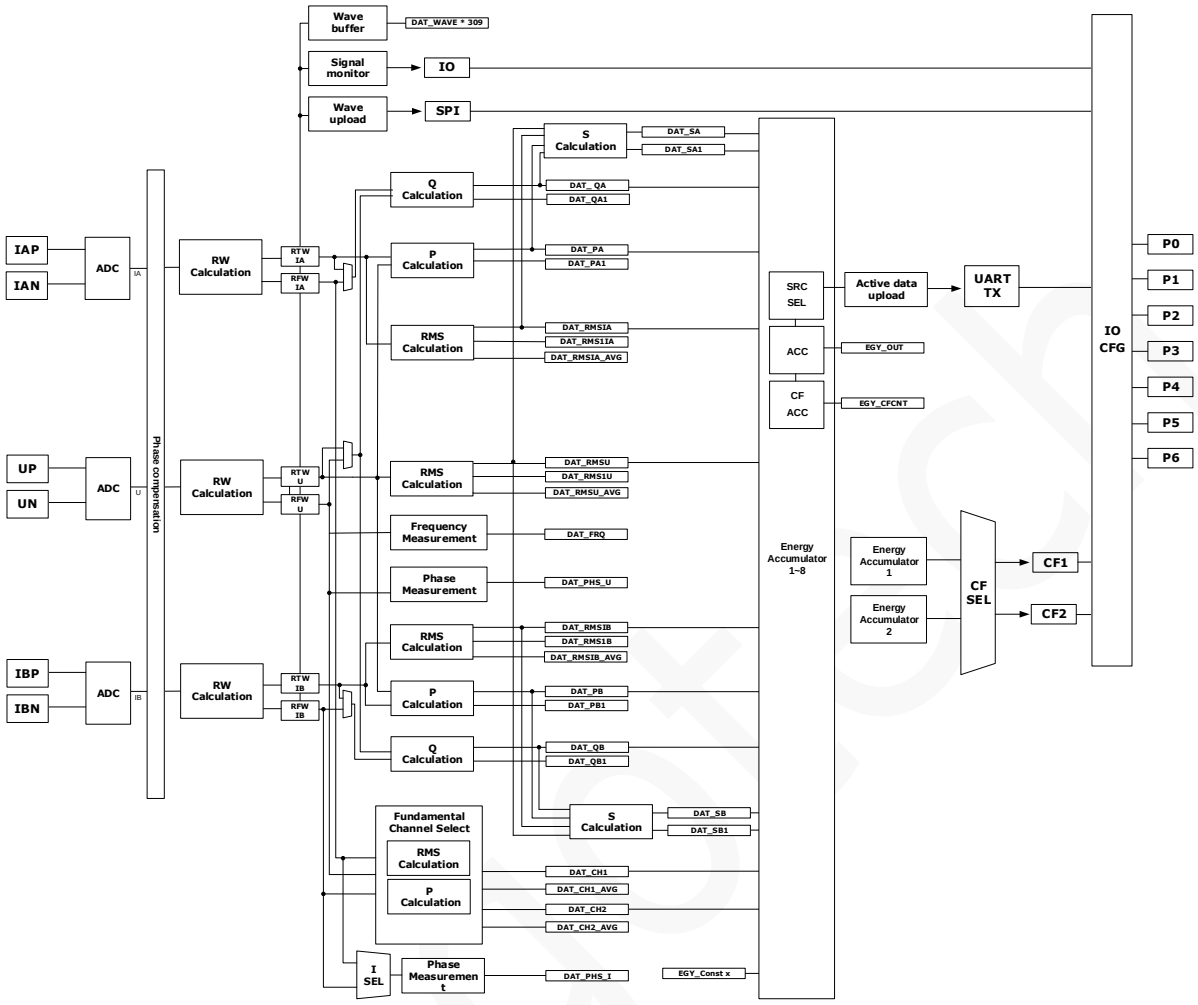


Figure 29-1 Electric energy metering functional block diagram

29.3. Registers

When POR reset occurs and RSTN reset is input outside the chip, all registers are reset to the default values. All "default values" in the following table are hexadecimal values.

Note: All register read/write accesses in this table need to be implemented by calling the function library provided by the company.
When reading and writing Class I register, the maximum speed can be 1/4 of the system clock; When reading and writing Class II registers, the maximum speed is 1/16 of the system clock.

The address range of Class II registers is 0x11~0x38, 0x43~0x54, 0x68, 0x69. The other addresses are class I register addresses.

29.3.1. Registers List

Note: All register read/write accesses in this table need to be implemented by calling the function library provided by the company.

Table 29-1 Register list

Register	Type	Address	Description	Default
EM_ANA_CTRL0	R/W	0x00	Analog Control Register 0.	0x00000000
EM_ANA_CTRL1	R/W	0X01	Analog Control Register 1.	0x00000000
EM_CTRL0	R/W	0x02	Metering Control Register 0.	0x00000000
EM_CTRL1	R/W	0x03	Metering Control Register 1.	0x00000000
EM_EGY_CTRL0	R/W	0x04	Energy Accumulator Control Register 0.	0x00000000
EM_EGY_CTRL1	R/W	0x05	Energy Accumulator Control Register 1.	0x00000000
EM_FD_CTRL	R/W	0x06	Fast Detection Control Register.	0x00000000
EM_WAVE_CTRL	R/W	0x07	Wave Upload And Buffer Control Register.	0x00000000
EM_DAT_PA	R	0x08	Instantaneous Active Power of channel A.	--
EM_DAT_QA	R	0x09	Instantaneous Reactive Power of channel A.	--
EM_DAT_SA	R	0x0A	Instantaneous Apparent Power of channel A.	--
EM_DAT_PB	R	0x0B	Instantaneous Active Power of channel B.	--
EM_DAT_QB	R	0x0C	Instantaneous Reactive Power of channel B.	--
EM_DAT_SB	R	0x0D	Instantaneous Apparent Power of channel B.	--
EM_DAT_RMS0UA	R	0x0E	Instantaneous RMS of Voltage.	--
EM_DAT_RMS0IA	R	0x0F	Instantaneous RMS of current A.	--
EM_DAT_RMS0IB	R	0x10	Instantaneous RMS of Current B.	--
EM_DAT_CH1	R	0x11	Instantaneous Value of Fundamental wave of Channel 1.	--
EM_DAT_CH2	R	0x12	Instantaneous Value of Fundamental wave of Channel 2.	--
EM_DAT_PA1	R	0x13	Average Active Power of Channel A.	--
EM_DAT_QA1	R	0x14	Average Reactive Power of Channel A.	--
EM_DAT_SA1	R	0x15	Average Apparent Power of Channel A.	--
EM_DAT_PB1	R	0x16	Average Active power of Channel B.	--
EM_DAT_QB1	R	0x17	Average Reactive power of Channel B.	--
EM_DAT_SB1	R	0x18	Average Apparent Power of Channel B.	--
EM_DAT_RMS1U	R	0x19	Average RMS of Voltage.	--
EM_DAT_RMS1IA	R	0x1A	Average RMS of Current A.	--
EM_DAT_RMS1IB	R	0x1B	Average RMS of Current B.	--
EM_DAT_CH1_AVG	R	0x1C	Average value of Fundamental wave of Channel 1.	--
EM_DAT_CH2_AVG	R	0x1D	Average value of Fundamental wave of Channel 2.	--
EM_DAT_RMSU_AVG	R	0x1E	Average RMS of Voltage for 10 or 12 cycles (chose by line frequency).	--
EM_DAT_RMSIA_AVG	R	0x1F	Average RMS of Current IA for 10 or 12 cycles (chose by line frequency).	--
EM_DAT_RMSIB_AVG	R	0x20	Average RMS of Current IB for 10 or 12 cycles (chose by line frequency).	--
EM_DAT_FRQ	R	0x21	Line Frequency.	--
EM_DAT_DCU	R	0x22	DC value of voltage channel.	--
EM_DAT_DCIA	R	0x23	DC value of current channel A.	--
EM_DAT_DCIB	R	0x24	DC value of Current channel B.	--
EM_CFG_CALI_PA	R/W	0x25	To set gain calibration for the active power A.	0x00000000

EM_CFG_DC_PA	R/W	0x26	To set offset calibration for the active power A.	0x00000000
EM_CFG_CALI_QA	R/W	0x27	To set gain calibration for Reactive power A.	0x00000000
EM_CFG_DC_QA	R/W	0x28	To set offset calibration for Reactive power A.	0x00000000
EM_CFG_CALI_PB	R/W	0x29	To set gain calibration for Active power B.	0x00000000
EM_CFG_DC_PB	R/W	0x2A	To set offset calibration for Active power B.	0x00000000
EM_CFG_CALI_QB	R/W	0x2B	To set gain calibration for Reactive power B.	0x00000000
EM_CFG_DC_QB	R/W	0x2C	To set offset calibration for Reactive power B.	0x00000000
EM_CFG_CALI_RMSU	R/W	0x2D	To set gain calibration for Voltage RMS.	0x00000000
EM_CFG_RMS_DCU	R/W	0x2E	To set offset calibration for Voltage RMS.	0x00000000
EM_CFG_CALI_RMSIA	R/W	0x2F	To set gain calibration for Current RMS A.	0x00000000
EM_CFG_RMS_DCIA	R/W	0x30	To set offset calibration for Current RMS A.	0x00000000
EM_CFG_CALI_RMSIB	R/W	0x31	To set gain calibration for Current RMS B.	0x00000000
EM_CFG_RMS_DCIB	R/W	0x32	To set offset calibration for Current RMS B.	0x00000000
EM_CFG_PHC	R/W	0x33	Phase Error Calibration Register. [10:0]= phase error calibration value for channel A [26:16]= phase error calibration value for channel B, where the range is from -766~767.	0x00000000
EM_CFG_DCU	R/W	0x34	To set the DC calibration for the voltage channel.	0x00000000
EM_CFG_DCIA	R/W	0x35	To set the DC calibration for the current channel A.	0x00000000
EM_CFG_DCIB	R/W	0x36	To set the DC calibration for the current channel B.	0x00000000
EM_CFG_BPF	R/W	0x37	Band-pass filter coefficient. Related to setting the EM_MODE by Bit[7:4] of metering control register 0 (0x02,EM_CTRL0). Setting 0x806764B6 at EM_MODE=0, 1, 2; Setting 0x80DD7A8C at EM_MODE=6,7; Setting 0x82B465F0 at EM_MODE=8. The frequency of other modes would be not supported to measure, so setting to 0x0.	0x00000000
EM_CFG_CKSUM	R/W	0x38	Configuration register for checksum.	0x00000000
EM_EGY_PROCTH	R/W	0x39	Anti-creep threshold for energy accumulator. When the accumulated value of the anti-creep energy accumulator over this threshold and the accumulated value of the high-speed energy accumulator under this threshold, the accumulated value of the high-speed energy accumulator will be cleared.	0x00000000
EM_EGY_PWRTH	R/W	0x3A	Accumulation threshold for energy accumulator. Because the energy accumulator was 46Bit, the accumulated value of the high-speed energy accumulator equals to this threshold*16384; the accumulated value of the low-speed energy accumulator equals to this value*4.	0x00000000

EM_EGY_CONST1	R/W	0x3B	Energy accumulator 1 accumulating constant.	0x00000000
EM_EGY_OUT1L	R/W	0x3C	Energy accumulator 1 accumulating lower bit.	0x00000000
EM_EGY_OUT1H	R/W	0x3D	Energy accumulator 1 accumulating higher bit. Effective for lower 14 bit.	0x00000000
EM_EGY_CFCNT1	R	0x3E	Energy accumulator 1 pulse counter.	0x00000000
EM_EGY_CONST2	R/W	0x3F	Energy accumulator 2 accumulating constant.	0x00000000
EM_EGY_OUT2L	R/W	0x40	Energy accumulator 2 accumulating lower bit.	0x00000000
EM_EGY_OUT2H	R/W	0x41	Energy accumulator 2 accumulating higher bit. Effective for lower 14 bit.	0x00000000
EM_EGY_CFCNT2	R	0x42	Energy accumulator 2 pulse counter.	0x00000000
EM_EGY_CONST3	R/W	0x43	Energy accumulator 3 accumulating constant.	0x00000000
EM_EGY_OUT3	R/W	0x44	Energy accumulator 3 accumulating value.	0x00000000
EM_EGY_CFCNT3	R	0x45	Energy accumulator 3 pulse counter.	0x00000000
EM_EGY_CONST4	R/W	0x46	Energy accumulator 4 accumulating constant.	0x00000000
EM_EGY_OUT4	R/W	0x47	Energy accumulator 4 accumulating value.	0x00000000
EM_EGY_CFCNT4	R	0x48	Energy accumulator 4 pulse counter.	0x00000000
EM_EGY_CONST5	R/W	0x49	Energy accumulator 5 accumulating constant.	0x00000000
EM_EGY_OUT5	R/W	0x4A	Energy accumulator 5 accumulating value.	0x00000000
EM_EGY_CFCNT5	R	0x4B	Energy accumulator 5 pulse counter.	0x00000000
EM_EGY_CONST6	R/W	0x4C	Energy accumulator 6 accumulating constant.	0x00000000
EM_EGY_OUT6	R/W	0x4D	Energy accumulator 6 accumulating value.	0x00000000
EM_EGY_CFCNT6	R	0x4E	Energy accumulator 6 pulse counter.	0x00000000
EM_EGY_CONST7	R/W	0x4F	Energy accumulator 7 accumulating constant.	0x00000000
EM_EGY_OUT7	R/W	0x50	Energy accumulator 7 accumulating value.	0x00000000
EM_EGY_CFCNT7	R	0x51	Energy accumulator 7 pulse counter.	0x00000000
EM_EGY_CONST8	R/W	0x52	Energy accumulator 8 accumulating constant.	0x00000000
EM_EGY_OUT8	R/W	0x53	Energy accumulator 8 accumulating value.	0x00000000
EM_EGY_CFCNT8	R	0x54	Energy accumulator 8 pulse counter.	0x00000000
EM_OV_THL	R/W	0x55	To set the lower threshold for the power-creep detection.	0x00000000
EM_OV_THH	R/W	0x56	To set the upper threshold for the power-creep detection.	0x00000000
EM_SWELL_THL	R/W	0x57	To set the lower threshold for the voltage swell.	0x00000000
EM_SWELL_THH	R/W	0x58	To set the upper threshold for the voltage dip.	0x00000000
EM_DIP_THL	R/W	0x59	To set the lower threshold for the voltage dip.	0x00000000
EM_DIP_THH	R/W	0x5A	To set the upper threshold for the voltage dip.	0x00000000
EM_FD_OVTH	R/W	0x5B	To set over-voltage threshold for fast detection. Bit width is 30bit.	0x00000000
EM_FD_LVTH	R/W	0x5C	To set under-voltage threshold for fast detection. Bit width is 30bit.	0x00000000
EM_FD_IA_OCTH	R/W	0x5D	To set over-current threshold in current channel A for fast detection. Bit width is 30bit.	0x00000000
EM_FD_IA_LCTH	R/W	0x5E	To set under-current threshold in current channel A for fast detection. Bit width is 30bit.	0x00000000
EM_FD_IB_OCTH	R/W	0x5F	To set over-current threshold in current channel B for fast detection. Bit width is 30bit.	0x00000000
EM_FD_IB_LCTH	R/W	0x60	To set under-current threshold in current	0x00000000

			channel B for fast detection. Bit width is 30bit.	
EM_PHS_STT	R/W	0x61	To control the phase measurement. Enable phase measurement once for writing operation.	--
EM_PHS_U	R	0x62	Voltage phase.	1
EM_PHS_UN	R	0x63	Voltage waveform data which before zero-crossing.	0
EM_PHS_UP	R	0x64	Voltage waveform data which after zero-crossing.	0x80000000
EM_PHS_I	R	0x65	Current phase.	1
EM_PHS_IN	R	0x66	Current waveform data which before zero-crossing.	0
EM_PHS_IP	R	0x67	Current waveform data which after zero-crossing.	0x80000000
-	R	0x68	Reserved	0
EM_DAT_WAVE	R	0x69	Waveform data reading. It can repeatable reading the address and obtain the overall waveform data. If there is no need to read all data, it would be reset the bit 31 of EM_WAVE_CTRL to read address.	0
EM_DAT_SWELL_CNT	R/C	0x6A	Voltage swell time records, half-wave as unit. Effective as 24bit. Writing any value into this address would be clear this counter to zero.	0
EM_DAT_DIP_CNT	R/C	0x6B	Voltage dip time records, half wave as unit. Effective as 24bit. Writing any value into this address would be clear this counter to zero.	0
EM_SYS_INTSTS	R/C	0x72	Interrupt status register.	--
EM_SYS_INTEN	R/W	0x73	Interrupt enable register.	0x00000000
EM_SYS_STS	R	0x74	System status register.	--
EM_SYS_MISC	R/W	0x75	System control register.	--
EM_SYS_IOCFGX0	R/W	0x7D	Output configuration register for P0, P1, P2 and P3.	0
EM_SYS_IOCFGX1	R/W	0x7E	Output configuration register for P4, P5 and P6.	0

29.3.2. Analog Control Registers

When power-on reset (POR), RSTN pin reset occurs, all analog control registers will be reset to the default value. The default value in the following tables of this section are in format of hexadecimal.

The address range of Analog Control Register is 0x00~0x01 which all is readable and writable. Also, all the metering control registers need to be configuration verification and self-checking.

29.3.2.1. EM_ANA_CTRL0 Register

Table 29-2 Analog Control Register 0 (0x00, EM_ANA_CTRL0)

0x00, R/W, Analog Control Register 0, EM_ANA_CTRL0			
Bit		**Default Value**	**Description**
31:12	Reserved	0	These bits must hold its default value for proper operation.
11	SHORT_I	0	Current IA channel ADC input short circuit. 0: short circuit 1: Normal
10	SHORT_V	0	Voltage U channel ADC input short circuit. 0: short circuit 1: Normal
9:8	IT	0	Simulates global bias current adjustment. 01：1 00：-33% 11：-66% 10：-75%
7:0	Reserved	-	To ensure the normal operation of the system, the default value must be written.

29.3.2.2. EM_ANA_CTRL1 Register

Table 29-3 Analog Control Register 1 (0x01, EM_ANA_CTRL1)

0x01, R/W, Analog Control Register 1, EM_ANA_CTRL1			
Bit		**Default Value**	**Description**
31:30	ADCKSEL[1:0]	0	The options of clock frequency divider rate for the ADC 00 corresponds to 819.2 KHz. 00: ×1 01: ×2 10: ×1/4 11: ×1/2
29:15	Reserved	0	These bits must hold its default value for proper operation.
14:12	GIB[2:0]	0	To adjust the gain of current ADC in the channel B. 000: 4 001: 1 010: 32 011: 16 100/101/110/111: prohibited GIB[2:0] is recommended set to 000 for proper operation.

0x01, R/W, Analog Control Register 1, EM_ANA_CTRL1			
Bit		**Default Value**	**Description**
11	GU	0	To adjust the gain of voltage ADC. 0: 8 1: 4 This bit must be set to 0 for proper operation.
10:8	GIA[2:0]	0	To adjust the gain of current ADC in the channel A. 000: 32 001: 16 010: 4 011: 1 100~111: prohibited GIA[2: 0] is recommended set to 000 for proper operation.
7	XRST_PD	0	The external input CTI clock enable. 0: enable 1: disable
6:5	Reserved	0	These bits must hold its default value for proper operation.
4:3	RESTL[1:0]	0	To roughly adjust the temperature coefficient of the Bandgap circuit. 00: 0 ppm 01: -58 ppm 10: +111 ppm 11: +56 ppm
2:0	REST[2:0]	0	To finely adjust the temperature coefficient of the Bandgap circuit. 000: 0 ppm 001: +7 ppm 010: +14 ppm 011: +28 ppm 100: -32 ppm 101: -21 ppm 110: -14 ppm 111: -7 ppm

29.3.3. System Control & Status Register

When power-on reset (POR), RSTN pin reset occurs, all system control registers will be reset to the default value. The default value in the following tables of this section are in format of hexadecimal.

29.3.3.1. EM_SYS_ INTSTS Register

Table 29-4 System Interrupt Register (0x72, EM_SYS_INTSTS)

0x72, System Interrupt Register, EM_SYS_INTSTS				
Bit		**R/W**	**Default value**	**Description**
31:30	-	-	-	Reserved.

0x72, System Interrupt Register, EM_SYS_INTSTS				
Bit		**R/W**	**Default value**	**Description**
29	EGY2OV	R/C	0	Flag bit for high-speed energy accumulator 2 overflow interrupt Read 0: high-speed energy accumulator overflow did not happen Read 1: high-speed energy accumulator overflow happened Write 0: no effects Write 1: clear the bit
28	EGY1OV	R/C	0	Flag bit for high-speed energy accumulator 1 overflow interrupt Read 0: high-speed energy accumulator overflow did not happen Read 1: high-speed energy accumulator overflow happened Write 0: no effects Write 1: clear the bit
27	UDIP	R/C	0	Flag bit for the voltage dip. Read 0: the voltage dip did not happen Read 1: the voltage dip happened Write 0: no effects Write 1: clear the bit
26	USWELL	R/C	0	Flag bit for the voltage swell. Read 0: the voltage swell did not happen Read 1: the voltage swell happened Write 0: no effects Write 1: clear the bit
25	IBLC	R/C	0	Flag bit for the IB under-current. Read 0: IB under-current did not happen Read 1: IB under-current happen Write 0: no effects Write 1: clear the bit
24	IBOC	R/C	0	Flag bit for the IB over-current. Read 0: IB over-current did not happen Read 1: IB over-current happened Write 0: no effects Write 1: clear the bit
23	IALC	R/C	0	Flag bit for the IA under-current. Read 0: IA under-current did not happen Read 1: IA under-current happened Write 0: no effects Write 1: clear the bit

0x72, System Interrupt Register, EM_SYS_INTSTS				
Bit		**R/W**	**Default value**	**Description**
22	IAOC	R/C	0	Flag bit for the IA over-current. Read 0: IA over-current did not happen Read 1: IA over-current happened Write 0: no effects Write 1: clear the bit
21	ULV	R/C	0	Flag bit for the channel U under-voltage. Read 0: channel U under-voltage did not happen Read 1: channel U under-voltage happened Write 0: no effects Write 1: clear the bit
20	UOV	R/C	0	Flag bit for the channel U over-voltage. Read 0: channel U over-voltage did not happen Read 1: channel U over-voltage happened Write 0: no effects Write 1: clear the bit
19:16	Reserved	-	-	-
15	WAVEOUT_FINISH	R/C	0	Flag bit for active waveform uploading finished. Read 0: active waveform uploading did not finish Read 1: active waveform uploading finished Write 0: no effects Write 1: clear the bit
14	CKERR	R/C		Flag bit for checksum error. Checksum from correct to error, it would be interrupted. Read 0: checksum error did not happen Read 1: checksum error happened Write 0: no effects Write 1: clear the bit
13	HSE_FAIL	R/C		6.5 MHz clock of EM status. Read 0: clock error did not happen Read 1: CTI external input clock error has happened Write 0: no effects Write 1: clear the bit
12	PMREF_ERR	R/C		Flag bit for EM reference error Read 0: EM reference error did not happen Read 1: EM reference error happened Write 0: no effects Write 1: clear the bit
11	BIST_ERR	R/C		Flag bit for EM RAM BIST error Read 0: BIST error did not happen Read 1: BIST error happened Write 0: no effects Write 1: clear the bit

0x72, System Interrupt Register, EM_SYS_INTSTS				
Bit		**R/W**	**Default value**	**Description**
10	ISIGN	R/C		Flag bit for current zero-crossing, it could to select the channel IA or IB by bit20 of metering control register (Table 29-12 Metering Control Register 1 (0x03, EM_CTRL1)), and to select the direction of zero-crossing by bit19~bit18 of metering control register (0x03,EM_CTRL1). Read 0: current zero-crossing did not happen Read 1: current zero-crossing happened Write 0: no effects Write 1: clear the bit
9	USIGN	R/C		Flag bit for voltage zero-crossing, it could to select the direction of zero-crossing by bit19~bit18 of EM_CTRL1 Read 0: voltage zero-crossing did not happen Read 1: voltage zero-crossing happened Write 0: no effects Write 1: clear the bit
8	WAVE_OVERFLOW	R/C	0	Flag bit for waveform storage overflow. Read 0: waveform storage did not overflow Read 1: waveform storage already overflowed Write 0: no effects Write 1: clear the bit
7	WAVE_STORE	R/C	0	Flag bit for waveform storage status. Read 0: waveform storage did not finish Read 1: waveform storage already finished Write 0: no effects Write 1: clear the bit
6	WAVE_UPD	R/C	0	Flag bit for waveform updating. Read 0: waveform data did not update Read 1: waveform data updated Write 0: no effects Write 1: clear the bit
5	CURRMS_UPD	R/C	0	Flag bit for instantaneous RMS data updating. Read 0: instantaneous RMS data did not update Read 1: instantaneous RMS data updated Write 0: no effects Write 1: clear the bit
4	AVGRMS_UPD	R/C	0	Flag bit for average RMS data updating. Read 0: average RMS data did not update Read 1: average RMS data updated Write 0: no effects Write 1: clear the bit

0x72, System Interrupt Register, EM_SYS_INTSTS				
Bit		**R/W**	**Default value**	**Description**
3	CURPOWER_UPD	R/C	0	Flag bit for instantaneous power data updating. Read 0: instantaneous power data did not update Read 1: instantaneous power data updated Write 0: no effects Write 1: clear the bit
2	AVGPOWER_UPD	R/C	0	Flag bit for average power data updating. Read 0: average power data did not update Read 1: average power data updated Write 0: no effects Write 1: clear the bit
1	INTVDDPDN	R/C	0	Flag bit for power down event. When the power input (VDD) is lower than 2.65V (±6%), it would be triggered. Read 0: power down did not happen Read 1: power down happened Write 0: no effects Write 1: clear the bit
0	INTUPHSDONE	R/C	0	Flag bit for Phase measurement finished. This bit will clear automatically when starts to phase measurement. Read 0: phase measurement did not finish Read 1: phase measurement already finished Write 0: no effects Write 1: clear the bit

29.3.3.2. EM_SYS_INTEN Register

Table 29-5 System Interrupt Enable Register (0x73, EM_SYS_INTEN)

0x73, System Interrupt Enable Register, EM_SYS_INTEN				
Bit		**R/W**	**Default Value**	**Description**
31:30	Reserved		0	These bits must hold its default value for proper operation.
29	EGY2OV	R/W	0	Interrupt for high-speed energy accumulator 2 overflow 0: disable interrupt 1: enable interrupt
28	EGY1OV	R/W	0	Interrupt for high-speed energy accumulator 1 overflow 0: disable interrupt 1: enable interrupt
27	UDIP	R/W	0	Interrupt for the voltage dip. 0: disable interrupt 1: enable interrupt

0x73, System Interrupt Enable Register, EM_SYS_INTEN				
Bit		**R/W**	**Default Value**	**Description**
26	USWELL	R/W	0	Interrupt for voltage swell. 0: disable interrupt 1: enable interrupt
25	IBLC	R/W	0	Interrupt for IB under-current. 0: disable interrupt 1: enable interrupt
24	IBOC	R/W	0	Interrupt for IB over-current. 0: disable interrupt 1: enable interrupt
23	IALC	R/W	0	Interrupt for IA under-current. 0: disable interrupt 1: enable interrupt
22	IAOC	R/W	0	Interrupt for IA over-current. 0: disable interrupt 1: enable interrupt
21	ULV	R/W	0	Interrupt for channel U under-voltage. 0: disable interrupt 1: enable interrupt
20	UOV	R/W	0	Interrupt for channel U over-voltage. 0: disable interrupt 1: enable interrupt
19:16	Reserved			These bits must hold its default value for proper operation.
15	WAVEOUT_FINISH	R/W	0	Waveform uploading finished. 0: disable interrupt 1: enable interrupt
14	CKERR	R/W	0	Interrupt for checksum error. 0: disable interrupt 1: enable interrupt
13	HSE_FAIL	R/W	0	Interrupt for 6.5M clock of EM error. 0: disable interrupt 1: enable interrupt
12	PMREF_ERR	R/W	0	Interrupt for EM reference error. 0: disable interrupt 1: enable interrupt
11	BIST_ERR	R/W	0	Interrupt for EM RAM BIST error. 0: disable interrupt 1: enable interrupt
10	ISIGN	R/W	0	Interrupt for the current zero-crossing. 0: disable interrupt 1: enable interrupt
9	USIGN	R/W	0	Interrupt for the voltage zero-crossing. 0: disable interrupt 1: enable interrupt

0x73, System Interrupt Enable Register, EM_SYS_INTEN				
Bit		**R/W**	**Default Value**	**Description**
8	WAVE_OVERFLOW	R/W	0	Interrupt for the Waveform storage overflow. 0: disable interrupt 1: enable interrupt
7	WAVE_STORE	R/W	0	Interrupt for the Waveform storage status. 0: disable interrupt 1: enable interrupt
6	WAVE_UPD	R/W	0	Interrupt for the Waveform data updating. 0: disable interrupt 1: enable interrupt
5	CURRMS_UPD	R/W	0	Interrupt for the Instantaneous RMS data updating. 0: disable interrupt 1: enable interrupt
4	AVGRMS_UPD	R/W	0	Interrupt for the average RMS data updating. 0: disable interrupt 1: enable interrupt
3	CURPOWER_UPD	R/W	0	Interrupt for the Instantaneous power data updating. 0: disable interrupt 1: enable interrupt
2	AVGPOWER_UPD	R/W	0	Interrupt for the Average power data updating. 0: disable interrupt 1: enable interrupt
1	INTPDN	R/W	0	Interrupt for the Power down. 0: disable interrupt 1: enable interrupt
0	INTUPHSDONE	R/W	0	Interrupt for the Phase measurement finished. 0: disable interrupt 1: enable interrupt

29.3.3.3. EM_SYS_STS Register

Table 29-6 System Status Register (0x74, EM_SYS_STS)

0x74, System Status Register, EM_SYS_STS				
Bit		**R/W**	**Default Value**	**Description**
31	-	-	-	Reserved
30	UDIP	R	0	Status bit for the voltage dip. 0: not happened 1: happened
29	USWELL	R	0	Status bit for voltage swell. 0: not happened 1: happened

0x74, System Status Register, EM_SYS_STS				
Bit		**R/W**	**Default Value**	**Description**
28	IBLC	R	0	Status bit for IB under-current. 0: not happened 1: happened
27	IBOC	R	0	Status bit for IB over-current. 0: not happened 1: happened
26	IALC	R	0	Status bit for IA under-current. 0: not happened 1: happened
25	IAOC	R	0	Status bit for IA over-current. 0: not happened 1: happened
24	ULV	R	0	Status bit for channel U under-voltage. 0: not happened 1: happened
23	UOV	R	0	Status bit for channel U over-voltage. 0: not happened 1: happened
22:20	RST_SOURCE	R	-	Status bit for reset. 1: power on reset 2: external reset Others are reserved.
19	CRP_OUT2	R	0	Status bit for energy-creep detection for energy accumulator 2. 0: start 1: energy-creep
18	CRP_OUT1	R	0	Status bit for energy-creep detection for energy accumulator 1. 0: start 1: energy-creep
17	SBCREEP	R	-	Status bit for no-load detection for apparent power Channel B. 0: start 1: power-creep
16	QBCREEP	R	-	Status bit for power-creep detection for reactive power Channel B. 0: start 1: power-creep
15	PBCREEP	R	-	Status bit for power-creep detection for active power Channel B. 0: start 1: power-creep

0x74, System Status Register, EM_SYS_STS				
Bit		**R/W**	**Default Value**	**Description**
14	SACREEP	R	-	Status bit for power-creep detection for apparent power Channel A. 0: start 1: power-creep
13	QACREEP	R	-	Status bit for power-creep detection for reactive power Channel A. 0: start 1: power-creep
12	PACREEP	R	-	Status bit for power-creep detection for active power Channel A. 0: start 1: power-creep
11	QBSIGN	R	0	Sign bit for reactive power Channel B. Under the power-creep detection, no refresh the flag bit. 0: positive 1: negative
10	PBSIGN	R	0	Sign bit for active power Channel B. Under the power-creep detection, no refresh the flag bit. 0: positive 1: negative
9	QASIGN	R	0	Sign bit for reactive power Channel A. Under the power-creep detection, no refresh the flag bit. 0: positive 1: negative
8	PASIGN	R	0	Sign bit for active power Channel A. Under the power-creep detection, no refresh the flag bit. 0: positive 1: negative
7	-	-	-	Reserved
6	HSEFAIL	R	0	Status bit for 6.5M clock of EM. 0: normal 1: abnormal
5	BISTERR	R	0	Status bit for EM SRAM BIST. 0: SRAM BIST normal 1: SRAM BIST error
4	RAMINITIAL		0	Status bit for EM RAM initialization finished 0: failed 1: finished
3	PHSDONE		0	Status bit for Phase measurement finished 0: failed 1: finished

0x74, System Status Register, EM_SYS_STS				
Bit		**R/W**	**Default Value**	**Description**
2	VDDPDN	R	0	Status bit for power down. When the power input (VDD) is lower than 2.65V (±6%), power down event happens. 0: VDD >= 2.65V (±6%) 1: VDD < 2.65V (±6%)
1	PMREFLK	R	0	Status bit for the reference of EM whether electric leaking. 0: EM reference circuit normal 1: EM reference circuit decrease is greater than 2.5%.
0	CHECKSUM	R	1	Status bit for Checksum. Checksum calculation address range: 0x0~0x7, 0x25~0x3A, 0x55~0x60 0: checksum correct 1: checksum incorrect

29.3.3.4. EM_SYS_MISC Register

Table 29-7 System Control Register (0x75, EM_SYS_MISC)

0x75, system Control Register, EM_SYS_MISC				
Bit		**R/W**	**Default Value**	**Description**
31:25	Reserved	R	0	These bits, must hold its default value for proper operation.
24:16	WAVE_STORE_CNT	R	0	Count value for Waveform storage.
15:6	Reserved		0	These bits must hold its default value for proper operation.
5	BIST_EM_EGY_EN	R/W	0	RAM self-test error occurs, the energy accumulator and CF output are forcibly closed. 0: enable 1: disable The control bits for the energy accumulator and CF counter (Bit[15] and Bit[7:6]) in EM_CTRL1 register will not change. Although the EM_CTRL1 register value has not changed, the energy accumulator and CF output functions will not be restored automatically and need to be opened manually by the user after the state returns to normal.

0x75, system Control Register, EM_SYS_MISC				
Bit		**R/W**	**Default Value**	**Description**
4	CK_EM_EGY_EN	R/W	0	When checksum has error, force the energy accumulator and CF output to disable. 0: enable 1: disable The control bits for the energy accumulator and CF counter (Bit[15] and Bit[7:6]) in EM_CTRL1 register will not change. Although the EM_CTRL1 register value has not changed, the energy accumulator and CF output functions will not be restored automatically and need to be opened manually by the user after the state returns to normal.
3	PD_EM_EGY_EN	R/W	0	When power-down, force the energy accumulator and CF output to disable. 0: enable 1: disable The control bits for the energy accumulator and CF counter (Bit[15] and Bit[7:6]) in EM_CTRL1 register will not change. Although the EM_CTRL1 register value has not changed, the energy accumulator and CF output functions will not be restored automatically and need to be opened manually by the user after the state returns to normal.
2	INTPOL	R/W	0	Reverse output on Interrupted pin. 0: interrupt pin triggered by high-level voltage, and default is low-level voltage. 1: interrupt pin triggered by low-level voltage, and default is high-level voltage.
1:0	Reserved		0	These bits must hold its default value for proper operation.

29.3.3.5. EM_SYS_IOCFGXX Register

Table 29-8 IO Configuration Register 0 (0x7D, EM_SYS_IOCFGX0)

0x7D, IO Configuration Register 0, EM_SYS_IOCFGX0				
Bit		**R/W**	**Default Value**	**Description**
31:24	P3CFG	R/W	0	Configuration as the same as P2CFG.

0x7D, IO Configuration Register 0, EM_SYS_IOCFGX0				
Bit		**R/W**	**Default Value**	**Description**
23:16	P2CFG	R/W	0	Bit[7:6]: 00: as shown in the Table 29-9, it can be configured the different combination interruption. 10: CF1 output. Bit[5:0] can be configured arbitrary value. 01: CF2 output. Bit[5:0] can be configured arbitrary value. 11: Actively energy accumulation data uploads. Bit[5:0] can be configured arbitrary value.
15:0	-	R/W	0	Reserved

Table 29-9 PxCFG Bit[5:0] Description

Bit[5:3]	**Bit[2:0]**	**Description**
0	0	High impedance.
0	1	Current zero-crossing interruption.
0	2	Voltage zero-crossing interruption.
0	3	Current zero-crossing interruption.
0	4	Voltage zero-crossing interruption.
0	5	High-speed energy accumulator 1 overflow interrupt
0	6	High-speed energy accumulator 2 overflow interrupt
0	7	1st type interruption.
1	0	Waveform refresh interruption.
1	1	Instantaneous RMS refresh interruption.
1	2	Average RMS refresh interruption.
1	3	Instantaneous power refresh interruption.
1	4	Average power refresh interruption.
1	5	Waveform storage finish interruption.
1	6	Waveform storage address overflow interruption.
1	7	Waveform data upload finish interruption.
2	0	IB channel under-current interruption.
2	1	IB channel over-current interruption.
2	2	IA channel under-current interruption.
2	3	IA channel over-current interruption.
2	4	Voltage Channel under-voltage interruption.
2	5	Voltage Channel over-voltage interruption.
2	6	Voltage dip interruption.
2	7	Voltage swell interruption.
3	0	EM Reference error.
3	1	EM clock error.
3	2	Reserved
3	3	Reserved
3	4	Power-down interruption.
3	5	Parameter self-checking error interruption.
3	6	Phase test finish interruption.
3	7	EM RAM self-checking error.
4	0	1st type interruption.

4	1	2nd type interruption.
4	2	3rd type interruption.
4	others	4th type interruption.
5	0	3rd type interruption.
5	1	1st and 2nd type interruption.
5	2	1st and 3rd type interruption.
5	3	1st and 4th type interruption.
5	4	2nd and 3rd type interruption.
5	5	2nd and 4th type interruption.
5	6	3rd and 4th type interruption.
5	7	All interruption.
6	0	1st, 2nd and 3rd type interruption.
6	1	1st, 2nd and 4th type interruption.
6	2	1st, 3rd and 4th type interruption.
6	3	2nd, 3rd and 4th type interruption.
6	others	All interruption.
7	1	Waveform updating for chip select of SPI, SPI_CSN.
7	2	Waveform updating for SPI clock, SPI_CLK.
7	4	Waveform updating for SPI data, SPI_MOSI.
7	others	Prohibited output.

While the IO interface is not configured (i.e. all zero), output is high impedance.

While the IO interface is not configured (i.e. all zero), output is high impedance.

- 1st type interruption: current zero-crossing interruption, voltage zero-crossing interruption, high-speed energy accumulator 1/2 overflow interruption.
- 2nd type interruption: waveform refreshes interruption, instantaneous RMS refresh interruption, average RMS refreshes interruption, instantaneous power value refresh interruption, average power value refreshes interruption, waveform storage finish interruption, waveform storage overflow interruption and waveform data upload finished interruption.
- 3rd type interruption: IB channel under-current interruption, IB channel over-current interruption, IA channel under-current interruption, IA channel over-current interruption, voltage channel under-voltage interruption, voltage channel over-voltage interruption, voltage dip interruption and voltage swell interruption.
- 4th type interruption: parameters self-checking error interruption, phase measurement finished interruption, power-down interruption, EM reference error interruption, EM clock error interruption and EM RAM self-checking error interruption.

Table 29-10 IO Configuration Register 1 (0x7E, EM_SYS_IOCFGX1)

0x7E, IO Configuration Register1, EM_SYS_IOCFGX1				
Bit		**R/W**	**Default Value**	**Description**
31:24	Reserved		0	These bits must hold its default value for proper operation.
23:16	P6CFG	R/W	0	Configuration as the same as P2CFG.

0x7E, IO Configuration Register1, EM_SYS_IOCFGX1				
Bit		**R/W**	**Default Value**	**Description**
15:8	EMINT1CFG	R/W	0	Configuration as the same as P2CFG.
7:0	EMINT0CFG	R/W	0	Configuration as the same as P2CFG.

29.3.4. Metering Control Registers

When power-on reset (POR), RSTN pin reset occurs, all metering control registers will be reset to the default value. The default value in the following tables of this section are in format of hexadecimal.

All the metering control registers need to be configuration verification and self-checking.

29.3.4.1. EM_CTRL0 Register

Table 29-11 Metering Control Register 0 (0x02, EM_CTRL0)

0x02, R/W, Metering Control Register 0, EM_CTRL0				
Bit		**R/W**	**Default Value**	**Description**
31	CUREM_DAT_RATE	R/W	0	Double refresh time for Instantaneous power value and RMS value. 0: refresh time for instantaneous power value is 20ms and instantaneous RMS value is 10ms. 1: refresh time for instantaneous power value is 40ms and instantaneous RMS value is 20ms.
30	Reserved		0	The bit must hold its default value for proper operation.
29:28	FRQ_SEL	R/W	0	Source comes from the register value of EM_DAT_FRQ. 00: accumulation value for line frequency test value of 16 cycles (the default update time is 320ms) 01: line frequency test value of 1 cycle (the default update time is 20ms) 10: line frequency test value of 64 cycles (the default update time is 1280ms) 11: Reserved
27	DC_METER_MODE	R/W	0	To enable the DC metering mode. 0: disable 1: enable
26:25	Rsvd	-	0	The bit must hold its default value for proper operation.
24	S_MODE	R/W	0	Source select for Apparent power calculation. 0: by RMS value 1: by power value

0x02, R/W, Metering Control Register 0, EM_CTRL0				
Bit		**R/W**	**Default Value**	**Description**
23:20	CFG_CHANNEL	R/W	0	Fundamental Channel selectable. 0: channel 1, fundamental active power A; channel 2, fundamental active power B 1: channel 1, fundamental active power A; channel 2, fundamental voltage RMS 2: channel 1, fundamental active power A; channel 2, fundamental current RMS A 3: channel 1, fundamental active power A; channel 2, fundamental current RMS B 4: channel 1, fundamental active power B, channel 2, fundamental voltage RMS 5: channel 1, fundamental active power B; channel 2, fundamental current RMS A 6: channel 1, fundamental active power B; channel 2, fundamental current RMS B 7: channel 1, fundamental voltage RMS; channel 2, fundamental current RMS A 8: channel 1, fundamental voltage RMS, channel 2, fundamental current RMS B 9: channel 1, fundamental current RMS A; channel 2, fundamental current RMS B 10~15: the same as configured 0
19	QB_MODE	R/W	0	To select mode for Reactive power B. 0: total wave, reactive power 1: fundamental wave, reactive power
18	QA_MODE	R/W	0	To select mode for Reactive power A. 0: total wave, reactive power 1: fundamental wave, reactive power
17	PQ_HPFSEL	R/W	0	Calculate the total power whether pass high-pass filter. 0: pass 1: not pass
16	FUND_HPFSEL	R/W	0	Calculate the fundamental data whether pass high-pass filter: 0: pass 1: not pass
15	RMSU_HPFSEL	R/W	0	Calculate the total voltage RMS data whether pass high-pass filter: 0: pass 1: not pass
14	RMSIA_HPFSEL	R/W	0	Calculate the total current IA RMS data whether pass high-pass filter: 0: pass 1: not pass

0x02, R/W, Metering Control Register 0, EM_CTRL0				
Bit		**R/W**	**Default Value**	**Description**
13	RMSIB_HPFSEL	R/W	0	Calculate current IB RMS data whether pass high-pass filter: 0: pass 1: not pass
12	RESPONSE_TIME	R/W	0	Metering data response time. 0: normal 1: 2 times
11:10	AVGRMS_RATE	R/W	0	Average RMS refresh time. 00: 40 ms 01: 80 ms 10: 320 ms 11: 640 ms
9:8	AVGPQ_RATE	R/W	0	Average power refresh time. 00: 40 ms 01: 80 ms 10: 320 ms 11: 640 ms
7:4	EM_MODE	R/W	0	DSP Operating Mode. 0: 128 sampling points per cycle by DSP at 6.5536MHz system clock 1: 64 sampling points per cycle by DSP at 6.5536MHz system clock 2: 32 sampling points per cycle by DSP at 6.5536MHz system clock. 3, 4, and 5: Reserved. 6: 64 sampling points per cycle by DSP at 3.2768MHz system clock 7: 32 sampling points per cycle by DSP at 3.2768MHz system clock 8: 32 sampling points per cycle by DSP at 819.2KHz system clock (supported only up to 2 channels instantaneous current RMS calculation.) 9: 16 sampling points per cycle by DSP at 409.6KHz system clock (supported only up to 2 channels instantaneous current RMS calculation.) Others: the same as mode 0
3	Rsvd	-	0	The bit must hold its default value for proper operation.
2	ADCUEN	R/W	0	To enable the voltage channel (including ADC and DSP).
1	ADCIBEN	R/W	0	To enable the current channel B (including ADC and DSP).
0	ADCIAEN	R/W	0	To enable the current channel A (including ADC and DSP).

29.3.4.2. EM_CTRL1 Register

Table 29-12 Metering Control Register 1 (0x03, EM_CTRL1)

0x03, R/W, Metering Control Register 1, EM_CTRL1				
Bit		**R/W**	**Default Value**	**Description**
31:24	Reserved		0	The bit must hold its default value for proper operation.
23	EM_EGY_CLK_SEL	R/W	0	To select the energy accumulator CLK. It needs the stable time around 107μs when CLK switch over. Please disable CF before it is stable. 0: 204.8 KHz(Internal frequency division of metering module system clock) 1: 32.768 KHz(X32KIN pin input)
22	LCF_ACC	R/W	0	0: disable To write "0" into the bit31 of the EM_CTRL0 the accumulating cycle of energy accumulator 3, 4, 5, 6, 7, and 8 is 20ms. To write "1" into the bit31 of the EM_CTRL0, the accumulating cycle of energy accumulator 3, 4, 5, 6, 7, and 8 is 40ms. 1: enable To write "0" into the bit31 of the EM_CTRL0, the accumulating cycle of energy accumulator 3, 4, and 5 is 10ms. Energy accumulator 6, 7, and 8 not accumulate. To write "1" into the bit31 of the EM_CTRL0, the accumulating cycle of energy accumulator 3, 4, and 5 is 20ms. Energy accumulator 6, 7, and 8 not accumulate.
21	PGA_U	R/W	0	Voltage channel digital PGA: 0: X1 1: X4
20	PHSI_SEL	R/W	0	To select the input source for current zero-crossing. 0: current channel IA 1: current channel IB
19:18	SIGN_SEL	R/W	0	To select the detect method of zero-crossing: 0: negative direction (it indicates the signal changing from positive to negative is occurring a zero-crossing event) 1: positive direction (it indicates the signal changing from negative to positive is occurring a zero-crossing event) 2: positive and negative direction 3: disable the zero-crossing detection function

0x03, R/W, Metering Control Register 1, EM_CTRL1				
Bit		**R/W**	**Default Value**	**Description**
17	AUTO_BAUD	R/W	0	Actively power accumulating data uploads, the upload interface can pass EM_ SYS_IOCFGX P0/ P1/ P2/ P3/ P4/ P5/ P6 pin configuration as the actively data uploads. Configure UART baud rate. 0: The baud rate is 4800. 1: The baud rate is 9600.
16	AUTO_TX_EN	R/W	0	To enable the active power accumulating data uploads. 0: disable 1: enable
15	EM_EGY_LC_EN	R/W	0	To enable the low-speed energy accumulator and CF counter. The accumulating speed of low-speed energy accumulator is 50 Hz. 0: disable 1: enable.
14	CF2_INV	R/W	0	To control the CF2 polarity. 0: original polarity 1: reverse polarity
13	CF2_EN	R/W	0	To Enable the CF2 output. 0: disable 1: enable.
12	CF2_SEL	R/W	0	To select the input source of CF2. 0: from the energy accumulator 1 1: from the energy accumulator 2
11	Reserved		0	The bit must hold its default value for proper operation.
10	CF1_INV	R/W	0	To control CF1 polarity. 0: original polarity 1: reverse polarity
9	CF1_EN	R/W	0	To enable CF1 output. 0: disable CF1 output 1: enable CF1 output
8	CF1_SEL	R/W	0	To select the input source of CF1. 0: from the energy accumulator 1 1: from the energy accumulator 2
7	CALCEN2	R/W	0	To enable the energy accumulator 2 and CF2 counter. The accumulating speed of energy accumulator 2 is 204.8 KHz. 0: disable 1: enable.
6	CALCEN1	R/W	0	To enable the energy accumulator 1 and CF1 counter. The accumulating speed of energy accumulator 1 is 204.8 KHz. 0: disable 1: enable

0x03, R/W, Metering Control Register 1, EM_CTRL1				
Bit		**R/W**	**Default Value**	**Description**
5:4	CF_PULSE	R/W	0	To select the CF pulse width 0: 80 ms 1: 40 ms 2: 20 ms 3: 10 ms
3:2	CF_FAST_EN	R/W	0	CF pulse speed up output. 0: Normal mode 1: 4x faster 2: 8x faster 3: 16x faster
1	PWR_CRP_EN	R/W	0	To determine power-creep of the power. The power-creep determination uses continuous 3 average and threshold compare. If lower the threshold, then here will be the power-creep status. 0: disable the power-creep detection 1: enable the power-creep detection
0	EGY_CRP_EN	R/W	0	To determine energy-creep of the High-speed energy accumulator 0: disable the energy-creep detection 1: enable the energy-creep detection

29.3.4.3. EM_EGY_CTRL0 Register

Table 29-13 Energy Accumulator Control Register 0 (0x04, EM_EGY_CTRL0)

0x04, R/W, Energy Accumulator Control Register0, EM_EGY_CTRL0				
Bit		**R/W**	**Default Value**	**Description**
31:30	INMODE4	R/W	0	The energy accumulator 4 accumulating mode. 0: power accumulation 1: current RMS accumulation 2: constant accumulation 3: configurable fundamental-wave channel accumulation
29	A_SEL4	R/W	0	To enable the energy accumulator 4, channel A accumulating. 0: disable 1: enable
28	B_SEL4	R/W	0	To enable the energy accumulator 4, channel B accumulating. 0: disable 1: enable

0x04, R/W, Energy Accumulator Control Register0, EM_EGY_CTRL0				
Bit		**R/W**	**Default Value**	**Description**
27:26	TYPE_SEL4	R/W	0	The energy accumulator 4, multiple channel accumulating mode choice. When power accumulating, 0, 3: active power accumulation 1: reactive power accumulation 2: apparent power accumulation When RMS accumulating, high bit zero represents accumulating sum; High bit one represents accumulating difference.
25:24	PROCMODE4	R/W	0	For each signal type choices which feed into the energy accumulator 4. 0: the positive value of the energy accumulator adding 1: the negative value of the energy accumulator adding (Here the actual accumulating value is the positive which exchanged from the original value.) 2: the original value of the energy accumulator adding 3: the absolute value of the energy accumulator adding
23:22	INMODE3	R/W	0	The energy accumulator 3 accumulation mode 0: power accumulation 1: current RMS accumulation 2: constant accumulation 3: configurable the fundamental wave channel accumulation
21	A_SEL3	R/W	0	To enable the energy accumulator 3, channel A accumulating. 0: disable; 1: enable
20	B_SEL3	R/W	0	To enable the energy accumulator 3, channel B accumulating. 0: disable 1: enable
19:18	TYPE_SEL3	R/W	0	The energy accumulator 3, multiple channel accumulating mode choice. When power accumulating, 0, 3: active power accumulation 1: reactive power accumulation 2: apparent power accumulation When RMS accumulating, High bit zero represents accumulating sum; high bit one represents accumulating difference.

0x04, R/W, Energy Accumulator Control Register0, EM_EGY_CTRL0				
Bit		**R/W**	**Default Value**	**Description**
17:16	PROCMODE3	R/W	0	For each signal type choices which feed into the energy accumulator 3. 0: the positive value of the energy accumulator adding 1: the negative value of the energy accumulator adding (Here the actual accumulating value is the positive which exchanged from the original value.) 2: the original value of the energy accumulator adding 3: the absolute value of the energy accumulator adding
15:14	INMODE2	R/W	0	The energy accumulator 2 accumulating mode. 0: power accumulation 1: current RMS accumulation 2: constant accumulation 3: configurable the fundamental wave channel accumulation
13	A_SEL2	R/W	0	To enable the energy accumulator 2, channel A accumulating. 0: disable 1: enable
12	B_SEL2	R/W	0	To enable the energy accumulator 2, channel B accumulating. 0: disable 1: enable
11:10	TYPE_SEL2	R/W		The energy accumulator 2, multiple channel accumulating mode choice. When power accumulating, 0, 3: active power accumulation 1: reactive power accumulation 2: apparent power accumulation When RMS accumulating, High bit zero represents accumulating sum; high bit one represents accumulating difference.
9:8	PROCMODE2	R/W	0	For each signal type choices which feed into the energy accumulator 2. 0: the positive value of the energy accumulator adding 1: the negative value of the energy accumulator adding (Here the actual accumulating value is the positive which exchanged from the original value.) 2: the original value of the energy accumulator adding 3: the absolute value of the energy accumulator adding
7:6	INMODE1	R/W	0	The energy accumulator 1 accumulating mode. 0: power accumulation 1: current RMS accumulation 2: constant accumulation 3: configurable the fundamental wave channel accumulation

0x04, R/W, Energy Accumulator Control Register0, EM_EGY_CTRL0				
Bit		**R/W**	**Default Value**	**Description**
5	A_SEL1	R/W	0	To enable the energy accumulator 1, channel A accumulating. 0: disable 1: enable
4	B_SEL1	R/W	0	To enable the energy accumulator 1, channel B accumulating. 0: disable 1: enable
3:2	TYPE_SEL1	R/W	0	Multiple channel accumulating mode choice. When power accumulating, 0, 3: active power accumulation 1: reactive power accumulation 2: apparent power accumulation When RMS accumulating, High bit zero represents accumulating sum; high bit one represents accumulating difference.
1:0	PROCMODE1	R/W	0	For each signal type choices which feed into the energy accumulator 1. 0: the positive value of the energy accumulator adding 1: the negative value of the energy accumulator adding (Here the actual accumulating value is the positive which exchanged from the original value.) 2: the original value of the energy accumulator adding 3: the absolute value of the energy accumulator adding

29.3.4.4. EM_EGY_CTRL1 Register

Table 29-14 Energy Accumulator Control Register 1 (0x05, EM_EGY_CTRL1)

0x05, R/W, Energy Accumulator Control Register 1, EM_EGY_CTRL1				
Bit		**R/W**	**Default Value**	**Description**
31:30	INMODE8	R/W	0	The energy accumulator 8 accumulating mode. 0: power accumulation 1: current RMS accumulation 2: constant accumulation 3: configurable the fundamental wave channel accumulation
29	A_SEL8	R/W	0	To enable the energy accumulator 8, channel A accumulating. 0: disable 1: enable

0x05, R/W, Energy Accumulator Control Register 1, EM_EGY_CTRL1				
Bit		**R/W**	**Default Value**	**Description**
28	B_SEL8	R/W	0	To enable the energy accumulator 8, channel B accumulating. 0: disable 1: enable
27:26	TYPE_SEL8	R/W	0	The energy accumulator 8, multiple channel accumulating mode choice. When power accumulating, 0, 3: active power accumulation 1: reactive power accumulation 2: apparent power accumulation When RMS accumulating, High bit zero represents accumulating sum; high bit one represents accumulating difference.
25:24	PROCMODE8	R/W	0	For each signal type choices which feed into the energy accumulator 8. 0: the positive value of the energy accumulator adding 1: the negative value of the energy accumulator adding (Here the actual accumulating value is the positive which exchanged from the original value.) 2: the original value of the energy accumulator adding 3: the absolute value of the energy accumulator adding
23:22	INMODE7	R/W	0	The energy accumulator 7 accumulating mode 0: power accumulation 1: current RMS accumulation 2: constant accumulation 3: configurable the fundamental wave channel accumulation
21	A_SEL7	R/W	0	To enable the energy accumulator 7, channel A accumulating 0: disable 1: enable
20	B_SEL7	R/W	0	To enable the energy accumulator 7, channel B accumulating 0: disable 1: enable
19:18	TYPE_SEL7	R/W	0	The energy accumulator 7, multiple channel accumulating mode choice. When power accumulating, 0, 3: active power accumulation 1: reactive power accumulation 2: apparent power accumulation When RMS accumulating, High bit zero represents accumulating sum; high bit one represents accumulating difference.

0x05, R/W, Energy Accumulator Control Register 1, EM_EGY_CTRL1				
Bit		**R/W**	**Default Value**	**Description**
17:16	PROCMODE7	R/W	0	For each signal type choices which feed into the energy accumulator 7. 0: the positive value of the energy accumulator adding 1: the negative value of the energy accumulator adding (Here the actual accumulating value is the positive which exchanged from the original value.) 2: the original value of the energy accumulator adding 3: the absolute value of the energy accumulator adding
15:14	INMODE6	R/W	0	The energy accumulator 6 accumulating mode. 0: power accumulation 1: current RMS accumulation 2: constant accumulation 3: configurable the fundamental wave channel accumulation
13	A_SEL6	R/W	0	To enable the energy accumulator 6, channel A accumulating. 0: disable 1: enable
12	B_SEL6	R/W	0	To enable the energy accumulator 6, channel B accumulating. 0: disable 1: enable
11:10	TYPE_SEL6	R/W		The energy accumulator 6, multiple channel accumulating mode choice. When power accumulating, 0, 3: active power accumulation 1: reactive power accumulation 2: apparent power accumulation When RMS accumulating, High bit zero represents accumulating sum; high bit one represents accumulating difference.
9:8	PROCMODE6	R/W	0	For each signal type choices which feed into the energy accumulator 6. 0: the positive value of the energy accumulator adding 1: the negative value of the energy accumulator adding (Here the actual accumulating value is the positive which exchanged from the original value.) 2: the original value of the energy accumulator adding 3: the absolute value of the energy accumulator adding
7:6	INMODE5	R/W	0	The energy accumulator 5 accumulating mode. 0: power accumulation 1: current RMS accumulation 2: constant accumulation 3: configurable the fundamental wave channel accumulation

0x05, R/W, Energy Accumulator Control Register 1, EM_EGY_CTRL1				
Bit		**R/W**	**Default Value**	**Description**
5	A_SEL5	R/W	0	To enable the energy accumulator 5, channel A accumulating. 0: disable 1: enable
4	B_SEL5	R/W	0	To enable the energy accumulator 5, channel B accumulating. 0: disable 1: enable
3:2	TYPE_SEL5	R/W	0	The energy accumulator 5, multiple channel accumulating mode choice. When power accumulating, 0, 3: active power accumulation 1: reactive power accumulation 2: apparent power accumulation When RMS accumulating, High bit zero represents accumulating sum; high bit one represents accumulating difference.
1:0	PROCMODE5	R/W	0	For each signal type choices which feed into the energy accumulator 5. 0: the positive value of the energy accumulator adding 1: the negative value of the energy accumulator adding (Here the actual accumulating value is the positive which exchanged from the original value.) 2: the original value of the energy accumulator adding 3: the absolute value of the energy accumulator adding

29.3.4.5. EM_FD_CTRL Register

Table 29-15 Fast Detection Control Register (0x06, EM_FD_CTRL)

0x06, R/W, Fast Detection Control Register, EM_FD_CTRL				
Bit		**R/W**	**Default Value**	**Description**
31:30	IPERIOD	R/W	0	To select the detection time of over-current or under-current. When the number of sampling points of over-current or under-current in the sampling points during the cycle is greater than or equal to the ITH value, it will be considered as the effective cycle. If the number of consecutive effective cycle reaches the value set by IPERIOD, it will be considered as this event happened. 0: half cycle 1: 1 cycle 2: 2 cycles 3: 4 cycles

0x06, R/W, Fast Detection Control Register, EM_FD_CTRL				
Bit		**R/W**	**Default Value**	**Description**
29:24	ITH	R/W	0	To determine the threshold of cycle is effective cycle. 0: 1 time 1: 2 times … 63: 64 times
23:22	UPERIOD	R/W	0	The same as IPERIOD configurable conditions. 0: half cycle 1: 1 cycle 2: 2 cycles 3: 4 cycles
21:16	UTH	R/W	0	The same as ITH configurable conditions. 0: 1 time 1: 2 times … 63: 64 times
15:10	Reserved			These bits must hold its default value for proper operation.
9	IBLCSEL	R/W	0	IB under-current test source. 0: no pass IB wave data of high pass filter 1: pass IB wave data of high pass filter
8	IBOCSEL	R/W	0	IB: over-current test source. 0: no pass IB wave data of high pass filter 1: pass IB wave data of high pass filter
7	IALCSEL	R/W	0	IA under-current test source. 0: no pass IA wave data of high pass filter 1: pass IA wave data of high pass filter
6	IAOCSEL	R/W	0	IA over-current test source. 0: no pass IA wave data of high pass filter 1: pass IA wave data of high pass filter
5	ULVSEL	R/W	0	Channel U under-voltage test source. 0: no pass channel U wave data of high pass filter 1: pass channel U wave data of high pass filter
4	UOVSEL	R/W	0	Channel U over-voltage test source. 0: no pass channel U wave data of high pass filter 1: pass channel U wave data of high pass filter
3	Reserved		0	The bit must hold its default value for proper operation.
2	FDIBEN	R/W	0	To enable the fast detection for IB. 0: disable IB over or under current test 1: enable IB over or under current test
1	FDIAEN	R/W	0	To enable the fast detection for IA. 0: disable IA over or under current test 1: enable IA over or under current test
0	FDUEN	R/W	0	To enable the fast detection. 0: disable channel U over or under voltage test 1: enable channel U over or under voltage test

29.3.4.6. EM_WAVE_CTRL Register

Table 29-16 Wave Upload And Buffer Control Register (0x07, EM_WAVE_CTRL)

0x07, R/W, Wave Upload And Buffer Control Register, EM_WAVE_CTRL				
Bit		**R/W**	**Default Value**	**Description**
31	WAVE_ADDR_CLR	R/W	0	Reset reading the address of waveform storage, write 1 to reset.
30:29	WAVE_MEM_MODE	R/W	0	The operating mode of waveform storage: 0: storage by manual, full then stop. This time is the single storage. 1: storage by manual, trigger or manual stop. This time is the cyclic storage. 2: storage by trigger, full then stop. This time is the single storage. 3: disable
28	WAVE_MEM_EN	R/W	0	Waveform storage to trigger manual switch: write 1 = enable, write 0 = disable 0: disable 1: enable
27	U_DIP_TRIG	R/W	0	Event trigger for the voltage dip. 0: disable 1: enable
26	U_SWELL_TRIG	R/W	0	Event trigger for the voltage swell. 0: disable 1: enable
25	IB_LC_TRIG	R/W	0	Event trigger for the IB under-current. 0: disable 1: enable
24	IB_OC_TRIG	R/W	0	Event trigger for the IB over-current. 0: disable 1: enable
23	IA_LC_TRIG	R/W	0	Event trigger for the IA under-current. 0: disable 1: enable
22	IA_OC_TRIG	R/W	0	Event trigger for the IA over-current. 0: disable 1: enable
21	U_LV_TRIG	R/W	0	Event trigger for Under-voltage. 0: disable 1: enable
20	U_OV_TRIG	R/W	0	Event trigger for Over-voltage. 0: disable 1: enable

0x07, R/W, Wave Upload And Buffer Control Register, EM_WAVE_CTRL				
Bit		**R/W**	**Default Value**	**Description**
19:16	WAVE_LENGTH	R/W	0	To select output waveform length 0: 1 cycle 1: 2 cycles 2: 3 cycles …… 15: 16 cycles
15	Reserved	-	-	The bit must hold its default value for proper operation.
14	WAVE_U_HPF_SEL	R/W	0	Voltage waveform whether pass high-pass filter choice: 0: no pass high-pass filter 1: pass high-pass filter
13	WAVE_IA_HPF_SEL	R/W	0	Current IA waveform whether pass high-pass filter choice: 0: no pass high-pass filter 1: pass high-pass filter
12	WAVE_IB_HPF_SEL	R/W	0	Current IB waveform whether pass high-pass filter choice: 0: no pass high-pass filter 1: pass high-pass filter
11	Reserved	-	-	The bit must hold its default value for proper operation.
10	WAVE_U_SEL	R/W	0	To enable the waveform storage and Waveform output via channel U. The bit decides whether storage or transmit data of channel U: 0: no 1: yes
9	WAVE_IA_SEL	R/W	0	To Enable the waveform storage and Waveform output via channel IA. The bit decides whether storage or transmit data of channel IA: 0: no 1: yes
8	WAVE_IB_SEL	R/W	0	To enable the waveform storage and Waveform output via channel IB. The bit decides whether storage or transmit data of channel IB (If waveform storage and configure bit 8, bit 9, and bit 10 enable at the same time, the bit becomes invalid): 0: no 1: yes
7	SP_CHECK	R/W	0	Waveform output parity check choice: 0: odd parity 1: even parity

0x07, R/W, Wave Upload And Buffer Control Register, EM_WAVE_CTRL				
Bit		**R/W**	**Default Value**	**Description**
6	SPI_POL	R/W	0	Waveform output polarity choice: 0: negative 1: positive
5	SPI_PHA	R/W	0	Waveform output phase choice: 0: negative 1: positive
4:3	WAVE_OUT_EN	R/W	0	Waveform output choice: 0: disable 1: enable by manual 2: stop by manual 3: reserved
2:0	WAVE_OUT_MODE	R/W	0	Waveform output operating mode: 0: transmit starting by manual, until maximum cycle then stops. 1: transmit starting by manual, trigger or by manual stop. 2: trigger starting, stop by manual. 3: trigger starting, until maximum cycle then stops. 4~7: transmit by manual, stop by manual. Before enabling Waveform output, at least one channel of waveform storage and output must be opened.

29.3.5. Metering Data Register

When power-on reset (POR), RSTN pin reset occurs, all metering control registers will be reset to the default value.

29.3.5.1. DC Component Register

Table 29-17 DC Component Register

Address	Register	R/W	Data Format	Description	
0x22	EM_DAT_DCU	R	32-bit Complement Code	DC value of voltage channel.	By default, the updating time is 40ms; stable time is 120ms.
0x23	EM_DAT_DCI	R	32-bit Complement Code	DC value of current channel A.	
0x24	EM_DAT_DCIB	R	32-bit Complement Code	DC value of Current channel B.	

29.3.5.2. RMS Register

Table 29-18 Voltage/ Current/ Measurement Signal (M) RMS Register

Address	Register	R/W	Data Format	Description	
0x0E	EM_DAT_RMS0U	R	32-bit Complement Code	Instantaneous RMS of voltage.	By default, the updating time is 10ms; stable time is 30ms.
0x0F	EM_DAT_RMS0IA	R	32-bit Complement Code	Instantaneous RMS of current A.	
0x10	EM_DAT_RMS0IB	R	32-bit Complement Code	Instantaneous RMS of current B.	
0x19	EM_DAT_RMS1U	R	32-bit Complement Code	Average RMS of voltage.	Under the default state, the updating time is 40ms; stable time is 120ms.
0x1A	EM_DAT_RMS1IA	R	32-bit Complement Code	Average RMS of Current A.	
0x1B	EM_DAT_RMS1IB	R	32-bit Complement Code	Average RMS of Current B.	
0x1E	EM_DAT_RMSU_AVG	R	32-bit Complement Code	Average RMS of Voltage for 10 or 12 cycles (chose by line frequency.)	
0x1F	EM_DAT_RMSIA_AVG	R	32-bit Complement Code	Average RMS of Current IA for 10 or 12 cycles (chose by line frequency.)	
0x20	EM_DAT_RMSIB_AVG	R	32-bit Complement Code	Average RMS of Current IB for 10 or 12 cycles (chose by line frequency.)	

29.3.5.3. Active/ Reactive Power Register

Table 29-19 Active/ Reactive Power Register

Address	Register	R/W	Data Format	Description	
0x08	EM_DAT_PA	R	32-bit Complement Code	Instantaneous Active Power of channel A.	By default, the updating time is 20ms; stable time is 60ms.
0x09	EM_DAT_QA	R	32-bit Complement Code	Instantaneous Reactive Power of channel A.	
0x0A	EM_DAT_SA	R	32-bit Complement Code	Instantaneous Apparent Power of channel A.	
0x0B	EM_DAT_PB	R	32-bit Complement Code	Instantaneous Active Power of channel B.	

Address	Register	R/W	Data Format	Description	
0x0C	EM_DAT_QB	R	32-bit Complement Code	Instantaneous Reactive Power of channel B.	
0x0D	EM_DAT_SB	R	32-bit Complement Code	Instantaneous Apparent Power of channel B.	
0x13	EM_DAT_PA1	R	32-bit Complement Code	Average Active power of Channel A.	By default, the updating time is 80ms; stable time is 240ms.
0x14	EM_DAT_QA1	R	32-bit Complement Code	Average Reactive power of Channel A.	
0x15	EM_DAT_SA1	R	32-bit Complement Code	Average Apparent Power of Channel A.	
0x16	EM_DAT_PB1	R	32-bit Complement Code	Average Active power of Channel B.	
0x17	EM_DAT_QB1	R	32-bit Complement Code	Average Reactive power of Channel B.	
0x18	EM_DAT_SB1	R	32-bit Complement Code	Average Apparent Power of Channel B.	

29.3.5.4. Fundamental Wave Channel Register

Table 29-20 Fundamental Wave Channel Instantaneous Register

Address	Register	R/W	Data Format	Description
0x11	EM_DAT_CH1	R	32-bit Complement Code	Instantaneous value of Fundamental wave of Channel 1.
0x12	EM_DAT_CH2	R	32-bit Complement Code	Instantaneous value of Fundamental wave of Channel 2.

Table 29-21 Fundamental Wave Channel Average Register

Address	Register	R/W	Data Format	Description
0x1C	EM_DAT_CH1_AVG	R	32-bit Complement Code	Average value of Fundamental wave of Channel 1.
0x1D	EM_DAT_CH2_AVG	R	32-bit Complement Code	Average value of Fundamental wave of Channel 2.

29.3.5.5. Line Frequency Register

Table 29-22 Line Frequency Register (0x21, EM_DAT_FRQ)

Address	Register	R/W	Data Format	Description
0x21	EM_DAT_FRQ	R	32-bit Complement Code	Line frequency is related to FRQ_SEL. By default, the updating time is 320ms; stable time is 640ms.

29.3.6. Energy Accumulator Register

Table 29-23 Energy Accumulator Register

Address	Register	R/W	Data Format	Description
0x39	EM_EGY_PROCTH	R	32-bit Unsigned	Anti-creep threshold for energy accumulator. When the accumulated value of the anti-creep energy accumulator over this threshold and the accumulated value of the high-speed energy accumulator under this threshold, the accumulated value of the high-speed energy accumulator will be cleared.
0x3A	EM_EGY_PWRTH	R/W	32-bit Unsigned	Accumulation threshold for energy accumulator. Due to the energy accumulator was 46bit, the accumulated value of the high-speed energy accumulator equals to this value*16384; the accumulated value of the low-speed energy accumulator equals to this value*4.
0x3B	EM_EGY_CONST1	R/W	32-bit Unsigned	Energy accumulator 1 accumulating constant.
0x3C	EM_EGY_OUT1L	R/W	32-bit Unsigned	Energy accumulator 1 accumulating low bit.
0x3D	EM_EGY_OUT1H	R/W	32-bit Unsigned	Energy accumulator 1 accumulating high bit Low 14bit effective.
0x3E	EM_EGY_CFCNT1	R/W	32-bit Unsigned	Energy accumulator 1 pulse counter.
0x3F	EM_EGY_CONST2	R	32-bit Unsigned	Energy accumulator 2 accumulating constant.
0x40	EM_EGY_OUT2L	R/W	32-bit Unsigned	Energy accumulator 2 accumulating low bit.
0x41	EM_EGY_OUT2H	R/W	32-bit Unsigned	Energy accumulator 2 accumulating high bit Low 14bit effective.
0x42	EM_EGY_CFCNT2	R/W	32-bit Unsigned	Energy accumulator 2 pulse counter.
0x43	EM_EGY_CONST3	R	32-bit Unsigned	Energy accumulator 3 accumulating constant.
0x44	EM_EGY_OUT3	R/W	32-bit Unsigned	Energy accumulator 3 accumulating value.
0x45	EM_EGY_CFCNT3	R/W	32-bit Unsigned	Energy accumulator 3 pulse counter.
0x46	EM_EGY_CONST4	R	32-bit Unsigned	Energy accumulator 4 accumulating constant.
0x47	EM_EGY_OUT4	R/W	32-bit Unsigned	Energy accumulator 4 accumulating value.
0x48	EM_EGY_CFCNT4	R/W	32-bit Unsigned	Energy accumulator 4 pulse counter.

0x49	EM_EGY_CONST5	R	32-bit Unsigned	Energy accumulator 5 accumulating constant.
0x4A	EM_EGY_OUT5	R/W	32-bit Unsigned	Energy accumulator 5 accumulating value.
0x4B	EM_EGY_CFCNT5	R/W	32-bit Unsigned	Energy accumulator 5 pulse counter.
0x4C	EM_EGY_CONST6	R	32-bit Unsigned	Energy accumulator 6 accumulating constant.
0x4D	EM_EGY_OUT6	R/W	32-bit Unsigned	Energy accumulator 6 accumulating value.
0x4E	EM_EGY_CFCNT6	R/W	32-bit Unsigned	Energy accumulator 6 pulse counter.
0x4F	EM_EGY_CONST7	R	32-bit Unsigned	Energy accumulator 7 accumulating constant.
0x50	EM_EGY_OUT7	R/W	32-bit Unsigned	Energy accumulator 7 accumulating value.
0x51	EM_EGY_CFCNT7	R/W	32-bit Unsigned	Energy accumulator 7 pulse counter.
0x52	EM_EGY_CONST8	R	32-bit Unsigned	Energy accumulator 8 accumulating constant.
0x53	EM_EGY_OUT8	R/W	32-bit Unsigned	Energy accumulator 8 accumulating value.
0x54	EM_EGY_CFCNT8	R/W	32-bit Unsigned	Energy accumulator 8 pulse counter.

29.3.7. Phase Measurement Register

Table 29-24 Phase Measurement Register

Address	Register	R/W	Data Format	Description
0x61	EM_PHS_STT	R/W	32-bit Unsigned	To control the phase measurement. Enable phase measurement once for writing operation.
0x62	EM_PHS_U	R	32-bit Unsigned	Voltage Phase Value.
0x63	EM_PHS_UN	R	32-bit Unsigned	The waveform data before voltage zero-crossing.
0x64	EM_PHS_UP	R	32-bit Unsigned	The waveform data after voltage zero-crossing.
0x65	EM_PHS_I	R	32-bit Unsigned	Current Phase Value.
0x66	EM_PHS_IN	R	32-bit Unsigned	The waveform data before current zero-crossing.
0x67	EM_PHS_IP	R	32-bit Unsigned	The waveform data after current zero-crossing.

29.3.8. Power-creep Threshold Register

Table 29-25 Power-creep Threshold Register

Address	Register	R/W	Data Format	Description
0x55	EM_OV_THL	R/W	32-bit Complement Code	To set the lower threshold for the power creep detection for instantaneous active power/ reactive power/ apparent power of channel A and B.
0x56	EM_OV_THH	R/W	32-bit Complement Code	To set the upper threshold for the power creep detection for instantaneous active power/ reactive power/ apparent power of channel A and B.

29.3.9. Voltage Swell or Dip Threshold Register

Table 29-26 Voltage Swell or Dip Threshold Register

Address	Register	R/W	Data Format	Description
0x57	EM_SWELL_THL	R/W	32-bit Complement Code	To set the lower threshold for the voltage swell.
0x58	EM_SWELL_THH	R/W	32-bit Complement Code	To set the upper threshold for the voltage swell.
0x59	EM_DIP_THL	R/W	32-bit Complement Code	To set the lower threshold for the voltage dip.
0x5A	EM_DIP_THH	R/W	32-bit Complement Code	To set the upper threshold for the voltage dip.
0x6A	EM_DAT_SWELL_CNT	R/C	32-bit Complement Code	Times records of voltage swell, half wave as a unit. 24bit effective. When write in any value, can clear zero the counter value.
0x6B	EM_DAT_DIP_CNT	R/C	32-bit Complement Code	Times records of voltage dip, half wave as a unit. 24bit effective. When write in any value, can clear zero the counter value.

29.3.10. Fast Detection Threshold Register

Table 29-27 Fast detection Threshold Register

Address	Register	R/W	Data Format	Description
0x5B	EM_FD_OVTH	R/W	30-bit Complement Code	To set over-voltage threshold for fast detection. Bit width is 30bit.
0x5C	EM_FD_LVTH	R/W	30-bit Complement Code	To set under-voltage threshold for fast detection. Bit width is 30bit.

Address	Register	R/W	Data Format	Description
0x5D	EM_FD_IA_OCTH	R/W	30-bit Complement Code	To set over-current threshold in channel A for fast detection. Bit width is 30bit.
0x5E	EM_FD_IA_LCTH	R/W	30-bit Complement Code	To set under-current threshold in channel A for fast detection. Bit width is 30bit.
0x5F	EM_FD_IB_OCTH	R/W	30-bit Complement Code	To set over-current threshold in channel B for fast detection. Bit width is 30bit.
0x60	EM_FD_IB_LCTH	R/W	30-bit Complement Code	To set under-current threshold in channel B for fast detection. Bit width is 30bit.

29.3.11. Waveform Data Register

Table 29-28 Waveform Data Register

Address	Register	R/W	Data Format	Description
0x69	EM_DAT_WAVE	R	32-bit Complement Code	Waveform reading. It can repeatable reading the address and obtain the overall wave data. If there is no need to read all data, it would be reset the bit 31 of metering control register (0x07, EM_WAVE_CTRL) to read address.

29.3.12. Calibration Register

When power-on reset (POR), RSTN pin reset occurs, all calibration registers will be reset to the default value. The default value in the following tables of this section are in format of hexadecimal.

All the calibration registers need to be configuration verification and self-checking.

29.3.12.1. DC Bias Setting Register

Table 29-29 DC Bias Setting Register

Address	Register	Default Value	R/W	Format Value	Description
0x34	EM_CFG_DCU	0	R/W	32-bit Complement Code	To set the DC compensation for the voltage channel.
0x35	EM_CFG_DCIA	0	R/W	32-bit Complement Code	To set the DC compensation for the current channel A.
0x36	EM_CFG_DCIB	0	R/W	32-bit Complement Code	To set the DC compensation for the current channel B.
All registers for calibration need to be configuration verification and self-checking.					

29.3.12.2. RMS Calibration Register

Table 29-30 Voltage/ Current/ Measurement RMS Calibration Register

Address	Register	Default Value	R/W	Data Format	Description
0x2D	EM_CFG_CALI_RMSU	0	R/W	32-bit Complement Code	To set gain calibration for Voltage RMS.
0x2E	EM_CFG_RMS_DCU	0	R/W	32-bit Complement Code	To set offset calibration for Voltage RMS.
0x2F	EM_CFG_CALI_RMSIA	0	R/W	32-bit Complement Code	To set gain calibration for Current RMS A.
0x30	EM_CFG_RMS_DCIA	0	R/W	32-bit Complement Code	To set offset calibration for Current RMS A.
0x31	EM_CFG_CALI_RMSIB	0	R/W	32-bit Complement Code	To set gain calibration for Current RMS B.
0x32	EM_CFG_RMS_DCIB	0	R/W	32-bit Complement Code	To set offset calibration for Current RMS.

29.3.12.3. Power Calibration Register

Table 29-31 Total-wave Active/ Reactive Power Calibration Register

Address	Register	Default Value	R/W	Data Format	Description
0x25	EM_CFG_CALI_PA	0	R/W	32-bit Complement Code	To set gain calibration for the active power A.
0x26	EM_CFG_DC_PA	0	R/W	32-bit Complement Code	To set offset calibration for the active power A.
0x27	EM_CFG_CALI_QA	0	R/W	32-bit Complement Code	To set gain calibration for Reactive power A.
0x28	EM_CFG_DC_QA	0	R/W	32-bit Complement Code	To set offset calibration for Reactive power A.
0x29	EM_CFG_CALI_PB	0	R/W	32-bit Complement Code	To set gain calibration for Active power B.
0x2A	EM_CFG_DC_PB	0	R/W	32-bit Complement Code	To set offset calibration for Active power B.
0x2B	EM_CFG_CALI_QB	0	R/W	32-bit Complement Code	To set gain calibration for Reactive power B.
0x2C	EM_CFG_DC_QB	0	R/W	32-bit Complement Code	To set offset calibration for Reactive power B.

29.3.12.4. Threshold Register

Table 29-32 Threshold Register

Address	Register	Default Value	R/W	Data Format	Description
0x39	EM_EGY_CRPTH	0	R/W	32-bit Complement Code	Energy accumulator anti-creep threshold.
0x3A	EM_EGY_PWRTH	0	R/W	32-bit Complement Code	Accumulation threshold for energy accumulator.
0x55	EM_OV_THL	0	R/W	32-bit Complement Code	To set the lower threshold for the power-creep determination.
0x56	EM_OV_THH	0	R/W	32-bit Complement Code	To set the upper threshold for the power-creep determination.

29.3.12.5. Phase Calibration Register

Table 29-33 Phase Calibration Register (0x33, EM_CFG_PHC)

Address	Register	Default Value	R/W	Data Format	Description
0x33	EM_CFG_PHC	0	R/W	32-bit Complement Code	Phase Error Calibration Register. The register needs to be configuration verification and self-checking. [10:0]= phase error calibration value for channel A; [26:16]= phase error calibration value for channel B; Where the range is from -766 to 767.

29.3.12.6. Bandpass Filter Register

Table 29-34 Bandpass Filter Register (0x37, EM_CFG_BPF)

Address	Register	Default Value	R/W	Data Format	Description
0x37	EM_CFG_BPF	0	R/W	32-bit Complement Code	Band-pass filter coefficient. Related to setting the EM_MODE by Bit[7:4] of metering control register 0 (0x02,EM_CTRL0) Setting 0x806764B6 at EM_MODE=0, 1, 2; setting 0x80DD7A8C at EM_MODE=6, 7; setting 0x82B465F0 at EM_MODE=8. The frequency of other modes would be not supported to measure, so setting to 0x0.

29.3.13. Checksum Register

Table 29-35 Checksum Register (0x38, EM_CFG_CKSUM)

Address	Register	Default Value	R/W	Data Format	Description
0x28	EM_CFG_CKSUM	0	R/W	32-bit Complement Code	This register needs to participate in parameter configuration self-check. This register participates in parameter configuration self-check along with the addresses 0x0~0x7, 0x25~0x3A, 0x55~0x60. If all the above register values add up to 0xFFFFFFFF, the parameter configuration self-check passes. To ensure parameter configuration self-check successful, the register should write correct value (0xFFFFFFFF - the sum of the configuration values of other registers participating in the check).

Table 29-36 Self-checking Register

Name	Type	Address	Description	Default
EM_ANA_CTRL0	R/W	0x00	Analog Control Register 0.	0x00000000
EM_ANA_CTRL1	R/W	0X01	Analog Control Register 1.	0x00000000
EM_CTRL0	R/W	0x02	Metering Control Register 0.	0x00000000
EM_CTRL1	R/W	0x03	Metering Control Register 1.	0x00000000
EM_EGY_CTRL0	R/W	0x04	Energy Accumulator Control Register 0.	0x00000000
EM_EGY_CTRL1	R/W	0x05	Energy Accumulator Control Register 1.	0x00000000
EM_FD_CTRL	R/W	0x06	Fast Detection Control Register.	0x00000000
EM_WAVE_CTRL	R/W	0x07	Wave Upload And Buffer Control Register.	0x00000000
EM_CFG_CALI_PA	R/W	0x25	To set gain calibration for the active power A.	0x00000000
EM_CFG_DC_PA	R/W	0x26	To set offset calibration for the active power A.	0x00000000
EM_CFG_CALI_QA	R/W	0x27	To set gain calibration for Reactive power A.	0x00000000
EM_CFG_DC_QA	R/W	0x28	To set offset calibration for Reactive power A.	0x00000000
EM_CFG_CALI_PB	R/W	0x29	To set gain calibration for Active power B.	0x00000000
EM_CFG_DC_PB	R/W	0x2A	To set offset calibration for Active power B.	0x00000000
EM_CFG_CALI_QB	R/W	0x2B	To set gain calibration for Reactive power B.	0x00000000
EM_CFG_DC_QB	R/W	0x2C	To set offset calibration for Reactive power B.	0x00000000
EM_CFG_CALI_RMSU	R/W	0x2D	To set gain calibration for Voltage RMS.	0x00000000
EM_CFG_RMS_DCU	R/W	0x2E	To set offset calibration for Voltage RMS.	0x00000000
EM_CFG_CALI_RMSIA	R/W	0x2F	To set gain calibration for Current RMS A.	0x00000000

EM_CFG_RMS_DCIA	R/W	0x30	To set offset calibration for Current RMS A.	0x00000000
EM_CFG_CALI_RMSIB	R/W	0x31	To set gain calibration for Current RMS B.	0x00000000
EM_CFG_RMS_DCIB	R/W	0x32	To set offset calibration for Current RMS.	0x00000000
EM_CFG_PHC	R/W	0x33	Phase Error Calibration Registers. [10:0]= phase error calibration value for channel A [26:16]= phase error calibration value for channel B. Where the range is from -766 to 767.	0x0000000
EM_CFG_DCU	R/W	0x34	To set the DC compensation for the voltage channel.	0x00000000
EM_CFG_DCIA	R/W	0x35	To set the DC compensation for the current channel A.	0x00000000
EM_CFG_DCIB	R/W	0x36	To set the DC compensation for the current channel B.	0x00000000
EM_CFG_BPF	R/W	0x37	Band-pass filter coefficient. Related to setting the EM_MODE by Bit[7:4] of metering control register 0 (0x02,EM_CTRL0). Setting 0x806764B6 at EM_MODE=0,1,2; setting 0x80DD7A8C at EM_MODE=6,7; setting 0x82B465F0 at EM_MODE=8. The frequency of other modes would be not supported to measure, so setting to 0x0.	0x00000000
EM_CFG_CKSUM	R/W	0x38	Configuration register for checksum.	0x00000000
EM_EGY_PROCTH	R/W	0x39	Anti-creep threshold for energy accumulator. When the accumulated value of the anti-creep energy accumulator over this threshold and the accumulated value of the high-speed energy accumulator under this threshold, the accumulated value of the high-speed energy accumulator will be cleared.	0x00000000
EM_EGY_PWRTH	R/W	0x3A	Accumulation threshold for energy accumulator. Due to the energy accumulator was 46bit, the accumulated value of the high-speed energy accumulator equals to this value*16384; the accumulated value of the low-speed energy accumulator equals to this value*4.	0x00000000
EM_OV_THL	R/W	0x55	To set the lower threshold for the no-load determination.	0x00000000
EM_OV_THH	R/W	0x56	To set the upper threshold for the no-load determination.	0x00000000
EM_SWELL_THL	R/W	0x57	To set the lower threshold for the voltage dip.	0x00000000
EM_SWELL_THH	R/W	0x58	To set the upper threshold for the voltage swell.	0x00000000

EM_DIP_THL	R/W	0x59	To set the lower threshold for the voltage dip.	0x00000000
EM_DIP_THH	R/W	0x5A	To set the upper threshold for the voltage swell.	0x00000000
EM_FD_OVTH	R/W	0x5B	To set over-voltage threshold for fast detection. Bit width is 30bit.	0x00000000
EM_FD_LVTH	R/W	0x5C	To set under-voltage threshold for fast detection. Bit width is 30bit.	0x00000000
EM_FD_IA_OCTH	R/W	0x5D	To set over-current threshold in channel A for fast detection. Bit width is 30bit.	0x00000000
EM_FD_IA_LCTH	R/W	0x5E	To set under-current threshold in channel A for fast detection. Bit width is 30bit.	0x00000000
EM_FD_IB_OCTH	R/W	0x5F	To set over-current threshold in channel B for fast detection. Bit width is 30bit.	0x00000000
EM_FD_IB_LCTH	R/W	0x60	To set under-current threshold in channel B for fast detection. Bit width is 30bit.	0x00000000

29.4. Electric energy metering clock

Two clock sources for the electric energy metering of V94XX(A):

- PCLK clock provides "CLK1" clock through switching and frequency division. After the frequency divider, SDIV, controlled by DSP_MODE (Bit<7:4>, Table 29-11 Metering Control Register 0 (0x02, EM_CTRL0)). This clock source for all digital block of electric energy metering uses. After the frequency divider, ADIV, controlled by ADCKSEL (Bit25<31:30>, analog control register, 0x01, ANA_CTRL1). This clock source for ADC uses.
- External CLK (32768 Hz), input from X32KIN pin. This clock source for low-speed energy accumulator uses. The clock source of energy accumulator would be controlled by EGY_CLK_SEL (bit23, metering control register 1 (Table 29-12 Metering Control Register 1 (0x03, EM_CTRL1))).

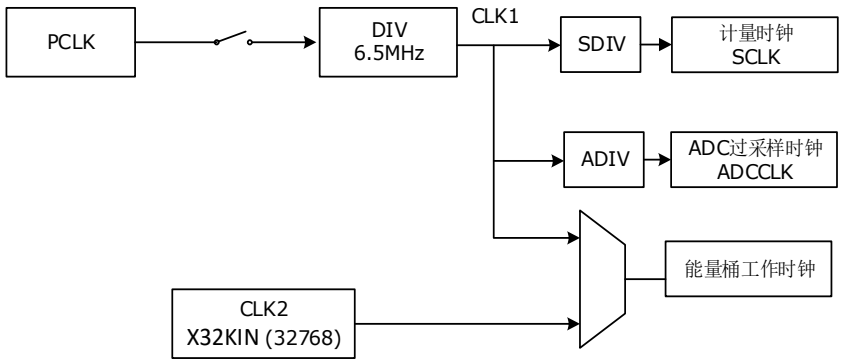


Figure 29-2 Electric energy metering clock generation

Table 29-37 Electric Energy Metering Clock Related Registers

Register	Bit	Default Value	Description
EM_ANA_CTRL1	Bit[31:30] ADCKSEL<1:0>	0	To select the clock frequency for the ADC. 00 corresponds to 819.2 KHz. 00: ×1 01: ×2 10: ×1/4 11: ×1/2
EM_CTRL0	Bit[7:4] DSP_MODE<1:0>	0	DSP Operating Mode. 0: 128 sampling points per cycle by DSP at 6.5536 MHz system clock 1: 64 sampling points per cycle by DSP at 6.5536 MHz system clock 2: 32 sampling points per cycle by DSP at 6.5536 MHz system clock. 3, 4, and 5: Reserved. 6: 64 sampling points per cycle by DSP at 3.2768 MHz system clock 7: 32 sampling points per cycle by DSP at 3.2768 MHz system clock 8: 32 sampling points per cycle by DSP at 819.2 KHz system clock (supported only up to 2 channels instantaneous current RMS calculation.) 9: 16 sampling points per cycle by DSP at 409.6 KHz system clock (supported only up to 2 channels instantaneous current RMS calculation.) Others: the same as mode 0
EM_CTRL1	Bit23 EGY_CLK_SEL	0	To selection the clock for Energy accumulator. It needs the stable time around 107 us when CLK switch over. Please disable CF before it is stable. 0: 204.8 KHz 1: 32768 Hz

29.4.1. External input high-frequency clock

Users can generate 6.5536MHz clock by frequency division of PCLK clock, and provide CLK1 clock for V94XX(A) for measuring VMA, ADC and energy modular. If the CLK1 clock is not enabled, two modes of application are supported: the energy accumulator function is not used; Use X32KIN pin to inject 32768Hz frequency clock as the energy bucket clock.

29.4.2. External Input Clock

The external can inject a 32768 Hz frequency clock into the X32KIN pin of V94XX(A) to provide CLK2 clock for low-speed accumulation of energy accumulator function of V94XX(A).

29.5. Electric energy metering bandgap circuit (EMBGP)

The Bandgap circuit outputs a reference voltage and bias current, about 1.21V with a typical temperature coefficient of 10ppm/°C, for ADCs and the 6.5MHz RC oscillator. By default, the Bandgap circuit was enabled. This circuit consumes about 0.09mA (typical).

Users can configure RESTL<1:0> (Bit[4:3]) and REST<2:0> (Bit[2:0]) of analog control register (0x01, EM_ANA_CTRL1) to adjust the temperature coefficient of Bandgap circuit to cancel the temperature coefficient introduced by the external components, with the following steps:

1) Assume the current settings of relative bits are REST<2:0>='010' and RESTL<1:0>='00', which corresponds to the temperature coefficient of Bandgap is +14ppm.
2) Measure meter errors in high and low temperature conditions. For example, this meter has 0 error at 20℃, and the measuring errors are 0.6% at 80℃ and -0.4% at -40℃ respectively. Then a -(0.6%-(-0.4%))/2=-0.5% measuring error needs to be compensated relative to high temperature working condition, equivalent to -0.5%/(80-20)=-5000/60=-83ppm.
3) As measured error is minus two times of Reference temperature coefficient error, to compensate a -83ppm error, an additional +41.5ppm of Bandgap REF temperature coefficient adjustment is needed. Taking the initial +14ppm setting into consideration, the actual adjustment should be +55.5ppm. According to the lookup table of RESTL<1:0> and REST<2:0>, user should set register RESTL<1:0> to '11' and REST<2:0> to '000', whose combination equals to a +56ppm temperature coefficient adjustment.

Attention: For the adjustment of Reference temperature parameters would influence the basic error; therefore, when customers designed each new product, please first confirm the temperature parameter of Reference then calibrate the error of the meter.

A temperature coefficient drift of x in the Bandgap circuit results in a drift of -2x in the measurement error.

Table 29-38 Register for Bandgap Circuit

Register	Bit	Default Value	Description
EM_ANA_CTRL1	Bit[4:3] RESTL<1:0>	0	To roughly adjust the temperature coefficient of the Bandgap circuit. 00: 0 ppm 01: -58 ppm 10: +111 ppm 11: +56 ppm In order to obtain the best metering performance and temperature performance during normal metering, it must be iterated according to the calculated result.

Register	Bit	Default Value	Description
	Bit[2:0] REST<2:0>	0	To finely adjust the temperature coefficient of the Bandgap circuit 000: 0 ppm 001: +7 ppm 010: +14 ppm 011: +28 ppm 100: -32 ppm 101: -21 ppm 110: -14 ppm 111: -7 ppm In order to obtain the best metering performance and temperature performance during normal metering, it must be iterated according to the calculated result.

29.6. Analog Inputs

The V94XX(A) has three pairs of analog inputs forming two current channels and one voltage channel. The current channels consist of two fully differential voltage inputs. And the voltage channel consists of a pseudo differential voltage input: UP is positive input for the voltage channel, and UN, grounded, is negative input for the voltage channel. Each input has a maximum voltage of ±200mV, and each pair has a maximum differential voltage of ±400mV.

In a current channel, a current transformer (CT) or a shunt resistor can be used for analog inputs.

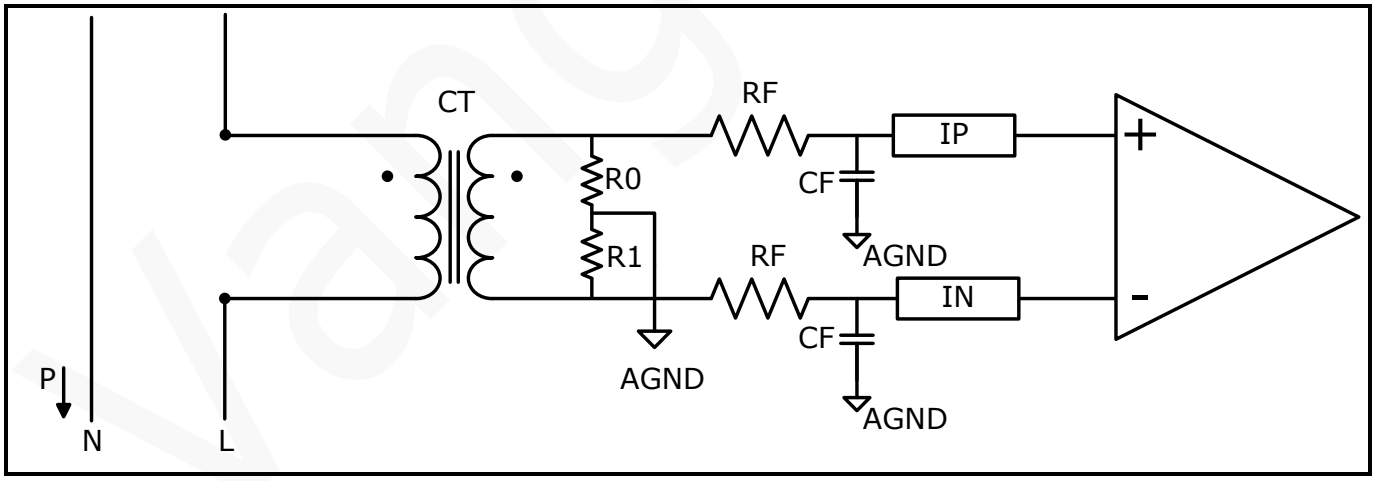


Figure 29-3 CT for Current Analog Input

Manganese copper resistance can also be used to shunt the network input current, and AGND can be used for grounding.

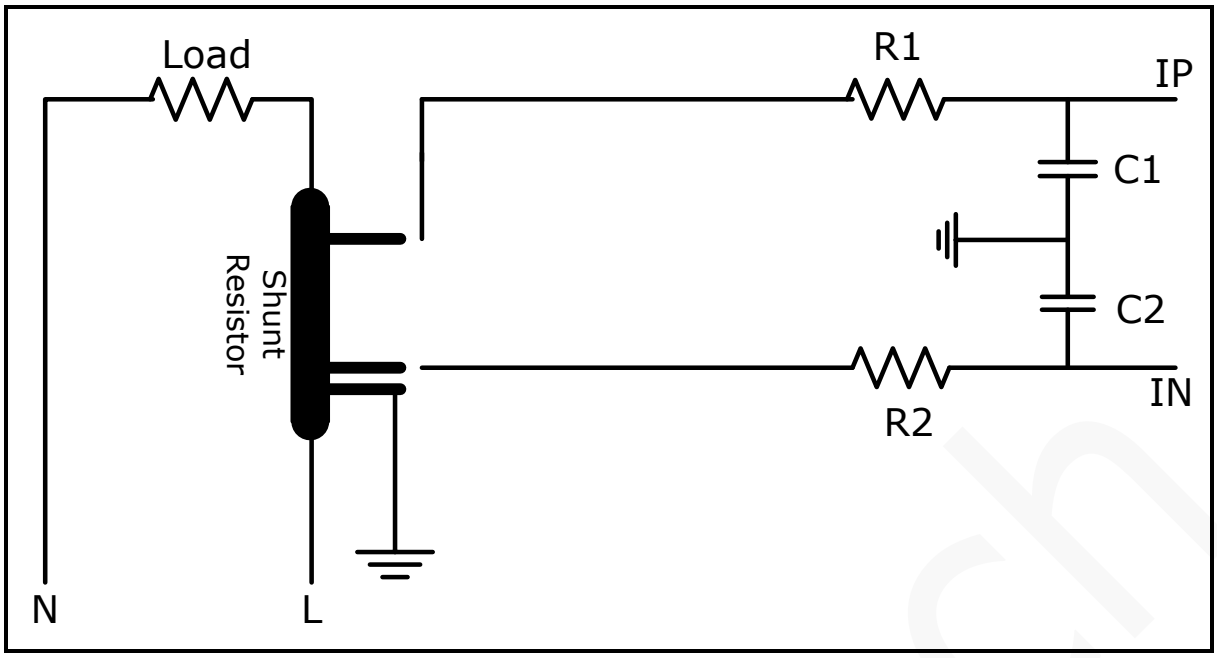


Figure 29-4 Shunt Resistor Network for Current Analog Input

V94XX (A) supports 1 circuit of voltage signal input. The pseudo differential input mode is adopted for voltage. Compared with the UN grounding, UP is a positive terminal, which requires two ports in total. The following are two typical connection methods of voltage channel, voltage transformer mode and resistance voltage division mode.

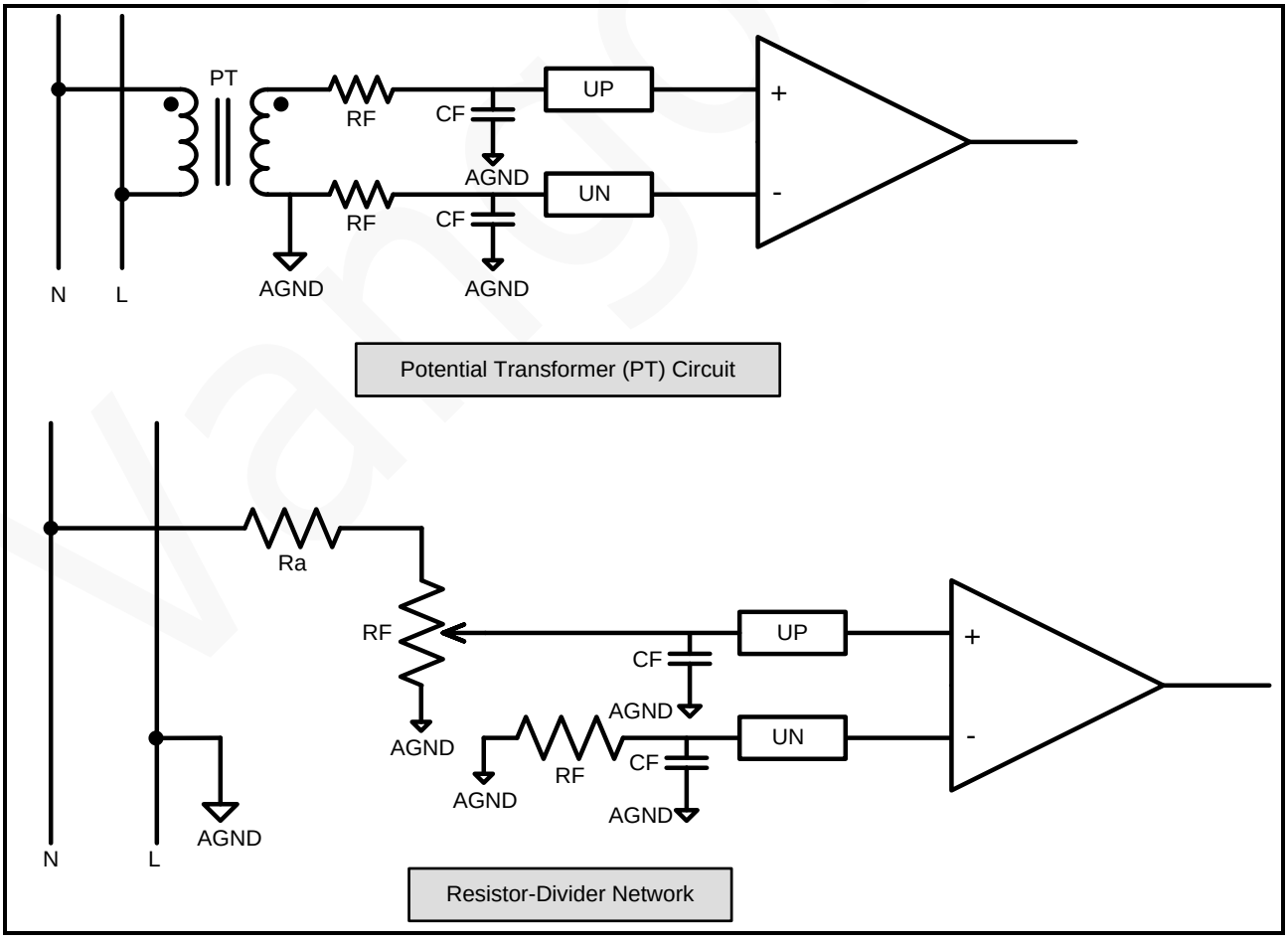


Figure 29-5 Analog Input of Voltage

The full measurement scale of ADCs is ±1.1 V. To match the output signal of the sensors with the

measurement scale of ADCs, groups of Analog Programmable Gain Amplifiers (APGA) are set. The product of the analog input and the set APGA should not be over ±1.1 V.

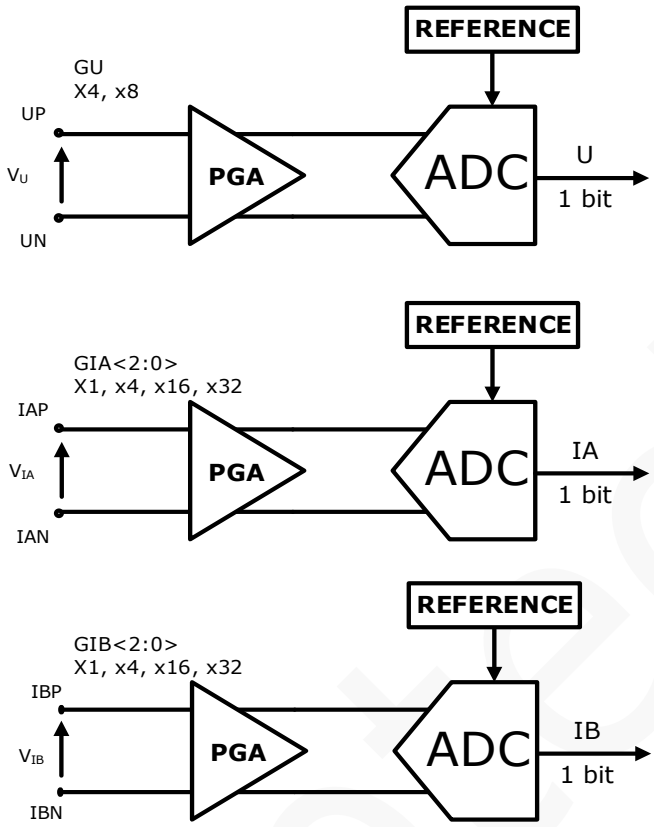


Figure 29-6 Current/voltage channel analog gain configuration

Table 29-39 Analog PGA Gain Configuration for Current and Voltage Analog Input

Register	Bit	Default	Description
EM_ANA_CTRL1 Register	Bit[14:12] GIB<2:0>	0	To adjust the gain of current ADC in the channel B. 000: 4 001: 1 010: 32 011: 16 100/101/110/111: prohibited GIB[2:0] is recommended set to 000 for proper operation.
	Bit11 GU	0	To adjust the gain of voltage ADC. 0: 8 1: 4 This bit must be set to 0 for proper operation.

Register	Bit	Default	Description
	Bit[10:8] GIA<2:0>	0	To adjust the gain of current ADC in the channel A. 000: 32 001: 16 010: 4 011: 1 100~111: prohibited GIA[2: 0] is recommended set to 000 for proper operation.

29.7. Analog-to-Digital Conversion

Second-order Σ-ΔADCs are designed in three channels of V94XX(A) for analog-to-digital conversion, and their full measurement scale is ±1.1 V. By default, Σ-ΔADCs are disabled. Users can turn on or off the ADC of each channel through ADCUEN, ADCIBEN and ADCIAEN (metering control register 0 (0x02, EM_CTRL0)). It should be noted that ADC and digital processing of each channel use the same control bit, so they are turned on and off at the same time.

Table 29-40 Enable/Disable ADCs

Register	Bit	Default	Description
EM_CTRL0 Register	Bit2 ADCUEN	0	To enable the voltage channel (including ADC and DSP).
	Bit1 ADCIBEN	0	To enable the current channel B (including ADC and DSP).
	Bit0 ADCIAEN	0	To enable the current channel A (including ADC and DSP).

29.8. Phase Compensation

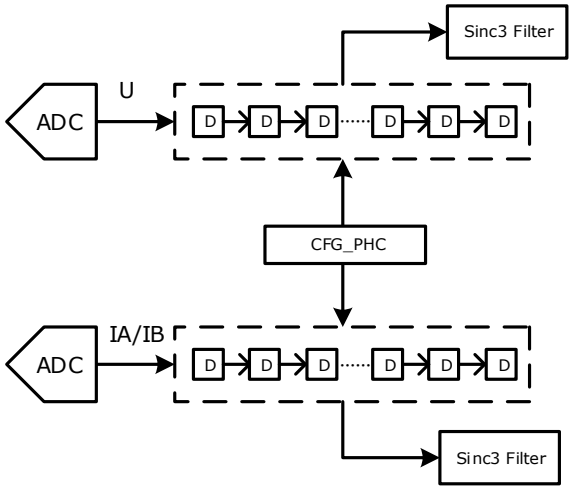


Figure 29-7 Phase Compensation Schematics

A phase compensation circuit composed of a time delay chain of fixed length is applied to correct the phase angle error via delaying the selected signal. Either current or voltage signals can be delayed.

By default phase compensation is disabled. Users can enable this function via configuring EM_CFG_PHC (Phase Measurement Register). If the register value is non-zero, turn on phase compensation automatically. When phase compensation is enabled, the phase angle error between I1 and U, and I2 and U, are corrected respectively.

In 50-Hz power grid, when the sampling frequency of the phase compensation circuit (f_{smpl}) is 3.2768 MHz, the calibration resolution is 0.0055°/lsb, and the maximum phase angle error to be corrected is ±4.21875°. The value of f_{smpl} is determined by the configuration of bits **"EM_MODE <3:0>"** (EM_CTRL0 Register).

At a lower power factor (PF), the phase angle error can cause greater energy metering error. So generally, the phase angle error is calibrated at PF=0.5L to ensure the metering accuracy. When PF=0.5L, users can use a simple equation as follows to calculate the value N.

$$N = Round(\frac{3011}{2} \times E \times \frac{f_{smpl}}{819200}) \qquad \text{Equation 29-1}$$

Where,

N is the value, signed, to be set to the phase compensation control registers to correct the phase angle error. A positive N indicates that current signal must be delayed, so "0" must be set to the sign bit; a negative N indicates that the voltage signal must be delayed, so "1" must be set to the sign bit;

E is the energy metering error displayed in LCD screen of the calibration equipment;

f_{smpl} is the sampling frequency of the phase compensation circuit, Hz.

Table 29-41 f_{smpl} Determines Phase Compensation Resolution and Correction Range

EM_MODE	fsmpl	calibration_accuracy	Calibration_range

		(degree)	(degree)
0x00，0x01，0x02	6.5536MHz	0.005493164	±4.21875
0x06，0x07	3.2768MHz	0.010986328	±8.4375
0x08	819.2KHz	0.021972656	±16.855

Table 29-42 Registers for Phase Compensation

Register	Bit	Default	Description
Phase Calibration Register	Bit[26:16] CFG_PHCB	0	Phase Error Calibration Register. The register needs to be configuration verification and self-checking. phase error calibration value for channel B; Where the range is from -766 to 767.
	Bit[10:0] CFG_PHCA	0	Phase Error Calibration Register. The register needs to be configuration verification and self-checking. phase error calibration value for channel A; Where the range is from -766 to 767.

29.9. Generation of raw waveform data

In V94XX(A), decimation filters are designed to reduce the noise of the 1-bit code stream output from the oversampling Σ/ΔADC and to reduce the sampling frequency to 1/256 of f_{ADC}.

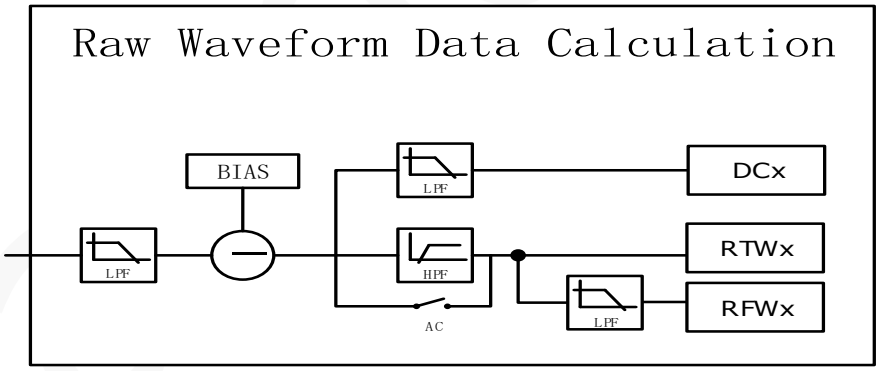


Figure 29-8 Generation of raw waveform data

Each ADC channel can generate DC raw instantaneous data, full wave AC raw instantaneous data and fundamental wave AC raw instantaneous data.

When configuring DC_METER_MODE (EM_CTRL0 Register) is 1, DC metering can be supported.

The user can turn on or off the ADC of each channel through ADCUEN, ADCIBEN and ADCIAEN (EM_CTRL0 Register). It should be noted that ADC and digital processing of each channel use the same control bit, so they are turned on and off at the same time.

Table 29-43 Enable/Disable Digital Inputs

Register	Bit	Default	Description
EM_CTRL0 Register	Bit2 ADCUEN	0	To enable the voltage channel (including ADC and DSP).
	Bit1 ADCIBEN	0	To enable the current channel B (including ADC and DSP).
	Bit0 ADCIAEN	0	To enable the current channel A (including ADC and DSP).

As depicted in the above figure, the signal output from the decimation filter in each channel will be sent to a high-pass filter (HPF) to remove the DC components introduced by the sensors and ADCs. In the V94XX(A), this high-pass filter can be disabled. When users want faster response time, they can bypass the high pass filter.

Digital programmable gain amplifiers (DPGA) with possible gain selection via PGA_U (EM_CTRL1 Register) is applied to U channel digital signals output from the high-pass filters to amplify its capability of depressing truncation noise when a low signal was input. Please note the product of the analog input and the total PGA gains, including APGA and DPGA, should not be over the measurement scales of the ADCs.

Table 29-44 DPGA Gain Selection for Digital Signals

Register	Bit	Default	Description
EM_CTRL1 Register	Bit21 PGA_U	0	Voltage channel digital PGA: 0: X1 1: X4

The following equations describe the digital signals processed by the digital programmable gain amplifiers:

$$Ua = PGAdua \times PGAua \times \frac{Aua}{1.21} \times \sin \omega t = DUa \times \sin \omega t$$

$$Ia = PGAdia \times \frac{Aia}{1.21} \times \sin(\omega t + \psi) = DIa \times \sin(\omega t + \psi)$$

Equation 29-2

where, *PGAdua* is the DPGA gain of U channel; *PGAua* and *PGAia* are the APGA gains; *Aua* and *Aia* are the amplitude of current and voltage inputs; and 1.21 is the reference voltage.

29.10. RMS Calculation and Calibration

The V94XX(A) supports RMS calculation.

As illustrated in Figure 29-9, the current or voltage raw waveform signal is multiplied with itself in the multiplier to get the product with the second harmonic which can be removed by the low-pass filter, and then the signal processed output from the low-pass filter, is offset corrected to remove noise. Then it is sent to the circuit for rooting processing that produces a 32-bit datum, the raw RMS value of current or voltage. The raw RMS data will be gain calibrated and then stored in instantaneous RMS registers. Besides, the instantaneous RMS data will be averaged to acquire the average RMS data that are stored in average RMS registers.

$$RMS = \sqrt{(Ia \times Ia - Offset * 256)} * (1 + S) \qquad \text{Equation 29-3}$$

Where, RMS is the instantaneous RMS data;

Ua or Ia is the value of digital signals of voltage or current.

Offset is the small signal correction value

S is the correction value of the ratio difference

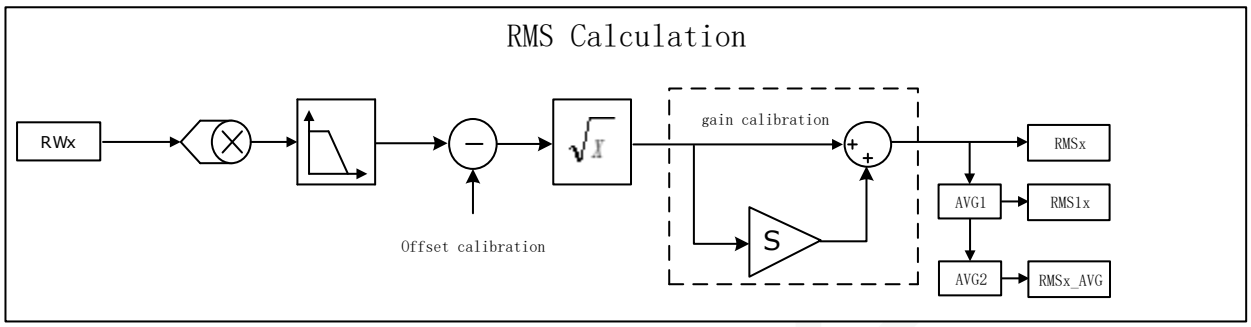


Figure 29-9 RMS Calculation and Calibration

The content of all the instantaneous and average RMS data registers are in the form of 32-bit 2'-complement. When POR/BOR, RSTn pin reset occurs, these registers are reset to their default states.

29.11. Active Power Calculation and Calibration

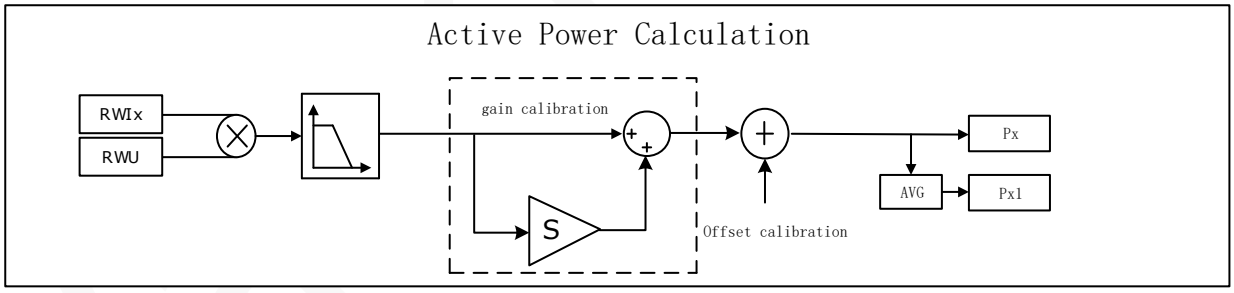


Figure 29-10 Signal Processing for Active Power Calculation and Calibration

The current and voltage raw waveform current signal multiply each other. Then, the product is input to the low-pass filter (LPF) to remove the harmonics and the ripples caused by the noise, and the output of the LPF is the raw active power. This raw power is gain calibrated and then offset calibrated to acquire the instantaneous active power. The instantaneous active power will be averaged to get the average active power. The content of all the registers are in the form of 32-bit 2'-complement, and they will be reset to their default states when POR/BOR, RSTn pin reset occurs. The calculation formula of active power is as follows:

$$P = (Ua \times Ia \times \cos\phi) * (1 + S) + Offset$$

Where, P is the active power (W);

Ua and Ia are the values of digital signals of voltage and current.

ϕ Is the angle between U and I

Offset is the small signal correction value

S is the correction value of the ratio difference

The active power data PA or PB after the ratio difference correction will be averaged and stored in PA1 or PB1 power average registers.

29.12. Reactive Power and Calibration

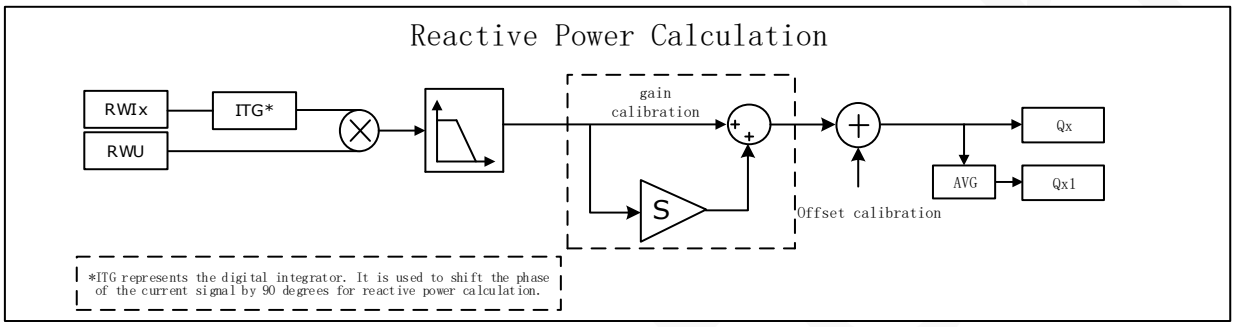


Figure 29-11 Signal Processing for Reactive Power Calculation and Calibration

The original current waveform signal is multiplied by the original voltage waveform signal after 90 ° phase adjustment by Hilbert filter. Then, the product is input to the low-pass filter (LPF) to remove the harmonics and the ripples caused by the noise, and the output of the LPF is the raw reactive power. This raw power is gain calibrated and then offset calibrated to acquire the instantaneous reactive power. The instantaneous reactive power will be averaged to get the average reactive power. The content of all the registers are in the form of 32-bit 2'-complement, and they will be reset to their default states when POR/BOR, RSTn pin reset occurs. The calculation formula of reactive power is as follows:

$$Q = (Ua \times Ia \times \sin\phi) * (1 + S) + Offset$$

Where, Q is the reactive power (W);

Ua and Ia are the values of digital signals of voltage and current.

ϕ Is the angle between U and I

Offset is the small signal correction value

S is the correction value of the ratio difference

The reactive power data QA or QB after the ratio difference correction will be averaged and stored in QA1 or QB1 power average registers.

Reactive power comes from full wave data and fundamental wave data, users can select by QB_MODE and QA_MODE selection (metering control register 0 (0x02, EM_CTRL0).

Table 29-45 Reactive power Selection

Register	Bit	Default	Description
错误!未找到引用源。	Bit19 QB_MODE	0	To select mode for Reactive power B. 0: total wave, reactive power 1: fundamental wave, reactive power
	Bit18 QA_MODE	0	To select mode for Reactive power A. 0: total wave, reactive power 1: fundamental wave, reactive power

29.13. Apparent Power Calculation

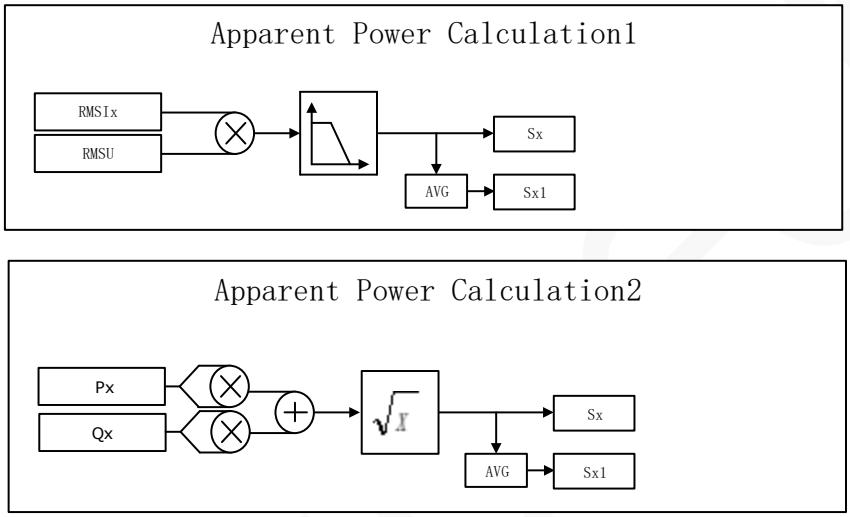


Figure 29-12 Apparent Power Calculation

The V94XX(A) supports apparent power calculation. There are two calculation methods for apparent power: calculation by RMS value and calculation by power value.

In the V94XX(A), the instantaneous current and voltage RMS are multiplied to acquire the apparent power, as described in the following equation:

$$S = Irms \times Urms$$ Equation 29-4

Where, *S* represents apparent power;

Irms and *Urms* are the average current and voltage RMS.

In the V94XX(A), the apparent power is obtained by square root of the sum of the square of the instantaneous active power and the square of the instantaneous reactive power, as described in the following equation:

$$S = \sqrt{P^2 + Q^2}$$ Equation 29-5

Where, S is the apparent power;

P is the instantaneous active power value;

Q is the instantaneous reactive power value.

The content of the apparent power registers are in the form of 32-bit 2'-complement. When POR/BOR, RSTn pin reset occurs, these registers are reset to their default states.

Table 29-46 Apparent Power Calculation

Register	Bit	Default	Description
EM_CTRL0 Register	Bit24 S_MODE	0	Source select for Apparent power calculation. 0: by RMS value 1: by power value

29.14. Power-creep Detection

Active power, reactive power, and apparent power support the power-creep function. See Table 29-25 Power-creep Threshold Register. When the instantaneous active power/reactive power/apparent power of the channel A and the channel B are higher than the upper threshold for three consecutive times, the startup state is entered. When the instantaneous active power/reactive power/apparent power of the channel A and the channel B are lower than the upper threshold for three consecutive times, the power-creep state is entered.

The user can check whether the instantaneous active power/reactive power/apparent power is in the power-creep state by Bit17~Bit12 of the EM_SYS_STS system status register description (0x74, EM_SYS_STS).

Table 29-47 Power-creep Detection Description

Register	Bit	Default	Description
EM_CTRL1 Register	Bit1 PWR_CRP_EN	0	To determine the power of power-creep. The power-creep determination uses continuous 3 average and threshold compare. If lower the threshold, then here will be the power-creep status. 0: disable the power-creep detection 1: enable the power-creep detection
EM_SYS_STS Register	Bit17 SBCREEP	0	Status bit for power-creep detection for reactive power Channel B. 0: start 1: power-creep
	Bit16 QBCREEP	0	Status bit for power-creep detection for active power Channel B. 0: start 1: power-creep

Register	Bit	Default	Description
	Bit15 PBCREEP	0	Status bit for power-creep detection for apparent power Channel A. 0: start 1: power-creep
	Bit14 SACREEP	0	Status bit for power-creep detection for reactive power Channel A. 0: start 1: power-creep
	Bit13 QACREEP	0	Status bit for power-creep detection for active power Channel A. 0: start 1: power-creep
	Bit12 PACREEP	0	Status bit for power-creep detection for reactive power Channel B. 0: start 1: power-creep

Table 29-48 Power-creep Threshold Register

Address	Register	R/W	Data Format	Description
0x55	EM_OV_THL	R/W	32-bit Complement Code	To set the lower threshold for the power creep detection for instantaneous active power/ reactive power/ apparent power of channel A and B.
0x56	EM_OV_THH	R/W	32-bit Complement Code	To set the upper threshold for the power creep detection for instantaneous active power/ reactive power/ apparent power of channel A and B.

29.15. Frequency measurement

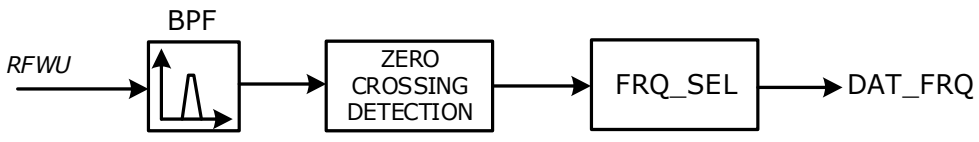


Figure 29-13 Frequency measurement

V94XX(A) supports frequency measurement, which is stored in the grid frequency register (0x21, EM_DAT_FRQ). Users need to configure the bandpass filter coefficient according to different EM_MODE (Table 29-11 Metering Control Register 0 (0x02, EM_CTRL0)). For details, please refer to the bandpass filter coefficient register (Table 29-34 Bandpass Filter Register (0x37, EM_CFG_BPF)).

The user accumulates the number of cycles and the EM_MODE configuration frequency constant through the FRQ_SEL configuration frequency test of the metering control register 0 (0x02, EM_CTRL0).

$$f = wave\_cnt * freq\_const/DSP\_DAT\_FRQ$$

Where,

f: Signal frequency, Hz;

wave_cnt: number of cycles;

freq_const: frequency constant, Hz;

EM_DAT_FRQ: The value of the frequency value register (in decimal). The value of the frequency value register is a 16 bit unsigned positive number.

Table 29-49 Frequency register source FRQ_SEL description

FRQ_SEL	wave_cnt
0	16
1	1
2	64

Table 29-50 Frequency Constant Description

EM_MODE	Frequency constant
0x08	1600
0x06, 0x07	3200
0x00, 0x01, 0x02	6400

29.16. Phase measurement

V94XX(A) supports voltage phase and current phase measurement. The operation principle is, write 1 to the register EM_PHS_STT (0x61) to start phase measurememt. It starts counting at a certain frequency, until zero-crossing events happened, it stops counting. This counting value will write into the voltage phase register or current phase register. It also records two sampling values before and after the zero-crossing. User can obtain better accurate phase value by interpolation method.

The certain frequency: When EM_MODE is 0, 1, 2, the sampling frequency of voltage signal used for phase testing is 6.4 KHz. When EM_MODE is 6 and 7, the sampling frequency of voltage signal used for phase testing is 3.2 KHz.

Current phase measurement only supports IA channel or IB channel at one time, which can be configured. The channel selection is consistent with the current zero crossing input source. Current zero crossing input source through PHSI_SEL (metering control register 1 (0x03, EM_CTRL1)) selects IA channel or IB

channel. Zero crossing event detection mode can be realized through SIGN_SEL (metering control register 1 (0x03, EM_CTRL1)) selects negative zero crossing or positive zero crossing.

Table 29-51 Frequency Constant Description

Register	Bit	Default	Description
EM_CTRL1 Register	Bit20 PHSI_SEL	0	To select the input source for current zero-crossing. 0: current channel IA 1: current channel IB
	Bit[19:18] SIGN_SEL	0	To select the detect method of zero-crossing: 0: negative direction (it indicates the signal changing from positive to negative is occurring a zero-crossing event) 1: positive direction (it indicates the signal changing from negative to positive is occurring a zero-crossing event) 2: positive and negative direction 3: disable the zero-crossing detection function

29.17. Waveform output and buffer

V94XX(A) waveform data can be transferred through Px, or stored locally through waveform buffer. Trigger mode supports command trigger and event trigger.

Table 29-52 Waveform output Control Register

0x07, R/W, Wave Upload And Buffer Control Register, EM_WAVE_CTRL				
Bit		R/W	Default Value	Description
31	WAVE_ADDR_CLR	R/W	0	Reset reading the address of waveform storage, write 1 to reset.
30:29	WAVE_MEM_MODE	R/W	0	The operating mode of waveform storage: 0: storage by manual, full then stop. This time is the single storage. 1: storage by manual, trigger or manual stop. This time is the cyclic storage. 2: storage by trigger, full then stop. This time is the single storage. 3: disable
28	WAVE_MEM_EN	R/W	0	Waveform storage to trigger manual switch: write 1 = enable, write 0 = disable 0: disable 1: enable
27	U_DIP_TRIG	R/W	0	Event trigger for the voltage dip. 0: disable 1: enable
26	U_SWELL_TRIG	R/W	0	Event trigger for the voltage swell. 0: disable 1: enable

0x07, R/W, Wave Upload And Buffer Control Register, EM_WAVE_CTRL				
Bit		**R/W**	**Default Value**	**Description**
25	IB_LC_TRIG	R/W	0	Event trigger for the IB under-current. 0: disable 1: enable
24	IB_OC_TRIG	R/W	0	Event trigger for the IB over-current. 0: disable 1: enable
23	IA_LC_TRIG	R/W	0	Event trigger for the IA under-current. 0: disable 1: enable
22	IA_OC_TRIG	R/W	0	Event trigger for the IA over-current. 0: disable 1: enable
21	U_LV_TRIG	R/W	0	Event trigger for Under-voltage. 0: disable 1: enable
20	U_OV_TRIG	R/W	0	Event trigger for Over-voltage. 0: disable 1: enable
19:16	WAVE_LENGTH	R/W	0	To select output waveform length 0: 1 cycle 1: 2 cycles 2: 3 cycles …… 15: 16 cycles
15	Reserved	-	-	The bit must hold its default value for proper operation.
14	WAVE_U_HPF_SEL	R/W	0	Voltage waveform whether pass high-pass filter choice: 0: no pass high-pass filter 1: pass high-pass filter
13	WAVE_IA_HPF_SEL	R/W	0	Current IA waveform whether pass high-pass filter choice: 0: no pass high-pass filter 1: pass high-pass filter
12	WAVE_IB_HPF_SEL	R/W	0	Current IB waveform whether pass high-pass filter choice: 0: no pass high-pass filter 1: pass high-pass filter
11	Reserved	-	-	The bit must hold its default value for proper operation.
10	WAVE_U_SEL	R/W	0	To enable the waveform storage and output of channel U. The bit decides whether storage or transmit data of channel U: 0: no 1: yes

0x07, R/W, Wave Upload And Buffer Control Register, EM_WAVE_CTRL				
Bit		**R/W**	**Default Value**	**Description**
9	WAVE_IA_SEL	R/W	0	To Enable the waveform storage and output of channel IA. The bit decides whether storage or transmit data of channel IA: 0: no 1: yes
8	WAVE_IB_SEL	R/W	0	To enable the waveform storage and output of channel IB. The bit decides whether storage or transmit data of channel IB (If waveform storage and configure bit 8, bit 9, and bit 10 enable at the same time, the bit becomes invalid): 0: no 1: yes
7	SP_CHECK	R/W	0	Waveform output parity check choice: 0: odd parity 1: even parity
6	SPI_POL	R/W	0	Waveform output polarity choice: 0: negative 1: positive
5	SPI_PHA	R/W	0	Waveform output phase choice: 0: negative 1: positive
4:3	WAVE_OUT_EN	R/W	0	Waveform output choice: 0: disable 1: enable by manual 2: stop by manual 3: reserved
2:0	WAVE_OUT_MODE	R/W	0	Waveform output operating mode: 0: transmit starting by manual, until maximum cycle then stops. 1: transmit starting by manual, trigger or by manual stop. 2: trigger starting, stop by manual. 3: trigger starting, until maximum cycle then stops. 4~7: transmit by manual, stop by manual. Before enabling transmission, at least one channel of waveform storage and upload must be opened.

29.17.1. Waveform Output

The V94XX(A) supports the data transmission and sends up to 3 original waveform data to the external MCU through the SPI interface host mode. The user can set the waveform output through the Wave Output And Buffer Control Register (0x07, EM_WAVE_CTRL), and configure the waveform data output IO port P2,P3 and P6 through IO configuration register 0 (0x7D, SYS_IOCFG0) and IO configuration

register 1 (0x7E, SYS_IOCFG1).

The number of sampling points per cycle of the transmission data is related to EM_MODE (Bit[7:4]) of EM_CTRL0 (Table 29-11 Metering Control Register 0 (0x02, EM_CTRL0)); the number of channels is related to Bit10~8 of EM_WAVE_CTRL (0x07, EM_WAVE_CTRL). Its relationship is shown in the following table:

Table 29-53 Active waveform data upload frequency

EM_MODE	EM_WAVE_CTRL Bit10~8	Channel	Sampling points (related to EM_MODE)	SPI frequency
0 or 10~15	111	3	128	819.2KHz
0 or 10~15	011 or 101 or 110	2	128	819.2KHz
0 or 10~15	001 or 010 or 100	1	128	409.6KHz
1 or 6	111	3	64	409.6KHz
1 or 6	011 or 101 or 110	2	64	409.6KHz
1 or 6	001 or 010 or 100	1	64	204.8KHz
3 or 7	001~111	1、2、3	32	204.8KHz

29.17.1.1. Timing and Format

The V94XX(A) transmits the original waveform of the signal to the peripheral device via the Px interface. The SPI polarity and phase are configurable. When the polarity is 0 and the phase is 0, the transmission timing is as follows:

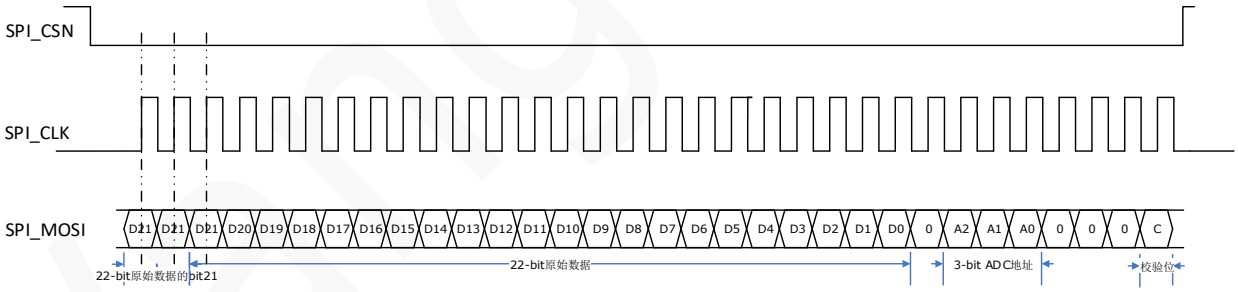


Figure 29-14 Communication timing of SPI

Transmission mode: The transmission of 32-bit data is completed at one time. The format of the data frame for each transmission is as follows:

Table 29-54 Waveform data output format

Bit	Contents
31:30	Same as Bit29.
29:8	The original waveform of 22-bit for each channel ADC signal source.
7	0
6	Indicates whether the present waveform data is

	from a voltage channel. 0: no 1: yes
5	Indicates whether the present waveform data is from a channel IA. 0: no 1: yes
4	Indicates whether the present waveform data is from a channel IB 0: no 1: yes
3:1	000
0	Odd parity bit. The check range is the forward 31bit.

29.17.2. Waveform Buffer

After the waveform buffer function is enabled, the waveform data is stored in the RAM, supporting single-channel waveform data storage and dual-channel waveform data simultaneous storage mode. If the waveform buffer of three channels is enabled at the same time, the channel IB is invalid. The user can configure the waveform buffer and start and end condition selection by Wave Output And Buffer Control Register (0x07, EM_WAVE_CTRL). After the waveform buffer configuration is completed, the user can check whether the waveform buffer is completed by the WAVE_STORE of the system interrupt status register (0x72, SYS_INTSTS). After completion, the user can obtain waveform buffer data by repeatedly reading the waveform data register (0x69, EM_DAT_WAVE), and it can read up to 309 data every time.

Table 29-55 waveform buffer data format

channel	**High 16Bit**	**Low 16Bit**
IA	$IADATA_{2n+1}$	$IADATA_{2n}$
IB	$IBDATA_{2n+1}$	$IBDATA_{2n}$
U	$UDATA_{2n+1}$	$UDATA_{2n}$
IA+IB	$IBDATA_n$	$IADATA_n$
IA+U	$IADATA_n$	$UDATA_n$
IB+U	$IBDATA_n$	$UDATA_n$
IA+IB+U (the channel IB is invalid at this time)	$IADATA_n$	$UDATA_n$

Where the range of n is 0~308

29.18. Electrical Signal monitoring

29.18.1. Zero-crossing Detection

The V94XX(A) supports zero-crossing detection for voltage channel and current channel (the zero-crossing channel can be selected as the channel IA or channel IB by Bit20 of Metering Control Register 1 (Table 29-12 Metering Control Register 1 (0x03, EM_CTRL1)). The zero-crossing direction can be

selected by Bit19~Bit18 of the metering control register 1 (0x03, EM_CTRL1). When the voltage/current channel signal has a zero-crossing event, the voltage zero-crossing flag USIGN/current zero-crossing flag ISIGN of the system interrupt status register (0x72, EM_SYS_INTSTS) is set to 1. The user needs to write 1 to clear.

Table 29-56 Zero-crossing Selection Description

Register	Bit	Default	Description
EM_CTRL1 Register	Bit20 PHSI_SEL	0	To select the input source for current zero-crossing. 0: current channel IA 1: current channel IB
	Bit[19:18] SIGN_SEL	0	To select the detect method of zero-crossing: 0: negative direction (it indicates the signal changing from positive to negative is occurring a zero-crossing event) 1: positive direction (it indicates the signal changing from negative to positive is occurring a zero-crossing event) 2: positive and negative direction 3: disable the zero-crossing detection function

When the voltage/current zero-crossing interrupt output is enabled, USIGN/ISIGN of the system interrupt enable register (0x73, EM_SYS_INTEN) is set to 1. To configure the voltage/current zero-crossing interrupt output by configuring IO Configuration Register 0 (0x7D, EM_SYS_IOCFG0) or IO Configuration Register 1 (0x7E, EM_SYS_IOCFG1). The output level of pin Px is automatically inverted according to the voltage zero-crossing flag USIGN/current zero-crossing flag ISIGN.

To configure the voltage/current zero-crossing interrupt output square wave by configuring IO Configuration Register 0 (0x7D, SYS_IOCFG0) or IO Configuration Register 1 (0x7E, EM_SYS_IOCFG1).The output level of pin Px is automatically inverted according to the voltage/current zero-crossing status in real time. Each time a zero-crossing event occurs, the IO port is inverted once.

The following figure is configured to enable the zero-crossing interrupt output. When the zero-crossing detection mode is selected as the negative zero-crossing point, the USIGN/ISIGN flag bit, the zero-crossing interrupt output, and the zero-crossing output square wave waveform.

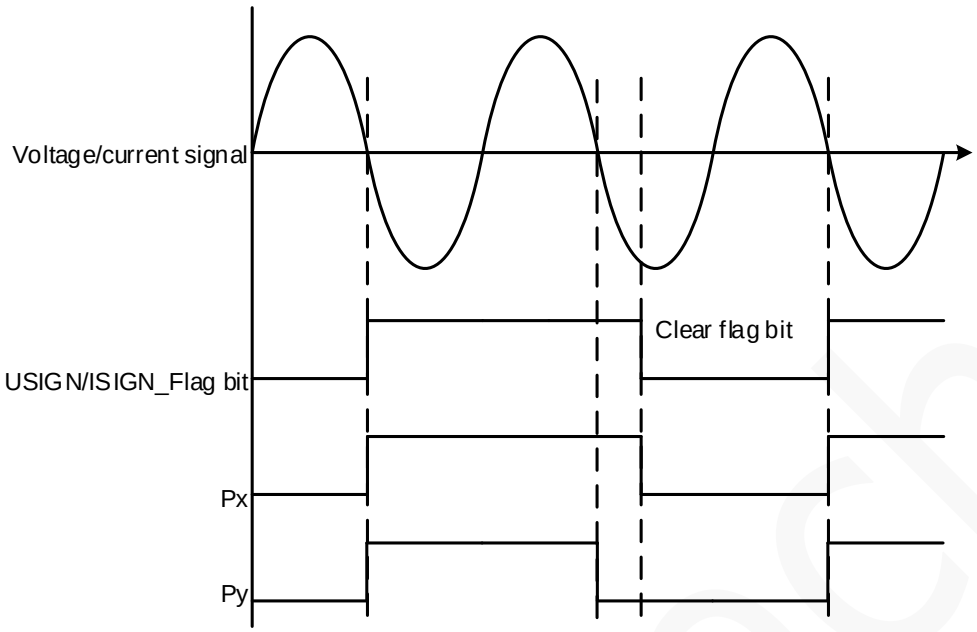


Figure 29-15 output waveform for voltage/current zero-crossing

29.18.2. Voltage Swell/Dip

The V94XX(A) can be programmed to indicate voltage swell/dip. See Table 29-26 Voltage Swell or Dip Threshold Register.

Table 29-57 Voltage Swell or Dip Threshold Register

Address	Register	R/W	Data Format	Description
0x57	EM_SWELL_THL	R/W	32-bit Complement Code	To set the lower threshold for the voltage swell.
0x58	EM_SWELL_THH	R/W	32-bit Complement Code	To set the upper threshold for the voltage swell.
0x59	EM_DIP_THL	R/W	32-bit Complement Code	To set the lower threshold for the voltage dip.
0x5A	EM_DIP_THH	R/W	32-bit Complement Code	To set the upper threshold for the voltage dip.
0x6A	EM_DAT_SWELL_CNT	R/C	32-bit Complement Code	Times records of voltage swell, half wave as a unit. 24bit effective. When write in any value, can clear zero the counter value.

Address	Register	R/W	Data Format	Description
0x6B	EM_DAT_DIP_CNT	R/C	32-bit Complement Code	Times records of voltage dip, half wave as a unit. 24bit effective. When write in any value, can clear zero the counter value.

When the voltage RMS value is above the upper limit of the voltage swell threshold, the voltage swell status bit (USWELL of the EM_SYS_STS system status register (0x74, EM_SYS_STS)) is set to 1. At the same time, the voltage swell flag (USWELL of the system interrupt status register (0x72, SYS_INTSTS)) is set to 1, and the flag bit is written to 1 to clear.

When the voltage RMS value is lower than the lower limit of the voltage swell threshold, the voltage swell status bit (USWELL of the EM_SYS_STS system status register description (0x74, EM_SYS_STS)) is restored to 0.

When the voltage RMS value is below the lower limit of the voltage dip threshold, the voltage dip status bit (UDIP of the EM_SYS_STS system status register (0x74, EM_SYS_STS)) is set to 1. At the same time, the voltage dip flag (UDIP of the system interrupt status register (0x72, SYS_INTSTS)) is set to 1, and the flag bit is written to 1 to clear.

When the voltage RMS value is lower than the lower limit of the voltage dip threshold, the voltage dip status bit (UDIP of the EM_SYS_STS system status register description (0x74, EM_SYS_STS)) is restored to 0.

At the same time, the voltage swell/sag time record can be obtained by reading the register EM_DAT_SWELL_CNT/EM_DAT_DIP_CNT, and the half wave is in units. 24Bit is valid. Write any value to this register to clear the count value.

The voltage swell interrupt flag and voltage dip interrupt flag can be configured by configuring the IO port output. See Table 29-8 IO Configuration Register 0 (0x7D, EM_SYS_IOCFGX0) and While the IO interface is not configured (i.e. all zero), output is high impedance.

- 1st type interruption: current zero-crossing interruption, voltage zero-crossing interruption, high-speed energy accumulator 1/2 overflow interruption.
- 2nd type interruption: waveform refreshes interruption, instantaneous RMS refresh interruption, average RMS refreshes interruption, instantaneous power value refresh interruption, average power value refreshes interruption, waveform storage finish interruption, waveform storage overflow interruption and waveform data upload finished interruption.
- 3rd type interruption: IB channel under-current interruption, IB channel over-current interruption, IA channel under-current interruption, IA channel over-current interruption, voltage channel under-voltage interruption, voltage channel over-voltage interruption, voltage dip interruption and voltage swell interruption.
- 4th type interruption: parameters self-checking error interruption, phase measurement finished interruption, power-down interruption, EM reference error interruption, EM clock error interruption and EM RAM self-checking error interruption.

Table 29-10 IO Configuration Register 1 (0x7E, EM_SYS_IOCFGX1).

29.18.3. Over-voltage and under-voltage/Over-current and under-current

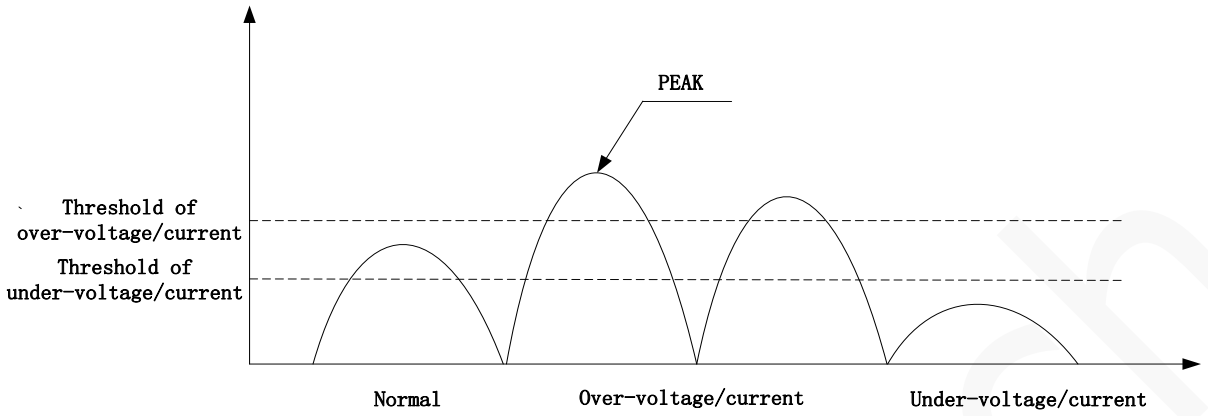


Figure 29-16 Over-voltage and under-voltage/Over-current and under-current detect

The V94XX(A) can be programmed to indicate over-voltage/under-voltage of channel U, over-voltage/under-voltage of channel IA, and over-voltage/under-voltage of channel IB. See Table 29-27 Fast detection Threshold Register. The user can enable the detection for over-voltage/under-voltage of channel U, over-current/under-current of channel IA, and over-current/under-current of channel IB by FDUEN, FDIAEN, and FFIBEN of Fast Detection Control Register (Table 29-15 Fast Detection Control Register (0x06, EM_FD_CTRL)). The detection source supports high-pass filters and by-pass. The over-voltage or under-voltage/over-current or under-current detection time length is selectable.

1) Support waveform monitoring of three ADCs.

2) Each ADC waveform monitor has two thresholds: upper threshold (over-voltage, over-current); lower threshold (under-voltage, under-current)

3) Exceeding the upper limit threshold sample points: For example, if the set value is 4, it means that if more than 4 of the half cycle sampling points exceed the upper limit threshold, the half cycle waveform is considered to exceed the upper limit.

4) Exceeding the upper threshold half-cycle number: For example, if the set value is 2, it means that if two consecutive half-cycles are exceeding the upper limit, an over-voltage or over-current event is considered to occur.

5) Below the lower limit threshold sample points: For example, if the set value is 4, it means that if low than or equal to 4 of the half cycle sampling points exceed the low limit threshold, the half cycle waveform is considered to below the lower limit.

6) below the lower threshold half-cycle number: For example, if the set value is 2, it means that if one-cycles are below the lower limit, an over-voltage or over-current event is considered to occur.

7) When the event occurs, the flag bit is generated. The user can check the system status bit (SYS_STS system status register (0x74, EM_SYS_STS)) and the flag bit (system interrupt status register (0x72, SYS_INTSTS)).

8) The corresponding event flag can be configured by interrupt enable and IO port output.

9) Response time: When IPERIOD is set to 0 and enabled or disabled the high-pass filter, the response

time is 10ms, that is, when the input signal exceeds the threshold, the event interrupt can be output after a half cycle.

Table 29-58 Fast Detection Control Register

0x06, R/W, Fast Detection Control Register, EM_FD_CTRL				
Bit		**R/W**	**Default Value**	**Description**
31:30	IPERIOD	R/W	0	To select the detection time of over-current or under-current. When the number of sampling points of over-current or under-current in the sampling points during the cycle is greater than or equal to the ITH value, it will be considered as the effective cycle. If the number of consecutive effective cycle reaches the value set by IPERIOD, it will be considered as this event happened. 0: half cycle 1: 1 cycle 2: 2 cycles 3: 4 cycles
29:24	ITH	R/W	0	To determine the threshold of cycle is effective cycle. 0: 1 time 1: 2 times … 63: 64 times
23:22	UPERIOD	R/W	0	The same as IPERIOD configurable conditions. 0: half cycle 1: 1 cycle 2: 2 cycles 3: 4 cycles
21:16	UTH	R/W	0	The same as ITH configurable conditions. 0: 1 time 1: 2 times … 63: 64 times
15:10	Reserved			These bits must hold its default value for proper operation.
9	IBLCSEL	R/W	0	IB under-current test source. 0: no pass IB wave data of high pass filter 1: pass IB wave data of high pass filter
8	IBOCSEL	R/W	0	IB: over-current test source. 0: no pass IB wave data of high pass filter 1: pass IB wave data of high pass filter
7	IALCSEL	R/W	0	IA under-current test source. 0: no pass IA wave data of high pass filter 1: pass IA wave data of high pass filter
6	IAOCSEL	R/W	0	IA over-current test source. 0: no pass IA wave data of high pass filter 1: pass IA wave data of high pass filter

0x06, R/W, Fast Detection Control Register, EM_FD_CTRL				
Bit		**R/W**	**Default Value**	**Description**
5	ULVSEL	R/W	0	Channel U under-voltage test source. 0: no pass channel U wave data of high pass filter 1: pass channel U wave data of high pass filter
4	UOVSEL	R/W	0	Channel U over-voltage test source. 0: no pass channel U wave data of high pass filter 1: pass channel U wave data of high pass filter
3	Reserved		0	The bit must hold its default value for proper operation.
2	FDIBEN	R/W	0	To enable the fast detection for IB. 0: disable IB over or under current test 1: enable IB over or under current test
1	FDIAEN	R/W	0	To enable the fast detection for IA. 0: disable IA over or under current test 1: enable IA over or under current test
0	FDUEN	R/W	0	To enable the fast detection. 0: disable channel U over or under voltage test 1: enable channel U over or under voltage test

Table 29-59 Fast detection Threshold Register

Address	Register	R/W	Data Format	Description
0x5B	EM_FD_OVTH	R/W	30-bit Complement Code	To set over-voltage threshold for fast detection. Bit width is 30bit.
0x5C	EM_FD_LVTH	R/W	30-bit Complement Code	To set under-voltage threshold for fast detection. Bit width is 30bit.
0x5D	EM_FD_IA_OCTH	R/W	30-bit Complement Code	To set over-current threshold in channel A for fast detection. Bit width is 30bit.
0x5E	EM_FD_IA_LCTH	R/W	30-bit Complement Code	To set under-current threshold in channel A for fast detection. Bit width is 30bit.
0x5F	EM_FD_IB_OCTH	R/W	30-bit Complement Code	To set over-current threshold in channel B for fast detection. Bit width is 30bit.
0x60	EM_FD_IB_LCTH	R/W	30-bit Complement Code	To set under-current threshold in channel B for fast detection. Bit width is 30bit.

29.19. Energy Accumulator

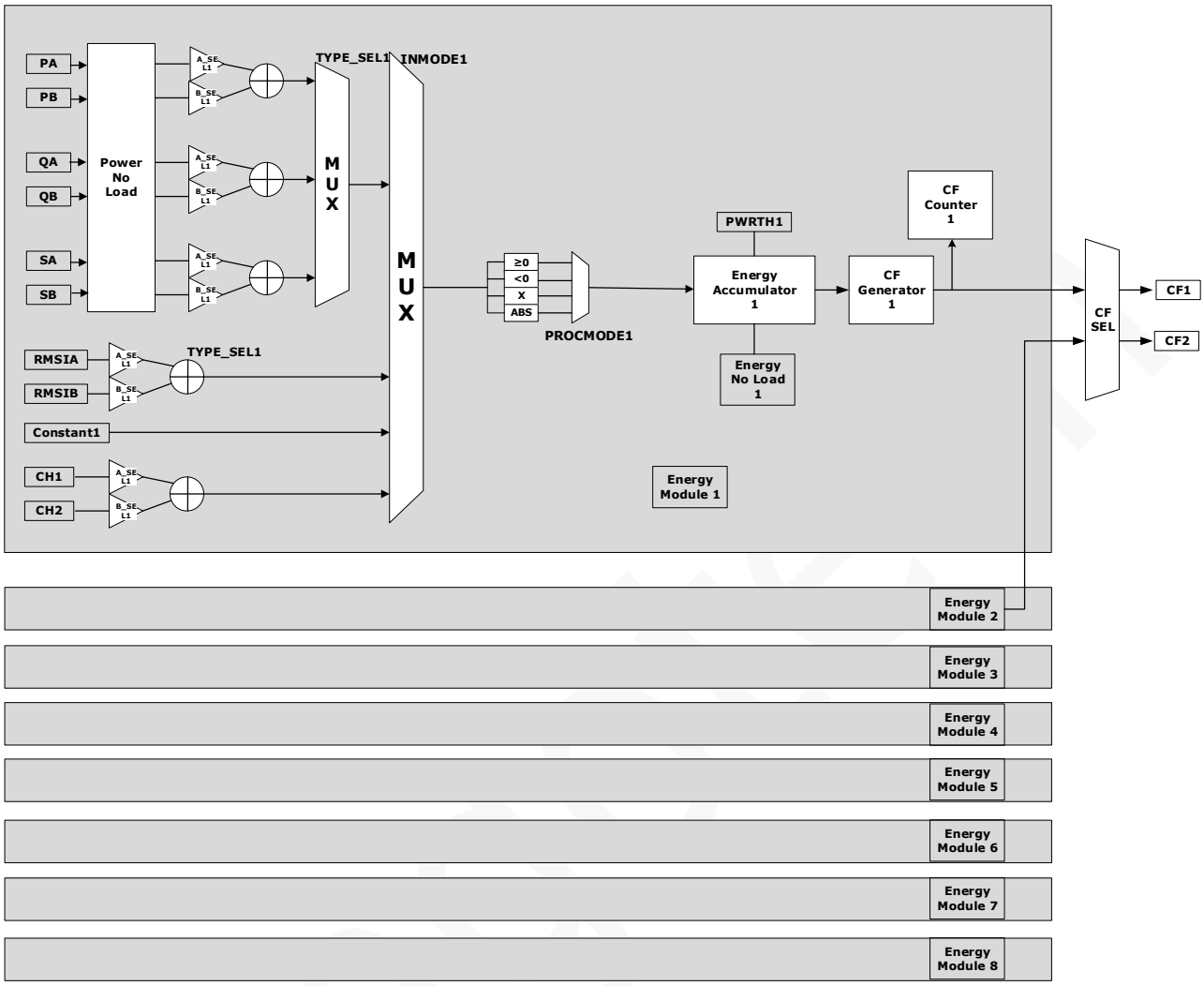


Figure 29-17 Functional block diagram of energy bucket

The V94XX(A) has eight energy accumulators, including two high-speed energy accumulators and six low-speed energy accumulators. Each energy accumulators have four accumulation modes: power accumulation, current RMS accumulation, constant accumulation, and configurable fundamental channel accumulation.

The power accumulation is enabled by the channel an accumulation (A_SEL) and the channel B accumulation (B_SEL), which can realize only accumulating channel A power, only accumulating channel B power, and accumulating A and B power. Power can be selected for active power, reactive power and apparent power by TYPE_SEL.

The current accumulation is enabled by the channel An accumulation (A_SEL) and the channel B accumulation (B_SEL), which can realize only accumulating channel IA RMS, only accumulating channel IB RMS, and accumulating IA and IB RMS. Accumulating two-channel IA and IB RMS value can be selected by TYPE_SEL to accumulate the summation or accumulation difference of two channels (RMSIA+RMSIB or RMSIA-RMSIB).

The constant accumulation is not affected by enabling the A/B channel accumulation.

The power accumulation is enabled by the channel an accumulation (A_SEL) and the channel B accumulation (B_SEL), which can realize only accumulating channel A power, only accumulating channel B power, and accumulating A and B power. Power can be selected for active power, reactive power and apparent power by TYPE_SEL.

Configurable fundamental channel accumulation, enabled by A channel accumulation (A_SEL) and B channel accumulation switch, which can realize only accumulating fundamental channel 1 data, accumulating only fundamental channel 2 data, accumulating fundamental channel 1 plus accumulating fundamental channel 2.

There are four types of data operation that are accumulated for each input energy accumulator. Taking the active power of two channels as an example, the operation method is as follows.

0: The energy accumulator only accumulates positive numbers. Only accumulate data with PA+PB>0. If PA+PB<0, do not accumulate.

1: The energy accumulator only accumulates negative numbers (in this case, the actual accumulated value is a positive value of the original value conversion). Only data with PA+PB<0 (abs (PA+PB)) is added. If PA+PB>0, do not accumulate.

2: The energy accumulator accumulates the original value. Accumulate PA+PB.

3: The energy accumulator accumulates the absolute value. Accumulate abs (PA+PB)

EM_EGY_PWRTH is the accumulation threshold for energy accumulator. Due to the energy accumulator was 46bit, the accumulated value of the high-speed energy accumulator equals to this value*16384; the accumulated value of the low-speed energy accumulator equals to this value*4.

Table 29-60 Energy Accumulato Setting Description

Register	Bit	Default	Description
EM_EGY_CTRL0 Register EM_EGY_CTRL1 Register	INMODEx[1:0]	0	The energy accumulator x accumulating mode. 0: power accumulation 1: current RMS accumulation 2: constant accumulation 3: configurable fundamental-wave channel accumulation
	A_SELx	0	To enable the energy accumulator x, channel A accumulating. 0: disable 1: enable
	B_SELx	0	To enable the energy accumulator x, channel B accumulating. 0: disable 1: enable
	TYPE_SELx	0	The energy accumulator x, multiple channel accumulating mode choice. When power accumulating, 0, 3: active power accumulation 1: reactive power accumulation 2: apparent power accumulation When RMS accumulating, high bit zero represents accumulating sum; High bit one represents accumulating difference.
	PROCMODEx	0	For each signal type choices which feed into the energy accumulator x. 0: the positive value of the energy accumulator adding 1: the negative value of the energy accumulator adding (Here the actual accumulating value is the positive which exchanged from the original value.) 2: the original value of the energy accumulator adding 3: the absolute value of the energy accumulator adding

Table 29-61 Energy Accumulator Register

Address	Register	R/W	Data Format	Description
0x39	EM_EGY_PROCTH	R	32-bit Unsigned	Anti-creep threshold for energy accumulator. When the accumulated value of the anti-creep energy accumulator over this threshold and the accumulated value of the high-speed energy accumulator under this threshold, the accumulated value of the high-speed energy accumulator will be cleared.
0x3A	EM_EGY_PWRTH	R/W	32-bit Unsigned	Accumulation threshold for energy accumulator. Due to the energy accumulator was 46bit, the accumulated value of the high-speed energy accumulator equals to this value*16384; the

				accumulated value of the low-speed energy accumulator equals to this value*4.
0x3B+x*4	EM_EGY_CONSTx	R/W	32-bit Unsigned	Energy accumulator x accumulating constant.
0x3C+x*4	EM_EGY_OUTxL	R/W	32-bit Unsigned	Energy accumulator x accumulating low bit.
0x3D+x*4	EM_EGY_OUTxH	R/W	32-bit Unsigned	Energy accumulator x accumulating high bit Low 14bit effective.
0x3E+x*4	EM_EGY_CFCNTx	R/W	32-bit Unsigned	Energy accumulator x pulse counter.

29.19.1. High-speed Energy Accumulator

To enable high-speed energy accumulator 1, it needs to configure CALCEN1 (Bit[6]) in EM_CTRL1 (Table 29-12 Metering Control Register 1 (0x03, EM_CTRL1)). To enable high-speed energy accumulator 2, it needs to configure CALCEN2 (Bit[7]) in EM_CTRL1. The default accumulative acceleration of the high-speed energy accumulator is 204.8 KHz, and 32768 Hz can also be selected by the energy accumulator clock (bit23 in EM_CTRL1).

High-speed energy accumulator supports CF output.

29.19.2. Low-speed Energy Accumulator

The six low-speed energy accumulators are enabled by DGY_LC_EN (Bit[15]) in EM_CTRL1 (Table 29-12 Metering Control Register 1 (0x03, EM_CTRL1)). The default accumulated acceleration is 50Hz.

The accumulation speed of low-speed energy accumulator is controlled by CUREM_DAT_RATE (Bit[31]) in EM_CTRL0 (Table 29-11 Metering Control Register 0 (0x02, EM_CTRL0)) and LCF_ACC (Bit[22]) in EM_CTRL1.

When CUREM_DAT_RATE=0:

LCF_ACC=0, the accumulation period of the energy buckets 3, 4, 5, 6, 7, 8 is 20 ms;

LCF_ACC=1, the accumulation period of the energy buckets 3, 4, and 5 is 10 ms, and the energy buckets 6, 7, and 8 are not accumulated.

- When CUREM_DAT_RATE=0:

LCF_ACC=0, the accumulation period of the energy accumulators 3, 4, 5, 6, 7, 8 is 20ms;

LCF_ACC=1, the accumulation period of the energy accumulators 3, 4, and 5 is 10ms, and the energy accumulators 6, 7, and 8 are not accumulated.

- When CUREM_DAT_RATE=1:

LCF_ACC=0, the accumulation period of the energy accumulators 3, 4, 5, 6, 7, 8 is 40ms;

LCF_ACC=1, the accumulation period of the energy accumulators 3, 4, and 5 is 20ms, and the energy accumulators 6, 7, and 8 are not accumulated.

29.19.3. Energy Accumulator creep Detection

EM_EGY_PROCTH is the energy accumulator anti-creep threshold. When anti-creep energy accumulator exceeds the EM_EGY_CRPTH and high-speed energy accumulator not exceeds the EM_EGY_PWRTH, the accumulating value of high-speed accumulator will be cleared.

V94XX(A) has an energy-creep energy accumulating register for energy accumulator 1 and 2 respectively, and they have the same accumulation speed. After enabling the energy-creep detection in the energy accumulator, the input would be fixed to 1 in this energy-creep energy accumulator.

User should configure threshold for the energy-creep detection register (EM_EGY_CRPTH) and energy accumulating threshold register (EM_EGY_PWRTH). If the accumulating value of energy-creep energy accumulator register reaches the value of EM_EGY_CRPTH first, the energy accumulating register will be cleared, and system enter the energy-creep status. When the accumulating value of energy accumulating register reaches the value of EM_EGY_PWRTH first, the energy-creep energy register will be cleared, system starts to work and operates normally.

The actual bit width of register EM_EGY_CRPTH is 32bit. The register contents will be padded with 0s automatically in the 4 least significant bits when the energy-creep calculated. It would be calculated after extended to 36 digits.

EM_EGY_PWRTH is the accumulation threshold for energy accumulator. Due to the energy accumulator was 46bit, the accumulated value of the high-speed energy accumulator equals to this value*16384.

User can judge whether in energy-creep status through EM_SYS_STS (BIT19, BIT18).

Table 29-62 Energy-creep Detection Description

Register	Bit	Default	Description
EM_CTRL1 Register	Bit0 EGY_CRP_EN	0	To determine energy-creep of the High-speed energy accumulator 0: disable the energy-creep detection 1: enable the energy-creep detection
EM_SYS_STS Register	Bit19 CRP_OUT2	0	Status bit for energy-creep detection for energy accumulator 2. 0: start 1: energy-creep
	Bit18 CRP_OUT1	0	Status bit for energy-creep detection for energy accumulator 1. 0: start 1: energy-creep

Table 29-63 Threshold Register

Address	Register	Default Value	R/W	Data Format	Description
0x39	EM_EGY_PROCTH	0	R/W	32-bit Complement Code	Energy accumulator anti-creep threshold.

0x3A	EM_EGY_PWRTH	0	R/W	32-bit Complement Code	Accumulation threshold for energy accumulator.

29.20. CF Output

V94XX(A) supports 2 channels of CF. The CF output is configured by the Meter Control Register 1 (Table 29-12 Metering Control Register 1 (0x03, EM_CTRL1)) to select the IO port output.

When energy bucket 1 or 2 enables energy accumulation and energy pulse counting, V94XX (A) accumulates the data to be accumulated to the energy accumulation register at a certain frequency according to the energy bucket configuration. When the value of the energy accumulation register exceeds the corresponding energy pulse threshold value, add 1 to the corresponding energy pulse counter, and subtract an energy pulse threshold value from the accumulated data of the energy accumulation register. If CF output is enabled, An energy pulse is generated.

CF supports source selection. It can be selected from the energy accumulator 1 or the energy accumulator 2.

CF supports polarity selection, pulse width selection, and accelerated weak-signal calibration.

Refer to the description of CF in Metering Control Register 1 (0x03, EM_CTRL1) for details.

Table 29-64 Active data uploading interface setting Description

Register	Bit	Default	Description
EM_CTRL1 Register	Bit14 CF2_INV	0	To control the CF2 polarity. 0: original polarity 1: reverse polarity
	Bit13 CF2_EN	0	To Enable the CF2 output. 0: disable 1: enable.
	Bit12 CF2_SEL	0	To select the input source of CF2. 0: from the energy accumulator 1 1: from the energy accumulator 2
	Bit10 CF1_INV	0	To control CF1 polarity. 0: original polarity 1: reverse polarity
	Bit9 CF1_EN	0	To enable CF1 output. 0: disable CF1 output 1: enable CF1 output
	Bit8 CF1_SEL	0	To select the input source of CF1. 0: from the energy accumulator 1 1: from the energy accumulator 2
	Bit[5:4] CF_PULSE	0	To select the CF pulse width 0: 80 ms 1: 40 ms 2: 20 ms 3: 10 ms
	Bit[3:2] CF_FAST_EN	0	CF pulse speed up output. 0: Normal mode 1: 4x faster 2: 8x faster 3: 16x faster

29.21. Signal IO Ports

The V94XX(A) provides up to five signal outputs, and five output signals are used to map the internal output sources.

The five signal output ports can be configured as CF output, energy upload interface, waveform output interface, zero-crossing square wave and four types of interrupt output. The signal output port can be set to output a single signal, or it can be set to output certain types of interrupt signals. See Table 29-8 IO Configuration Register 0 (0x7D, EM_SYS_IOCFGX0) and While the IO interface is not configured (i.e. all zero), output is high impedance.

- 1st type interruption: current zero-crossing interruption, voltage zero-crossing interruption, high-speed energy accumulator 1/2 overflow interruption.
- 2nd type interruption: waveform refreshes interruption, instantaneous RMS refresh interruption, average RMS refreshes interruption, instantaneous power value refresh interruption, average power value refreshes interruption, waveform storage finish interruption, waveform storage overflow interruption and waveform data upload finished interruption.

- 3rd type interruption: IB channel under-current interruption, IB channel over-current interruption, IA channel under-current interruption, IA channel over-current interruption, voltage channel under-voltage interruption, voltage channel over-voltage interruption, voltage dip interruption and voltage swell interruption.
- 4th type interruption: parameters self-checking error interruption, phase measurement finished interruption, power-down interruption, EM reference error interruption, EM clock error interruption and EM RAM self-checking error interruption.

Table 29-10 IO Configuration Register 1 (0x7E, EM_SYS_IOCFGX1) for details.

1st type interruption: current zero-crossing interruption, voltage zero-crossing interruption

2nd type interruption: waveform refreshes interruption, instantaneous RMS refresh interruption, average RMS refreshes interruption, instantaneous power value refresh interruption, average power value refreshes interruption, waveform storage finish interruption, waveform storage overflow interruption and waveform data upload finished interruption.

3rd type interruption: IB channel under-current interruption, IB channel over-current interruption, IA channel under-current interruption, IA channel over-current interruption, voltage channel under-voltage interruption, voltage channel over-voltage interruption, voltage dip interruption and voltage swell interruption.

4th type interruption: parameters self-checking error interruption, phase measurement finished interruption, power-down interruption, EM reference error interruption, EM clock error interruption and EM RAM self-checking error interruption.

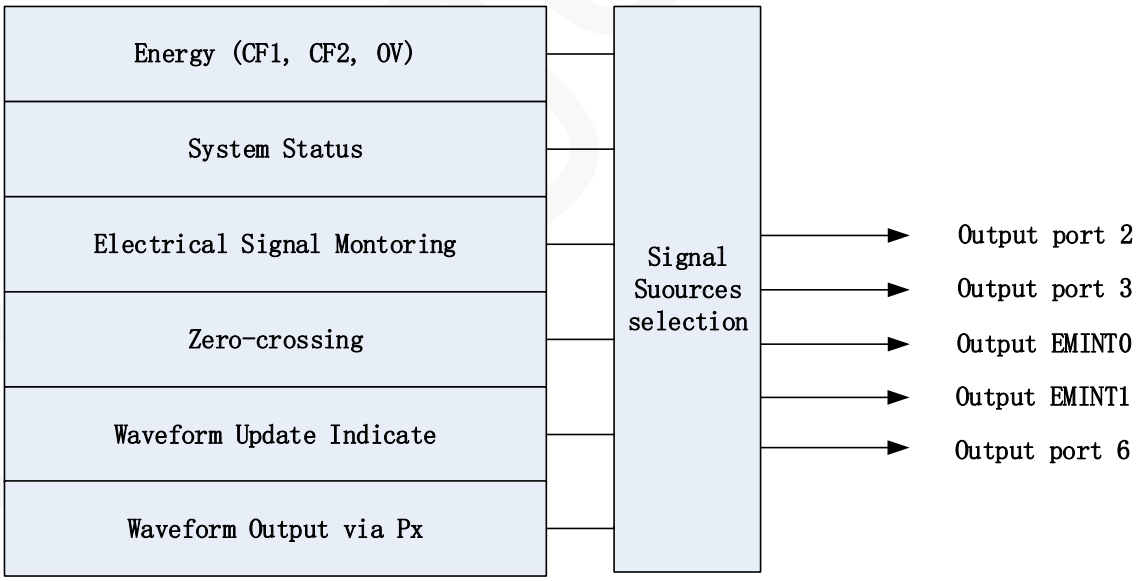


Figure 29-18 Functional Block Diagram of signal IO ports

Description:

1) When the output port is used as the CF output, it is supported to set the width of the output pulse and select the output polarity. When the output period is less than twice the CF output pulse width, CF is output at a duty cycle of 50%. For example, if the output width is 80ms and the output period is less than 160ms, it will be output according to the duty cycle of 50%.

2) When used as the interrupt event output port, the output port defaults to low level output. If the event occurs, it outputs a high level until the user clears the event flag bit, and the output state returns to the default level.

3) When used as a zero-crossing square wave output, the output port defaults to a low-level output. If configured as a positive zero-crossing, the IO port flips when the signal transitions from a negative signal to a positive signal.

4) When used as a output port, the SPI protocol is required, and the user is required to select the SPI_CLK, SPI_MOSI, and SPI_CSN ports.

Table 29-65 IO Configuration Register 0 (0x7D, EM_SYS_IOCFGX0)

0x7D, IO Configuration Register 0, EM_SYS_IOCFGX0				
Bit		**R/W**	**Default Value**	**Description**
31:24	P3CFG	R/W	0	Configuration as the same as P0CFG.
23:16	P2CFG	R/W	0	Configuration as the same as P0CFG.
15:8	P1CFG	R/W	0	Configuration as the same as P0CFG.
7:0	P0CFG	R/W	0	Bit[7:6]: 00: as shown in the Table 29-9, it can be configured the different combination interruption. 10: CF1 output. Bit[5:0] can be configured arbitrary value. 01: CF2 output. Bit[5:0] can be configured arbitrary value. 11: Actively energy accumulation data uploads. Bit[5:0] can be configured arbitrary value.

Table 29-66 P0CFG Bit[5:0] Description

Bit[5:3]	**Bit[2:0]**	**Description**
0	0	High impedance.
0	1	Current zero-crossing interruption.
0	2	Voltage zero-crossing interruption.
0	3	Current zero-crossing interruption.
0	4	Voltage zero-crossing interruption.
0	5	High-speed energy accumulator 1 overflow interrupt
0	6	High-speed energy accumulator 2 overflow interrupt
0	7	1st type interruption.
1	0	Waveform refresh interruption.
1	1	Instantaneous RMS refresh interruption.
1	2	Average RMS refresh interruption.
1	3	Instantaneous power refresh interruption.
1	4	Average power refresh interruption.
1	5	Waveform storage finish interruption.
1	6	Waveform storage address overflow interruption.
1	7	Waveform data upload finish interruption.
2	0	IB channel under-current interruption.
2	1	IB channel over-current interruption.
2	2	IA channel under-current interruption.
2	3	IA channel over-current interruption.

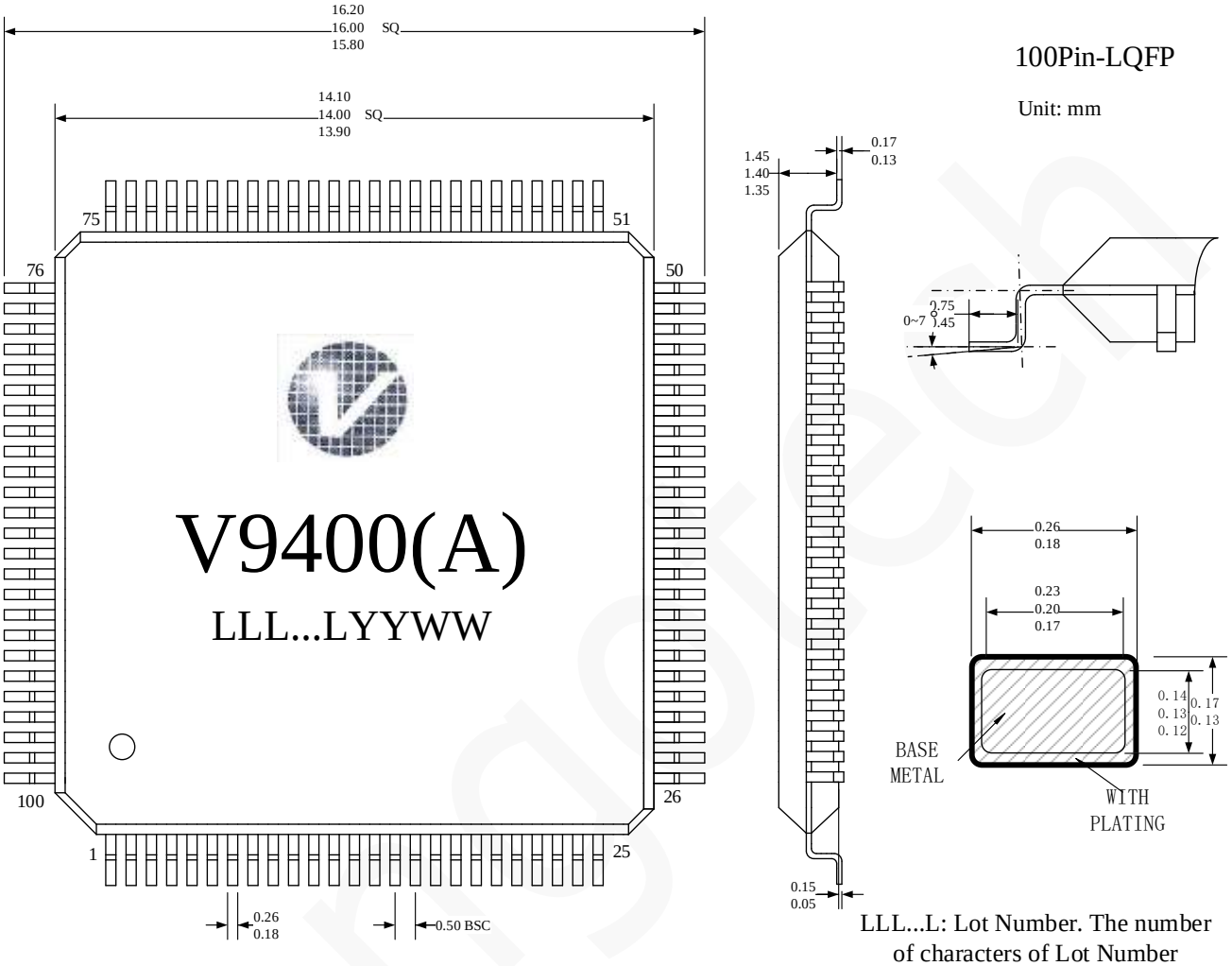
2	4	Voltage Channel under-voltage interruption.
2	5	Voltage Channel over-voltage interruption.
2	6	Voltage dip interruption.
2	7	Voltage swell interruption.
3	0	EM Reference error.
3	1	EM clock error.
3	2	Reserved
3	3	Reserved
3	4	Power-down interruption.
3	5	Parameter self-checking error interruption.
3	6	Phase test finish interruption.
3	7	EM RAM self-checking error.
4	0	1st type interruption.
4	1	2nd type interruption.
4	2	3rd type interruption.
4	others	4th type interruption.
5	0	3rd type interruption.
5	1	1st and 2nd type interruption.
5	2	1st and 3rd type interruption.
5	3	1st and 4th type interruption.
5	4	2nd and 3rd type interruption.
5	5	2nd and 4th type interruption.
5	6	3rd and 4th type interruption.
5	7	All interruption.
6	0	1st, 2nd and 3rd type interruption.
6	1	1st, 2nd and 4th type interruption.
6	2	1st, 3rd and 4th type interruption.
6	3	2nd, 3rd and 4th type interruption.
6	others	All interruption.
7	1	Active waveform updating for chip select of SPI, SPI_CSN.
7	2	Active waveform updating for SPI clock, SPI_CLK.
7	4	Active waveform updating for SPI data, SPI_MOSI.
7	others	Prohibited output.

Table 29-67 IO Configuration Register 1 (0x7E, EM_SYS_IOCFGX1)

0x7E, IO Configuration Register1, EM_SYS_IOCFGX1				
Bit		**R/W**	**Default Value**	**Description**
31:24	Reserved		0	These bits must hold its default value for proper operation.
23:16	P6CFG	R/W	0	Configuration as the same as P0CFG.
15:8	P5CFG	R/W	0	Configuration as the same as P0CFG.
7:0	P4CFG	R/W	0	Configuration as the same as P0CFG.

30. Outline Dimensions

30.1. Outline Dimensions_V9400(A)

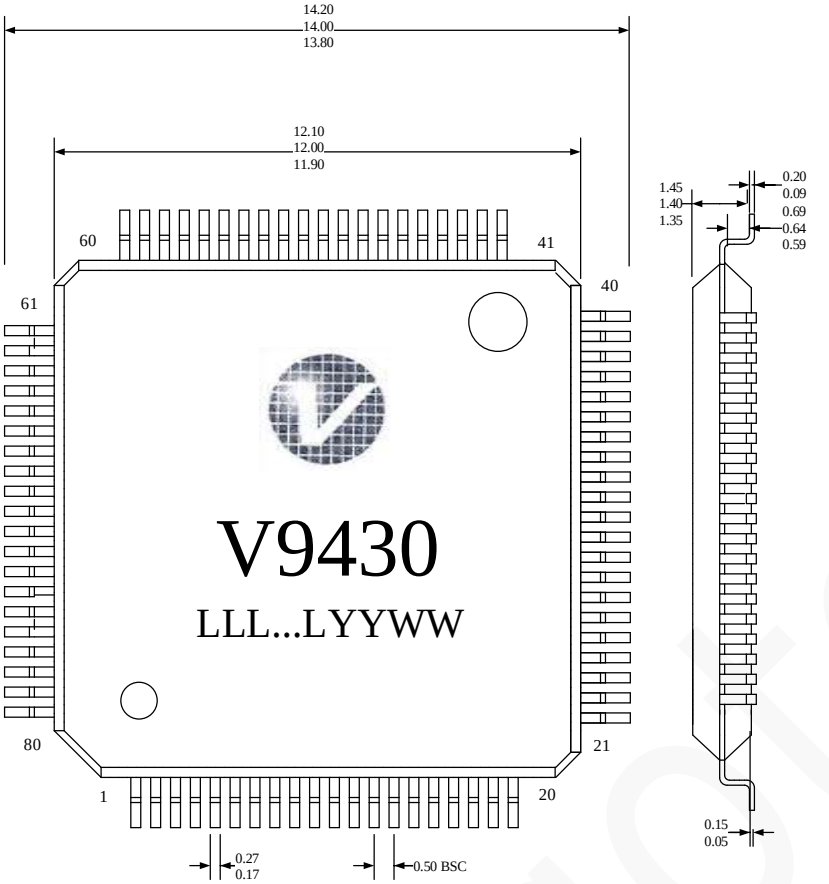


100Pin-LQFP

Unit: mm

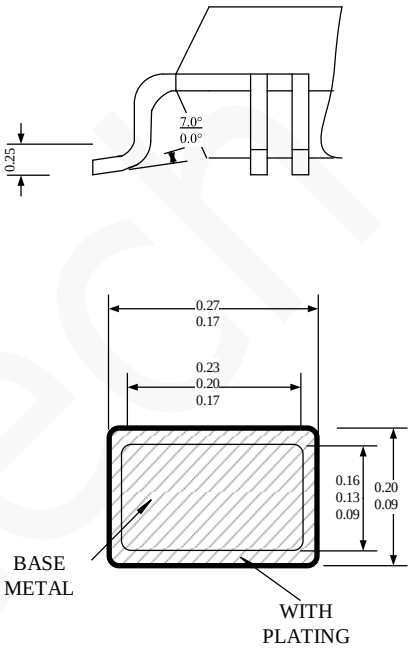
LLL...L: Lot Number. The number of characters of Lot Number varies between 8 to 11.
YY: Year
WW: Week

30.2. Outline Dimensions_V9430



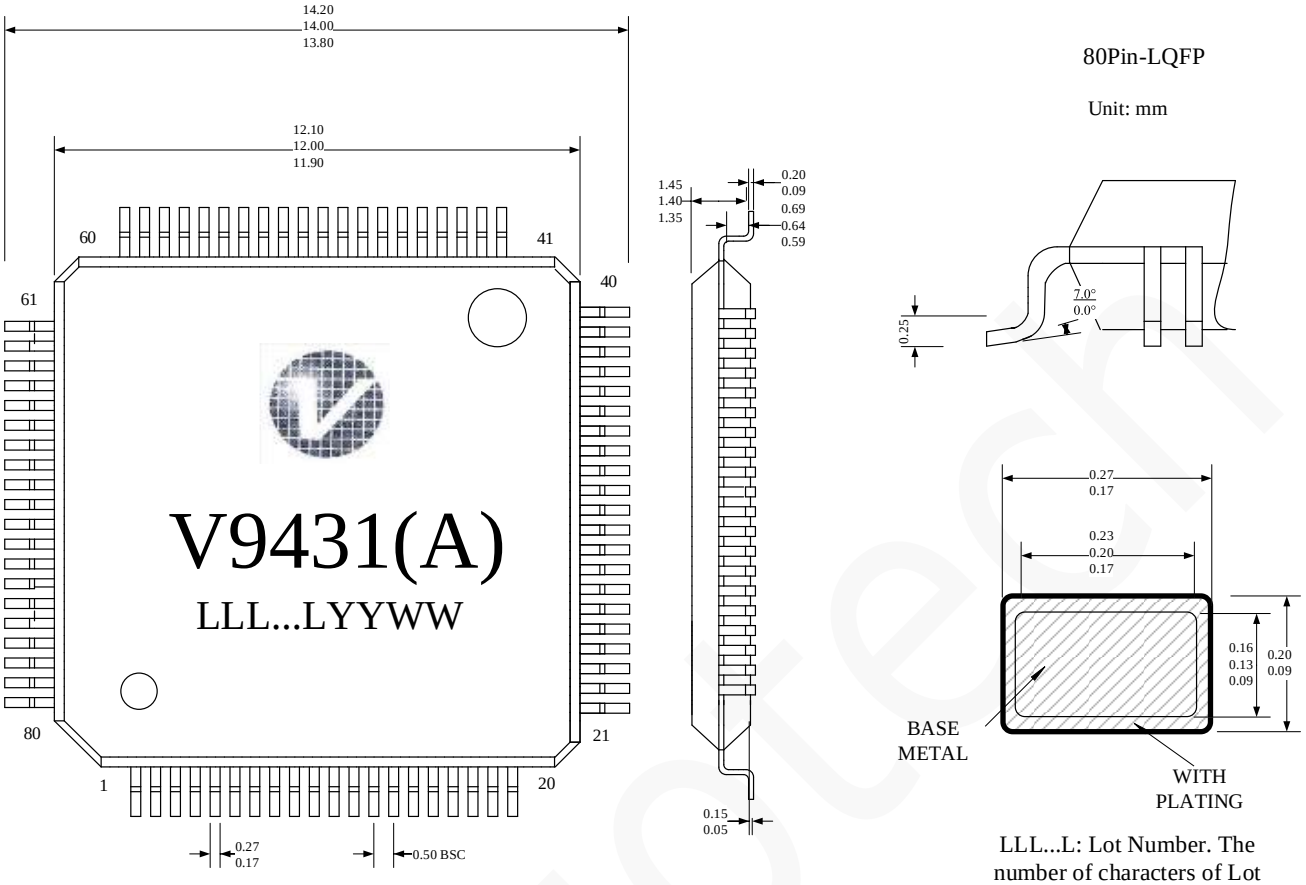
80Pin-LQFP

Unit: mm



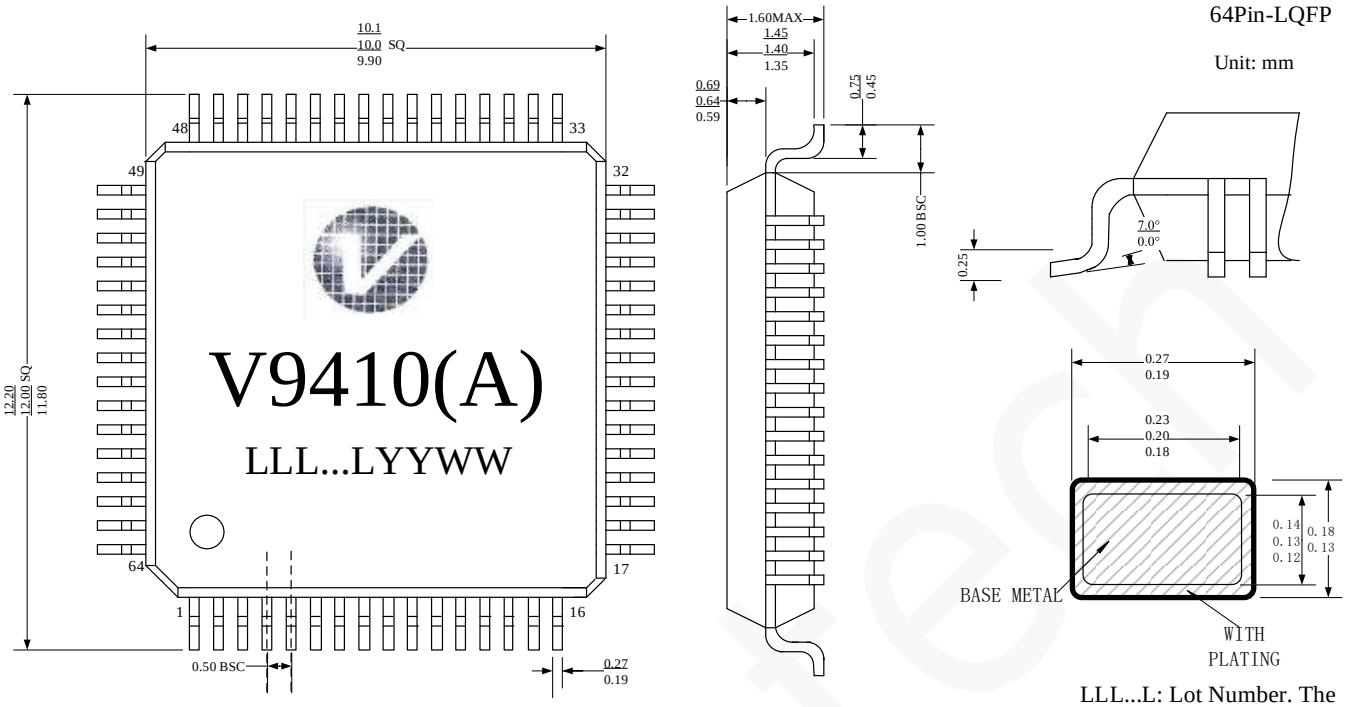
LLL...L: Lot Number. The number of characters of Lot Number varies between 8 to 11.
YY: Year
WW: Week

30.3. Outline Dimensions_V9431(A)



LLL...L: Lot Number. The number of characters of Lot Number varies between 8 to 11.
YY: Year
WW: Week

30.4. Outline Dimensions_V9410(A)



LLL...L: Lot Number. The number of characters of Lot Number varies between 8 to 11.
YY: Year
WW: Week

30.5. Outline Dimensions_V9420A

48Pin-LQFP

Unit：mm