V9203

Multifunction 3-Phase Energy Metering IC

- Highly accurate:
  - ✓ Supports IEC 62053-21:2020,IEC 62053-22:2020 and IEC 62053-23:2020;
  - ✓ <0.1% error in active energy over a dynamic range of 10000:1;
  - ✓ <0.1% error in reactive energy over a dynamic range of 5000:1;
- Supplies Irms, Vrms, active/reactive/apparent power, active/reactive/apparent energy, line frequency, phase, and power factor of every phase and on the overall system;
- Supports neutral current input;
- Supplies raw waveform of current and voltage in DMA mode with updating frequency of 6.4 KHz;
- Supports low power operating modes;
- Supports software calibration:
  - ✓ Phase compensation in 5 sections over the range of ±2.8°;
  - ✓ Gain calibration in 3 sections and offset calibration of total active power;
  - ✓ Gain and offset calibration of total/fundamental reactive power and fundamental active power;
  - ✓ Accelerating calibration when weak current is applied;
  - ✓ Self-check of the configuration for the calibration;
- Supports current transformer and di/dt current sensor;
- Supports 3-phase, 3-wire service, and 3-phase, 4-wire service;
- Single 3.3V supply, wide range: 2.6V~3.6V;
- Internal reference: 1.185V (drift 10ppm/°C);
- Supports SPI communication;
- Crystal frequency: 13.1072MHz;
- Operating temperature: -40~+85°C;
- Storage temperature: -55~+150°C;
- Package: 44 – LQFP.

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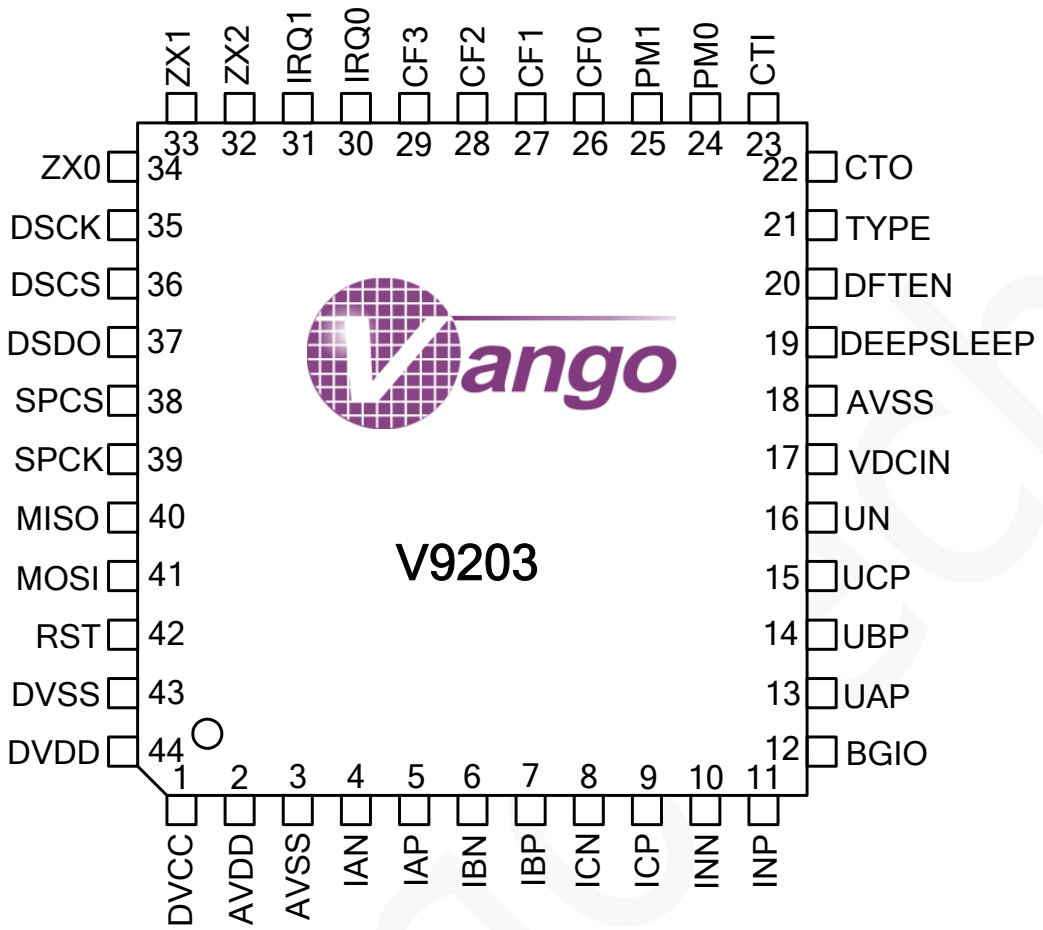
3. Pin Description



*AVDD: Both Pin2 and Pin21 must be used for analog 3.3V voltage input simultaneously.

**AVSS: Both Pin3 and Pin18 must be grounded simultaneously.

No.	Mnemonic	Type	Description
1	DVCC	Power	Digital power output. This pin must be connected to a parallel circuit combined by a 10μF capacitor and 0.1μF capacitor.
2	AVDD	Power	3.3-V power supply.
3	AVSS	Ground	Analog ground.
4~5	IAN, IAP	Input	Analog input pins for Current Channel A (IA).
6~7	IBN, IBP	Input	Analog input pins for Current Channel B (IB).
8~9	ICN, ICP	Input	Analog input pins for Current Channel C (IC).
10~11	INN, INP	Input	Analog input pins for Neutral Current Channel (IN).
12	BGIO	Input /	On-chip reference. This pin must be connected to a 1μF capacitor.

No.	Mnemonic	Type	Description	
		Output		
13	UAP	Input	Positive input pin for Voltage Channel A (UA).	
14	UBP	Input	Positive input pin for Voltage Channel B (UB).	
15	UCP	Input	Positive input pin for Voltage Channel C (UC).	
16	UN	Input	Negative input pin for the three voltage channels.	
17	VDCIN	Input	Power supply monitor input. When the level on this pin is higher than 1.1-V, the power supply is in a normal state. When the level on this pin is lower than 1.0-V, the system is powered down.	
18	AVSS	Ground	Analog ground.	
19	DEEPSLEEP	Input	Deep sleep enable pin. Hold high logic for more than 4ms to enable the system entering the deep sleep state. Hold low logic for more than 4ms to wake up and retrieve the system.	
20	DFTEN	Input	DFT enable pin, high active. Hold low logic for proper operation.	
21	TYPE	Input	Hold high logic for proper operation.	
22	CTO	Output	Crystal output.	The load capacitance (CL) of the embedded oscillator is 10-pF. Both pins must be directly connected to a 13.1072-MHz crystal with about 8-pF CL for clock generation. Both pins must be connected to a 15-pF capacitor respectively, which increases the power consumption by about 36-μA, and then to a 13.1072-MHz crystal with about 18-pF CL.
23	CTI	Input	Crystal input.	

No.	Mnemonic	Type	Description
24~25	PM0, PM1	Input	Operation mode select input. PM0, 0; PM1, 0: Sleep (not recommended). In this operation mode, only the RC oscillator, the crystal oscillator, the digital power circuit, the clock management circuit, the reset circuits, and the filters for input signals on the pins PM0/PM1/RST/DFTEN, are operating, other circuits stop working. The memory and register configuration hold the values. PM0, 1; PM1, 0: power-off/no-voltage pre-detection mode. In this operation mode, only the RC oscillator, the crystal oscillator, the digital power circuit, the current channels of Phase A/B/C, the clock scaler, the Bandgap circuit, the clock management circuit, the reset circuits, the filters for input signals on the pins PM0/PM1/RST/DFTEN, the phase compensation circuit, the CIC filter, the current detection circuit, the interrupt circuits, and the SPI interfaces, are operating, other circuits stop working. In this mode, the SPI interfaces cannot communicate normally. Users can detect the current signal for energy metering via the no-voltage interrupt of the current channel. PM0, 0; PM1, 1: RMS mode. In this operation mode, only the RC oscillator, the crystal oscillator, the digital power circuit, the current channels of Phase A/B/C, the clock scaler, the Bandgap circuit, the clock management circuit, the reset circuits, the filters for input signals on the pins PM0/PM1/RST/DFTEN, the phase compensation circuit, the CIC filter, the RMS/power/power factor calculation circuits, the normal and high-speed energy accumulation circuits, the pulse generation circuits, DC-stopping circuits, the current detection circuit, the frequency/phase measurement circuit, the interrupt circuits, and the SPI interfaces, are operating, other circuits stop working. The master MCU can read the fundamental current RMS of each phase. PM0, 1; PM1, 1: normal operation mode. In this mode, all circuits can work according to the register configurations. All the registers, except the analog control registers, must be configured in this mode.
26	CF0	Output	CF pulse output. Via configuring the registers ZZPA0 (0xEC23) or ZZPA1 (0xEC24), this pin can be used to output total or fundamental active energy CF pulse of each phase or on the overall system.
27	CF1	Output	CF pulse output. Via configuring the registers ZZQA0 (0xEC47) or ZZQA1 (0xEC48), this pin can be used to output total or fundamental reactive energy CF pulse of each phase or on the overall system.

No.	Mnemonic	Type	Description	
28	CF2	Output	CF pulse output. Via configuring the registers ZZPA0 (0xEC23) or ZZPA1 (0xEC24), this pin can be used to output total or fundamental active energy CF pulse of each phase or on the overall system.	
29	CF3	Output	CF pulse output. Via configuring the registers ZZQA0 (0xEC47), ZZQA1 (0xEC48), or ZZAPPA (0xEC05), this pin can be used to output total reactive energy CF pulse, or total/fundamental apparent energy CF pulse of each phase or on the overall system.	
30	IRQ0	Output	Interrupt Output 0.	Configure the registers IRQEN0 or IRQEN1 to enable the interrupts generation and output on the pin IRQ0 or IRQ1.
31	IRQ1	Output	Interrupt Output 1.	
32	ZX2	Output	This pin outputs the sign of the Voltage Channel C. 1, negative; 0, positive. When the output of this pin is on the transition from logic "1" to "0", meaning the signal of Voltage Channel C is crossing zero positively, the pins IRQ0 or IRQ1 will output zero-crossing interrupt.	
33	ZX1	Output	This pin outputs the sign bit of the Voltage Channel B. 1, negative; 0, positive. When the output of this pin is on the transition from logic "1" to "0", meaning the signal of Voltage Channel B is crossing zero positively, the pins IRQ0 or IRQ1 will output zero-crossing interrupt.	
34	ZX0	Output	This pin outputs the sign bit of the Voltage Channel A. 1, negative; 0, positive. When the output of this pin is on the transition from logic "1" to "0", meaning the signal of Voltage Channel A is crossing zero positively, the pins IRQ0 or IRQ1 will output zero-crossing interrupt.	
35	DSCK	Output	DMA_SPI interface in mater mode. This pin is used to output the serial communication clock.	

No.	Mnemonic	Type	Description
36	DSCS	Output	DMA_SPI interface in master mode. This pin is used to select the slave, active low. When this pin outputs high logic, the DMA_SPI circuit is reset, and DSDO outputs low logic.
37	DSDO	Output	DMA_SPI interface in master mode. This pin is used to output the serial communication data.
38	SPCS	Input	SPI interface in slave mode. This pin is used for salve select, low active. When this pin holds high logic, the SPI circuit is reset, and enables the pin MISO to follow the MOSI input level state.
39	SPCK	Input	SPI interface in slave mode. This pin is used for clock input.
40	MISO	Output	SPI interface in slave mode. This pin is used for data output.
41	MOSI	Input	SPI interface in slave mode. This pin is used for data input.
42	RST	Input	Reset input, low active. Hold low logic for at least 5ms to reset the system.
43	DVSS	Ground	Digital ground.
44	DVDD	Power	3.3-V digital power supply.

4. Absolute Maximum Ratings

Operating circumstance exceeding **"Absolute Maximum Ratings"** may cause the permanent damage to the device.

Parameter	Min.	Max.	Unit	Description
Analog Current Input	-0.3	+3.3	V	Relative to ground.
Analog Voltage Input	-0.3	+3.3	V	Relative to ground.
Operating Temperature	-40	+85	°C	
Storage Temperature	-55	+150	°C	

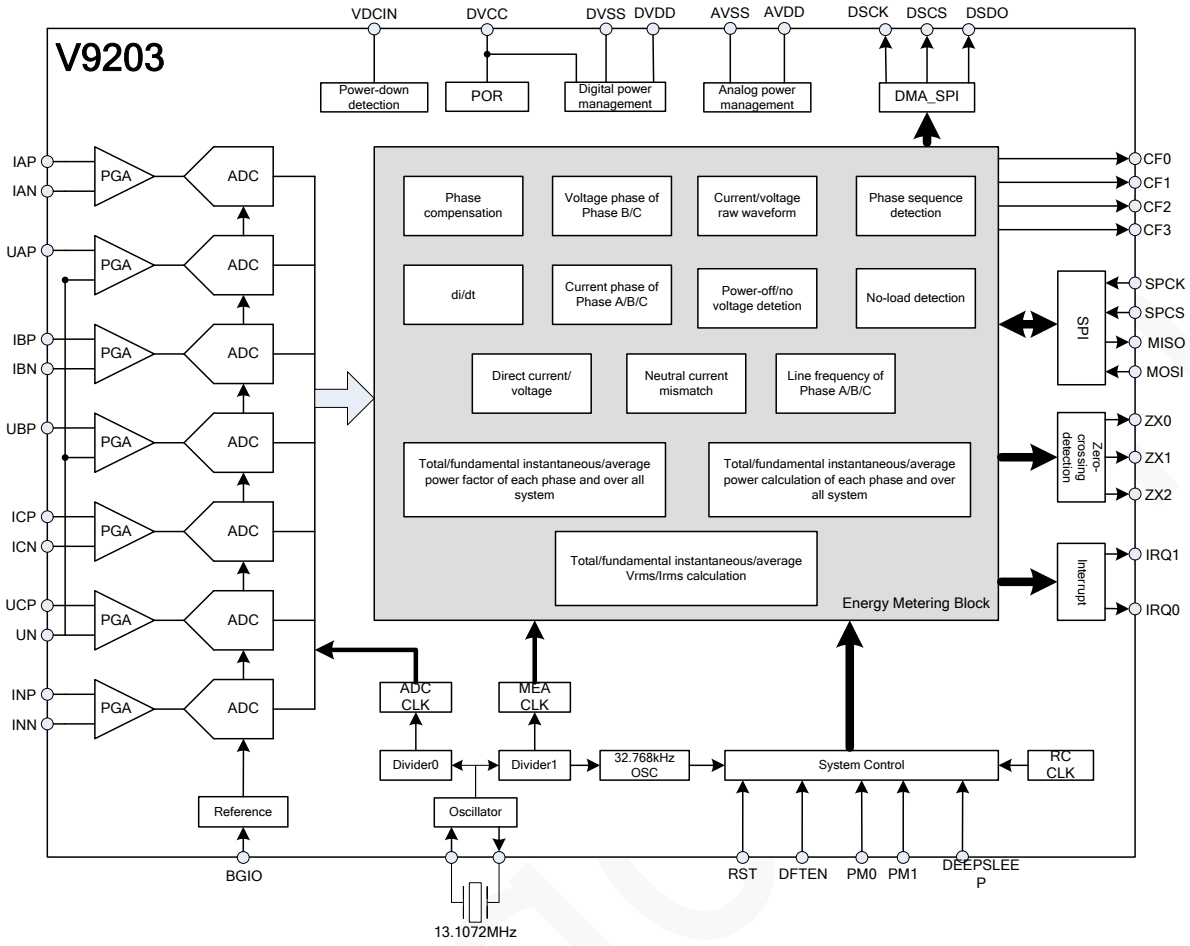
5. Parameters

Parameter	Min.	Typ.	Max.	Unit	Remark
Analog Input					
Maximum Signal Level			±200	mV	Peak value
Bandwidth (-3dB)		3.2		kHz	
ADC					
DC Offset			2	mV	
Resolution		22		Bit	Sign bit is excluded.
SNR		100		dB	
On-chip Reference					
Reference Error	-20		20	mV	
Power Supply Rejection Ratio		80		dB	
Temperature Coefficient		10		ppm/°C	
Output Voltage		1.185		V	
POR					
Detection Threshold (DVCC)	1.7	1.8	1.9	V	
VDCIN					
Input Voltage	0		VDD	V	
Impedance Input		1.5		MΩ	
Detection Threshold for Power-Down		1.0		V	
Detection Threshold for Power-UP		1.1		V	
Phase Error Between Channels					
PF=0.8 Capacitive		0.05		Degree	
PF=0.5 Inductive		0.05		Degree	
Total Active Energy Metering Error		0.1		%	Dynamic Range 10000:1 @ 25°C
Total Active Energy Metering Bandwidth		3.2		kHz	

Parameter	Min.	Typ.	Max.	Unit	Remark
Total Reactive Energy Metering Error		0.1		%	Dynamic Range 5000:1 @ 25°C
Total Reactive Energy Metering Bandwidth		3.2		kHz	
Fundamental Active Energy Metering Error		0.1		%	Dynamic Range 10000:1 @ 25°C
Fundamental Active Energy Metering Bandwidth		65		Hz	
Fundamental Reactive Energy Metering Error		0.1		%	Dynamic Range 5000:1 @ 25°C
Fundamental Reactive Energy Metering Bandwidth		65		Hz	
Total Apparent Energy Metering Error		0.5		%	Dynamic Range 2000:1 @ 25°C
Fundamental Apparent Energy Metering Error		0.5		%	Dynamic Range 2000:1 @ 25°C
VRMS Metering Error		0.5		%	Dynamic Range 2000:1 @ 25°C
VRMS Metering Bandwidth		3.2		kHz	
IRMS Metering Error		0.5		%	Dynamic Range 2000:1 @ 25°C
IRMS Metering Bandwidth		3.2		kHz	
CF Pulse Output					
Maximum Output Frequency		102.4		kHz	
Duty Cycle		50		%	160ms When the pulse period is less than 160ms.
Active High Pulse Width		80		ms	
Logic Output					
Output High Voltage, V_{OH}	2.4			V	Load of 16-mA current in a short time may not damage the chip. But, load of 16-mA for a long time may damage the chip. If the pin DVDD33 is powered by the 3.3-V LDO, the total load on the IOs cannot exceed
I_{SOURCE}		12	16	mA	
Output Low Voltage, V_{OL}			0.4	V	
I_{SINK}		12	16	mA	

Parameter	Min.	Typ.	Max.	Unit	Remark
					the maximum load of the 3.3-V LDO.
Logic Input					
Input High Voltage, V_{INH}	2.0			V	
Input Low Voltage, V_{INL}			0.4	V	
SPI Interface	512		6553600	Hz	
DMA_SPI Interface		3.2768		MHz	
Power Input					
AVDD	2.6	3.3	3.6	V	
DVDD	2.6	3.3	3.6	V	
Digital Power Output(DVCC)					
Voltage	2.2	2.43	2.7	V	
Current			35	mA	

6. Functional Block Diagram



7. Analog Control Registers

All analog control registers of the V9203 will be reset to their default values when power-on reset or RST pin reset occurs. All the default values in the following tables are in hexadecimal form.

Table 7-1 Analog Control Register 0 (ANCtrl0, 0x8000)

0x8000, R/W, Analog Control Register 0, ANCtrl0				
Bit		Default Value	Function Description	
Bit[31:19]	Reserved	0		These bits must be set to their default values for proper operation.
Bit18	GUC	0	To set analog PGA gain of UC input.	0, ×1; 1, ×2. ×2 is recommended.
Bit17	GUB	0	To set analog PGA gain of UB input.	0, ×1; 1, ×2. ×2 is recommended.
Bit16	GUA	0	To set analog PGA gain of UA input.	0, ×1; 1, ×2. ×2 is recommended.
Bit15	Reserved	0		This bit must be set to its default value for proper operation.
Bit[14:12]	GIN<2:0>	0	To set analog PGA gain of IN input.	000, ×2; 001, ×4; 010, ×16; 011/100/101/110/111, ×32 To ensure the output from the sensor matches the full scale of ADC, the default value should not be used.
Bit11	Reserved	0		This bit must be set to its default value for proper operation.
Bit[10:8]	GIC<2:0>	0	To set analog PGA gain of IC input.	000, ×2; 001, ×4; 010, ×16; 011/100/101/110/111, ×32

0x8000, R/W, Analog Control Register 0, ANCtrl0				
Bit		Default Value	Function Description	
				To ensure the output from the sensor matches the full scale of ADC, the default value should not be used. In the power-off/no-voltage pre-detection mode, it is recommended to set to ×32.
Bit7	Reserved	0		This bit must be set to its default value for proper operation.
Bit[6:4]	GIB<2:0>	0	To set analog PGA gain of IB input.	000, ×2; 001, ×4; 010, ×16; 011/100/101/110/111, ×32 To ensure the output from the sensor matches the full scale of ADC, the default value should not be used. In the power-off/no-voltage pre-detection mode, it is recommended to set to ×32.
Bit3	Reserved	0		This bit must be set to its default value for proper operation.
Bit[2:0]	GIA<2:0>	0	To set analog PGA gain of IA input.	000, ×2; 001, ×4; 010, ×16; 011/100/101/110/111, ×32 To ensure the output from the sensor matches the full scale of ADC, the default value should not be used. In the power-off/no-voltage pre-detection mode, it is recommended to set to ×32.
Note: The configuration of this register can be read out of the register ZZANA0 (0xEC01) which is used to calculate the checksum for system check.				

Table 7-2 Analog Control Register 1 (ANCtrl1, 0x8001)

0x8001, R/W, Analog Control Register 1, ANCtrl1				
Bit		Default Value	Function Description	
Bit[31:14]	Reserved	0		These bits must be set to their default values for proper operation.
Bit13	REFGIT	0	To adjust the bias current of the ADC reference generator.	0, ×1 (recommended); 1, ×1.5
Bit12	REFBIT	0	To adjust the bias current of the ADC reference buffer.	0, ×1 (recommended); 1, ×1.33
Bit[11:10]	ADIT2<1:0>	0	To adjust the 2nd bias current of the ADC.	00, ×1 (recommended); 01, ×1.5; 10, ×2; 11, ×2.5
Bit[9:8]	ADIT1<1:0>	0	To adjust the 1st bias current of the ADC.	00, ×1 (recommended); 01, ×1.5; 10, ×2; 11, ×2.5
Bit7	Reserved	0		This bit must be set to its default value for proper operation.
Bit6	ADRSTUC	0	To reset the integrator of the modulator of Channel UC.	When the ADC doesn't work well, set this bit to 1 to reset the integrator. By default, it is set to 0 to disable this reset.
Bit5	ADRSTUB	0	To reset the integrator of the modulator of Channel UB.	When the ADC doesn't work well, set this bit to 1 to reset the integrator. By default, it is set to 0 to disable this reset.
Bit4	ADRSTUA	0	To reset the integrator of the modulator of Channel UA.	When the ADC doesn't work well, set this bit to 1 to reset the integrator. By default, it is set to 0 to disable this reset.
Bit3	ADRSTIN	0	To reset the integrator of the modulator of	When the ADC doesn't work well, set this bit to 1 to reset the integrator. By default, it is set to 0 to disable this reset.

0x8001, R/W, Analog Control Register 1, ANCtrl1				
Bit		Default Value	Function Description	
			Channel IN.	
Bit2	ADRSTIC	0	To reset the integrator of the modulator of Channel IC.	When the ADC doesn't work well, set this bit to 1 to reset the integrator. By default, it is set to 0 to disable this reset.
Bit1	ADRSTIB	0	To reset the integrator of the modulator of Channel IB.	When the ADC doesn't work well, set this bit to 1 to reset the integrator. By default, it is set to 0 to disable this reset.
Bit0	ADRSTIA	0	To reset the integrator of the modulator of Channel IA.	When the ADC doesn't work well, set this bit to 1 to reset the integrator. By default, it is set to 0 to disable this reset.
Note: The configuration of this register can be read out of the register ZZANA1 (0xEC02) which is used to calculate the checksum for system check.				

Table 7-3 Analog Control Register 2 (ANCtrl2, 0x8002)

0x8002, R/W, Analog Control Register 2, ANCtrl2				
Bit		Default Value	Function Description	
Bit31	Reserved	0		This bit must be set to its default value for proper operation. About 976μs after reset, this bit is set to 1 automatically. So it must be cleared for proper operation.
Bit30	ADPDUCN	0	To enable the ADC of Channel UC.	0, disable; 1, enable. About 976μs after reset, these bits are set to 0b01111111 automatically, to enable all ADCs of the channels.
Bit29	ADPDUBN	0	To enable the ADC of Channel UB.	
Bit28	ADPDUAN	0	To enable the ADC of Channel UA.	
Bit27	ADPDINN	0	To enable the ADC of Channel IN.	
Bit26	ADPDICN	0	To enable the ADC of Channel IC.	
Bit25	ADPDIBN	0	To enable the ADC of Channel IB.	

0x8002, R/W, Analog Control Register 2, ANCtrl2				
Bit		Default Value	Function Description	
Bit24	ADPDIAN	0	To enable the ADC of Channel IA.	
Bit23	AMPITN	0	To adjust the bias current of the amplifier of Channel IN.	1, lower to 50%. The default value is recommended.
Bit22	AMPITI	0	To adjust the bias current of the amplifier of the current channels.	1, lower to 50%. The default value is recommended.
Bit21	Reserved	0		This bit must be set to its default value for proper operation.
Bit20	AMPITU	0	To adjust the bias current of the amplifier of the voltage channels.	1, lower to 50%. The default value is recommended.
Bit[19:18]	Reserved	0		These bits must be set to their default values for proper operation.
Bit[17:16]	CURRIT<1:0>	0	To adjust the bias current of the analog circuits.	00, 100%; 01, -33%; 10, -66%; 11, -75%
Bit[15:13]	REST<2:0>	0	To finely adjust the temperature coefficient of the Bandgap circuit.	000, 0; 001, +6ppm; 010, +12ppm (recommended); 011, +18ppm; 100, -24ppm; 101, -18ppm; 110, -12ppm; 111, -6ppm
Bit[12:11]	RESTL<1:0>	0	To roughly adjust the temperature coefficient of the Bandgap circuit.	00, 0; 01, -60ppm; 10, -120ppm (recommended); 11, -180ppm
Bit10	CLKOSEL	0	To select the ADC clock output.	0, the same phase as the input clock; 1, the inverse of the input clock. This bit must be set to 1 for proper operation.
Bit9	Reserved	0		This bit must be set to its default value for proper operation.
Bit8	BGPCHOPN	0	To disable the	1, disable; 0, enable (by default).

0x8002, R/W, Analog Control Register 2, ANCtrl2				
Bit		Default Value	Function Description	
			chopper of the Bandgap circuit.	
Bit[7:0]	Reserved	0		These bits must be set to their default values for proper operation.
Note: The configuration of this register can be read out of the register ZZANA2 (0xEC03) which is used to calculate the checksum for system check.				

Table 7-4 Analog Control Register 3 (ANCtrl3, 0x8003)

0x8003, R/W, Analog Control Register 3, ANCtrl3				
Bit		Default Value	Function Description	
Bit[31:20]	Reserved	0		These bits must be set to their default values for proper operation.
Bit[19:18]	ADCLKSEL<1:0>	0	To select the sampling frequency for the oversampling ADC (ADC frequency).	Base: 204.8kHz. 00, ×4; 01, ×8; 10, ×1; 11, ×2 When logic high is input to both the pins PM0 and PM1, in which the V9203 works in OPM0 (normal operation mode), the metering frequency must be 8 times of the ADC frequency.
Bit[17:16]	MEACLKSEL<1:0>	0	To select the frequency for the energy metering block (metering frequency).	Base: 819.2kHz. 00, ×8; 01, ×4; 10, ×2; 11, ×1 When both the pins PM0 and PM1 are input high logic, in which the V9203 works in OPM0 (normal operation mode), the metering frequency must be 8 times of the ADC frequency.
Bit[15:11]	Reserved	0		These bits must be set to their default values for proper operation.

0x8003, R/W, Analog Control Register 3, ANCtrl3				
Bit		Default Value	Function Description	
Bit10	REFBUFEN	0	To enable the reference buffer of the ADCs.	0, disable (default); 1, enable. This bit must be set to 1 for proper operation.
Bit[9:3]	Reserved	0		These bits must be set to their default values for proper operation.
Bit2	CLKPDN	0	To enable the clock scaler.	0, disable; 1, enable. About 488μs after reset, these bits are set to 0b101 automatically, to enable the clock scaler and Bandgap Circuit A and disable the Bandgap Circuit B. Then, users must set these bits to 0b110 to enable the Bandgap Circuit B and the clock scaler, and disable the Bandgap Circuit A.
Bit1	BGPPDNB	0	To enable the Bandgap Circuit B.	
Bit0	BGPPDNA	0	To enable the Bandgap Circuit A.	
Note: The configuration of this register can be read out of the register ZZANA3 (0xEC04) which is used to calculate the checksum for system check.				

8. Reset

In the V9203, two events can reset the system: power-on and RST pin input.

8.1. Power-on Reset (POR)

In the V9203, the internal power-on reset circuit supervises the output voltage on the pin DVCC (Pin1) all the time. When the output voltage is higher than 1.8V, the reset signal is released, and the reset state holds 244μs. When the output voltage is lower than 1.8V, the system is in the reset state.

The threshold, 1.8V, a typical value, is associated with the chips.

8.2. RST Pin Reset

When the level on the pin RST holds low for more than 5ms, the system is reset, and the reset state holds at least 244μs.

To protect the RST pin input from the electrostatic interference, the input is filtered by the RC oscillator clock.

9. Clock Generation

The on-chip RC oscillator circuit and the crystal oscillator circuit provide clock for the V9203.

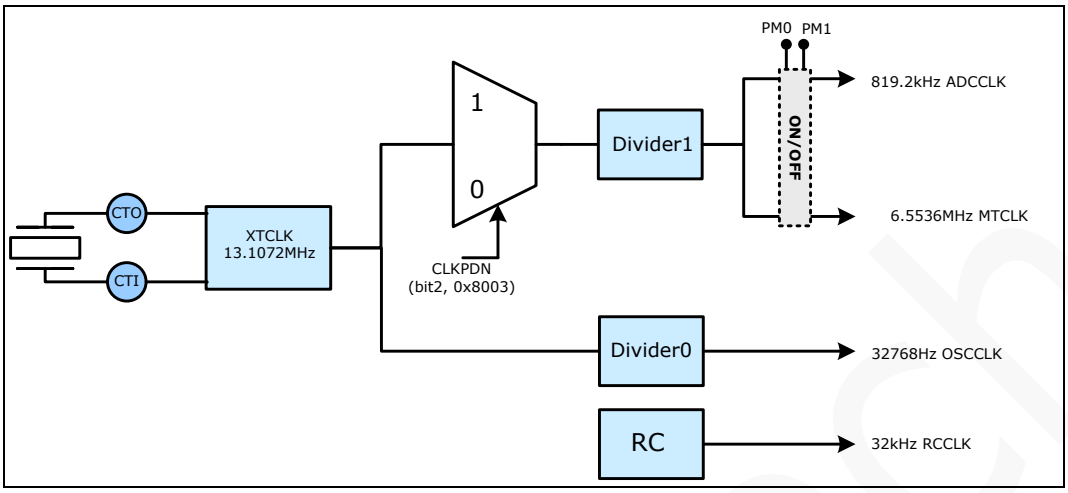


Figure 9-1 Clock Generation

9.1. RC Oscillator

The on-chip RC oscillator can generate a 32 KHz RC clock (RCCLK) which can be used to filter the input signals on the pin PM0/PM1/RST/DFTEN. This oscillator cannot be turned off.

9.2. Crystal Oscillator

The on-chip crystal oscillator can be used with a 13.1072MHz crystal to generate 3 clock signals:

- OSCCLK: 32768 Hz OSC clock. The OSCCLK is crystal oscillator clock source divided by 400. This clock signal is used by the reset circuits.
- ADCCLK: 819.2 KHz ADC clock. The ADCCLK is crystal oscillator clock source divided by 16. This clock signal is used by the ADCs and the phase compensation circuits. This clock can be disabled via disabling the clock scaler via configuring bit[2:0] of register ANCtrl3 (0x8003).
- MTCLK: 6.5536MHz metering clock. The MTCLK is crystal oscillator clock source divided by 2. This clock signal is used as the system clock. This clock can be disabled via disabling the clock scaler via configuring bit[2:0] of register ANCtrl3 (0x8003). When this clock is disabled, OSCCLK is used as the system clock. When the system works in OPM0, or normal operating mode, the MTCLK must be 8 times of ADCCLK.

The load capacitance (CL) of the crystal oscillator is 10-pF. Both pins, CTI and CTO, must be directly connected to a 13.1072-MHz crystal with about 8-pF CL externally for clock generation. Both pins must be connected to a 15-pF capacitor respectively externally, which increases the power consumption by about 36-μA, and then to a 13.1072-MHz crystal with about 18-pF CL.

The crystal oscillator works all the time, consuming about 0.26mA.

10. Operating Mode

The POR or RST pin input event can reset the system to default state. Immediately after the reset, bit[31:24] of ANCtrl2 register (0x8002) are automatically set to 0b11111111 to enable the signal input of the 7 ADCs, and then bit[2:0] of ANCtrl3 register (0x8003) are automatically set to 0b101 to enable the clock scaler to generate 6.5536MHz MTCLK for the energy metering block and 819.2kHz ADCCLK for ADC sampling and phase compensation. 488μs later, the system is ready for the inputs on the pins PM0 (Pin24) and PM1 (Pin25) which determine the operating mode of the V9203.

Whatever operating mode the V9203 is in, an input of logic "1" on the pin DEEPSLEEP (Pin19) forces the system to the deep sleep mode.

Table 10-1 PM0/PM1/DEEPSLEEP Determining the Operating Mode

PM0	PM1	DEEPSLEEP	Operating Mode
1	1	0	OPM0, normal operation mode.
1	0	0	OPM1, power-off/no-voltage pre-detection mode.
0	1	0	OPM2, RMS mode.
0	0	0	OPM3, sleep mode (not recommended).
X	X	1	OPM4, deep sleep mode.

10.1. OPM0

In OPM0, or normal operation mode, all analog circuits can work according to the analog control registers configurations, the digital circuits work, and the ADC sampling frequency is 819.2kHz and the metering frequency is 6.5536MHz by default.

All the registers, except for the analog control registers, must be configured in this mode.

In this mode, users can configure the registers ANCtrl2 and ANCtrl3 to reduce the ADC sampling and energy metering frequency to bring the system into underclocking operation to lower the power consumption.

Table 10-2 Configuration for Underclocking Operation in OPM0

Register	bit		Description
ANCtrl3, 0x8003	Bit[19:18]	ADCLKSEL<1:0>	0b10, 204.8kHz ADC sampling frequency.
	Bit[17:16]	MEACLKSEL<1:0>	0b10, 1.6384MHz metering frequency.
ANCtrl2, 0x8002	Bit[17:16]	CURRIT<1:0>	0b11, to lower the bias current of the analog circuits by 75%.

10.2. OPM1

In OPM1, or power-off/no-voltage pre-detection mode, only the RC oscillator, the crystal oscillator,

the digital power circuit, the current channels of Phase A/B/C, the clock scaler, the Bandgap circuit, the clock management circuit, the reset circuits, the filters for input signals on the pins PM0/PM1/RST/DFTEN, the phase compensation circuit, the CIC filter, the current detection circuit, the interrupt circuits, and the SPI interfaces, are operating, and other circuits stop working. In this mode, the SPI interfaces cannot communicate normally.

When any bit of bit[13:11] of the register IRQEN0 (0xA000) or IRQEN1 (0xA001) is set to logic 1, the current interrupt is enabled. When a current signal is caught, a current detection interrupt is triggered, the interrupt flag is set bit, a logic high is output on the pin IRQ0 or IRQ1 to signal the master MCU that the current is strong enough for energy metering.

In this mode, by default, the ADC sampling frequency is 819.2kHz, and the metering frequency is 6.5536MHz. But, users can configure the registers ANCtrl2 and ANCtrl3 to reduce the ADC sampling and energy metering frequency to bring the system into underclocking operation to lower the power consumption. In the underclocking operation, the settling time is less than 20ms.

Table 10-3 Configuration for Underclocking Operation in OPM1 or OPM2

Register	bit		Description
ANCtrl3, 0x8003	Bit[19:18]	ADCLKSEL<1:0>	0b10, 204.8kHz ADC sampling frequency
	Bit[17:16]	MEACLKSEL<1:0>	0b11, 819.2kHz metering frequency
ANCtrl2, 0x8002	Bit[17:16]	CURRIT<1:0>	0b11, to lower the bias current of the analog circuits by 75%.

10.3. OPM2

In OPM2, or RMS mode, that is accumulating current RMS for energy metering, only the RC oscillator, the crystal oscillator, the digital power circuit, the current channels of Phase A/B/C, the clock scaler, the Bandgap circuit, the clock management circuit, the reset circuits, the filters for input signals on the pins PM0/PM1/RST/DFTEN, the phase compensation circuit, the CIC filter, the RMS/power/power factor calculation circuits, the normal and high-speed energy accumulation circuits, the pulse generation circuits, DC-stopping circuits, the current detection circuit, the frequency/phase measurement circuit, the interrupt circuits, and the SPI interfaces, are operating, and other circuits stop working.

In this mode, by default, the ADC sampling frequency is 819.2kHz, and the metering frequency is 6.5536 MHz. In full operation, the settling time is less than 135ms. But, users can configure the registers ANCtrl2 and ANCtrl3 to reduce the ADC sampling and energy metering frequency to bring the system into underclocking operation to lower the power consumption. Refer to the above table for details of the register configuration.

10.4. OPM3

When low level (00) is input to both pins PM0 and PM1 when the V9203 is working in the OPM0 (or normal operation mode), the system clock is switched to 32768Hz OSCCLK, and inputs to all ADCs are disabled. Immediately 488μs later, the system enters to OPM3, or sleep mode, which is not recommended.

In this mode, only the RC oscillator, the crystal oscillator, the digital power circuit, the clock

management circuit, the reset circuits, and the filters for input signals on the pins PM0/PM1/RST/DFTEN, are operating, and other circuits stop working. The memory and register configuration hold the values. And the system is in a low-power state, consuming 273μA (typical). If high level is input to either PM0 or PM1, the system is awoken.

10.5. OPM4

Hold high logic on the pin DEEPSLEEP for more than 4ms to enable the system entering to the OPM4, or deep sleep mode.

In this mode, the digital power circuit is turned off, the power supply for the digital circuits is driven down to 0V, and only the RC oscillator is working. The system is in an ultralow power state, consuming 0.19μA (typical) only.

Hold low logic on the pin DEEPSLEEP for more than 4ms to wake up and retrieve the system.

10.6. Power Consumption

Table 10-4 Power Consumption of V9203

Operating	Operating Mode	Power Consumption		Description
Full operating	OPM0	9.16	mA	Metering frequency is 6.5536MHz, ADC sampling frequency is 819.2kHz, ADCs of current and voltage of Phase A/B/C are enabled.
		9.9	mA	Metering frequency is 6.5536MHz, ADC sampling frequency is 819.2kHz, ADCs of current and voltage of Phase A/B/C and Channel IN are enabled.
	OPM2	5.1	mA	Metering frequency is 6.5536MHz, ADC sampling frequency is 819.2kHz, ADCs of current and voltage of Phase A/B/C are enabled.
Underclocking Operating	OPM0	3.21	mA	Metering frequency is 1.6384MHz, ADC sampling frequency is 204.8kHz, ADCs of current and voltage of Phase A/B/C are enabled.
	OPM1	1.65	mA	Metering frequency is 819.2kHz, ADC sampling frequency is 204.8kHz, ADCs of current and voltage of Phase A/B/C are enabled.
	OPM2	2.2	mA	
	OPM4	0.19	μA	Deep sleep mode.

11. Power Supply Management

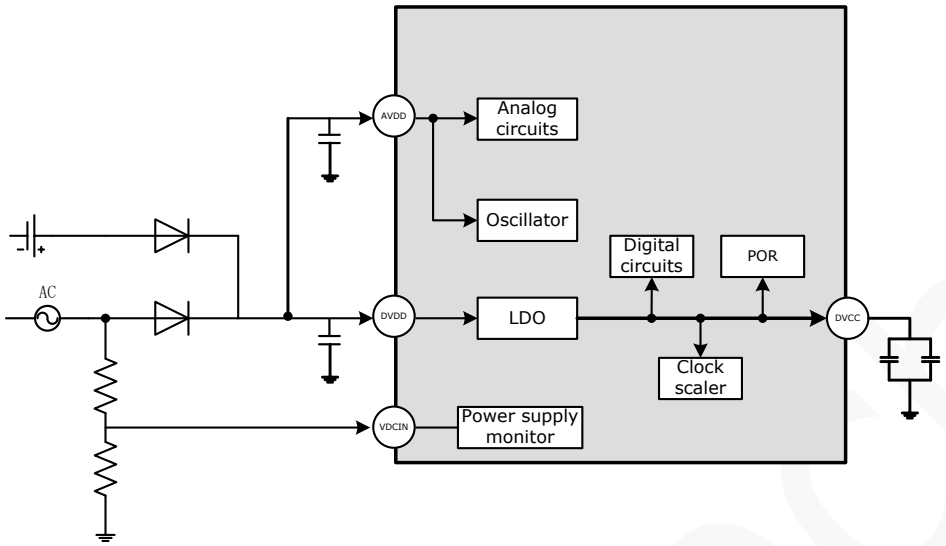


Figure 11-1 Power Supply Architecture

The V9203 has a power input 3.3V (2.6~3.6V). The analog circuits, such as the ADCs, Bandgap circuits, and the oscillator, are powered by the input of AVDD. And the digital circuits, clock scaler and the power-on reset circuit are powered by the digital power supply circuit.

11.1. Digital Power Supply

The digital power supply for digital circuits, clock scaler and power-on reset circuit is derived by an on-chip LDO（DVCC） from power input (DVDD). DVCC will output a stable voltage, avoiding the digital power fluctuation caused by the variation of the power input. This LDO keeps working until the system is powered down.

The LDO has a driving capability of 35mA, which means when the load current on the digital circuits is less than 35mA, the LDO outputs stable voltage; but when the load current is higher than 35mA, the output reduces as the current increases.

The internal power-on reset circuit supervises the output voltage on the pin DVCC (Pin1) all the time. When the output voltage is higher than 1.8V, the reset signal is released, and the reset state holds 244μs. When the output voltage is lower than 1.8V, the system is in the reset state. The threshold, 1.8V, a typical value, is associated with the chips. It is recommended to decouple the pin externally with a 10μF capacitor in parallel with a 0.1μF capacitor.

11.2. Power Supply Monitor

The V9203 contains a power supply monitor circuit which monitors the input on the pin VDCIN (Pin17).

When the input level on the pin is less than 1-V, the monitor circuit outputs logic 1, signaling the master MCU that the V9203 has been powered down. If bit16 of either IRQEN0 register (0xA000) or IRQEN1 register (0xA001) is set to 1 to enable the power down interrupt, the interrupt flag, bit16 of the

register IRQFLAG (0xA002), is set bit when the power-down event occurs, and either pin IRQ0 (Pin30) or IRQ1 (Pin31) outputs logic 1.

12. Bandgap Circuits

In the V9203, the Bandgap Circuits output a reference voltage, about 1.185V with a typical temperature coefficient of 10ppm/°C, for ADCs. This circuit consumes about 0.1mA.

About 488μs after reset, bit[2:0] of ANCtrl3 (0x8003) register is set to 0b101 automatically, to enable the clock scaler and Bandgap Circuit A, and disable the Bandgap Circuit B. Then, users must set these bits to 0b110 to enable the Bandgap Circuit B and the clock scaler, as well as disable the Bandgap Circuit A, because the Bandgap Circuit B delivers a better temperature performance.

Users can adjust the temperature performance as follows:

1. Set bit1 of ANCtrl3 register (0x8003) to 1, to enable the Bandgap Circuit B;
2. Enable the chopper to eliminate the bias current of the Bandgap circuits (by default). When the chopper is enabled, the output of the Bandgap circuit varies in the range of -50~+50mV, and the temperature coefficient can be improved by 5ppm.
3. Configure bit[15:13] and bit[12:11] of ANCtrl2 register (0x8002) to adjust the temperature coefficient to kill the temperature coefficient introduced by the external components. It is recommended to configure the bits as follows:

Table 12-1 Adjusting the Temperature Coefficient

Register	bit		Configuration
Analog Control Register 2 (0x8002, ANCtrl2)	Bit[15:13]	REST<2:0>	0b010
	Bit[12:11]	RESTL<1:0>	0b10

13. SPI

The data frame received and transmitted via the SPI interfaces of the V9203 is composed of 32 bits, including 2-bit Start Bits (bit[31:30], "10"), 6-bit Command Bits (bit[29:24]), 16-bit Data (bit[23:16], DATAH, and bit[15:8], DATA L), and 8-bit Checksum (bit[7:0]), as shown in the following figure. When the V9203 receives or sends the frame, the most significant bit always is shifted in or out first.

Note: The SPI slave mode of V9203 is fixed to mode 3 (clock phase is 1, clock polarity is 1).

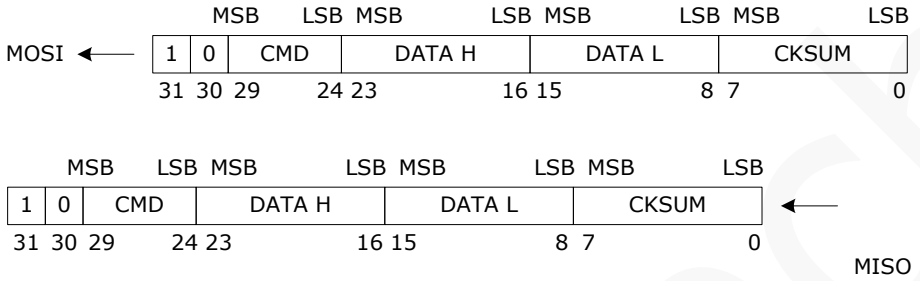


Figure 13-1 Data Frame Structure

Table 13-1 Description of Data Frame

Data Frame		Description
Start Bits, "10"	Bit31~bit30	On a low-to-high SCLK transition, the V9203 receives a bit on MOSI; and on a high-to-low SCLK transition, the V9203 transmits a bit on MISO. On two continuous low-to-high SCLK transition, the V9203 receives "1" and then "0", the Start Bits.
Command Bits, CMD	Bit29~bit24	To determine the function of the data frame. The most significant bit is shifted in or out first.
Data, DATA H, DATA L	Bit23~bit8	The data to be operated according to the command bits. The most significant bit is shifted in or out first.
Checksum, CKSUM	Bit7~bit0	CKSUM is the checksum. Checksum is the 2's complement of the sum of the 3 bytes (Bit[31:24], bit[23:16] and bit[15:8]). The most significant bit is shifted in or out first.

Table 13-2 Description of Command Bits

CMD		Description
0b001000	0x08	To write of lower 16 bits of SPI buffer.
0b001010	0x0A	To write of higher 16 bits of SPI buffer.
0b001100	0x0C	To give the address of the target register to be write operated.
0b010000	0x10	To give the address of the target register to be read operated.
0b010010	0x12	To read out the lower 16 bits of the target register.

CMD		Description
0b010100	0x14	To read out the higher 16 bits of the target register.
0b001110	0x0E	To read out the last target address operated.
0b010110	0x16	To read out the lower 16 bits of the last target register operated.
0b011000	0x18	To read out the higher 16 bits of the last target register operated.

13.1. SPI Write Operation

The master must send 3 data frames to complete writing of a 32-bit datum using the SPI interface of the V9203, 2 data frames for a 16-bit datum, or 1 data frame for an 8-bit datum. For example, the following table shows the 3 data frames for the SPI write operation of a 32-bit datum.

Table 13-3 SPI Write Operation: Description of the CMD and DATA of the Frames

No. of Frame	CMD	DATA H & DATA L	Description
1	0x08	The lower 16 bits of the target data.	The master MCU sends the lower 16 bits of the target data, and the data is written to the lower 16 bits of SPI buffer of the V9203 on the last (the 32nd) low-to-high SPCK transition.
2	0x0A	The higher 16 bits of the target data.	The master MCU sends the higher 16 bits of the target data, and the data is written to the higher 16 bits of SPI buffer of the V9203 on the last (the 32nd) low-to-high SPCK transition.
3	0x0C	The address of the target register for write.	The above 32-bit data is written into the target register after the last bit of the data frame is received.

The master sends the checksums of the above three data frames. If any error is detected in the received data frames, the data frames are invalid. If the SPI error interrupt is enabled (bit15 of IRQEN0 [0xA000] or IRQEN1[0xA001] is set to 1), the interrupt flag (bit15 of IRQFLAG[0xA002]) is set bit, and a logic high is output on the pin IRQ0 or IRQ1.

During the SPI write operation, the V9203 sends the content on the MISO pin that is shifted in on the MOSI pin on the high-to-low SPCK transition. So users can read the content sent on the MISO pin to detect whether the V9203 received the right data.

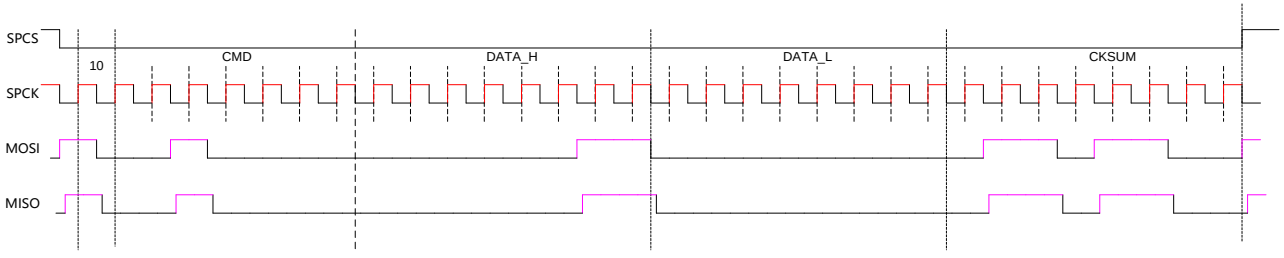


Figure 13-2 SPI Write Operation of a 32-bit Register

13.2. SPI Read Operation

The master must send 3 data frames to complete reading a 32-bit datum using the SPI interface of the V9203, 2 data frames for a 16-bit datum, or 1 data frame for an 8-bit datum. For example, the following table shows the 3 data frames for the SPI read operation of a 32-bit datum.

Table 13-4 SPI Read Operation: Description of the CMD and DATA of the Frames

No. of Frame	CMD	DATA H & DATA L	Description
1	0x10	The address of the target register for read.	The master MCU sends the address of the target register to be read. The master MCU sends the checksum.
2	0x12	The lower 16 bits of the target register.	From the 1st to 8th high-to-low SPCK transition, the master MCU sends the start bits and command bits to the V9203 on the pin MOSI, and the V9203 sends the received bits to the mater MCU on the pin MISO. From the 9th to 32nd high-to-low SPCK transition, whatever is received on the MOSI pin of the V9203, from the 9th to 24th SPCK transition, the V9203 sends the lower 16 bits of the target register on the MISO pin, and then from the 25th to 32nd high-to-low SPCK transition, the V9203 sends the checksum calculated by the SPI module of the V9203 on the MISO pin. The master MCU can read the content sent from the MISO pin of the V9203 and combine them to be a data frame to detect whether the transfer operation is right.
3	0x14	The higher 16 bits of the target register.	From the 1st to 8th high-to-low SPCK transition, the master MCU sends the start bits and command bits to the V9203 on the pin MOSI, and the V9203 sends the received bits to the mater MCU on the pin MISO. From the 9th to 32nd high-to-low SPCK transition, whatever is received on the MOSI pin of the V9203, from the 9th to 24th SPCK transition, the V9203 sends the higher 16 bits of the target register on the MISO pin, and then from the 25th to 32nd high-to-low SPCK transition, the V9203 sends the checksum calculated by the SPI module of the V9203 on the MISO pin. The master MCU can read the content sent from the MISO pin of the V9203 and combine them to be a data frame to detect whether the transfer operation is right.

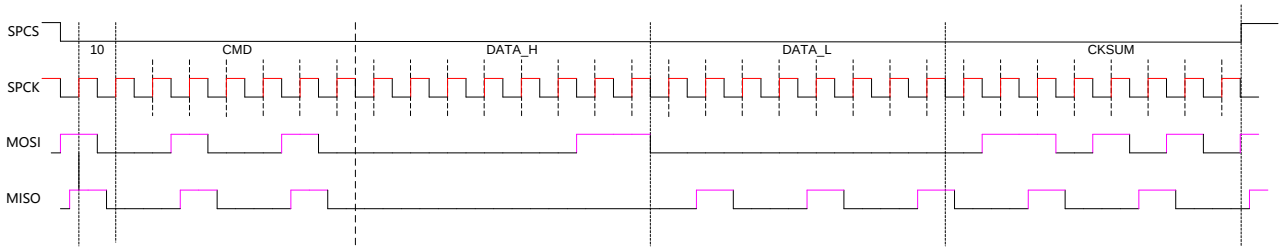


Figure 13-3 SPI Read Operation of a 32-bit Register

13.3. Check The Last Operation

The master MCU can check the last write or read operation via the SPI interface of the V9203. The master must send 3 data frames as follows to complete the checking.

Table 13-5 SPI Read Operation: Description of the CMD and DATA of the Frames

No. of Frame	CMD	DATA H & DATA L	Description
1	0x0E	The last address operated.	From the 1st to 8th high-to-low SPCK transition, the master MCU sends the start bits and command bits to the V9203 on the pin MOSI, and the V9203 sends the received bits on the pin MISO. From the 9th to 32nd high-to-low SPCK transition, whatever is received on the MOSI pin of the V9203, from the 9th to 24th SPCK transition, the MISO sends address of the target register, and then from the 25th to 32nd high-to-low SPCK transition, the MISO sends the checksum calculated by the SPI module of the V9203.
2	0x16	The lower 16 bits of the last target register operated.	From the 1st to 8th high-to-low SPCK transition, the master MCU sends the start bits and command bits to the V9203 on the pin MOSI, and the V9203 sends the received bits to the mater MCU on the pin MISO. From the 9th to 32nd high-to-low SPCK transition, whatever is received on the MOSI pin of the V9203, from the 9th to 24th SPCK transition, the V9203 sends the lower 16 bits of the target register on the MISO pin, and then from the 25th to 32nd high-to-low SPCK transition, the V9203 sends the checksum calculated by the SPI module of the V9203 on the MISO pin.
3	0x18	The higher 16 bits of the last target register operated.	From the 1st to 8th high-to-low SPCK transition, the master MCU sends the start bits and command bits to the V9203 on the pin MOSI, and the V9203 sends the received bits to the mater MCU on the pin MISO. From the 9th to 32nd high-to-low SPCK transition, whatever is received on the MOSI pin of the V9203, from the 9th to 24th SPCK transition, the V9203 sends the higher 16 bits of the target register on the MISO pin, and then from the 25th to 32nd high-to-low SPCK transition, the V9203 sends the checksum calculated by

No. of Frame	CMD	DATA H & DATA L	Description
			the SPI module of the V9203 on the MISO pin.

13.4. Reset

The SPI interfaces of the V9203 can be reset by 3 events:

- Holding low input on the RST pin for more than 5ms: the SPI buffer is cleared and the SPI interfaces are reset;
- High input on the SPCS pin: the SPI interfaces are reset, and the MISO pin follows the MOSI input level state until the RST pin reset occurs. The SPI can work normally when a low logic is input on the SPCS pin and no RST pin reset occurs.
- Low input on the SPCS pin , High input on the MOSI pin during 32 continuous SPCK: the SPI interfaces get back to idle state, and the MISO pin output low logic.

13.5. Filters

4 optional filters can be used to adjust the communication rate. By default, the Filter 0 is used, and the communication rate is less than 409.6 kHz.

Table 13-6 Select the Filters for Communication Rate Adjustment.

CMD	DATA H	DATA L	Description
0x10	0xFC	Do not care.	To use Filter 1.
0x10	0xFB	Do not care.	To use Filter 2.
0x10	0xFA	Do not care.	To use Filter 3.
0x10	0xF9	Do not care.	To use Filter 0.

Table 13-7 Relationships between Filter, Master Clock and SPI Communication Rate

Master Clock	Filter			
	Filter 0	Filter 1	Filter 2	Filter 3
6.5536MHz	409.6 kHz	6.5536 MHz	655.36 kHz	102.4 kHz
3.2768MHz	204.8 kHz	3.2768 MHz	327.68 kHz	51.2 kHz
1.6384MHz	102.4 kHz	1.6384 MHz	163.84 kHz	25.6 kHz
819.2kHz	51.2 kHz	819.2 kHz	81.92 kHz	12.8 kHz
32.768kHz	2.048 kHz	32.768 kHz	3.2768 kHz	512 Hz

14. Energy Metering Registers

All energy metering registers of the V9203 will be reset to their default values when power-on reset or RST pin reset happens. All the default values in the following tables are in hexadecimal form.

14.1. Energy Metering Configuration Registers

14.1.1. Metering Control Registers

Table 14-1 Metering Control Register 0 (0xC000, MTPARA0)

0xC000, R/W, Metering Control Register 0, MTPARA0					
Bit		Default Value	Function Description		
Bit[31:24]	MTRAM<7:0>	0	To clear the data RAM located at addresses as followings in the energy metering block, or force the data RAM to go to the sleep: 0xC800~0xC837 0xC880~0xC8B7 0xE000~0xE08F 0xE800~0xEAB7 0xF800~0xF87F 0xF000~0xF1EF	Write of 0b10101010, 20ms later, the RAM located at addresses of the range of 0xE000~0xE08F/ 0xE800~0xEAB7/ 0xF800~0xF87F/ 0xF000~0xF1EF is cleared. Write of 0b01010101, the RAM located at addresses of the range of 0xE000~0xE08F/ 0xE800~0xEAB7/ 0xF800~0xF87F/ 0xF000~0xF1EF enters to sleep. Write of 0b00010000, and then write 0s in the RAM located at addresses of the range of 0xC800~0xC837 and 0xC880~0xC8B7 to clear the RAM.	Access bit [7:0] of the register located at address 0xC013 to access bit[31:24] of the register MTPARA0.
Bit[23:21]	Reserved	0			Access bit [7:0] of the register located at address 0xC012 to access bit[23:16]
Bit[20:16]	MSKP	0	To set the range of the hysteresis error of the fundamental current threshold for the total active	For example, if the value of MSKP is set to 0x8, and the fundamental current threshold is set to 0xabcd, the 8 least significant bits of register of the fundamental current threshold represents the hysteresis error	

0xC000, R/W, Metering Control Register 0, MTPARA0					
Bit		Default Value	Function Description		
			power gain calibration in sections.	range, that is the top threshold is 0xabff, and the bottom threshold is 0xab00.	of the register MTPARA0.
Bit[15:13]	Reserved	0			Access bit [7:0] of the register located at address 0xC011 to access bit[15:8] of the register MTPARA0.
Bit[12:8]	MSKA	0	To set the range of the hysteresis error of the fundamental current threshold for the phase compensation in sections.	For example, if the value of MSKA is set to 0x8, and the fundamental current threshold is set to 0xabcd, the 8 least significant bits of the register of the fundamental current threshold represents the hysteresis error range, that is the top threshold is 0xabff, and the bottom threshold is 0xab00.	
Bit7	Reserved	0			Access bit [7:0] of the register located at address 0xC010 to access bit[7:0] of the register MTPARA0.
Bit6	ADCIC	0	To enable digital signal input of Channel IC for digital signal processing.	1, enable. 0, disable. When this bit is set to 0, a constant "0" is input for digital signal processing.	
Bit5	ADCIB	0	To enable digital signal input of Channel IB for digital signal processing.	1, enable. 0, disable. When this bit is set to 0, a constant "0" is input for digital signal processing.	
Bit4	ADCIA	0	To enable digital signal input of Channel IA for digital signal processing.	1, enable. 0, disable. When this bit is set to 0, a constant "0" is input for digital signal processing.	
Bit3	ADCIN	0	To enable digital signal input of Channel IN for digital signal processing.	1, enable. 0, disable. When this bit is set to 0, a constant "0" is input for digital signal processing.	
Bit2	ADCUC	0	To enable digital signal input of Channel UC for digital signal	1, enable. 0, disable. When this bit is set to 0, a constant "0" is input for	

0xC000, R/W, Metering Control Register 0, MTPARA0					
Bit		Default Value	Function Description		
			processing.	digital signal processing.	
Bit1	ADCUB	0	To enable digital signal input of Channel UB for digital signal processing.	1, enable. 0, disable. When this bit is set to 0, a constant "0" is input for digital signal processing.	
Bit0	ADCUA	0	To enable digital signal input of Channel UA for digital signal processing.	1, enable. 0, disable. When this bit is set to 0, a constant "0" is input for digital signal processing.	
Note: The configuration of this register can be read out of the register ZZPARA0 (0xEC27) which is to calculate the checksum for system check.					

Table 14-2 Metering Control Register 1 (0xC001, MTPARA1)

0xC001, R/W, Metering Control Register 1, MTPARA1				
Bit		Default Value	Function Description	
Bit[31:27]	Reserved	0		
Bit[26:24]	ATXIN	0	To set digital PGA gain of IN input.	×1~×128 (2^{ATXIN})
Bit23	Reserved	0		
Bit[22:20]	ATXIC	0	To set digital PGA gain of IC input.	×1~×128 (2^{ATXIC})
Bit19	Reserved	0		
Bit[18:16]	ATXUC	0	To set digital PGA gain of UC input.	×1~×128 (2^{ATXUC}) If the voltage multiplying the set analog PGA gain is still far smaller than the full scale of the ADC, it is recommended to set the digital PGA gain to ×8 or ×16, to improve the performance.
Bit15	Reserved	0		
Bit[14:12]	ATXIB	0	To set digital PGA gain of IB input.	×1~×128 (2^{ATXIB})
Bit11	Reserved	0		
Bit[10:8]	ATXUB	0	To set digital PGA gain of UB input.	×1~×128 (2^{ATXUB})

0xC001, R/W, Metering Control Register 1, MTPARA1				
Bit		Default Value	Function Description	
				If the voltage multiplying the set analog PGA gain is still far smaller than the full scale of the ADC, it is recommended to set the digital PGA gain to ×8 or ×16, to improve the performance.
Bit7	Reserved	0		
Bit[6:4]	ATXIA	0	To set digital PGA gain of IA input.	×1~×128 (2^{ATXIA})
Bit3	Reserved	0		
Bit[2:0]	ATXUA	0	To set digital PGA gain of UA input.	×1~×128 (2^{ATXUA}) If the voltage multiplying the set analog PGA gain is still far smaller than the full scale of the ADC, it is recommended to set the digital PGA gain to ×8 or ×16, to improve the performance.
Note: The configuration of this register can be read out of the register ZZPARA1 (0xEC28) which is to calculate the checksum for system check.				

Table 14-3 Metering Control Register 2 (0xC002, MTPARA2)

0xC002, R/W, Metering Control Register 2, MTPARA2					
Bit		Default Value	Function Description		
Bit[31:28]	Reserved				Access bit [7:0] of the register located at address 0xC01B to access bit[31:24] of the register MTPARA2.
Bit27	DSPICK	0	To select the parity type for the output data from the DMA_SPI interfaces.	0, even parity; 1, odd parity.	
Bit26	DSPIMD	0	To select the frame format of the output data from the DMA_SPI interfaces.	0, 32-bit, one frame for a 32-bit data output; 1, 16-bit, two frames for a 32-bit data output.	
Bit25	PECEN	0	To disable gain calibrate the total active power in sections.	1, disable; 0, enable.	
Bit24	AECEN	0	To disable phase compensation in sections.	1, disable; 0, enable.	
Bit23	Reserved				Access bit

0xC002, R/W, Metering Control Register 2, MTPARA2					
Bit		Default Value	Function Description		
Bit[22:16]	DSPIEN	0	To enable the raw waveform output of the channels from the DMA_SPI interfaces.	1, enable; 0, disable. Bit22, raw waveform of IN; Bit21, raw waveform of IC; Bit20, raw waveform of UC; Bit19, raw waveform of IB; Bit18, raw waveform of UB; Bit17, raw waveform of IA; Bit16, raw waveform of UA.	[7:0] of the register located at address 0xC01A to access bit[23:16] of the register MTPARA2.
Bit15	EGYEN	0	To enable accumulating energy in normal mode.	0, disable; 1, enable.	Access bit [7:0] of the register located at address 0xC019 to access bit[15:8] of the register MTPARA2.
Bit14	MTMODE	0	To select the 3-wire or 4-wire application.	0, 3-phase, 4-wire; 1, 3-phase, 3-wire.	
Bit13	APPMODE	0	To select the apparent power calculation method.	0, to calculate the apparent power based on the current RMS; 1, to calculate the apparent power based on the active and reactive power.	
Bit12	DIDTEN	0	To enable the digital integrator when a Rogowski coil is used for analog current input.	0, disable; 1, enable.	
Bit11	DCBYPASS	0	To switch on the direct current/voltage.	1, enable. When the direct current/voltage is switched on, no high-pass filter is applied to the raw waveform. And the signal composed of direct and alternating components is used for RMS calculation and energy metering.	
Bit[10:8]	CFFAST	0	To accelerate the pulse generation speed.	000~011, ×1; 100, ×4; 101, ×16; 110, ×64; 111, ×128.	

0xC002, R/W, Metering Control Register 2, MTPARA2					
Bit		Default Value	Function Description		
Bit[7:4]	CFCALC	0	To enable accumulating the total/fundamental active/reactive/apparent energy in high-speed mode.	1, enable; 0, disable. Bit7, total/fundamental apparent energy on the overall system, or total reactive energy on the overall system (CF3); Bit6, total/fundamental active energy on the overall system (CF2); Bit5, total/fundamental reactive energy on the overall system (CF1); Bit4, total/fundamental active energy on the overall system (CF0).	Access bit [7:0] of the register located at address 0xC018 to access bit[7:0] of the register MTPARA2.
Bit[3:0]	CFON	0	To enable CF pulse output.	1, enable; 0, disable. Bit3, pulse output on the pin CF3; Bit2, pulse output on the pin CF2; Bit1, pulse output on the pin CF1; Bit0, pulse output on the pin CF0.	
Note: The configuration of this register can be read out of the register ZZPARA2 (0xEC29) which is to calculate the checksum for system check.					

Table 14-4 Metering Control Register 3 (0xC003, MTPARA3)

0xC003, R/W, Metering Control Register 3, MTPARA3			
Bit		Default Value	Function Description
Bit[31:0]	CHECKSUM	0	The configuration of this register can be read out of the register ZZPARA3 (0xEC2A) which is to calculate the checksum for system check. The sum of the values of the register ZZPARA3 (0xEC2A), on behalf of this register, and the other 109 registers for system check, is the

0xC003, R/W, Metering Control Register 3, MTPARA3			
Bit		Default Value	Function Description
			checksum. If the checksum is equal to 0xFFFFFFFF, the configuration is accurate; otherwise, some error happens, and an interrupt is generated and output from the pin IRQ0 all the time, or from the pin IRQ0 when it is enabled.

14.1.2.Registers for Power On The Overall System Calculation Mode

Table 14-5 Register for Total/Fundamental Active Power on The Overall System Calculation Mode 0 (0xEC23, ZZPA0)

0xEC23, R/W, Register for Total/Fundamental Active Power on The Overall System Calculation Mode 0, ZZPA0			
Bit		Default Value	Function Description
Bit[31:6]	Reserved		
Bit5	PCABS0	0	To select three power values to calculate the total or fundamental active power on the overall system. 1, select; 0, clear. Bit5, the absolute value of the instantaneous active power of Phase C; Bit4, the algebra value of the instantaneous active power of Phase C; Bit3, the absolute value of the instantaneous active power of Phase B; Bit2, the algebra value of the instantaneous active power of Phase B; Bit1, the absolute value of the instantaneous active power of Phase A; Bit0, the algebra value of the instantaneous active power of Phase A. For example, if the register is set to 0b100001, the total or fundamental active power on the overall system is the sum of the absolute value of the instantaneous active power of Phase C, 0, and the algebra value of the instantaneous active power of Phase A.
Bit4	PC0	0	
Bit3	PBABS0	0	
Bit2	PB0	0	
Bit1	PAABS0	0	
Bit0	PA0	0	

0xEC23, R/W, Register for Total/Fundamental Active Power on The Overall System Calculation Mode 0, ZZPA0			
Bit		Default Value	Function Description
			It is recommended to set to 0x15. The selection of the absolute and algebra value of the instantaneous active power of one phase cannot concur. This register is used to calculate the checksum for system check as a 32-bit register with the 26 most significant bits padded with 0s.

Table 14-6 Register for Total/Fundamental Active Power On The Overall System Calculation Mode 1 (0xEC24, ZZPA1)

0xEC24, R/W, Register for Total/Fundamental Active Power On The Overall System Calculation Mode 1, ZZPA1					
Bit		Default Value	Function Description		
Bit[31:6]	Reserved				
Bit5	PCABS1	0	To select three power values to calculate the total or fundamental active power on the overall system. 1, select; 0, clear. Bit5, the absolute value of the instantaneous active power of Phase C; Bit4, the algebra value of the instantaneous active power of Phase C; Bit3, the absolute value of the instantaneous active power of Phase B; Bit2, the algebra value of the instantaneous active power of Phase B; Bit1, the absolute value of the instantaneous active power of Phase A; Bit0, the algebra value of the instantaneous active power of Phase A. For example, if the register is set to 0b000110, the total or fundamental active power on the overall system is the sum of 0, the algebra value of the instantaneous active power of Phase B, and the absolute value of the instantaneous active power of Phase A. It is recommended to set to 0x2A.		
Bit4	PC1	0			
Bit3	PBABS1	0			
Bit2	PB1	0			
Bit1	PAABS1	0			
Bit0	PA1	0			

0xEC24, R/W, Register for Total/Fundamental Active Power On The Overall System Calculation Mode 1, ZZPA1			
Bit		Default Value	Function Description
			The selection of the absolute and algebra value of the instantaneous active power of one phase cannot concur. This register is used to calculate the checksum for system check as a 32-bit register with the 26 most significant bits padded with 0s.

Table 14-7 Register for Total/Fundamental Reactive Power On The Overall System Calculation Mode 0 (0xEC47, ZZQA0)

0xEC47, R/W, Register for Total/Fundamental Reactive Power on the overall system Calculation Mode 0, ZZQA0			
Bit		Default Value	Function Description
Bit[31:6]	Reserved	-	To select three power values to calculate the total or fundamental reactive power on the overall system. 1, select; 0, clear. Bit5, the absolute value of the instantaneous reactive power of Phase C; Bit4, the algebra value of the instantaneous reactive power of Phase C; Bit3, the absolute value of the instantaneous reactive power of Phase B; Bit2, the algebra value of the instantaneous reactive power of Phase B; Bit1, the absolute value of the instantaneous reactive power of Phase A; Bit0, the algebra value of the instantaneous reactive power of Phase A. For example, if the register is set to 0b100001, the total or fundamental reactive power on the overall system is the sum of the absolute value of the instantaneous reactive power of Phase C, 0, and the algebra value of the instantaneous reactive power of Phase A. It is recommended to set to 0x15. The selection of the absolute and algebra value of the instantaneous reactive power of one phase cannot concur.
Bit5	QCABS0	0	
Bit4	QC0	0	
Bit3	QBABS0	0	
Bit2	QB0	0	
Bit1	QAABS0	0	
Bit0	QA0	0	

0xEC47, R/W, Register for Total/Fundamental Reactive Power on the overall system Calculation Mode 0, ZZQA0			
Bit		Default Value	Function Description
			This register is used to calculate the checksum for system check as a 32-bit register with the 26 most significant bits padded with 0s.

Table 14-8 Register for Total/Fundamental Reactive Power On The Overall System Calculation Mode 1 (0xEC48, ZZQA1)

0xEC48, R/W, Register for Total/Fundamental Reactive Power On The Overall System Calculation Mode 1, ZZQA1			
Bit		Default Value	Function Description
Bit[31:6]	Reserved	-	To select three power values to calculate the total or fundamental reactive power on the overall system. 1, select; 0, clear. Bit5, the absolute value of the instantaneous reactive power of Phase C; Bit4, the algebra value of the instantaneous reactive power of Phase C; Bit3, the absolute value of the instantaneous reactive power of Phase B; Bit2, the algebra value of the instantaneous reactive power of Phase B; Bit1, the absolute value of the instantaneous reactive power of Phase A; Bit0, the algebra value of the instantaneous reactive power of Phase A. For example, if the register is set to 0b000110, the total or fundamental reactive power on the overall system is the sum of 0, the algebra value of the instantaneous reactive power of Phase B, and the absolute value of the instantaneous reactive power of Phase A. It is recommended to set to 0x2A. The selection of the absolute and algebra value of the instantaneous reactive power of one phase cannot concur. This register is used to calculate the checksum for system check as a 32-bit register with the 26 most significant bits padded with 0s.
Bit5	QCABS1	0	
Bit4	QC1	0	
Bit3	QBABS1	0	
Bit2	QB1	0	
Bit1	QAABS1	0	
Bit0	QA1	0	

Table 14-9 Register for Total/Fundamental Apparent Power On The Overall System Calculation Mode

(0xEC05, ZZAPPA)

0xEC05, R/W, Register for Total/Fundamental Apparent Power over All System Calculation Mode, ZZAPPA			
Bit		Default Value	Function Description
Bit[31:3]	Reserved	-	To select three power values to calculate the total or fundamental apparent power on the overall system. 1, select; 0, clear. Bit2, the instantaneous apparent power of Phase C; Bit1, the instantaneous apparent power of Phase B; Bit0, the instantaneous apparent power of Phase A; For example, if the register is set to 0b110, the total or fundamental apparent power on the overall system is the sum of the instantaneous apparent power of Phase C, the instantaneous apparent power of Phase B, and 0. It is recommended to set to 0x07. This register is used to calculate the checksum for system check as a 32-bit register with the 29 most significant bits padded with 0s.
Bit2	APPC	0	
Bit1	APPB	0	
Bit0	APPA	0	

14.1.3.Register for CF Pulse Source Selection

Table 14-10 Register for CF Pulse Source Selection (0xEC34, ZZPCF0A)

0xEC34, R/W, Register for CF Pulse Source Selection, ZZPCF0A				
Bit		Default Value	Function Description	
Bit[31:16]	Reserved	-	-	
Bit[15:12]	CF3PS	0	To set the source for the CF pulse output on the pin CF3.	1000~1111, the fundamental apparent power on the overall system; 0100~0111, the total apparent power on the overall system; 0010~0011, the absolute value of the total reactive power on the overall system in Mode 1; 0001, the absolute value of the total reactive power on the overall system in Mode 0; 0000, a non-zero random value. Via configuring the registers ZZQA0 (0xEC47), ZZQA1 (0xEC48), and ZZAPPA (0xEC05), the pin CF3 can be

0xEC34, R/W, Register for CF Pulse Source Selection, ZZPCF0A				
Bit		Default Value	Function Description	
				used to output CF pulse sourced the total reactive power or total/fundamental apparent power of each phase or on the overall system.
Bit[11:8]	CF2PS	0	To set the source for the CF pulse output on the pin CF2.	1000~1111, the absolute value of the fundamental active power on the overall system in Mode 1; 0100~0111, the absolute value of the fundamental active power on the overall system in Mode 0; 0010~0011, the absolute value of the total active power on the overall system in Mode 1; 0001, the absolute value of the total active power on the overall system in Mode 0; 0000, a non-zero random value. Via configuring the registers ZZPA0 (0xEC23) and ZZPA1 (0xEC24), the pin CF2 can be used to output CF pulse sourced the total/fundamental active power of each phase or on the overall system.
Bit[7:4]	CF1PS	0	To set the source for the CF pulse output on the pin CF1.	1000~1111, the absolute value of the fundamental reactive power on the overall system in Mode 1; 0100~0111, the absolute value of the fundamental reactive power on the overall system in Mode 0; 0010~0011, the absolute value of the total reactive power on the overall system in Mode 1; 0001, the absolute value of the total reactive power on the overall system in Mode 0; 0000, a non-zero random value. Via configuring the registers ZZQA0 (0xEC47) and ZZQA1 (0xEC48), the pin CF1 can be used to output CF pulse sourced the total/fundamental reactive power of each phase or on the overall system.
Bit[3:0]	CF0PS	0	To set the source for the CF pulse output on the pin CF0.	1000~1111, the absolute value of the fundamental active power on the overall system in Mode 1; 0100~0111, the absolute value of the fundamental active power on the overall system in Mode 0; 0010~0011, the absolute value of the total active power on the overall system in Mode 1;

0xEC34, R/W, Register for CF Pulse Source Selection, ZZPCF0A				
Bit		Default Value	Function Description	
				0001, the absolute value of the total active power on the overall system in Mode 0; 0000, a non-zero random value. Via configuring the registers ZZPA0 (0xEC23) and ZZPA1 (0xEC24), the pin CF0 can be used to output CF pulse sourced the total/fundamental active power of each phase or on the overall system.
This register is used to calculate the checksum for system check as a 32-bit register with the 16 most significant bits padded with 0s.				

14.2. Metering Data Registers

14.2.1.Registers for DC Component

Table 14-11 Registers for DC Component (R/W)

Address	Mnemonic	Description	R/W	Format	Remark
0xF02C	DCUA	The instantaneous direct voltage of Phase A.	R/W	24-bit, 2's complement	These registers, with bit23 being the sign bit, are accessed as a 32-bit register with sign extended to 32 bits. When the metering frequency is 6.5536MHz, these registers are updated once every 20ms, and the settling time is 100ms.
0xF02D	DCIA	The instantaneous direct current of Phase A.	R/W	24-bit, 2's complement	
0xF02E	DCUB	The instantaneous direct voltage of Phase B.	R/W	24-bit, 2's complement	
0xF02F	DCIB	The instantaneous direct current of Phase B.	R/W	24-bit, 2's complement	
0xF030	DCUC	The instantaneous direct voltage of Phase C.	R/W	24-bit, 2's complement	
0xF031	DCIC	The instantaneous direct current of Phase C.	R/W	24-bit, 2's complement	
0xF032	DCIN	The instantaneous direct current of Channel IN.	R/W	24-bit, 2's complement	

14.2.2.Registers for Line Frequency and Phase Angle of Each Phase

Table 14-12 Registers for Line Frequency and Phase Angle of Each Phase (R)

Address	Mnemonic	Description	R/W	Format	Default Value	Remark
0xC008	FA	The line frequency of Phase A.	R	17-bit, 2's complement	0	Positive, constantly. These registers are accessed as 32-bit registers with the 15 most significant bits padded with 0s. The measurement resolution is 0.0008Hz. When the metering frequency is 6.5536MHz, these registers are updated once every 640ms, and the settling time is associated with the signal strength. The weaker the signal is, the longer the settling time is, usually more than 1s.
0xC009	FB	The line frequency of Phase B.	R	17-bit, 2's complement	0	
0xC00A	FC	The line frequency of Phase C.	R	17-bit, 2's complement	0	
0xC00B	PHSUB	The voltage phase angle of Phase B.	R	12-bit, 2's complement	0	The phase angle of each signal is measured relative to the voltage phase angle of Phase A. So, the voltage phase angle of Phase A is 0, constantly. These registers are accessed as a 32-bit register with the 20 most significant bits padded with 0s. The measurement resolution is 0.175°. When the metering frequency is 6.5536MHz, these registers is updated once every 20ms, and the settling time is associated with the signal strength. The smaller the signal is, the longer the settling time is, usually more than 1s.
0xC00C	PHSUC	The voltage phase angle of Phase C.	R	12-bit, 2's complement	0	
0xC00D	PHSIA	The current phase angle of Phase A.	R	12-bit, 2's complement	0	
0xC00E	PHSIB	The current phase angle of Phase B.	R	12-bit, 2's complement	0	
0xC00F	PHSIC	The current	R	12-bit, 2's complement	0	

Address	Mnemonic	Description	R/W	Format	Default Value	Remark
		phase angle of Phase C.				

14.2.3.Registers for Power Factor

Table 14-13 Registers for Total Power Factor (R/W)

Address	Mnemonic	Description	R/W	Format	Remark
0xE811	AFA	The instantaneous total power factor of Phase A.	R/W	32-bit, unsigned	Power factor is calculated following the equation: $Powerfactor = \frac{\lvert instantaneousactivepower \rvert}{instantaneousapparentpower}$ When the ratio of the value of these registers to the number 2^31 is more than 1, the power factor is 1. When the metering frequency is 6.5536MHz, the updating time of the instantaneous power factor registers is 80ms, and the settling time is 400ms; the updating time of the average power factor registers is 640ms, and the settling time is 1s. When the metering frequency is 1.6384MHz, the updating time of the instantaneous power factor registers is 320ms, and the settling time is 1.6s; the updating time of the average power factor registers is 2.56s, and the settling time is 4s. When the metering frequency is 819.2kHz, the updating time of the instantaneous power factor registers is 640ms, and the settling time is 3.2s; the updating time of the average power factor registers is 5.12s, and the settling time is 8s.
0xE812	AFB	The instantaneous total power factor of Phase B.	R/W	32-bit, unsigned	
0xE813	AFC	The instantaneous total power factor of Phase C.	R/W	32-bit, unsigned	
0xE814	AFS	The instantaneous total power factor on the overall system.	R/W	32-bit, unsigned	
0xE8E4	MAFA	The average total power factor of Phase A.	R/W	32-bit, unsigned	
0xE8E5	MAFB	The average total power factor of Phase B.	R/W	32-bit, unsigned	
0xE8E6	MAFC	The average total power factor of Phase C.	R/W	32-bit, unsigned	

Address	Mnemonic	Description	R/W	Format	Remark
0xE8E7	MAFS	The average total power factor on the overall system.	R/W	32-bit, unsigned	

Table 14-14 Registers for Fundamental Power Factor (R/W)

Address	Mnemonic	Description	R/W	Format	Remark
0xE857	BFA	The instantaneous fundamental power factor of Phase A.	R/W	32-bit, unsigned	Power factor is calculated following the equation: $Powerfactor = \frac{\lvert instantaneousactivepower \rvert}{instantaneousapparentpower}$ When the ratio of the value of these registers to the number 2^31 is more than 1, the power factor is 1. When the metering frequency is 6.5536MHz, the updating time of the instantaneous power factor registers is 80ms, and the settling time is 450ms; the updating time of the average power factor registers is 640ms, and the settling time is 1s. When the metering frequency is 1.6384MHz, the updating time of the instantaneous power factor registers is 320ms, and the settling time is 1.8s; the updating time of the average power factor registers is 2.56s, and the settling time is 4s. When the metering frequency is 819.2kHz, the updating time of the instantaneous power factor registers is 640ms, and the settling time is 3.6s; the updating time of the average power factor registers is 5.12s, and the settling time is 8s.
0xE858	BFB	The instantaneous fundamental power factor of Phase B.	R/W	32-bit, unsigned	
0xE859	BFC	The instantaneous fundamental power factor of Phase C.	R/W	32-bit, unsigned	
0xE85A	BFS	The instantaneous fundamental power factor on the overall system.	R/W	32-bit, unsigned	
0xE8F9	MBFA	The average fundamental power factor of Phase A.	R/W	32-bit, unsigned	
0xE8FA	MBFB	The average fundamental power factor of Phase B.	R/W	32-bit, unsigned	
0xE8FB	MBFC	The average fundamental power factor of Phase C.	R/W	32-bit, unsigned	
0xE8FC	MBFS	The average	R/W	32-bit,	

Address	Mnemonic	Description	R/W	Format	Remark
		fundamental power factor on the overall system.		unsigned	

14.2.4.Registers for RMS

All the RMS registers are in the format of 32-bit 2's complement, and positive constantly.

Table 14-15 Registers for Total Current/Voltage RMS (R/W)

Address	Mnemonic	Description	R/W	Format	Remark
0xE83E	ARTIA	The instantaneous total current RMS of Phase A.	R/W	32-bit, 2's complement	When the metering frequency is 6.5536MHz, the updating time of the registers is 20ms, and the settling time is 150ms. When the metering frequency is 1.6384MHz, the updating time of the registers is 80ms, and the settling time is 600ms. When the metering frequency is 819.2kHz, the updating time of content of the registers is 160ms, and the settling time is 1200ms.
0xE83F	ARTIB	The instantaneous total current RMS of Phase B.	R/W	32-bit, 2's complement	
0xE840	ARTIC	The instantaneous total current RMS of Phase C.	R/W	32-bit, 2's complement	
0xE841	ARTIN	The instantaneous total current RMS of Channel IN.	R/W	32-bit, 2's complement	
0xE842	ARTUA	The instantaneous total voltage RMS of Phase A.	R/W	32-bit, 2's complement	
0xE843	ARTUB	The instantaneous total voltage RMS of Phase B.	R/W	32-bit, 2's complement	
0xE844	ARTUC	The instantaneous total voltage RMS of Phase C.	R/W	32-bit, 2's complement	
0xE944	MUA	The average total voltage RMS of Phase A.	R/W	32-bit, 2's complement	When the metering frequency is 6.5536MHz, the updating time of the registers is 640ms, and the settling time is 1s. When the metering frequency is 1.6384MHz, the updating time of the registers is 2.56s, and the settling time is 4s. When the metering frequency is 819.2kHz, the updating time of content
0xE945	MUB	The average total voltage RMS of Phase B.	R/W	32-bit, 2's complement	
0xE946	MUC	The average total voltage RMS of Phase C.	R/W	32-bit, 2's complement	
0xE90E	MIA	The average total current RMS of Phase A.	R/W	32-bit, 2's complement	
0xE90F	MIB	The average total current RMS of Phase B.	R/W	32-bit, 2's complement	
0xE910	MIC	The average total current RMS of Phase C.	R/W	32-bit, 2's complement	

Address	Mnemonic	Description	R/W	Format	Remark
0xE911	MIN	The average total current RMS of Channel IN.	R/W	32-bit, 2's complement	of the registers is 5.12s, and the settling time is 8s.
0xE94B	MUM	The algebra sum of the total current RMS on the overall system.	R/W	32-bit, 2's complement	

Table 14-16 Registers for Fundamental Current/Voltage RMS (R/W)

Address	Mnemonic	Description	R/W	Format	Remark
0xE880	BRTIA	The instantaneous fundamental current RMS of Phase A.	R/W	32-bit, 2's complement	When the metering frequency is 6.5536MHz, the updating time of the registers is 20ms, and the settling time is 200ms. When the metering frequency is 1.6384MHz, the updating time of the registers is 80ms, and the settling time is 800ms. When the metering frequency is 819.2kHz, the updating time of content of the registers is 160ms, and the settling time is 1.6s.
0xE881	BRTIB	The instantaneous fundamental current RMS of Phase B.	R/W	32-bit, 2's complement	
0xE882	BRTIC	The instantaneous fundamental current RMS of Phase C.	R/W	32-bit, 2's complement	
0xE883	BRTUA	The instantaneous fundamental voltage RMS of Phase A.	R/W	32-bit, 2's complement	
0xE884	BRTUB	The instantaneous fundamental voltage RMS of Phase B.	R/W	32-bit, 2's complement	
0xE885	BRTUC	The instantaneous fundamental voltage RMS of Phase C.	R/W	32-bit, 2's complement	
0xE8FD	MBIA	The average fundamental current RMS of Phase A.	R/W	32-bit, 2's complement	When the metering frequency is 6.5536MHz, the updating time of the registers is 640ms, and the settling time is 1s. When the metering frequency is 1.6384MHz, the updating time of the registers is 2.56s, and the settling time is 4s. When the metering frequency is 819.2kHz, the updating time of content of the registers is 5.12s,
0xE8FE	MBIB	The average fundamental current RMS of Phase B.	R/W	32-bit, 2's complement	
0xE8FF	MBIC	The average fundamental current RMS of Phase C.	R/W	32-bit, 2's complement	
0xE90B	MBUA	The average fundamental voltage RMS of Phase A.	R/W	32-bit, 2's complement	
0xE90C	MBUB	The average fundamental voltage RMS of Phase B.	R/W	32-bit, 2's complement	
0xE90D	MBUC	The average fundamental voltage RMS of Phase C.	R/W	32-bit, 2's complement	

Address	Mnemonic	Description	R/W	Format	Remark
					and the settling time is 8s.

14.2.5.Power Registers

Table 14-17 Total Active/Reactive/Apparent Power Registers (R/W)

Address	Mnemonic	Description	R/W	Format	Remark
0xE801	AABSPSUM0	The absolute value of the instantaneous total active power on the overall system in Calculation Mode 0.	R/W	32-bit, 2's complement	Positive, constantly. When the metering frequency is 6.5536MHz, the updating time of the registers is 80ms, and the settling time is 400ms. When the metering frequency is 1.6384MHz, the updating time of the registers is 320ms, and the settling time is 1.6s. When the metering frequency is 819.2kHz, the updating time of content of the registers is 640ms, and the settling time is 3.2s.
0xE802	AABSPSUM1	The absolute value of the instantaneous total active power on the overall system in Calculation Mode 1.	R/W	32-bit, 2's complement	
0xE803	AABSQSUM0	The absolute value of the instantaneous total reactive power on the overall system in Calculation Mode 0.	R/W	32-bit, 2's complement	
0xE804	AABSQSUM1	The absolute value of the instantaneous total reactive power on the overall system in Calculation Mode 1.	R/W	32-bit, 2's complement	
0xE805	ABSAPA	The absolute value of the instantaneous total active power of Phase A.	R/W	32-bit, 2's complement	
0xE806	ABSAPB	The absolute value of the instantaneous total active power of Phase B.	R/W	32-bit, 2's complement	
0xE807	ABSAPC	The absolute value of the instantaneous total active power of Phase C.	R/W	32-bit, 2's complement	
0xE808	ABSAQA	The absolute value of the instantaneous total reactive power of Phase A.	R/W	32-bit, 2's complement	
0xE809	ABSAQB	The absolute value of the instantaneous total reactive power of Phase B.	R/W	32-bit, 2's complement	
0xE80A	ABSAQC	The absolute value of the instantaneous total reactive	R/W	32-bit, 2's complement	

Address	Mnemonic	Description	R/W	Format	Remark
		power of Phase C.			
0xE81F	APPA	The instantaneous total apparent power of Phase A.	R/W	32-bit, 2's complement	When the metering frequency is 6.5536MHz, the updating time of the registers is 80ms, and the settling time is 400ms. When the metering frequency is 1.6384MHz, the updating time of the registers is 320ms, and the settling time is 1.6s. When the metering frequency is 819.2kHz, the updating time of content of the registers is 640ms, and the settling time is 3.2s.
0xE820	APPB	The instantaneous total apparent power of Phase B.	R/W	32-bit, 2's complement	
0xE821	APPC	The instantaneous total apparent power of Phase C.	R/W	32-bit, 2's complement	
0xE822	APSUM0	The algebra value of the instantaneous total active power on the overall system in Calculation Mode 0.	R/W	32-bit, 2's complement	
0xE823	APSUM1	The algebra value of the instantaneous total active power on the overall system in Calculation Mode 1.	R/W	32-bit, 2's complement	
0xE824	APTLA	The algebra value of the instantaneous total active power of Phase A.	R/W	32-bit, 2's complement	
0xE825	APTLB	The algebra value of the instantaneous total active power of Phase B.	R/W	32-bit, 2's complement	
0xE826	APTLC	The algebra value of the instantaneous total active power of Phase C.	R/W	32-bit, 2's complement	
0xE831	AQSUM0	The algebra value of the instantaneous total reactive power on the overall system in Calculation Mode 0.	R/W	32-bit, 2's complement	
0xE832	AQSUM1	The algebra value of the instantaneous total reactive power on the overall system in Calculation Mode 1.	R/W	32-bit, 2's complement	
0xE833	AQTLA	The algebra value of the instantaneous total reactive power of Phase A.	R/W	32-bit, 2's complement	
0xE834	AQTLB	The algebra value of the instantaneous total reactive power of Phase B.	R/W	32-bit, 2's complement	
0xE835	AQTLC	The algebra value of the	R/W	32-bit, 2's	

Address	Mnemonic	Description	R/W	Format	Remark
		instantaneous total reactive power of Phase C.		complement	
0xE84E	ASSUM	The instantaneous total apparent power on the overall system.	R/W	32-bit, 2's complement	
0xE8E8	MAPA	The average total active power of Phase A.	R/W	32-bit, 2's complement	When the metering frequency is 6.5536MHz, the updating time of the registers is 640ms, and the settling time is 1s. When the metering frequency is 1.6384MHz, the updating time of the registers is 2.56s, and the settling time is 4s. When the metering frequency is 819.2kHz, the updating time of content of the registers is 5.12s, and the settling time is 8s.
0xE8E9	MAPB	The average total active power of Phase B.	R/W	32-bit, 2's complement	
0xE8EA	MAPC	The average total active power of Phase C.	R/W	32-bit, 2's complement	
0xE8EB	MAPPA	The average total apparent power of Phase A.	R/W	32-bit, 2's complement	
0xE8EC	MAPPB	The average total apparent power of Phase B.	R/W	32-bit, 2's complement	
0xE8ED	MAPPC	The average total apparent power of Phase C.	R/W	32-bit, 2's complement	
0xE8EE	MAPSUM0	The average total active power on the overall system 0.	R/W	32-bit, 2's complement	
0xE8EF	MAPSUM1	The average total active power on the overall system 1.	R/W	32-bit, 2's complement	
0xE8F0	MAQA	The average total reactive power of Phase A.	R/W	32-bit, 2's complement	
0xE8F1	MAQB	The average total reactive power of Phase B.	R/W	32-bit, 2's complement	
0xE8F2	MAQC	The average total reactive power of Phase C.	R/W	32-bit, 2's complement	
0xE8F3	MAQSUM0	The average total reactive power on the overall system 0.	R/W	32-bit, 2's complement	
0xE8F4	MAQSUM1	The average total reactive power on the overall system 1.	R/W	32-bit, 2's complement	
0xE8F5	MASSUM	The average total apparent power on the overall system.	R/W	32-bit, 2's complement	

Table 14-18 Fundamental Active/Reactive/Apparent Power Registers (R/W)

Address	Mnemonic	Description	R/W	Format	Remark
0xE80B	ABSBPA	The absolute value of the instantaneous fundamental active power of Phase A.	R/W	32-bit, 2's complement	Positive, constantly. When the metering frequency is 6.5536MHz, the updating time of the registers is 80ms, and the settling time is 450ms. When the metering frequency is 1.6384MHz, the updating time of the registers is 320ms, and the settling time is 1.8s. When the metering frequency is 819.2kHz, the updating time of content of the registers is 640ms, and the settling time is 3.6s.
0xE80C	ABSBPB	The absolute value of the instantaneous fundamental active power of Phase B.	R/W	32-bit, 2's complement	
0xE80D	ABSBPC	The absolute value of the instantaneous fundamental active power of Phase C.	R/W	32-bit, 2's complement	
0xE80E	ABSBQA	The absolute value of the instantaneous fundamental reactive power of Phase A.	R/W	32-bit, 2's complement	
0xE80F	ABSBQB	The absolute value of the instantaneous fundamental reactive power of Phase B.	R/W	32-bit, 2's complement	
0xE810	ABSBQC	The absolute value of the instantaneous fundamental reactive power of Phase C.	R/W	32-bit, 2's complement	
0xE850	BABSPSUM0	The absolute value of the instantaneous fundamental active power on the overall system in Calculation Mode 0.	R/W	32-bit, 2's complement	
0xE851	BABSPSUM1	The absolute value of the instantaneous fundamental active power on the overall system in Calculation Mode 1.	R/W	32-bit, 2's complement	
0xE852	BABSQSUM0	The absolute value of the instantaneous fundamental reactive power on the overall system in Calculation Mode 0.	R/W	32-bit, 2's complement	

Address	Mnemonic	Description	R/W	Format	Remark
0xE853	BABSQSUM1	The absolute value of the instantaneous fundamental reactive power on the overall system in Calculation Mode 1.	R/W	32-bit, 2's complement	
0xE854	BAPPA	The instantaneous fundamental apparent power of Phase A.	R/W	32-bit, 2's complement	When the metering frequency is 6.5536MHz, the updating time of the registers is 80ms, and the settling time is 450ms. When the metering frequency is 1.6384MHz, the updating time of the registers is 320ms, and the settling time is 1.8s. When the metering frequency is 819.2kHz, the updating time of content of the registers is 640ms, and the settling time is 3.6s.
0xE855	BAPPB	The instantaneous fundamental apparent power of Phase B.	R/W	32-bit, 2's complement	
0xE856	BAPPC	The instantaneous fundamental apparent power of Phase C.	R/W	32-bit, 2's complement	
0xE864	BPSUM0	The algebra value of the instantaneous fundamental active power on the overall system in Calculation Mode 0.	R/W	32-bit, 2's complement	
0xE865	BPSUM1	The algebra value of the instantaneous fundamental active power on the overall system in Calculation Mode 1.	R/W	32-bit, 2's complement	
0xE866	BPTLA	The algebra value of the instantaneous fundamental active power of Phase A.	R/W	32-bit, 2's complement	
0xE867	BPTLB	The algebra value of the instantaneous fundamental active power of Phase B.	R/W	32-bit, 2's complement	
0xE868	BPTLC	The algebra value of the instantaneous fundamental active power of Phase C.	R/W	32-bit, 2's complement	
0xE875	BQSUM0	The algebra value of the instantaneous fundamental reactive power on the overall	R/W	32-bit, 2's complement	

Address	Mnemonic	Description	R/W	Format	Remark
		system in Calculation Mode 0.			
0xE876	BQSUM1	The algebra value of the instantaneous fundamental reactive power on the overall system in Calculation Mode 1.	R/W	32-bit, 2's complement	
0xE877	BQTLA	The algebra value of the instantaneous fundamental reactive power of Phase A.	R/W	32-bit, 2's complement	
0xE878	BQTLB	The algebra value of the instantaneous fundamental reactive power of Phase B.	R/W	32-bit, 2's complement	
0xE879	BQTLC	The algebra value of the instantaneous fundamental reactive power of Phase C.	R/W	32-bit, 2's complement	
0xE88C	BSSUM	The instantaneous fundamental apparent power on the overall system.	R/W	32-bit, 2's complement	
0xE8F6	MBAPPA	The average fundamental apparent power of Phase A.	R/W	32-bit, 2's complement	When the metering frequency is 6.5536MHz, the updating time of the registers is 640ms, and the settling time is 1s. When the metering frequency is 1.6384MHz, the updating time of the registers is 2.56s, and the settling time is 4s. When the metering frequency is 819.2kHz, the updating time of content of the registers is 5.12s, and the settling time is 8s.
0xE8F7	MBAPPB	The average fundamental apparent power of Phase B.	R/W	32-bit, 2's complement	
0xE8F8	MBAPPC	The average fundamental apparent power of Phase C.	R/W	32-bit, 2's complement	
0xE900	MBPA	The average fundamental active power of Phase A.	R/W	32-bit, 2's complement	
0xE901	MBPB	The average fundamental active power of Phase B.	R/W	32-bit, 2's complement	
0xE902	MBPC	The average fundamental active power of Phase C.	R/W	32-bit, 2's complement	
0xE903	MBPSUM0	The average fundamental	R/W	32-bit, 2's	

Address	Mnemonic	Description	R/W	Format	Remark
		active power on the overall system 0.		complement	
0xE904	MBPSUM1	The average fundamental active power on the overall system 1.	R/W	32-bit, 2's complement	
0xE905	MBQA	The average fundamental reactive power of Phase A.	R/W	32-bit, 2's complement	
0xE906	MBQB	The average fundamental reactive power of Phase B.	R/W	32-bit, 2's complement	
0xE907	MBQC	The average fundamental reactive power of Phase C.	R/W	32-bit, 2's complement	
0xE908	MBQSUM0	The average fundamental reactive power on the overall system 0.	R/W	32-bit, 2's complement	
0xE909	MBQSUM1	The average fundamental reactive power on the overall system 1.	R/W	32-bit, 2's complement	
0xE90A	MBSSUM	The average fundamental apparent power on the overall system.	R/W	32-bit, 2's complement	

14.2.6.Registers for Energy Accumulation and Pulse Generation in Normal Mode

Table 14-19 Registers for Total Active/Reactive/Apparent Energy Accumulation (R/W)

Address	Mnemonic	Description	R/W	Format
0xE8AC	EGYAPPAH	Higher 32 bits of the register for the total apparent energy of Phase A.	R/W	64-bit, unsigned, positive
0xE8AD	EGYAPPAL	Lower 32 bits of the register for the total apparent energy of Phase A.	R/W	
0xE8AE	EGYAPPBH	Higher 32 bits of the register for the total apparent energy of Phase B.	R/W	64-bit, unsigned, positive
0xE8AF	EGYAPPBL	Lower 32 bits of the register for the total apparent energy of Phase B.	R/W	

Address	Mnemonic	Description	R/W	Format
0xE8B0	EGYAPPCH	Higher 32 bits of the register for the total apparent energy of Phase C.	R/W	64-bit, unsigned, positive
0xE8B1	EGYAPPCL	Lower 32 bits of the register for the total apparent energy of Phase C.	R/W	
0xE8B2	EGYAPPSH	Higher 32 bits of the register for the total apparent energy on the overall system.	R/W	64-bit, unsigned, positive
0xE8B3	EGYAPPSL	Lower 32 bits of the register for the total apparent energy on the overall system.	R/W	
0xE8D0	EGYPAH	Higher 32 bits of the register for the total active energy of Phase A.	R/W	64-bit, unsigned, positive
0xE8D1	EGYPAL	Lower 32 bits of the register for the total active energy of Phase A.	R/W	
0xE8D2	EGYPBH	Higher 32 bits of the register for the total active energy of Phase B.	R/W	64-bit, unsigned, positive
0xE8D3	EGYPBL	Lower 32 bits of the register for the total active energy of Phase B.	R/W	
0xE8D4	EGYPCH	Higher 32 bits of the register for the total active energy of Phase C.	R/W	64-bit, unsigned, positive
0xE8D5	EGYPCL	Lower 32 bits of the register for the total active energy of Phase C.	R/W	
0xE8D6	EGYPS0H	Higher 32 bits of the register for the total active energy 0, accumulated by the total active power on the overall system in Calculation Mode 0.	R/W	64-bit, unsigned, positive
0xE8D7	EGYPS0L	Lower 32 bits of the register for the total active energy 0, accumulated by the total active power on the overall system in Calculation Mode 0.	R/W	
0xE8D8	EGYPS1H	Higher 32 bits of the register for the total active energy 1, accumulated by the total active power on the overall system in Calculation Mode 1.	R/W	64-bit, unsigned, positive
0xE8D9	EGYPS1L	Lower 32 bits of the register for the total active energy 1, accumulated by the total active power on the overall system in Calculation Mode 1.	R/W	
0xE8DA	EGYQAH	Higher 32 bits of the register for the total reactive energy of Phase A.	R/W	64-bit, unsigned, positive
0xE8DB	EGYQAL	Lower 32 bits of the register for the total reactive energy of Phase A.	R/W	
0xE8DC	EGYQBH	Higher 32 bits of the register for the total reactive energy	R/W	64-bit,

Address	Mnemonic	Description	R/W	Format
		of Phase B.		unsigned, positive
0xE8DD	EGYQBL	Lower 32 bits of the register for the total reactive energy of Phase B.	R/W	
0xE8DE	EGYQCH	Higher 32 bits of the register for the total reactive energy of Phase C.	R/W	64-bit, unsigned, positive
0xE8DF	EGYQCL	Lower 32 bits of the register for the total reactive energy of Phase C.	R/W	
0xE8E0	EGYQS0H	Higher 32 bits of the register for the total reactive energy 0, accumulated by the total reactive power on the overall system in Calculation Mode 0.	R/W	64-bit, unsigned, positive
0xE8E1	EGYQS0L	Lower 32 bits of the register for the total reactive energy 0, accumulated by the total reactive power on the overall system in Calculation Mode 0.	R/W	
0xE8E2	EGYQS1H	Higher 32 bits of the register for the total reactive energy 1, accumulated by the total reactive power on the overall system in Calculation Mode 1.	R/W	64-bit, unsigned, positive
0xE8E3	EGYQS1L	Lower 32 bits of the register for the total reactive energy 1, accumulated by the total reactive power on the overall system in Calculation Mode 1.	R/W	
When the metering frequency is 6.5536MHz, the energy accumulation frequency in normal mode is 12.5Hz.				

Table 14-20 Pulse Counters of the Total Active/Reactive/Apparent Energy (R/W)

Address	Mnemonic	Description	R/W	Format
0xE88D	CFAPPA	Pulse counter of the total apparent energy of Phase A.	R/W	32-bit, unsigned, positive
0xE88E	CFAPPB	Pulse counter of the total apparent energy of Phase B.	R/W	32-bit, unsigned, positive
0xE88F	CFAPPC	Pulse counter of the total apparent energy of Phase C.	R/W	32-bit, unsigned, positive
0xE890	CFAPPS	Pulse counter of the total apparent energy on the overall system.	R/W	32-bit, unsigned, positive
0xE89F	CFPA	Pulse counter of the total active energy of Phase A.	R/W	32-bit, unsigned, positive
0xE8A0	CFPB	Pulse counter of the total active energy of Phase B.	R/W	32-bit, unsigned, positive
0xE8A1	CFPC	Pulse counter of the total active energy of Phase C.	R/W	32-bit, unsigned, positive

Address	Mnemonic	Description	R/W	Format
0xE8A2	CFPS0	Pulse counter of the total active energy 0 on the overall system.	R/W	32-bit, unsigned, positive
0xE8A3	CFPS1	Pulse counter of the total active energy 1 on the overall system.	R/W	32-bit, unsigned, positive
0xE8A4	CFQA	Pulse counter of the total reactive energy of Phase A.	R/W	32-bit, unsigned, positive
0xE8A5	CFQB	Pulse counter of the total reactive energy of Phase B.	R/W	32-bit, unsigned, positive
0xE8A6	CFQC	Pulse counter of the total reactive energy of Phase C.	R/W	32-bit, unsigned, positive
0xE8A7	CFQS0	Pulse counter of the total reactive energy 0 on the overall system.	R/W	32-bit, unsigned, positive
0xE8A8	CFQS1	Pulse counter of the total reactive energy 1 on the overall system.	R/W	32-bit, unsigned, positive

Table 14-21 Registers for Fundamental Active/Reactive/Apparent Energy Accumulation (R/W)

Address	Mnemonic	Description	R/W	Format
0xE8B4	EGYBAPPAH	Higher 32 bits of the register for the fundamental apparent energy of Phase A.	R/W	64-bit, unsigned, positive
0xE8B5	EGYBAPPAL	Lower 32 bits of the register for the fundamental apparent energy of Phase A.	R/W	
0xE8B6	EGYBAPPBH	Higher 32 bits of the register for the fundamental apparent energy of Phase B.	R/W	64-bit, unsigned, positive
0xE8B7	EGYBAPPBL	Lower 32 bits of the register for the fundamental apparent energy of Phase B.	R/W	
0xE8B8	EGYBAPPCH	Higher 32 bits of the register for the fundamental apparent energy of Phase C.	R/W	64-bit, unsigned, positive
0xE8B9	EGYBAPPCL	Lower 32 bits of the register for the fundamental apparent energy of Phase C.	R/W	
0xE8BA	EGYBAPPSH	Higher 32 bits of the register for the fundamental apparent energy on the overall system.	R/W	64-bit, unsigned, positive
0xE8BB	EGYBAPPSL	Lower 32 bits of the register for the fundamental apparent energy on the overall system.	R/W	
0xE8BC	EGYBPAH	Higher 32 bits of the register for the fundamental active energy of Phase A.	R/W	64-bit, unsigned, positive
0xE8BD	EGYBPAL	Lower 32 bits of the register for the fundamental active energy of Phase A.	R/W	

Address	Mnemonic	Description	R/W	Format
0xE8BE	EGYBPBH	Higher 32 bits of the register for the fundamental active energy of Phase B.	R/W	64-bit, unsigned, positive
0xE8BF	EGYBPBL	Lower 32 bits of the register for the fundamental active energy of Phase B.	R/W	
0xE8C0	EGYBPCH	Higher 32 bits of the register for the fundamental active energy of Phase C.	R/W	64-bit, unsigned, positive
0xE8C1	EGYBPCL	Lower 32 bits of the register for the fundamental active energy of Phase C.	R/W	
0xE8C2	EGYBPS0H	Higher 32 bits of the register for the fundamental active energy 0, accumulated by the fundamental active power on the overall system in Calculation Mode 0.	R/W	64-bit, unsigned, positive
0xE8C3	EGYBPS0L	Lower 32 bits of the register for the fundamental active energy 0, accumulated by the fundamental active power on the overall system in Calculation Mode 0.	R/W	
0xE8C4	EGYBPS1H	Higher 32 bits of the register for the fundamental active energy 1, accumulated by the fundamental active power on the overall system in Calculation Mode 1.	R/W	64-bit, unsigned, positive
0xE8C5	EGYBPS1L	Lower 32 bits of the register for the fundamental active energy 1, accumulated by the fundamental active power on the overall system in Calculation Mode 1.	R/W	
0xE8C6	EGYBQAH	Higher 32 bits of the register for the fundamental reactive energy of Phase A.	R/W	64-bit, unsigned, positive
0xE8C7	EGYBQAL	Lower 32 bits of the register for the fundamental reactive energy of Phase A.	R/W	
0xE8C8	EGYBQBH	Higher 32 bits of the register for the fundamental reactive energy of Phase B.	R/W	64-bit, unsigned, positive
0xE8C9	EGYBQBL	Lower 32 bits of the register for the fundamental reactive energy of Phase B.	R/W	
0xE8CA	EGYBQCH	Higher 32 bits of the register for the fundamental reactive energy of Phase C.	R/W	64-bit, unsigned, positive
0xE8CB	EGYBQCL	Lower 32 bits of the register for the fundamental reactive energy of Phase C.	R/W	
0xE8CC	EGYBQS0H	Higher 32 bits of the register for the fundamental reactive energy 0, accumulated by the fundamental	R/W	64-bit, unsigned,

Address	Mnemonic	Description	R/W	Format
		reactive power on the overall system in Calculation Mode 0.		positive
0xE8CD	EGYBQS0L	Lower 32 bits of the register for the fundamental reactive energy 0, accumulated by the fundamental reactive power on the overall system in Calculation Mode 0.	R/W	
0xE8CE	EGYBQS1H	Higher 32 bits of the register for the fundamental reactive energy 1, accumulated by the fundamental reactive power on the overall system in Calculation Mode 1.	R/W	64-bit, unsigned, positive
0xE8CF	EGYBQS1L	Lower 32 bits of the register for the fundamental reactive energy 1, accumulated by the fundamental reactive power on the overall system in Calculation Mode 1.	R/W	
When the metering frequency is 6.5536MHz, the energy accumulation frequency in normal mode is 12.5Hz.				

Table 14-22 Pulse Counters of the Fundamental Active/Reactive/Apparent Energy (R/W)

Address	Mnemonic	Description	R/W	Format
0xE891	CFBAPPA	Pulse counter of the fundamental apparent energy of Phase A.	R/W	32-bit, unsigned, positive
0xE892	CFBAPPB	Pulse counter of the fundamental apparent energy of Phase B.	R/W	32-bit, unsigned, positive
0xE893	CFBAPPC	Pulse counter of the fundamental apparent energy of Phase C.	R/W	32-bit, unsigned, positive
0xE894	CFBAPPS	Pulse counter of the fundamental apparent energy on the overall system.	R/W	32-bit, unsigned, positive
0xE895	CFBPA	Pulse counter of the fundamental active energy of Phase A.	R/W	32-bit, unsigned, positive
0xE896	CFBPB	Pulse counter of the fundamental active energy of Phase B.	R/W	32-bit, unsigned, positive
0xE897	CFBPC	Pulse counter of the fundamental active energy of Phase C.	R/W	32-bit, unsigned, positive
0xE898	CFBPS0	Pulse counter of the fundamental active energy 0 on the overall system.	R/W	32-bit, unsigned, positive
0xE899	CFBPS1	Pulse counter of the fundamental active energy 1 on the overall system.	R/W	32-bit, unsigned, positive
0xE89A	CFBQA	Pulse counter of the fundamental reactive energy of Phase A.	R/W	32-bit, unsigned, positive

Address	Mnemonic	Description	R/W	Format
0xE89B	CFBQB	Pulse counter of the fundamental reactive energy of Phase B.	R/W	32-bit, unsigned, positive
0xE89C	CFBQC	Pulse counter of the fundamental reactive energy of Phase C.	R/W	32-bit, unsigned, positive
0xE89D	CFBQS0	Pulse counter of the fundamental reactive energy 0 on the overall system.	R/W	32-bit, unsigned, positive
0xE89E	CFBQS1	Pulse counter of the fundamental reactive energy 1 on the overall system.	R/W	32-bit, unsigned, positive

14.2.7.Registers for Energy Accumulation and Pulse Generation in High-Speed Mode

Table 14-23 Registers for Power for Energy Accumulation in High-Speed Mode (R/W)

Address	Mnemonic	Description	R/W	Format	Remark
0xEC33	ZZPCF0	The total/fundamental active power on the overall system for energy accumulation in high-speed mode.	R/W	32-bit 2's complement	Positive, constantly. When the metering frequency is 6.5536MHz, the updating time of these registers is 80ms, and the settling time is 400ms. When the metering frequency is 1.6384MHz, the updating time of these registers is 320ms, and the settling time is 1.6s. When the metering frequency is 819.2kHz, the updating time of these registers is 640ms, and the settling time is 3.2s.
0xEC38	ZZPCF1	The total/fundamental reactive power on the overall system for energy accumulation in high-speed mode.	R/W	32-bit 2's complement	
0xEC3D	ZZPCF2	The total/fundamental active power on the overall system for energy accumulation in high-speed mode.	R/W	32-bit 2's complement	
0xEC42	ZZPCF3	The total/fundamental apparent power or the total reactive power on the overall system for energy accumulation in high-speed mode.	R/W	32-bit 2's complement	

Table 14-24 Energy Accumulation Registers in High-Speed Mode (R/W)

Address	Mnemonic	Description	R/W	Format	Remark
0xD000	EGY0L	Lower 32 bits of the register for the total/fundamental active energy on the	R/W	64-bit, unsigned,	When the metering

Address	Mnemonic	Description	R/W	Format	Remark
		overall system in high-speed mode (CF0).		positive	frequency is 6.5536MHz, the energy accumulation frequency in high-speed mode is 204.8kHz.
0xD001	EGY0H	Higher 32 bits of the register for the total/fundamental active energy on the overall system in high-speed mode (CF0).	R/W		
0xD002	EGY1L	Lower 32 bits of the register for the total/fundamental reactive energy on the overall system in high-speed mode (CF1).	R/W	64-bit, unsigned, positive	
0xD003	EGY1H	Higher 32 bits of the register for the total/fundamental reactive energy on the overall system in high-speed mode (CF1).	R/W		
0xD004	EGY2L	Lower 32 bits of the register for the total/fundamental active energy on the overall system in high-speed mode (CF2).	R/W	64-bit, unsigned, positive	
0xD005	EGY2H	Higher 32 bits of the register for the total/fundamental active energy on the overall system in high-speed mode (CF2).	R/W		
0xD006	EGY3L	Lower 32 bits of the register for the total/fundamental apparent energy or the total reactive energy on the overall system in high-speed mode (CF3).	R/W	64-bit, unsigned, positive	
0xD007	EGY3H	Higher 32 bits of the register for the total/fundamental apparent energy or the total reactive energy on the overall system in high-speed mode (CF3).	R/W		

Table 14-25 Pulse Counter in High-Speed Mode (R/W)

Address	Mnemonic	Description	R/W	Format	Remark
0xD008	CF0	Pulse counter of the total/fundamental active energy on the overall system in high-speed mode (CF0).	R/W	32-bit, unsigned, positive	When the CF pulse output is enabled, one CF pulse is output when the pulses counter increments by 2.
0xD009	CF1	Pulse counter of the total/fundamental reactive energy on the overall system in high-speed mode (CF1).	R/W	32-bit, unsigned, positive	

Address	Mnemonic	Description	R/W	Format	Remark
0XD00A	CF2	Pulse counter of the total/fundamental active energy on the overall system in high-speed mode (CF2).	R/W	32-bit, unsigned, positive	
0XD00B	CF3	Pulse counter of the total/fundamental apparent energy or the total reactive energy on the overall system in high-speed mode (CF3).	R/W	32-bit, unsigned, positive	

14.3. Registers for Calibration

14.3.1.Registers for Presetting Bias for Direct Current/Voltage

Table 14-26 Registers for Presetting Bias for Direct Current/Voltage

Address	Mnemonic	Description	R/W	Format	Remark
0xEC16	ZZDCIA	To preset the bias for the current of Phase A.	R/W	24-bit 2's complement	These registers, with bit23 being the sign bit, are accessed as 32-bit registers with sign extended to 32 bits. These registers are used to calculate the checksum for system check as 32-bit registers with sign extended to 32 bits.
0xEC17	ZZDCIB	To preset the bias for the current of Phase B.	R/W	24-bit 2's complement	
0xEC18	ZZDCIC	To preset the bias for the current of Phase C.	R/W	24-bit 2's complement	
0xEC19	ZZDCIN	To preset the bias for the current of Channel IN.	R/W	24-bit 2's complement	
0xEC1A	ZZDCUA	To preset the bias for the voltage of Phase A.	R/W	24-bit 2's complement	
0xEC1B	ZZDCUB	To preset the bias for the voltage of Phase B.	R/W	24-bit 2's complement	
0xEC1C	ZZDCUC	To preset the bias for the voltage of Phase C.	R/W	24-bit 2's complement	

14.3.2.Registers for Phase Compensation

Table 14-27 Phase Compensation Registers in Sections (R/W)

Address	Mnemonic	Description	R/W	Format	bit 31	.. .	Bit 24	Bit 23	...	Bit 16	Bit 15	...	Bit 8	Bit 7	...	Bit 0
0xE954	WAEC0	Section 0	R/W	32-bit 2's complement	Reserved			To set the phase compensation for Phase C.			To set the phase compensation for Phase B.			To set the phase compensation for Phase A.		
0xE955	WAEC1	Section 1	R/W	32-bit 2's complement	Reserved			To set the phase compensation for Phase C.			To set the phase compensation for Phase B.			To set the phase compensation for Phase A.		
0xE956	WAEC2	Section 2	R/W	32-bit 2's complement	Reserved			To set the phase compensation for Phase C.			To set the phase compensation for Phase B.			To set the phase compensation for Phase A.		
0xE957	WAEC3	Section 3	R/W	32-bit 2's complement	Reserved			To set the phase compensation for Phase C.			To set the phase compensation for Phase B.			To set the phase compensation for Phase A.		
0xE958	WAEC4	Section 4	R/W	32-bit 2's complement	Reserved			To set the phase compensation for Phase C.			To set the phase compensation for Phase B.			To set the phase compensation for Phase A.		

Note: bit23/bit15/bi7 is the sign bit of the phase compensation. 1, negative; 0, positive. The phase compensation resolution is 0.022°/lsb, and the compensation is over the range -2.8°~+2.8°. When the function of phase compensation in sections is disabled, only the registers of Section 0 are used, and it is recommended to write the content of the Section 0 registers to the other registers.

All the registers are used to calculate the checksum for system check.

Table 14-28 Current Threshold for Phase Compensation in Sections (R/W)

Address	Mnemonic	Description	R/W	Format	Remark
0xE97C	WTPA0A	To set Current Threshold 0 for Phase A	R/W	32-bit 2's complement	Compare the instantaneous fundamental current RMS after calibration (IRMS) to the set current thresholds for each
0xE97D	WTPA0B	To set Current	R/W	32-bit 2's	

Address	Mnemonic	Description	R/W	Format	Remark
		Threshold 0 for Phase B		complement	phase, and then decide to use the register for phase compensation in sections for calibrating phase angle error. Take Phase A for example, When IRMS<WTPA0A, WAEC0 register is used; When WTPA0A<IRMS<WTPA1A, WAEC1 register is used; When WTPA1A<IRMS<WTPA2A, WAEC2 register is used; When WTPA2A<IRMS<WTPA3A, WAEC3 register is used; When IRMS>WTPA3A, WAEC4 register is used. All the registers are used to calculate the checksum for system check.
0xE97E	WTPA0C	To set Current Threshold 0 for Phase C	R/W	32-bit 2's complement	
0xE97F	WTPA1A	To set Current Threshold 1 for Phase A	R/W	32-bit 2's complement	
0xE980	WTPA1B	To set Current Threshold 1 for Phase B	R/W	32-bit 2's complement	
0xE981	WTPA1C	To set Current Threshold 1 for Phase C	R/W	32-bit 2's complement	
0xE982	WTPA2A	To set Current Threshold 2 for Phase A	R/W	32-bit 2's complement	
0xE983	WTPA2B	To set Current Threshold 2 for Phase B	R/W	32-bit 2's complement	
0xE984	WTPA2C	To set Current Threshold 2 for Phase C	R/W	32-bit 2's complement	
0xE985	WTPA3A	To set Current Threshold 3 for Phase A	R/W	32-bit 2's complement	
0xE986	WTPA3B	To set Current Threshold 3 for Phase B	R/W	32-bit 2's complement	
0xE987	WTPA3C	To set Current Threshold 3 for Phase C	R/W	32-bit 2's complement	

14.3.3.Registers for RMS Calibration

Table 14-29 Registers for Calibrating Total Voltage/Current RMS (R/W)

Address	Mnemonic	Description	R/W	Format
0xE968	WARTIA	To set gain calibration of the total current RMS of Phase A.	R/W	32-bit 2's complem

Address	Mnemonic	Description	R/W	Format
0xE969	WARTIB	To set gain calibration of the total current RMS of Phase B.	R/W	32-bit 2's complem
0xE96A	WARTIC	To set gain calibration of the total current RMS of Phase C.	R/W	32-bit 2's complem
0xE96B	WARTIN	To set gain calibration of the total current RMS of Channel IN.	R/W	32-bit 2's complem
0xE96C	WARTUA	To set gain calibration of the total voltage RMS of Phase A.	R/W	32-bit 2's complem
0xE96D	WARTUB	To set gain calibration of the total voltage RMS of Phase B.	R/W	32-bit 2's complem
0xE96E	WARTUC	To set gain calibration of the total voltage RMS of Phase C.	R/W	32-bit 2's complem
0xE994	WWARTIA	To set offset calibration of the total current RMS of Phase A.	R/W	32-bit 2's complem
0xE995	WWARTIB	To set offset calibration of the total current RMS of Phase B.	R/W	32-bit 2's complem
0xE996	WWARTIC	To set offset calibration of the total current RMS of Phase C.	R/W	32-bit 2's complem
0xE997	WWARTIN	To set offset calibration of the total current RMS of Channel IN.	R/W	32-bit 2's complem
0xE998	WWARTUA	To set offset calibration of the total voltage RMS of Phase A.	R/W	32-bit 2's complem
0xE999	WWARTUB	To set offset calibration of the total voltage RMS of Phase B.	R/W	32-bit 2's complem
0xE99A	WWARTUC	To set offset calibration of the total voltage RMS of Phase C.	R/W	32-bit 2's complem

Table 14-30 Registers for Calibrating Fundamental Voltage/Current RMS (R/W)

Address	Mnemonic	Description	R/W	Format
0xE976	WBRTIA	To set gain calibration of the fundamental current RMS of Phase A.	R/W	32-bit complement
0xE977	WBRTIB	To set gain calibration of the fundamental current RMS of Phase B.	R/W	32-bit complement
0xE978	WBRTIC	To set gain calibration of the fundamental current RMS of Phase C.	R/W	32-bit complement
0xE979	WBRTUA	To set gain calibration of the fundamental voltage RMS of Phase A.	R/W	32-bit complement
0xE97A	WBRTUB	To set gain calibration of the fundamental voltage RMS of Phase B.	R/W	32-bit complement
0xE97B	WBRTUC	To set gain calibration of the fundamental voltage RMS of Phase C.	R/W	32-bit complement
0xE9A2	WWBRTIA	To set offset calibration of the fundamental current RMS of Phase A.	R/W	32-bit complement
0xE9A3	WWBRTIB	To set offset calibration of the fundamental current RMS of Phase B.	R/W	32-bit complement

Address	Mnemonic	Description	R/W	Format
0xE9A4	WWBRTIC	To set offset calibration of the fundamental current RMS of Phase C.	R/W	32-bit complement
0xE9A5	WWBRTUA	To set offset calibration of the fundamental voltage RMS of Phase A.	R/W	32-bit complement
0xE9A6	WWBRTUB	To set offset calibration of the fundamental voltage RMS of Phase B.	R/W	32-bit complement
0xE9A7	WWBRTUC	To set offset calibration of the fundamental voltage RMS of Phase C.	R/W	32-bit complement

14.3.4.Registers for Power Calibration

Table 14-31 Registers for Calibrating Total Active/Reactive Power (R/W)

Address	Mnemonic	Description	R/W	Format	Remark
0xE959	WAPTA	To set gain calibration of the total active power of Phase A.	R/W	32-bit 2's complement	The read of the registers in decimal form is obtained via dividing the read in hexadecimal form by 2^31. The value of power before and after calibration have a relationship as follows: P=P'×(1+S)+C Where, P is the active or reactive power after calibration; P' is the active or reactive power before calibration; S is the gain calibration of the power; C is the offset calibration of the power. When the power calibration in sections is enabled, the content of the register gain calibration Section X of the power of each phase being used will be written in the register of power gain
0xE95A	WAPTAK0	To set gain calibration Section 0 of the total active power of Phase A.	R/W	32-bit 2's complement	
0xE95B	WAPTAK1	To set gain calibration Section 1 of the total active power of Phase A.	R/W	32-bit 2's complement	
0xE95C	WAPTAK2	To set gain calibration Section 2 of the total active power of Phase A.	R/W	32-bit 2's complement	
0xE95D	WAPTB	To set gain calibration of the total active power of Phase B.	R/W	32-bit 2's complement	
0xE95E	WAPTBK0	To set gain calibration Section 0 of the total active power of Phase B.	R/W	32-bit 2's complement	
0xE95F	WAPTBK1	To set gain calibration Section 1 of the total active power of Phase	R/W	32-bit 2's complement	

Address	Mnemonic	Description	R/W	Format	Remark
		B.			calibration. For example, if WAPTAK1 register is being used, its content will be written in the WAPTA register for power calibration of Phase A. When the function of power calibration in sections is disabled, only the registers of Section 0 are used, and it is recommended to write the content of the Section 0 register in the other registers. All the registers are used to calculate the checksum for system check.
0xE960	WAPTBK2	To set gain calibration Section 2 of the total active power of Phase B.	R/W	32-bit 2's complement	
0xE961	WAPTC	To set gain calibration of the total active power of Phase C.	R/W	32-bit 2's complement	
0xE962	WAPTCK0	To set gain calibration Section 0 of the total active power of Phase C.	R/W	32-bit 2's complement	
0xE963	WAPTCK1	To set gain calibration Section 1 of the total active power of Phase C.	R/W	32-bit 2's complement	
0xE964	WAPTCK2	To set gain calibration Section 2 of the total active power of Phase C.	R/W	32-bit 2's complement	
0xE965	WAQTA	To set gain calibration of the total reactive power of Phase A.	R/W	32-bit 2's complement	
0xE966	WAQTB	To set gain calibration of the total reactive power of Phase B.	R/W	32-bit 2's complement	
0xE967	WAQTC	To set gain calibration of the total reactive power of Phase C.	R/W	32-bit 2's complement	
0xE98E	WWAPTA	To set offset calibration of the total active power of Phase A.	R/W	32-bit 2's complement	
0xE98F	WWAPTB	To set offset calibration of the total active power of Phase B.	R/W	32-bit 2's complement	
0xE990	WWAPTC	To set offset calibration of the total active power of Phase C.	R/W	32-bit 2's complement	
0xE991	WWAQTA	To set offset calibration of the total reactive	R/W	32-bit 2's complement	

Address	Mnemonic	Description	R/W	Format	Remark
		power of Phase A.			
0xE992	WWAQTB	To set offset calibration of the total reactive power of Phase B.	R/W	32-bit 2's complement	
0xE993	WWAQTC	To set offset calibration of the total reactive power of Phase C.	R/W	32-bit 2's complement	

Table 14-32 Current Threshold for Calibrating Total Active Power in Sections (R/W)

Address	Mnemonic	Description	R/W	Format	Remark
0xE988	WTPP0A	To set Current Threshold 0 for calibrating the total active power of Phase A.	R/W	32-bit 2's complement	Compare the instantaneous current RMS after calibration (IRMS) to the set current thresholds for each phase, and then decide to use the register for power calibration in sections to calibrate the total active power of each phase. Take Phase A for example, When IRMS<WTPP0A, WAPTAK0 register is used; When WTPP0A<IRMS<WTPP1A, WAPTAK1 register is used; When WTPP1A<IRMS, WAPTAK2 register is used; All the registers are used to calculate the checksum for system check.
0xE989	WTPP0B	To set Current Threshold 0 for calibrating the total active power of Phase B.	R/W	32-bit 2's complement	
0xE98A	WTPP0C	To set Current Threshold 0 for calibrating the total active power of Phase C.	R/W	32-bit 2's complement	
0xE98B	WTPP1A	To set Current Threshold 1 for calibrating the total active power of Phase A.	R/W	32-bit 2's complement	
0xE98C	WTPP1B	To set Current Threshold 1 for calibrating the total active power of Phase B.	R/W	32-bit 2's complement	
0xE98D	WTPP1C	To set Current Threshold 1 for calibrating the total active power of Phase C.	R/W	32-bit 2's complement	

Table 14-33 Registers for Calibrating Fundamental Active/Reactive Power (R/W)

Address	Mnemonic	Description	R/W	Format	Remark
0xE970	WBPTA	To set gain calibration of the fundamental active power of Phase A.	R/W	32-bit 2's complement	The read of the registers in decimal form is obtained via dividing the read in hexadecimal form by 2^31. The value of power before and after calibration have a relationship as follows: P=P'×(1+S)+C Where, P is the active or reactive power after calibration; P' is the active or reactive power before calibration; S is the gain calibration of the power; C is the offset calibration of the power. All the registers are used to calculate the checksum for system check.
0xE971	WBPTB	To set gain calibration of the fundamental active power of Phase B.	R/W	32-bit 2's complement	
0xE972	WBPTC	To set gain calibration of the fundamental active power of Phase C.	R/W	32-bit 2's complement	
0xE973	WBQTA	To set gain calibration of the fundamental reactive power of Phase A.	R/W	32-bit 2's complement	
0xE974	WBQTB	To set gain calibration of the fundamental reactive power of Phase B.	R/W	32-bit 2's complement	
0xE975	WBQTC	To set gain calibration of the fundamental reactive power of Phase C.	R/W	32-bit 2's complement	
0xE99C	WWBPTA	To set offset calibration of the fundamental active power of Phase A.	R/W	32-bit 2's complement	
0xE99D	WWBPTB	To set offset calibration of the fundamental active power of Phase B.	R/W	32-bit 2's complement	
0xE99E	WWBPTC	To set offset calibration of the fundamental active power of Phase C.	R/W	32-bit 2's complement	
0xE99F	WWBQTA	To set offset calibration of the fundamental reactive power of Phase A.	R/W	32-bit 2's complement	
0xE9A0	WWBQTB	To set offset calibration of the fundamental reactive power of Phase B.	R/W	32-bit 2's complement	
0xE9A1	WWBQTC	To set offset calibration of the fundamental reactive power of Phase C.	R/W	32-bit 2's complement	

14.3.5.Threshold Registers

Table 14-34 Energy Threshold Registers (R/W)

Address	Mnemonic	Description	R/W	Format	Remark
0xEC1E	ZZEGYTHH	To set the higher 32 bits of the energy threshold.	R/W	32-bit 2's complement	The threshold for the energy accumulation and pulse generation in high-speed mode is 16384 times of that in normal mode. These registers are accessed as 32-bit registers with 14 most significant bits padded with 0s. All the registers are used to calculate the checksum for system check.
0xEC1F	ZZEGYTHL	To set the lower 32 bits of the energy threshold.	R/W	32-bit 2's complement	

Table 14-35 Table 14-36 Threshold for Current Detection (0xEC1D, ZZDCUM, R/W)

Address	Mnemonic	Description	R/W	Format	Remark
0xEC1D	ZZDCUM	To set the threshold for current detection.	R/W	24-bit 2's complement	This register, with bit23 being the sign bit, is accessed as a 32-bit register with sign extended to 32bits. This register is used to calculate the checksum for system check with sign extended to 32 bits.

14.4. System State Registers

Table 14-37 State Register for Phase Compensation and Gain Calibration of the Total Active Power (0xC004, PECAEC)

0xC004, R, State Register for Phase Compensation and Gain Calibration of the Total Active Power, PECAEC				
Bit		Default Value	Function Description	
Bit[31:22]	Reserved	-		
Bit[21:20]	PECC	-	To indicate the section being used for gain calibrating the total active power of Phase C.	00, Section 0; 01, Section 1; 10, Section 2.
Bit[19:18]	Reserved	-		
Bit[17:16]	PECB	-	To indicate the section being used for gain calibrating the total active power of Phase B.	00, Section 0; 01, Section 1; 10, Section 2.

0xC004, R, State Register for Phase Compensation and Gain Calibration of the Total Active Power, PECAEC				
Bit		Default Value	Function Description	
Bit[15:14]	Reserved	-		
Bit[13:12]	PECA	-	To indicate the section being used for gain calibrating the total active power of Phase A.	00, Section 0; 01, Section 1; 10, Section 2.
Bit11	Reserved	-		
Bit[10:8]	AECC	-	To indicate the section being used for phase compensation of Phase C.	000, Section 0; 001, Section 1; 010, Section 2; 011, Section 3; 100, Section 4.
Bit7	Reserved	-		
Bit[6:4]	AECB	-	To indicate the section being used for phase compensation of Phase C.	000, Section 0; 001, Section 1; 010, Section 2; 011, Section 3; 100, Section 4.
Bit3	Reserved	-		
Bit[2:0]	AECA	-	To indicate the section being used for phase compensation of Phase C.	000, Section 0; 001, Section 1; 010, Section 2; 011, Section 3; 100, Section 4.
When the metering frequency is 6.5536MHz, the updating time of the register is 80ms, and the settling time 500ms.				

15. Energy Metering

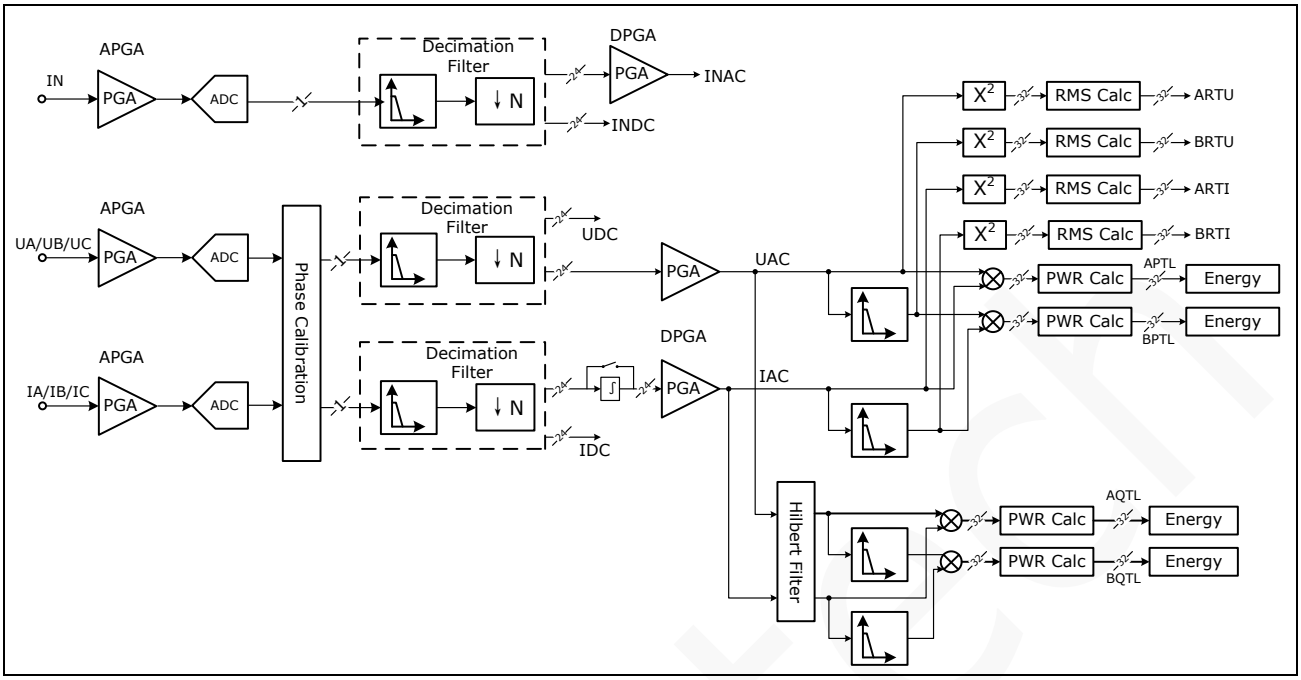


Figure 15-1 Digital Signal Processing in Energy Metering Block

In the OPM0, or normal operating mode, the metering frequency is 6553.6kHz, and the sampling frequency of the ADCs is 819.2kHz.

15.1. Data RAM

The following table describes the allocation of data RAM of the energy metering block of the V9203.

The registers of the V9203, which have respective length, are accessed by the master MCU as 32-bit registers.

Table 15-1 Description of Data RAM of Energy Metering Block

Address Range	Length	Content	Read	Write
0xC800~0xC837	32-bit	Reserved. When the energy metering block is initialized, the MTPARA0 (0xC000) is initialized to 0x10000000, and then write 0s in the RAM located at addresses of the range of 0xC800~0xC837 and 0xC880~0xC8B7 to clear the RAM.		
0xC880~0xC8B7	32-bit			
0xD000~0xD00B	32-bit	Energy accumulation registers and pulse counter in high-speed mode	The master MCU read of the register directly.	The master MCU write of the register directly.
0xE000~0xE08F	48-bit	Reserved. These addresses must not be accessed for proper operation.		
0xE800~0xE9A7	32-bit	Metering data	The master MCU read of	The master MCU write of

Address Range	Length	Content	Read	Write
		registers and registers for calibration.	the register directly.	the register directly.
0xE9A8~0xEAB7	32-bit	Reserved. These addresses must not be accessed for proper operation.		
0xEC00~0xEC52	32-bit	Energy metering configuration registers, and system state registers.	The master MCU read of the register directly.	The master MCU write of the register directly.
0xF000~0xF02B	48-bit	Reserved. These addresses must not be accessed for proper operation.		
0xF02C~0xF032	24-bit	Registers for DC component.	These registers, with bit23 being the sign bit, are accessed as a 32-bit register with sign extended to 32 bits.	These registers, with bit23 being the sign bit, are accessed as a 32-bit register with sign extended to 32 bits.
0xF034~0xF1EF	48-bit	Reserved. These addresses must not be accessed for proper operation.		
0xF800~0xF87F	24-bit	Reserved. These addresses must not be accessed for proper operation.		

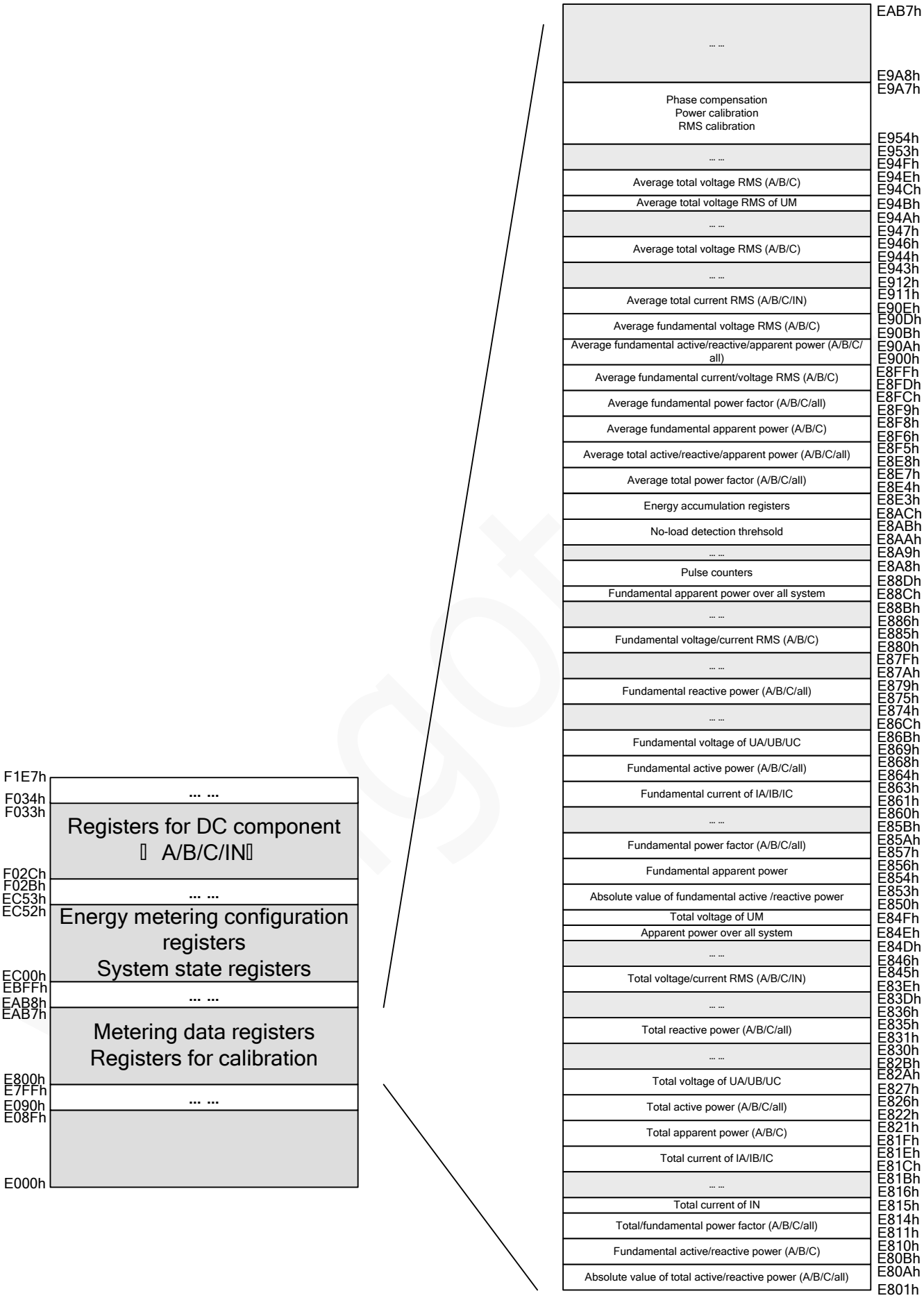


Figure 15-2 RAM Allocation

Table 15-2 Metering Parameters

	Raw waveform	DC	Total / Fundamental				Phase	Line frequency	Power factor
			Instantaneous and average RMS	Instantaneous/ average algebra/absolute values of active power	Instantaneous/ average algebra/absolute values of reactive power	Instantaneous and average apparent power			
Current of IA	√	√	√	√	√	√	√	√	√
Current of IB	√	√	√	√	√	√	√	√	√
Current of IC	√	√	√	√	√	√	√	√	√
Voltage of UA	√	√	√	√	√	√	X	√	√
Voltage of UB	√	√	√	√	√	√	√	√	√
Voltage of UC	√	√	√	√	√	√	√	√	√
Current of IN	√	√	√	X	X	X	X	X	X
On the overall system	X	X	X	√	√	√	X	X	√

15.2. Analog Input

The V9203 has 7 analog inputs forming current and voltage channels. The current channels consist of 4 fully differential voltage inputs: 2 inputs for each phase and 2 for neutral wire. And the voltage channels consist of 3 pseudo differential voltage inputs: UAP, UBP and UCP are positive inputs for voltage channels, and UN is negative input for all voltage channels. Each input has a maximum voltage of

±200mV, and each pair of a maximum differential voltage of ±400mV.

For current channels, a current transformer (CT) or Rogowski coil can be used for analog inputs.

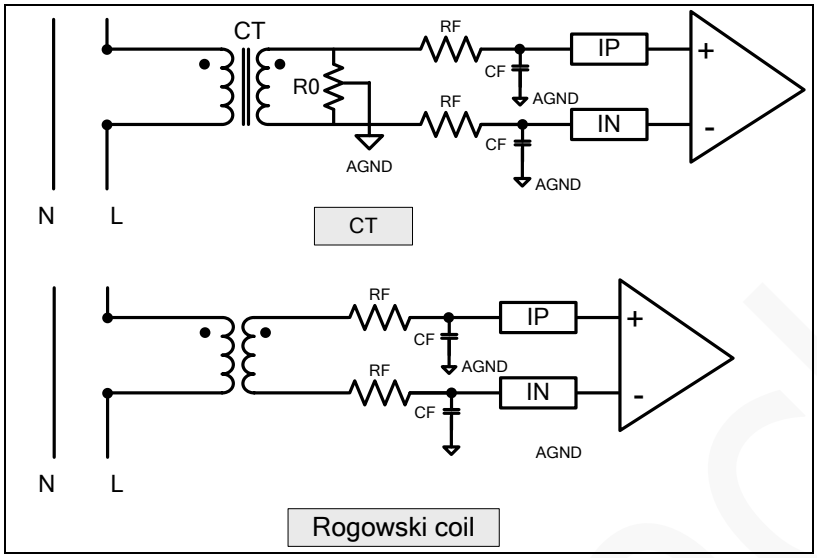


Figure 15-3 Analog Input of Current Channels

If a Rogowski coil is used for analog inputs, users must enable the digital integrator to shift the phase by 90 degrees, which introduces a gain A which is related to the line frequency, after the direct current / voltage is switched off. The integrator can be enabled via bit12 (DIDTEN) of MTPARA2 (0xC002).

When the line frequency is 50Hz, the gain A0 for RMS calculation is 0.636043109985836, and the gain A1 for active / reactive power calculation is 0.635598782982145.

Table 15-3 Enabling Digital Integrator

Register	Bit	Description
MTPARA2, 0xC002	Bit12, DIDTEN	0, disable; 1, enable.

For voltage channels, a potential transformer (PT) or a resistor-divider network can be used for analog inputs.

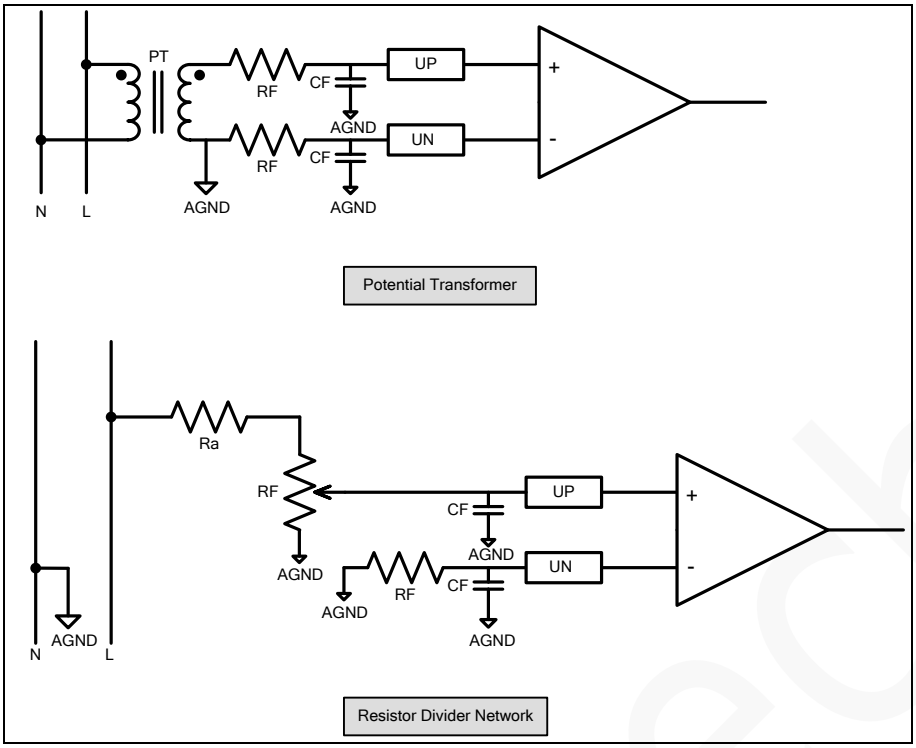


Figure 15-4 Analog Input of Voltage Channels

The full measurement scale of the ADCs is ±1.1V. To match the output signal of the transformers to the measurement scale of the ADCs, analog programmable gain amplifiers (APGA) with possible gain selection of 2, 4, 16, and 32 for current inputs, and of 1 and 2 for voltage inputs, are set. The product of the analog input and the set APGA should not be over ±1.1V.

$$Ua' = PGAua \times Aua \times \sin \omega t$$
$$Ia' = PGAia \times Aia \times \sin(\omega t + \psi)$$

Equation 15-1

Where, PGAua and PGAia are the APGA for the current and voltage channel of Phase A; Aua and Aia are the amplitude of current and voltage inputs.

In OPM1, or power-off/no-voltage pre-detection mode, the APGA for current input is recommended to be 32.

Table 15-4 APGA Configuration

Register	Bit		Description
ANCtrl0, 0x8000	Bit18	GUC	To set analog PGA gain of UC input. 0, ×1; 1, ×2. ×2 is recommended.
	Bit17	GUB	To set analog PGA gain of UB input. 0, ×1; 1, ×2. ×2 is recommended.
	Bit16	GUA	To set analog PGA gain of UA input. 0, ×1; 1, ×2. ×2 is recommended.
	Bit[14:12]	GIN<2:0>	To set analog PGA gain of IN input. 000, ×2; 001, ×4; 010, ×16; 011/100/101/110/111, ×32

Register	Bit		Description
			To ensure the output from the sensor matches the full scale of ADC, the default value should not be used.
	Bit[10:8]	GIC<2:0>	To set analog PGA gain of IC input. 000, ×2; 001, ×4; 010, ×16; 011/100/101/110/111, ×32 To ensure the output from the sensor matches the full scale of ADC, the default value should not be used.
	Bit[6:4]	GIB<2:0>	To set analog PGA gain of IB input. 000, ×2; 001, ×4; 010, ×16; 011/100/101/110/111, ×32 To ensure the output from the sensor matches the full scale of ADC, the default value should not be used.
	Bit[2:0]	GIA<2:0>	To set analog PGA gain of IA input. 000, ×2; 001, ×4; 010, ×16; 011/100/101/110/111, ×32 To ensure the output from the sensor matches the full scale of ADC, the default value should not be used.

15.3. Analog-to-Digital Conversion

Second-order Σ-Δ ADCs are used in the 7 channels of the V9203, and its full measurement scale is ±1.1V. Σ-Δ ADCs can be enabled or disabled via configuring ANCtrl2 register (0x8002).

Table 15-5 Enable/Disable ADCs of Each Channel

Register	Bit		Description	
ANCtrl2, 0x8002	Bit30	ADPDUCN	To enable the ADC of Channel UC.	0, disable; 1, enable. About 976μs after reset, these bits will be set to 0b11111111 automatically, to enable all ADCs of the channels.
	Bit29	ADPDUBN	To enable the ADC of Channel UB.	
	Bit28	ADPDUAN	To enable the ADC of Channel UA.	
	Bit27	ADPDINN	To enable the ADC of Channel IN.	
	Bit26	ADPDICN	To enable the ADC of Channel IC.	
	Bit25	ADPDIBN	To enable the ADC of Channel IB.	
	Bit24	ADPDIAN	To enable the ADC of Channel IA.	

The sampling frequency of ADCs, or ADC clock (ADCCLK), is derived from the 13.1072MHz crystal oscillator when the clock scaler is enabled. By default, it is 819.2kHz, one eighth of the metering clock (MTCLK), and can be configured via bit[19:18] of ANCtrl3 (0x8003).

Table 15-6 Configuring ADCCLK

Register	Bit	Description
ANCtrl3, 0x8003	Bit[19:18] ADCLKSEL<1:0>	To select the sampling frequency for the oversampling ADC (ADC frequency). Base: 204.8kHz. 00, ×4; 01, ×8; 10, ×1; 11, ×2

When logic high is input to both the pins PM0 and PM1, in which the V9203 works in OPM0 (normal operation mode), the metering frequency must be 8 times of the ADC frequency.

After the analog-to-digital conversion, the analog input is converted to be 24-bit digital signal with both bit23 and bit22 being the sign bit.

The digital signal must be input to a phase compensation circuit to correct the phase angle error introduced by the transformers.

15.4. Phase Compensation

A phase compensation circuit composed of a time delay chain of fixed length is applied to correct the phase angle error via delaying the selected signal. Either current or voltage signals can be delayed.

In 50Hz power grid, when the sampling frequency of the phase compensation circuit (f_{smpl}) is 819.2kHz, the calibration resolution is 0.022°/lsb, and the maximum phase angle error to be corrected is 2.8°. The value of f_{smpl} is determined by the configuration of bits ADCLKSEL<1:0> (bit[19:18] of ANCtrl3, 0x8003).

The value (N) to be set to the phase compensation control registers can be calculated via the following equation:

$$\mathrm{N} = Round(\frac{1}{\pi} \times \frac{f_{smpl}}{100} \times \{\pm arccos[cos\theta \times (1+E)] - \theta\}) \qquad \text{Equation 15-2}$$

where

N is the value, signed, to be set to the registers to correct the phase angle error. A positive N indicates that the current signal must be delayed, so "0" must be set to the sign bit; a negative N indicates that the voltage signal must be delayed, so "1" must be set to the sign bit;

θ is the phase angle between current and voltage signals, in unit of radian. A positive θ indicates a phase lead in current signal; a negative θ indicates a phase lead in voltage signal;

E is the energy metering error displayed in LCD screen of the calibration equipment;

f_{smpl} is the sampling frequency of the phase compensation circuit, Hz.

Table 15-7 f_{smpl} Determines Phase Compensation Resolution and Correction Range

N	ADCLKSEL<1:0> Configuration		f_{smpl} (Hz)	Resolution (°/lsb)	Correction Range (°)
[-127,	bit[19:18], 0x8003	00	819200	0.022	2.8

N	ADCLKSEL<1:0> Configuration		f_{smpl} (Hz)	Resolution (°/lsb)	Correction Range (°)
+127]		01	1638400	0.011	1.4
		10	204800	0.088	11.2
		11	409600	0.044	5.6

Table 15-8 Registers for phase compensation

Register	Bit		Description
MTPARA0, 0xC000, R/W	Bit[12:8]	MSKA	To set the range of the hysteresis error of the fundamental current threshold for the phase compensation. 0, default. For example, if the value of MSKA is set to 0x8, and the fundamental current threshold is set to 0xabcd, the 8 least significant bits of the register of the fundamental current threshold represents the hysteresis error range, that is the top threshold is 0xabff and the bottom threshold is 0xab00.
MTPARA2, 0xC002, R/W	Bit24	AECEN	To disable phase compensation in sections. 1, disable; 0, enable (by default).
Registers for Phase Compensation in Sections (R/W)	Bit[23:0]		Address range: 0xE954~0xE958. To set the phase compensation for Phase C/B/A. bit23/bit15/bi7 is the sign bit of the phase compensation.
Current Threshold for Phase Compensation in Sections (R/W)	32-bit		Address range: 0xE97C~0xE987. To set current threshold for phase compensation in sections.
State Register for Phase Compensation and Gain Calibration of Total Active Power (0xC004, PECAEC, R)	Bit[10:8]	AECC	To indicate the section being used for phase compensation of Phase C. 000, Section 0; 001, Section 1; 010, Section 2; 011, Section 3; 100, Section 4.
	Bit[6:4]	AECB	To indicate the section being used for phase compensation of Phase B. 000, Section 0; 001, Section 1; 010, Section 2; 011, Section 3; 100, Section 4.
	Bit[2:0]	AECA	To indicate the section being used for phase compensation of Phase A. 000, Section 0; 001, Section 1; 010, Section 2; 011, Section 3; 100, Section 4.

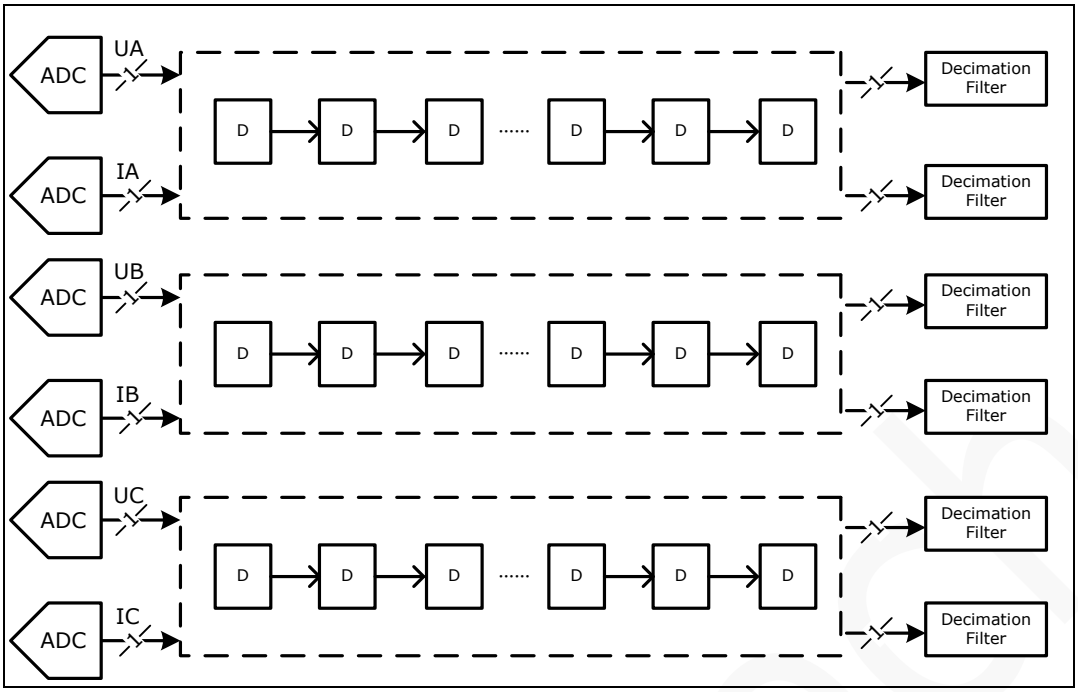


Figure 15-5 Phase Compensation

Phase compensation in 5 sections is applied to the V9203 to widen the dynamic range. By default, this function is enabled, and it can be disabled via setting bit24 in MTPARA2 (0xC002). When phase compensation in sections is enabled, the circuit compares the fundamental instantaneous current RMS after calibration (IRMS) to the pre-set current thresholds for each phase, and then decides to use the register for phase compensation in sections for correcting phase angle error. When this function is disabled, the registers of Section0 are used. The PECAEC register (0xC004) gives phase compensation states.

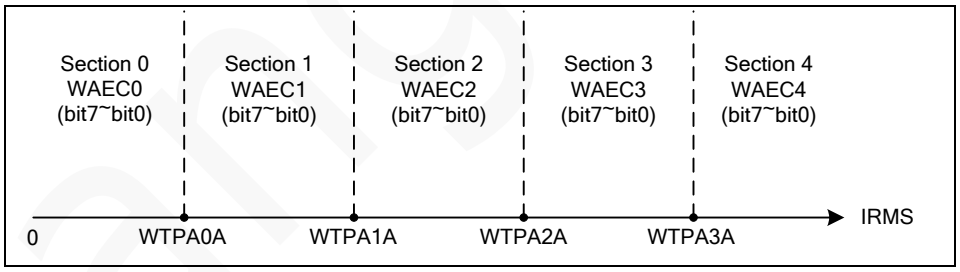


Figure 15-6 Phase Compensation in Sections (Phase A)

A hysteresis error mechanism is applied to the current threshold for phase compensation in sections. It means the threshold is not an accurate value but a value in a range which is determined by bit[12:8] (MSKA) of MTPARA0 (0xC000). The configuration of MSKA sets the range of the hysteresis error of the fundamental current threshold for the phase compensation. For example, if the value of MSKA is set to 0x8, and the fundamental current threshold is set to 0xabcd, the 8 least significant bits of the register of the fundamental current threshold represents the hysteresis error range, that is the top threshold is 0xabff, and the bottom threshold is 0xab00.

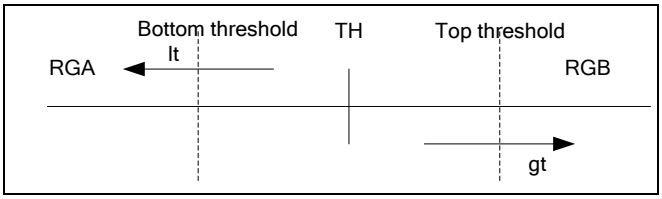


Figure 15-7 Hysteresis Error Mechanism for Phase Compensation

15.5. Digital Input

Decimation filters are used to reduce the noise of the 1-bit code stream output from the oversampling Σ/Δ ADC. The decimation filter can reduce the sampling frequency, and after being sampled in a lower frequency, the raw waveform of each signal is acquired.

Bit[6:0] of MTPARA0 (0xC000) enables or disables the code stream input into the decimation filters. When this function is enabled, the code stream is accumulated to the filter; when this function is disabled, a constant "0" is input for digital signal processing.

Table 15-9 Enable/Disable Digital Inputs

Register	Bit		Description
MTPARA0, 0xC000	Bit6	ADCIC	To enable digital signal input of Channel IC for digital signal processing. 1, enable. 0, disable.
	Bit5	ADCIB	To enable digital signal input of Channel IB for digital signal processing. 1, enable. 0, disable.
	Bit4	ADCIA	To enable digital signal input of Channel IA for digital signal processing. 1, enable. 0, disable.
	Bit3	ADCIN	To enable digital signal input of Channel IN for digital signal processing. 1, enable. 0, disable.
	Bit2	ADCUC	To enable digital signal input of Channel UC for digital signal processing. 1, enable. 0, disable.
	Bit1	ADCUB	To enable digital signal input of Channel UB for digital signal processing. 1, enable. 0, disable.
	Bit0	ADCUA	To enable digital signal input of Channel UA for digital signal processing. 1, enable. 0, disable.

Digital programmable gain amplifiers (DPGA) with possible gain selection of 1~128, via MTPARA1 (0xC001), are applied to digital signals output from the decimation filters to amplify the signals. It is recommended to set the DPGA to 8 or 16 if the voltage signal after APGA is much less than the measurement scales of the ADCs, to improve the performance.

Table 15-10 DPGA gain selection for digital signals

Register	Bit		Description
MTPARA1, 0xC001	Bit[26:24]	ATXIN	To set digital PGA gain of IN input.

Register	Bit		Description
			×1~×128 (2^{ATXIN})
	Bit[22:20]	ATXIC	To set digital PGA gain of IC input. ×1~×128 (2^{ATXIC})
	Bit[18:16]	ATXUC	To set digital PGA gain of UC input. ×1~×128 (2^{ATXUC})
	Bit[14:12]	ATXIB	To set digital PGA gain of IB input. ×1~×128 (2^{ATXIB})
	Bit[10:8]	ATXUB	To set digital PGA gain of UB input. ×1~×128 (2^{ATXUB})
	Bit[6:4]	ATXIA	To set digital PGA gain of IA input. ×1~×128 (2^{ATXIA})
	Bit[2:0]	ATXUA	To set digital PGA gain of UA input. ×1~×128 (2^{ATXUA})

After the digital programmable gain amplifiers, the digital signals are acquired via the following equation:

$$Ua = PGAdua \times PGAua \times \frac{Aua}{1.185} \times \sin\omega t = DUa \times \sin\omega t$$
$$Ia = PGAdia \times PGAia \times \frac{Aia}{1.185} \times \sin(\omega t + \psi) = DIa \times \sin(\omega t + \psi)$$

Equation 15-3

Where, PGAdua and PGAdia are the DPGA gain, PGAua and PGAia are the APGA gain, Aua and Aia are the amplitude of current and voltage inputs, and 1.185 is the reference voltage.

15.6. Raw Waveform Output

Direct Memory Access (DMA) is used for transferring raw waveform of the 7 voltage and current signals to the peripheral components via the DMA_SPI interfaces. When some bits of bit[22:16] of MTPARA2 (0xC002) is set to 1s, the pins DSCK (Pin35), DSCS (Pin36) and DSDO (Pin37) are used to transfer the raw waveform of the corresponding channel. When all bits of bit[22:16] are set to 1s, the raw waveform of the 7 channels, in the sequence of UA, IA, UB, IB, UC, IC, and then IN, is transferred from the three interfaces.

Note: The DMA mode of V9203 is fixed to SPI master mode 1 (clock phase is 1, clock polarity is 0).

Table 15-11 Registers for Raw Waveform Output

Register	Bit		Description
MTPARA2, 0xC002	Bit27	DSPICK	To select the parity type for the output data from the DMA_SPI interfaces.

Register	Bit		Description
			0, even parity; 1, odd parity.
	Bit26	DSPIMD	To select the frame format of the output data from the DMA_SPI interfaces. 0, 32-bit, one frame for a 32-bit data output; 1, 16-bit, two frames for a 32-bit data output.
	Bit[22:16]	DSPIEN	To enable the raw waveform output of the channels fron the DMA_SPI interfaces. 1, enable; 0, disable. Bit22, raw waveform of IN; Bit21, raw waveform of IC; Bit20, raw waveform of UC; Bit19, raw waveform of IB; Bit18, raw waveform of UB; Bit17, raw waveform of IA; Bit16, raw waveform of UA.

When the metering frequency is 6.5536MHz, the updating frequency of the raw waveform is 6.4kHz. To ensure the transfer of waveform in time, the frequency for transferring a data frame should be at least 51.2kHz. If the data frame is a 32-bit serial data, the baud rate should be at least 1638.4kbps. So, to ensure the transfer of serial data in time and reliably, the baud rate is set to 3.2768Mbps.

The raw waveform can be transferred to the peripheral components via the DMA_SPI interfaces in two modes.

1. Mode 0: transferring 22-bit raw waveform in one 32-bit data frame. The form of the data frame transferred is as shown in the following table.

When a low logic is output on the pin DSCS (Pin36), the data is ready to be transferred. During the transfer, 32 DSCK signals are derived. And on the low-to-high DSCK transition, the transfer starts. If a high logic is output on the pin DSCS when all the 32 bits of data are transferred, the transfer is finished. The slave SPI interfaces of the peripheral components receive the 32-bit data, and sample the signal on the high-to-low DSCK transition when the DSCS is active low.

Table 15-12 Transferring Data Frame via DMA_SPI Interfaces (Mode 0)

Bit	Description
Bit[31:30]	Bit21 of the 22-bit raw waveform of each channel.
Bit[29:8]	Bit21~bit0, the 22-bit raw waveform of each channel.
Bit7	0
Bit[6:4]	3-bit ADC address.

Bit	Description
	000, for Channel UA; 001, for Channel IA; 010, for Channel UB; 011, for Channel IB; 100, for Channel UC; 101, for Channel IC; 110, for Channel IN.
Bit[3:1]	000
Bit0	Parity bit. Users can select the parity via configuring bit27 (DSPICK) of MTPARA2 (0xC002).

2. Mode 1: transferring 22-bit raw waveform in two 16-bit data frames. The form of the data frame transferred is as shown in the following table.

When a low logic is output on the pin DSCS (Pin36), the data is ready to be transferred. During the transfer, 16 DSCK signals are derived. And on the low-to-high DSCK transition, the transfer starts. If a high logic is output on the pin DSCS when all the 16 bits of data are transferred, the transfer of the higher bytes (bit[21:11]) of the raw waveform of each channel is finished. A DSCK signal later, a low logic is output on the pin DSCS (Pin36) again, and the lower bytes of the raw waveform is ready to be transferred. During the transfer, 16 DSCK signals are derived. And on the low-to-high DSCK transition, the transfer starts. If a high logic is output on the pin DSCS when all the 16 bits of data are transferred, the transfer of the lower bytes (bit[10:0]) of the raw waveform of each channel is finished. The slave SPI interfaces of the peripheral components receive the 16-bit serial data, and sample the signal on the high-to-low DSCK transition when the DSCS is active low.

Table 15-13 Transferring Data Frame via DMA_SPI Interfaces (Mode 1)

Step	Bit	Description
Step 1	Bit15	1, indicates the higher bytes of the raw waveform of each channel is being transferred.
	Bit[14:4]	The 11 most significant bits (bit[21:11]) of the raw waveform of the each channel.
	Bit[3:1]	3-bit ADC address 000, for Channel UA; 001, for Channel IA; 010, for Channel UB; 011, for Channel IB; 100, for Channel UC; 101, for Channel IC; 110, for Channel IN.
	Bit0	Parity bit. Users can select the parity via configuring bit27 (DSPICK) of MTPARA2 (0xC002).
Step 2	Bit15	0, indicates the lower bytes of the raw waveform of each channel is being transferred.
	Bit[14:4]	The 11 least significant bits (bit[10:0]) of the raw waveform of the each channel.
	Bit[3:1]	3-bit ADC address 000, for Channel UA; 001, for Channel IA; 010, for Channel UB; 011, for Channel IB; 100, for Channel UC; 101, for Channel IC; 110, for Channel IN.
	Bit0	Parity bit. Users can select the parity via configuring bit27 (DSPICK) of MTPARA2 (0xC002).

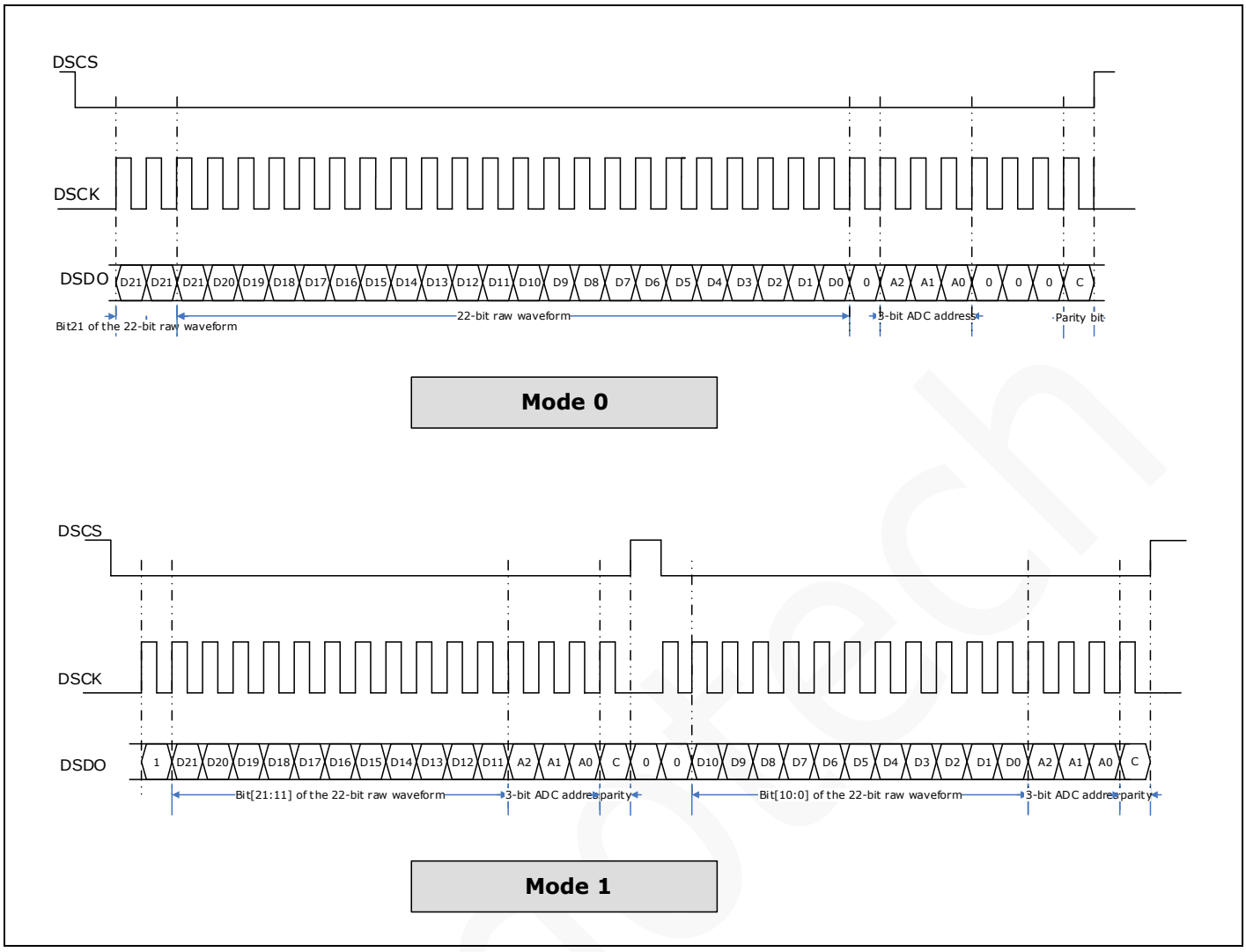


Figure 15-8 Modes for Raw Waveform Output

15.7. DC Components

By default, the output signals output from the decimation filters is input to the DC-stopping circuit to switch off the direct current/voltage to distinguish the alternating component which is for the power and RMS calculation to improve the accuracy, from the direct component which is stored in the registers for DC components (0xF02C~0xF032).

If the direct component in the raw waveforms is known, users can preset a value in the registers located at the address 0xEC16~0xEC1C for each channel. Then, the system can switch off the direct voltage or current of each phase automatically.

The registers for DC components (0xF02C~0xF032) and for presetting bias for direct current/voltage (0xEC16~0xEC1C) are accessed as 32-bit registers with bit23 being the sign bit and being extended to 32 bits.

As for the registers for DC components, when the metering frequency is 6.5536MHz, the updating time is 20ms, and the settling time is 100ms; when the metering frequency is 1.6384MHz, the updating time is 80ms, and the settling time is 400ms; when the metering frequency is 819.2kHz, the updating time is 160ms, and the settling time is 800ms.

When the V9203 is used for direct current application, users can switch on the direct current / voltage via setting bit11 (DCBYPASS) to 1 to prevent the raw waveform from being high-pass filtered, and the signal composed of direct and alternating component will be used for RMS calculation and energy metering.

15.8. RMS Calculation

The alternating component of the phase current and voltage can be used for:

1. The total current and voltage RMS calculation directly;
2. The fundamental current and voltage RMS calculation after being processed the bandpass filter which introduces a gain of 1/1.175435.

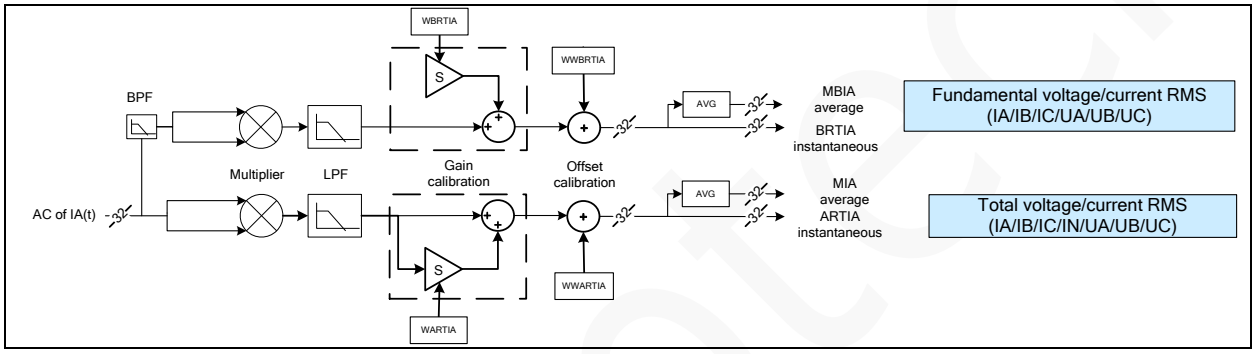


Figure 15-9 Total / Fundamental RMS Calculation

15.8.1.RMS Calculation

The value of the total current or voltage RMS is equal to that of the digital signal. Take Phase A as an example,

$$Iarms = DIa = PGAdia \times PGAia \times \frac{Aia}{1.185} \qquad \text{Equation 15-4}$$

And the fundamental current or voltage RMS is acquired following the equation:

$$BIarms = BDIa = PGAdia \times PGAia \times \frac{Aia}{1.185} \times \frac{1}{1.175435} \qquad \text{Equation 15-5}$$

Where,

PGAdia is the digital gain;

PGAia is the analog gain;

Aia is the amplitude of current and voltage inputs;

1.185 is the reference voltage.

After gain calibration and offset calibration, the RMS is stored in the registers for total/fundamental current/voltage RMS. All the registers are in the format of 32-bit 2's complement, positive constantly.

Table 15-14 Registers Related to RMS Calculation

Register	Address	Data Format	Description
Registers for Total Current/Voltage RMS	0xE83E~0xE844	32-bit, 2's complement, positive.	Instantaneous total current and voltage RMS of each phase and neutral wire.
	0xE90E~0xE911		Average total current RMS of each phase and neutral wire.
	0xE944~0xE946		Average total voltage RMS of each phase.
Registers for Fundamental Current/Voltage RMS	0xE880~0xE885	32-bit, 2's complement, positive.	Instantaneous fundamental current and voltage RMS of each phase.
	0xE8FD~0xE8FF		Average fundamental current RMS of each phase.
	0xE90B~0xE90D		Average fundamental voltage RMS of each phase.

As for all the registers for total current/voltage RMS, when the metering frequency is 6.5536MHz, the instantaneous data are updated in 20ms and settled in 150ms, and the average data are updated in 640ms, and settled in 1s; when the metering frequency is 1.6384MHz, the instantaneous data are updated in 80ms and settled in 600ms, and the average data are updated in 2.56s and settled in 4s; when the metering frequency is 819.2kHz, the instantaneous data are updated in 160ms and settled in 1.2s, and the average data are updated in 5.12s and settled in 8s.

As for all the registers for fundamental current/voltage RMS, when the metering frequency is 6.5536MHz, the instantaneous data are updated in 20ms and settled in 200ms, and the average data are updated in 640ms, and settled in 1s; when the metering frequency is 1.6384MHz, the instantaneous data are updated in 80ms and settled in 800ms, and the average data are updated in 2.56s and settled in 4s; when the metering frequency is 819.2kHz, the instantaneous data are updated in 160ms and settled in 1.6s, and the average data are updated in 5.12s and settled in 8s.

15.8.2.RMS Calibration

To improve the linearity of the data when weak signals are input, the current or voltage RMS calculated via Equation 15-4 or Equation 15-5 must be gain and offset calibrated, as shown in the following equation, and then the calibrated RMS is stored in the registers.

$$RMS = RMS' \times (1 + S) + C \qquad \text{Equation 15-6}$$

Where,

RMS' is the current or voltage RMS calculated via Equation 15-4 or Equation 15-5;

RMS is the current or voltage RMS after calibration;

S is the gain calibration;

C is the offset calibration.

Users can set the calibration value in the registers listed in the following table.

Table 15-15 Registers Related to RMS Calibration

Registers	Address	Data Format	Description
Registers for Calibrating the Total Voltage/Current RMS	0xE968~0xE96E	32-bit, 2's complement	To set gain calibration for the total current / voltage RMS of each phase and Channel IN.
	0xE994~0xE99A		To set offset calibration for the total current / voltage RMS of each phase and Channel IN.
Registers for Calibrating the Fundamental Voltage/Current RMS	0xE976~0xE97B	32-bit, 2's complement	To set gain calibration for the fundamental current / voltage RMS of each phase.
	0xE9A2~0xE9A7		To set offset calibration for the fundamental current / voltage RMS of each phase.

15.9. Power Calculation

The alternating component of the phase current and voltage can be used for:

1. The active power calculation directly;
2. The reactive power calculation after a phase shift by 90 degrees via a Hilbert filter.

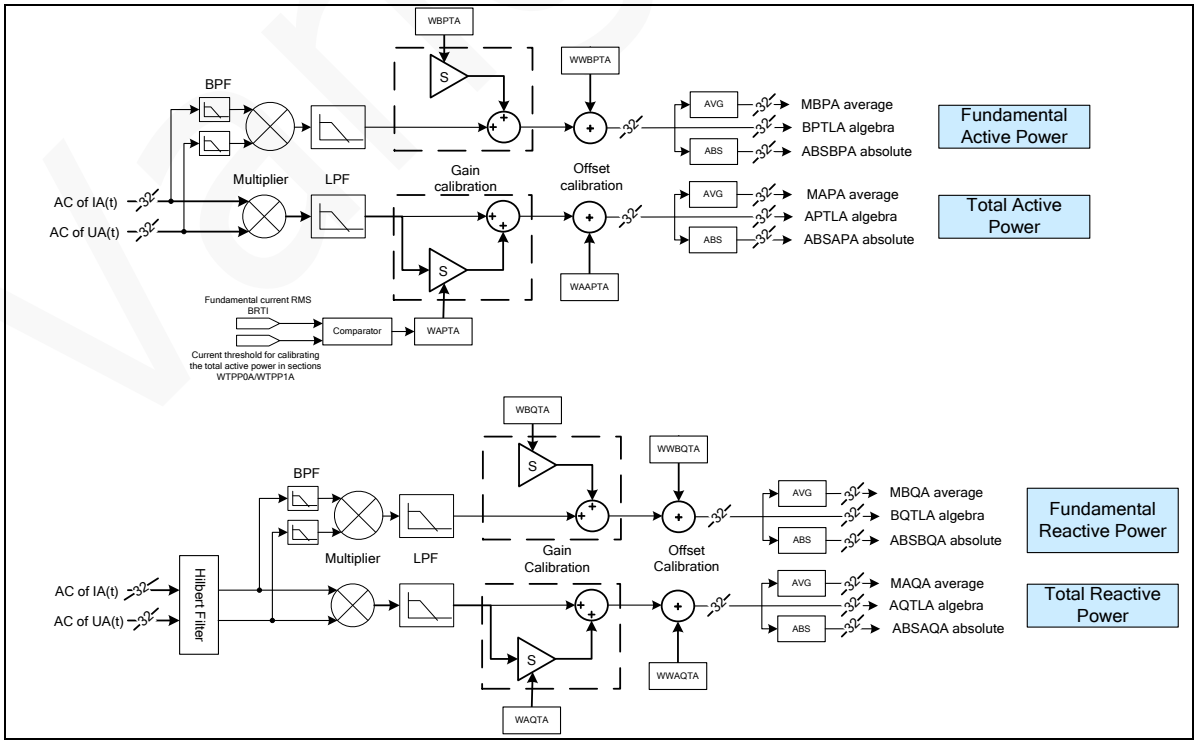


Figure 15-10 Active/Reactive Power Calculation

15.9.1.Total Active/Reactive Power Calculation

The total signal, including fundamental wave and harmonic wave, is used to calculate total active and reactive power directly. Take Phase A as an example, the active power is acquired via the following equation:

$$PA = \frac{DUa \times DIa \times \cos\psi}{4} \qquad \text{Equation 15-7}$$

And the reactive power is acquired following the equation:

$$QA = \frac{DUa \times DIa \times \sin\psi}{4} \qquad \text{Equation 15-8}$$

Where, DUa and DIa are the value of the digital signal.

After gain calibration and offset calibration, the active and reactive power is stored in the total active/reactive power registers. And the active and reactive power can be averaged and processed to acquire the absolute value. All the registers are in the format of 32-bit 2's complement.

The algebra and absolute value of the total active and reactive power of each phase is used for calculating total power on the overall system, and the absolute value of the total power is for the energy accumulation and pulse generation in normal mode.

Table 15-16 Registers for Total Active/Reactive Power

Register	Address	Data Format	Description
Total active/reactive power registers	0xE805~0xE807	32-bit, 2's complement, positive	Absolute value of the instantaneous total active power of each phase.
	0xE808~0xE80A		Absolute value of the instantaneous total reactive power of each phase.
	0xE824~0xE826	32-bit, 2's complement	Algebra value of the instantaneous total active power of each phase.
	0xE833~0xE835		Algebra value of the instantaneous total reactive power of each phase.
	0xE8E8~0xE8EA		Average total active power of each phase.
	0xE8F0~0xE8F2		Average total reactive power of each phase.

As for all the registers for total active/reactive power, when the metering frequency is 6.5536MHz, the instantaneous algebra and absolute data are updated in 80ms and settled in 400ms, and the average data are updated in 640ms, and settled in 1s; when the metering frequency is 1.6384MHz, the instantaneous algebra and absolute data are updated in 320ms and settled in 1.6s, and the average data are updated in 2.56s and settled in 4s; when the metering frequency is 819.2kHz, the instantaneous algebra and absolute data are updated in 640ms and settled in 3.2s, and the average data are updated in 5.12s and settled in 8s.

15.9.2.Fundamental Active/Reactive Power Calculation

Filtered by the bandpass filter, introducing a gain of 1/1.175435, the signal of each phase, is used to calculate the fundamental active and reactive power. Take Phase A as an example,

Fundamental active power: $BPA = \frac{BDUa \times BDIa \times \cos\psi}{4} = \frac{PA}{1.38165}$ Equation 15-9

Fundamental reactive power: $BQA = \frac{BDUa \times BDIa \times \sin\psi}{4} = \frac{QA}{1.38165}$ Equation 15-10

Where, BDUa and BDIa are the fundamental voltage and current, calculated as follows,

$$BDUa = \frac{DUa}{1.175435}$$
$$BDIa = \frac{DIa}{1.175435}$$ Equation 15-11

After gain calibration and offset calibration, the active and reactive power is stored in the fundamental active/reactive power registers. And the active and reactive power can be averaged and processed to acquire the absolute values. All the registers are in the format of 32-bit 2's complement.

The algebra and absolute value of the fundamental active and reactive power of each phase is used for calculating fundamental power on the overall system, and the absolute value of the fundamental power is for the energy accumulation and pulse generation in normal mode.

Table 15-17 Registers for Fundamental Active/Reactive Power

Register	Address	Data Format	Description
Registers for fundamental active and reactive power	0xE80B~0xE80D	32-bit, 2's complement, positive.	Absolute value of the instantaneous fundamental active power of each phase.
	0xE80E~0xE810		Absolute value of the instantaneous fundamental reactive power of each phase.
	0xE866~0xE868	32-bit, 2's complement	Algebra value of the instantaneous fundamental active power of each phase.
	0xE877~0xE879		Algebra value of the instantaneous fundamental reactive power of each phase.
	0xE900~0xE902		Average fundamental active power of each phase of each phase.
	0xE905~0xE907		Average fundamental reactive power of each phase.

As for all the registers for fundamental active/reactive power, when the metering frequency is 6.5536MHz, the instantaneous algebra and absolute data are updated in 80ms and settled in 450ms, and the average data are updated in 640ms, and settled in 1s; when the metering frequency is

1.6384MHz, the instantaneous algebra and absolute data are updated in 320ms and settled in 1.8s, and the average data are updated in 2.56s and settled in 4s; when the metering frequency is 819.2kHz, the instantaneous algebra and absolute data are updated in 640ms and settled in 3.6s, and the average data are updated in 5.12s and settled in 8s.

15.9.3.Power Calibration

To improve the linearity of the data when weak signals are input, the active or reactive power calculated must be gain and offset calibrated, as shown in the following equation, and then the calibrated power is stored in the registers.

$$P = P' \times (1 + S) + C \qquad \text{Equation 15-12}$$

Where,

P' is the active or reactive power calculated via Equation 15-7, Equation 15-8, Equation 15-9 or Equation 15-10;

P is the active or reactive power after calibration;

S is the gain calibration;

C is the offset calibration.

15.9.3.1. Gain Calibration

Users can set the gain calibration values in the registers listed in the following table.

Table 15-18 Registers Related to Power Gain Calibration

Register	Bit		Description
MTPARA0, 0xC000, R/W	Bit[20:16]	MSKP	To set the range of the hysteresis error of the fundamental current threshold for the total active power gain calibration. For example, if the value of MSKP is set to 0x8, and the fundamental current threshold is set to 0xabcd, the 8 least significant bits of register of the fundamental current threshold represents the hysteresis error range, that is the top threshold is 0xabff, and the bottom threshold is 0xab00.
MTPARA2, 0xC002, R/W	Bit25	PECEN	To disable gain calibrate the total active power in sections. 1, disable; 0, enable (by default).
PECAEC, 0xC004, R	Bit[21:20]	PECC	To indicate the section being used for gain calibrating the total active power of Phase C. 00, Section 0; 01, Section 1; 10, Section 2.

Register	Bit		Description
	Bit[17:16]	PECB	To indicate the section being used for gain calibrating the total active power of Phase B. 00, Section 0; 01, Section 1; 10, Section 2.
	Bit[13:12]	PECA	To indicate the section being used for gain calibrating the total active power of Phase A. 00, Section 0; 01, Section 1; 10, Section 2.
Registers for calibrating the total active/reactive power	32-bit		Address: 0xE959~0xE967. To set the gain calibration for the total active/reactive power of each phase.
Current threshold for calibrating the total active power in sections	32-bit		Address: 0xE988~0xE98D. To set current threshold for calibrating the total active power of each phase.
Registers for calibrating the fundamental active/reactive power	32-bit		Address: 0xE970~0xE975. To set the gain calibration for the fundamental active/ reactive power of each phase.

Gain Calibration of the total active power in 3 sections is applied to the V9203 to widen the dynamic range. By default, this function is enabled, and it can be disabled via setting bit25 in MTPARA2 (0xC002). When gain calibration of the total active power in sections is enabled, the circuit compares the instantaneous fundamental current RMS after calibration (IRMS) to the pre-set current thresholds for each phase, and then decides to use the register for gain calibration in sections for correcting gain error. When this function is disabled, the registers of Section0 are used. The PECAEC register (0xC004) gives gain calibration states.

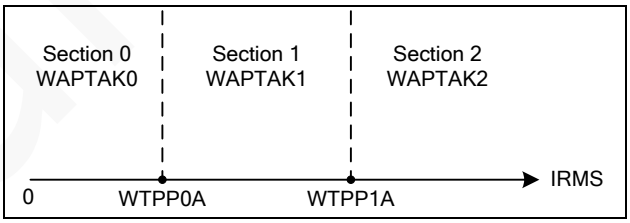


Figure 15-11 Gain Calibration of the Total Active Power in Sections (Phase A)

A hysteresis error mechanism is applied to the current threshold for gain calibration in sections. It means the threshold is not an accurate value but a value in a range which is determined by bit[20:16] (MSKP) of MTPARA0 (0xC000). The configuration of MSKP sets the range of the hysteresis error of the fundamental current threshold for the gain calibration. For example, if the value of MSKP is set to 0x8, and the fundamental current threshold is set to 0xabcd, the 8 least significant bits of register of the fundamental current threshold represents the hysteresis error range, that is the top threshold is 0xabff, and the bottom threshold is 0xab00.

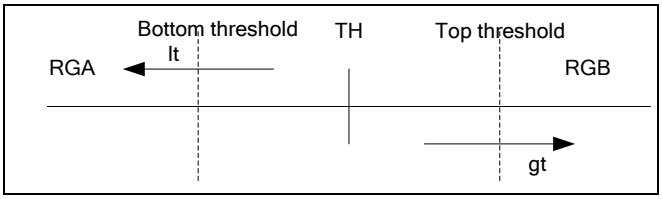


Figure 15-12 Hysteresis Error Mechanism for Gain Calibration of Total Active Power

15.9.3.2. Offset Calibration

To improve the energy metering accuracy, the offset calibration is introduced to the power calculation to eliminate the offset caused by the crosstalk.

Users can set the offset calibration values in the registers listed in the following table.

Table 15-19 Registers Related to Power Offset Calibration

Register	Address	Data Format	Description
Registers for calibrating the total active/reactive power	0xE98E~0xE993	32-bit	To set offset calibration for the total active/reactive power of each phase.
Registers for calibrating the fundamental active/reactive power	0xE99C~0xE9A1	32-bit	To set offset calibration for the fundamental active/reactive power of each phase.

15.10. Apparent Power Calculation

The apparent power can be calculated in two methods:

1. Based on the instantaneous total/fundamental current and voltage RMS:

$$S = \frac{Irms \times Urms}{4}$$ Equation 15-13

Where, S is the total/fundamental apparent power;

Irms is the total/fundamental current RMS after calibration;

Urms is the total/fundamental voltage RMS after calibration.

2. Based on the instantaneous total/fundamental active and reactive power:

$$S = \sqrt{P^2 + Q^2}$$ Equation 15-14

Where, S is the total/fundamental apparent power;

P is the total/fundamental active power after calibration;

Q is the total/fundamental reactive power after calibration.

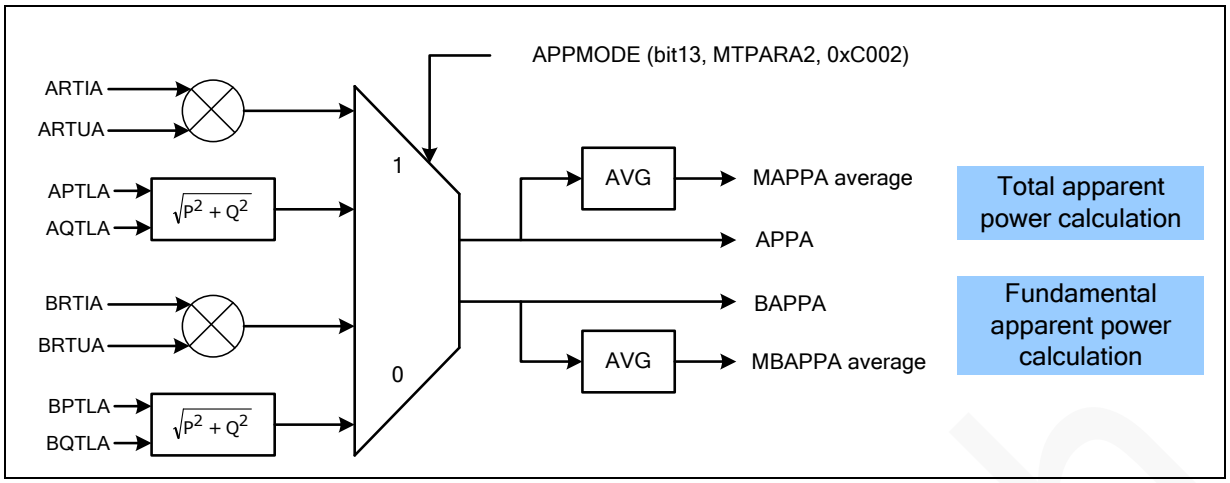


Figure 15-13 Apparent Power Calculation

The apparent power is stored in the instantaneous apparent power registers. And the apparent power can be averaged to acquire the average value. All the registers are in the format of 32-bit 2's complement.

The instantaneous apparent power of each phase is used for calculating the apparent power on the overall system, and for the energy accumulation and pulse generation in normal mode.

Table 15-20 Registers Related to Apparent Power Calculation

Register	Bit	Description
MTPARA2, 0xC002	Bit13 APPMODE	To select the apparent power calculation method. 0, to calculate the apparent power based on the current RMS; 1, to calculate the apparent power based on the active and reactive power.
Registers for total apparent power		Address: 0xE81F~0xE821. The instantaneous total apparent power of each phase, 32-bit, 2's complement, positive.
		Address: 0xE8EB~0xE8ED. The average total apparent power of each phase, 32-bit, 2's complement, positive.
Registers for fundamental apparent power		Address: 0xE854~0xE856. The instantaneous fundamental apparent power of each phase, 32-bit, 2's complement, positive.
		Address: 0xE8F6~0xE8F8 The average fundamental apparent power of each phase, 32-bit, 2's complement, positive.

As for all the registers for total apparent power, when the metering frequency is 6.5536MHz, the instantaneous data are updated in 80ms and settled in 400ms, and the average data are updated in 640ms, and settled in 1s; when the metering frequency is 1.6384MHz, the instantaneous data are

updated in 320ms and settled in 1.6s, and the average data are updated in 2.56s and settled in 4s; when the metering frequency is 819.2kHz, the instantaneous data are updated in 640ms and settled in 3.2s, and the average data are updated in 5.12s and settled in 8s.

As for all the registers for fundamental apparent power, when the metering frequency is 6.5536MHz, the instantaneous data are updated in 80ms and settled in 450ms, and the average data are updated in 640ms, and settled in 1s; when the metering frequency is 1.6384MHz, the instantaneous data are updated in 320ms and settled in 1.8s, and the average data are updated in 2.56s and settled in 4s; when the metering frequency is 819.2kHz, the instantaneous data are updated in 640ms and settled in 3.6s, and the average data are updated in 5.12s and settled in 8s.

15.11. Power Factor Calculation

The power factor of each phase or on the overall system can be calculated following the equation:

$$\cos\theta = \frac{|P|}{S} \qquad \text{Equation 15-15}$$

Where, cosθ, is the reading of the power factor registers, 32-bit, unsigned;

|P|, is the value of the registers for the absolute value of the total/fundamental instantaneous active power of each phase/on the overall system;

S, is the value of the registers for the total/fundamental instantaneous apparent power of each phase/on the overall system.

The power factor is stored in the 32-bit unsigned registers. And the power factor can be averaged to acquire the average value.

Table 15-21 Registers Related to Power Factor Calculation

Register	Address	Format	Description
Registers for the total power factor.	0xE811~0xE813	32-bit, unsigned.	The instantaneous total power factor of each phase.
	0xE8E4~0xE8E6		The average total power factor of each phase.
	0xE814		The instantaneous total power factor on the overall system.
	0xE8E7		The average total power factor on the overall system.
Registers for the fundamental power factor.	0xE857~0xE859	32-bit, unsigned.	The instantaneous fundamental power factor of each phase.
	0xE8F9~0xE8FB		The average fundamental power factor of each phase.
	0xE85A		The instantaneous fundamental power factor on the overall system.

Register	Address	Format	Description
	0xE8FC		The average fundamental power factor on the overall system.

The actual power factor is the ratio of the reading of the above registers to 2^31, which should be in the range of 2~0. When the ratio is higher than 1, the power factor is defined to be 1.

As for all the registers for total power factor, when the metering frequency is 6.5536MHz, the instantaneous data are updated in 80ms and settled in 400ms, and the average data are updated in 640ms, and settled in 1s; when the metering frequency is 1.6384MHz, the instantaneous data are updated in 320ms and settled in 1.6s, and the average data are updated in 2.56s and settled in 4s; when the metering frequency is 819.2kHz, the instantaneous data are updated in 640ms and settled in 3.2s, and the average data are updated in 5.12s and settled in 8s.

As for all the registers for fundamental power factor, when the metering frequency is 6.5536MHz, the instantaneous data are updated in 80ms and settled in 450ms, and the average data are updated in 640ms, and settled in 1s; when the metering frequency is 1.6384MHz, the instantaneous data are updated in 320ms and settled in 1.8s, and the average data are updated in 2.56s and settled in 4s; when the metering frequency is 819.2kHz, the instantaneous data are updated in 640ms and settled in 3.6s, and the average data are updated in 5.12s and settled in 8s.

15.12. Calculating Power On The Overall System

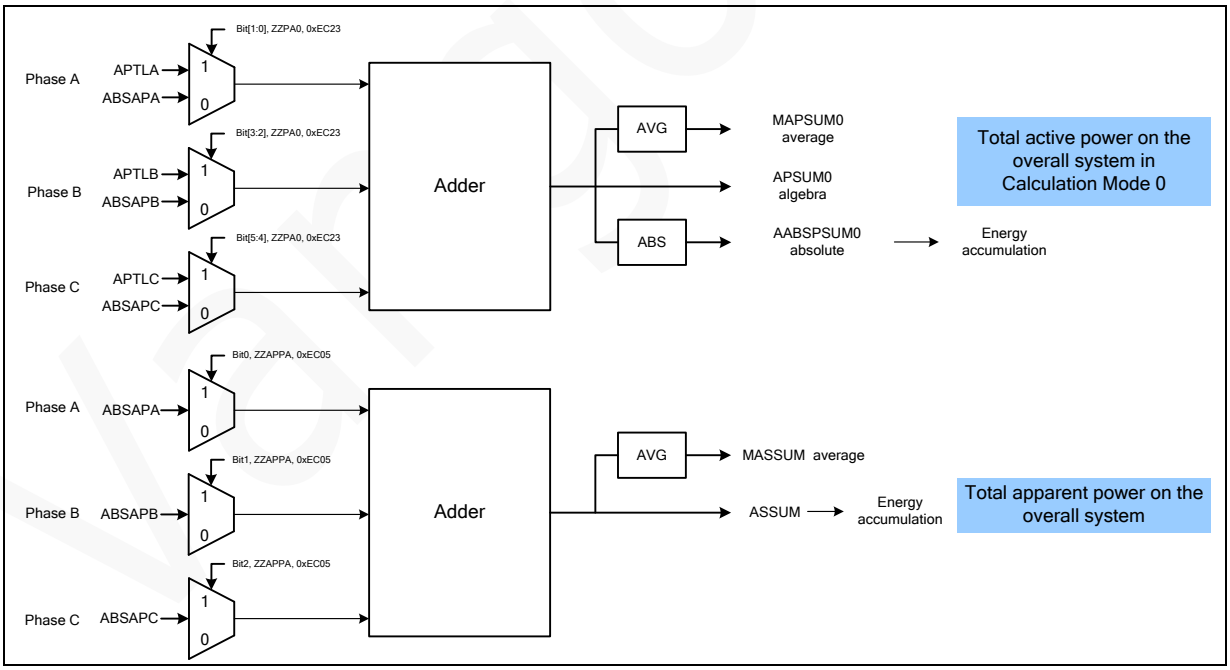


Figure 15-14 Power on the overall system Calculation

In the V9203, there are two methods to calculate the active/reactive power on the overall system, but only one method to calculate the apparent power on the overall system.

15.12.1. Active/Reactive Power on the Overall System

Select one of the three values, algebra value, absolute value, and the value "0", for each phase, and sum them up, to acquire the total/fundamental active/reactive power on the overall system. When the selection is done via configuring the registers ZZPA0 (0xEC23) or ZZQA0 (0xEC47), the sum is the total/fundamental active/reactive power on the overall system in Calculation Mode 0. And, when the selection is done via configuring the registers ZZPA1 (0xEC24) or ZZQA1 (0xEC48), the sum is the instantaneous total/fundamental active/reactive power on the overall system in Calculation Mode 1. Then, the sum is averaged or processed to acquire the absolute value. The absolute value is for energy accumulation.

Table 15-22 Registers Related to Active/Reactive Power On the overall system Calculation

Register	Description
Register for total/fundamental active power on the overall system Calculation Mode 0 (0xEC23, ZZPA0).	0x15 is recommended.
Register for total/fundamental active power on the overall system Calculation Mode 1 (0xEC24, ZZPA1).	0x2A is recommended.
Register for total/fundamental reactive power on the overall system Calculation Mode 0 (0xEC47, ZZQA0).	0x15 is recommended.
Register for total/fundamental reactive power on the overall system Calculation Mode 1 (0xEC48, ZZQA1).	0x2A is recommended.
Registers for total active/reactive power on the overall system.	Address: 0xE801~0xE804. The absolute value of the instantaneous total active/reactive power on the overall system, 32-bit, 2's complement, positive.
	Address: 0xE822~0xE823. The algebra value of the instantaneous total active power on the overall system, 32-bit, 2's complement.
	Address: 0xE831~0xE832. The algebra value of the instantaneous total reactive power on the overall system, 32-bit, 2's complement.
	Address: 0xE8EE~0xE8EF. The average total active power on the overall system, 32-bit, 2's complement.

Register	Description
	Address: 0xE8F3~0xE8F4. The average total reactive power on the overall system, 32-bit, 2's complement.
Registers for fundamental active/reactive power on the overall system.	Address: 0xE850~0xE853. The absolute value of the instantaneous fundamental active/reactive power on the overall system, 32-bit, 2's complement, positive.
	Address: 0xE864~0xE865. The algebra value of the instantaneous fundamental active power on the overall system, 32-bit, 2's complement.
	Address: 0xE875~0xE876. The algebra value of the instantaneous fundamental reactive power on the overall system, 32-bit, 2's complement.
	Address: 0xE903~0xE904. The average fundamental active power on the overall system, 32-bit, 2's complement.
	Address: 0xE908~0xE909. The average fundamental reactive power on the overall system, 32-bit, 2's complement.

As for all the registers for total active/reactive power on the overall system, when the metering frequency is 6.5536MHz, the instantaneous data are updated in 80ms and settled in 400ms, and the average data are updated in 640ms, and settled in 1s; when the metering frequency is 1.6384MHz, the instantaneous data are updated in 320ms and settled in 1.6s, and the average data are updated in 2.56s and settled in 4s; when the metering frequency is 819.2kHz, the instantaneous data are updated in 640ms and settled in 3.2s, and the average data are updated in 5.12s and settled in 8s.

As for all the registers for fundamental active/reactive power on the overall system, when the metering frequency is 6.5536MHz, the instantaneous data are updated in 80ms and settled in 450ms, and the average data are updated in 640ms, and settled in 1s; when the metering frequency is 1.6384MHz, the instantaneous data are updated in 320ms and settled in 1.8s, and the average data are updated in 2.56s and settled in 4s; when the metering frequency is 819.2kHz, the instantaneous data are updated in 640ms and settled in 3.6s, and the average data are updated in 5.12s and settled in 8s.

15.12.2. Apparent Power on the Overall System

Select one of the two values, the apparent power and the value "0", for each phase, and sum them up, to acquire the instantaneous total/fundamental apparent power on the overall system, which is for

apparent energy accumulation. The selection is done via configuring the register ZZAPPA (0xEC05). Then, the sum is averaged to acquire the average value.

Table 15-23 Registers Related to Apparent Power On the overall system Calculation

Register	Description
Register for total/fundamental apparent power on the overall system calculation (0xEC05, ZZAPPA).	0x07 is recommended.
Registers for the total apparent power on the overall system.	Address: 0xE84E. The instantaneous total apparent power on the overall system, 32-bit, 2's complement, positive.
	Address: 0xE8F5. The average total apparent power on the overall system, 32-bit, 2's complement, positive.
Registers for the fundamental apparent power on the overall system.	Address: 0xE88C. The instantaneous fundamental apparent power on the overall system, 32-bit, 2's complement, positive.
	Address: 0xE90A. The average fundamental apparent power on the overall system, 32-bit, 2's complement, positive.

As for all the registers for total apparent power on the overall system, when the metering frequency is 6.5536MHz, the instantaneous data are updated in 80ms and settled in 400ms, and the average data are updated in 640ms, and settled in 1s; when the metering frequency is 1.6384MHz, the instantaneous data are updated in 320ms and settled in 1.6s, and the average data are updated in 2.56s and settled in 4s; when the metering frequency is 819.2kHz, the instantaneous data are updated in 640ms and settled in 3.2s, and the average data are updated in 5.12s and settled in 8s.

As for all the registers for fundamental apparent power on the overall system, when the metering frequency is 6.5536MHz, the instantaneous data are updated in 80ms and settled in 450ms, and the average data are updated in 640ms, and settled in 1s; when the metering frequency is 1.6384MHz, the instantaneous data are updated in 320ms and settled in 1.8s, and the average data are updated in 2.56s and settled in 4s; when the metering frequency is 819.2kHz, the instantaneous data are updated in 640ms and settled in 3.6s, and the average data are updated in 5.12s and settled in 8s.

15.13. Energy Accumulation and Pulse Generation

The V9203 supports accumulating the absolute value of the active/ reactive/ apparent power on the overall system to the energy accumulator at normal speed, and accumulating the selected power on the overall system to the energy accumulator at high speed.

15.13.1. Normal Mode

Set the bit EGYEN (bit15, 0xC002, MTPARA2) to 1 enable accumulating the absolute value of the active/reactive/apparent power on the overall system to the energy accumulators in normal mode, at normal speed, 12.5Hz. When the value of the register outnumbers that preset in the energy threshold register, an energy pulse is generated, a value equal to the energy threshold is minus from the energy register, and the energy pulse counter increments by 1.

In this mode, no CF pulse can be output.

The energy threshold is calculated in the following equation:

$$PGAT = P \times T \times 6.25 \qquad \text{Equation 15-16}$$

Where, P, is the value of register for the total or fundamental active power on the overall system when rate voltage/current is applied.

T, is the time constant, acquired via the equation:

$$T = \frac{3600 \times 1000}{PulseConstant \times U_n \times I_n \times PhaseNumber} \qquad \text{Equation 15-17}$$

15.13.2. High-Speed Mode

To improve the resolution of the CF pulse output, the circuits for energy accumulation at high speed is provided in the V9203. In this mode, the accumulation rate is 204800Hz.

Set one or some of bit[7:4] of MTPARA2 (0xC002) to enable the energy accumulation at high speed.

When this function is enabled, the power on the overall system is selected according to the configuration of the register ZZPCF0A (0xEC34), and is transferred to the corresponding power register, such as ZZPCF0 (0xEC33), for energy accumulation in high-speed mode, which is updated in 80ms. The power is accumulated to the energy accumulation registers in high-speed mode, such as EGY0L (0xD000) and EGY0H (0xD001), at a rate of 204800Hz. When the value of the register outnumbers that preset in the energy threshold register, an energy pulse is generated, a value equal to the energy threshold is minus from the energy register, and the energy pulse counter increments by 1. When the CF pulse output is enabled, one CF pulse is output when the pulses counter increments by 2.

The threshold for the energy accumulation and pulse generation in high-speed mode is 16384 times of that in normal mode, so, the 14 most significant bits must be padded with 0s.

Set the bits CFON (bit[3:0], 0xC002, MTPARA2) to enable or disable the CF pulse output. When the metering frequency is 6.5536MHz and the ADC sampling frequency is 819.2kHz, the maximum CF pulse output frequency is 102.4Hz with a pulse width of 80ms. When the pulse period is shorter than 160ms, the duty cycle is 50%.

When a weak signal is input, the V9203 can increase the meter constant to reduce the energy threshold to accelerate the pulse generation rate to improve the calibration rate. Users can accelerate the rate via configuring the bits CFFAST (bit[10:8], 0xC002, MTPARA2).

Table 15-24 Pins for CF Pulse Output

Pin #	Mnemonic	Description
26	CF0	CF pulse output. Via configuring the registers ZZPA0 (0xEC23) and ZZPA1 (0xEC24), this pin can be used to output total or fundamental active energy CF pulse of each phase or on the overall system.
27	CF1	CF pulse output. Via configuring the registers ZZQA0 (0xEC47) and ZZQA1 (0xEC48), this pin can be used to output total or fundamental reactive energy CF pulse of each phase or on the overall system.
28	CF2	CF pulse output. Via configuring the registers ZZPA0 (0xEC23) and ZZPA1 (0xEC24), this pin can be used to output total or fundamental active energy CF pulse of each phase or on the overall system.
29	CF3	CF pulse output. Via configuring the registers ZZQA0 (0xEC47), ZZQA1 (0xEC48), and ZZAPPA (0xEC05), this pin can be used to output total reactive energy, or total/fundamental apparent energy CF pulse of each phase or on the overall system.

Table 15-25 Registers Related to Energy Accumulation and CF Pulse Output in High-Speed Mode

Register	Bit		Description
Register for CF pulse source selection (0xEC34, ZZPCF0A)	Bit[15:12]	CF3PS	To set the source for the CF pulse output on the pin CF3. By default, these bits are set to 0b0000, representing a non-zero value is set to be the source for the pulse output on the pin CF3.
	Bit[11:8]	CF2PS	To set the source for the CF pulse output on the pin CF2. By default, these bits are set to 0b0000, representing a non-zero value is set to be the source for the pulse output on the pin CF2.
	Bit[7:4]	CF1PS	To set the source for the CF pulse output on the pin CF1. By default, these bits are set to 0b0000, representing a non-zero value is set to be the source for the pulse output on the pin CF1.
	Bit[3:0]	CF0PS	To set the source for the CF pulse output on the pin CF0.

Register	Bit		Description
			By default, these bits are set to 0b0000, representing a non-zero value is set to be the source for the pulse output on the pin CF0.
MTPARA2, 0xC002	Bit[10:8]	CFFAST	To accelerate the pulse generation speed. 000~011, ×1 (by default); 100, ×4; 101, ×16; 110, ×64; 111, ×128.
	Bit[7:4]	CFCALC	To enable accumulating the total/fundamental active/reactive/apparent energy in high-speed mode. 1, enable; 0, disable. Bit7, total/fundamental apparent energy on the overall system, or total reactive energy on the overall system (CF3); Bit6, total/fundamental active energy on the overall system (CF2); Bit5, total/fundamental reactive energy on the overall system (CF1); Bit4, total/fundamental active energy on the overall system (CF0).
	Bit[3:0]	CFON	To enable CF pulse output. 1, enable; 0, disable. Bit3, pulse output on the pin CF3; Bit2, pulse output on the pin CF2; Bit1, pulse output on the pin CF1; Bit0, pulse output on the pin CF0.

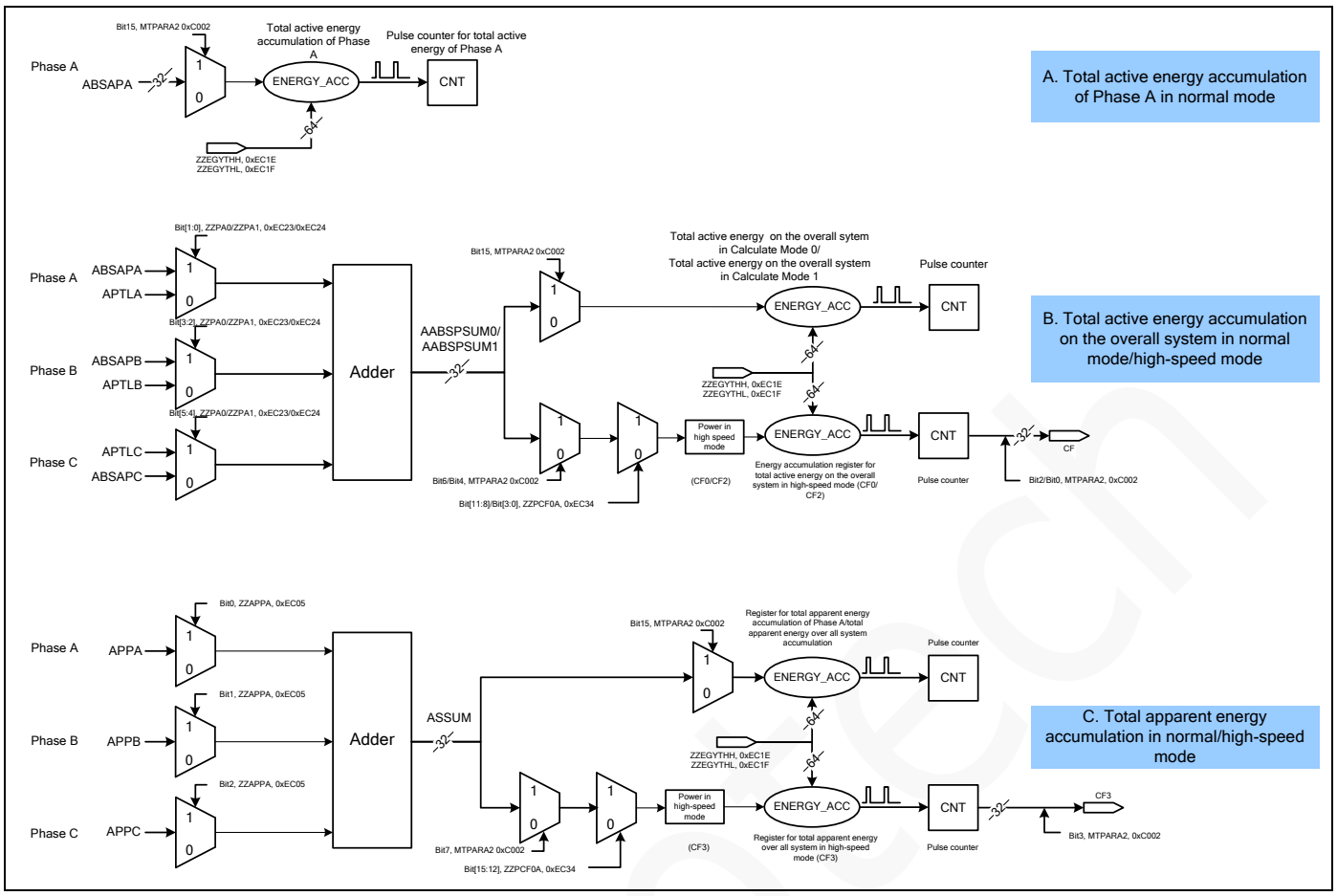


Figure 15-15 Energy Accumulation (Phase A)

15.14. Line Frequency Measurement

The V9203 supports line frequency measurement.

In the line frequency measurement circuit, the fundamental current or voltage signal of each phase is sampled at a frequency of 102.4kHz for zero-crossing detection, and the number of the samples among continuous 33 negative-to-positive zero-crossing points is equal to the line frequency. So the line frequency of each phase is calculated as follows:

$$f = \frac{3276800}{FRQ}$$ Equation 15-18

Where, f is the line frequency to be measured; FRQ is the content of the registers for line frequency of each phase, in the address range of 0xC008~0xC00A, in the form of decimal.

The positive registers for line frequency are accessed as 32-bit registers with the 15 most significant bits padded with 0s. The measurement resolution is 0.0008Hz.

When the metering frequency is 6.5536MHz, these registers are updated once every 640ms, and the settling time is associated with the signal strength. The weaker the signal is, the longer the settling time is, usually more than 1s.

When the metering frequency is 1.6384MHz, these registers are updated once every 2.56s, and the settling time is associated with the signal strength. The weaker the signal is, the longer the settling time

is, usually more than 4s.

When the metering frequency is 819.2kHz, these registers are updated once every 5.12s, and the settling time is associated with the signal strength. The weaker the signal is, the longer the settling time is, usually more than 8s.

15.15. Phase Angle Measurement

In the V9203, the difference between the phase angle of the signal to be measured and that of the voltage of Phase A, which is defined as 0, is equal to the phase angle of the signal to be measured.

The phase angle measurement circuit samples the fundamental current or voltage signal of each phase at a frequency of 102.4kHz for zero-crossing detection, and the number of the samples between the N^{th} negative-to-positive zero-crossing point of the signal to be measured and the $(N-1)^{th}$ negative-to positive zero-crossing point of the voltage of Phase A is equal to the phase angle of the signal to be measured. So the phase angle of signal to be measured is calculated as follows:

$$PH = \frac{(\mathrm{PHS} + 1) * 360 * \mathrm{f}}{102400}$$

Where,

PH is the difference between the phase angle of the signal to be measured and that of the voltage of Phase A which is defined as 0;

PHS is the content of the registers for phase, in the address range of 0xC00B~0xC00F, in the form of decimal;

f is line frequency, unit HZ.

The positive registers for phase angle are accessed as 32-bit registers with the 20 most significant bits padded with 0s. The measurement resolution is 0.175 degrees.

When the metering frequency is 6.5536MHz, these registers are updated once every 20ms, and the settling time is associated with the signal strength. The weaker the signal is, the longer the settling time is, usually more than 1s.

When the metering frequency is 1.6384MHz, these registers are updated once every 80ms, and the settling time is associated with the signal strength. The weaker the signal is, the longer the settling time is, usually more than 4s.

When the metering frequency is 819.2kHz, these registers are updated once every 160ms, and the settling time is associated with the signal strength. The weaker the signal is, the longer the settling time is, usually more than 8s.

15.16. Neutral Current Mismatch

As for a three-phase energy meter, the current RMS of the neutral wire should be equal to the RMS of the algebra sum of the phase currents:

$$I_N(t) = I_A(t) + I_B(t) + I_C(t) \qquad \text{Equation 15-20}$$

If there is mismatch between the two values, a neutral current mismatch occurs.

In the 3-phase, 4-wire system, the measured current RMS of the neutral wire is stored in the register ARTIN (0xE841). But when the neutral wire is not used, the V9203 calculated the RMS of the algebra sum of the phase currents automatically. To prevent overflow, divide the calculated RMS data by 4 and store it in the register MUM (0xE94B) for neutral current mismatch detection.

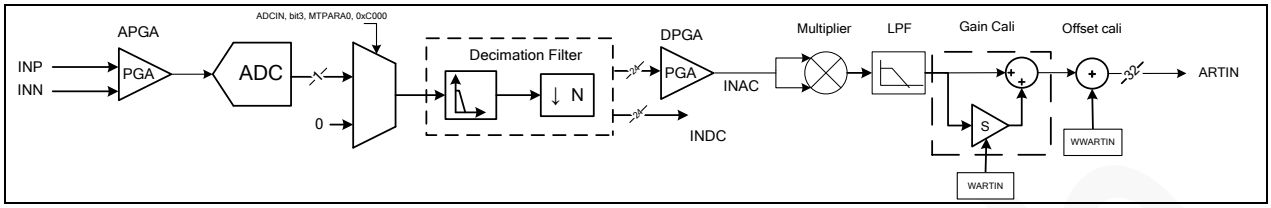


Figure 15-16 Digital Signal Processing in Neutral Wire

15.17. Zero-Crossing Detection

The V9203 supports to output the sign of the fundamental voltage and current of each phase on the pins ZX0 ~ ZX2: UA/IA on ZX0 (Pin 34), UB/IB on ZX1 (Pin 33), and UC/IC on ZX2 (Pin 32). When a high logic (1) is output on the pin, it indicates the sign is negative; when a low logic (0) is output on the pin, it indicates the sign is positive; when a high-to-low transition is output on the pin, it indicates a zero-crossing from negative to positive is occurring.

Set some bits of bit[6:1] to 1s to enable the zero-crossing interrupt. When a zero-crossing from negative to positive is detected, a zero-crossing interrupt is triggered, the flag bit is set bit, and a high logic is output on the pin IRQ0 /IRQ1 to generate an interrupt to the master MCU.

The interrupt flags can be cleared via SPI communication.

15.18. Power-off/No-Voltage Detection

In OPM1, or power-off/no-voltage pre-detection mode, use the same circuits for analog input of current, set the same analog programmable gain amplifier (APGA, 32 is recommended), and select the same digital programmable gain amplifier (DPGA), for the three current channel ADCs. Enable the output of the raw waveform of the current from the DMA_SPI interfaces. And then, users can make the current detection.

The current detection circuit in the V9203 supports full wave rectification to the raw waveform of the current output from the DMA_SPI interfaces at a sampling frequency of 6.4kHz.

If 5 continuous samples of the current waveform are higher than the pre-set threshold for current detection in ZZDCUM register (0xEC1D), a current signal is caught, and a current detection interrupt is triggered if it was enabled via setting some bits of bit[13:11] to 1s in IRQEN0 (0xA000) or IRQEN1 (0xA001). When the samples of the current wave are lower than the threshold, the interrupt bit is cleared automatically.

This interrupt can be used to fast detect the current signal in OPM1 (power-off/no-voltage pre-detection mode) and OPM2 (RMS mode).

Preset the detection threshold in the register ZZDCUM (0xEC1D) as follows:

1. Setting the gain and offset calibration for the current RMS to 0;
2. Applying rate current (In) to any current channel, and read the RMS (Irms, a 32-bit integer, the amplitude of In);
3. Writing of the threshold register if the preset threshold is 0.1% of In:

$TH = -\frac{Irms}{1000 \times 512}$, or right shifting the value $TH = -\frac{Irms}{1000}$ by 9 bits.

15.19. Initializing the V9203

When the V9203 is powered on, the clock scaler and ADCs are enabled, and the metering clock is switched to 6553.6kHz, automatically.

It is recommended to initialize the chip as follows:

1. Input high logic on the pins both PM0 and PM1, and then input low logic on the pin DEEPSLEEP for more than 4ms. The system enters OPM0, or the normal operating mode;
2. Write 0x10000000 to the register MTPARA0 (0xC000);
3. Write 0s to the registers in the address range of 0xC800~0xC837 and 0xC880~0xC8B7 to clear the RAM;
4. Write 0xAA000000 to the register MTPARA0 (0xC000), 20ms later, the RAM in the address range of 0xE000~0xE08F/0xE800~0xEAB7/0xF800~0xF87F/0xF000~0xF1EF is cleared;
5. Write 0x000000FF to the register MTPARA0 (0xC000) to enable digital input of the 7 channels;
6. Configure the registers MTPARA1 (0xC001) and MTPARA2 (0xC002) according to the application requirements;
7. Configure the analog control registers and the registers for calibration;
8. Calculate the checksum, and write it to the register MTPARA3 (0xC003);
9. 1s later, write 0 to bit0 of IRQFLAG (0xA002), and read the output logic on the pin IRQ0: A logic low indicates the configuration is right and the system works normally; otherwise, re-initialize the V9203 as the above steps.

15.20. 3-Phase, 3-Wire Service

The V9203 supports both 3-phase, 4-wire service, and 3-phase, 3-wire service.

In the 3-phase, 3-wire service, Phase B is not used, so users should configure the registers as follows:

1. Set the bit MTMODE (bit14, MTPARA2, 0xC002) to 1;
2. Set the registers for the gain calibration of Phase B to 0x80000000. And, set the registers for the power offset calibration of Phase B to 0. Then the power of Phase B does not contribute any to the energy metering;
3. In the registers for power on the overall system calculation, ZZPA0 (0xEC23), ZZPA1 (0xEC24),

ZZQA0 (0xEC47), ZZQA1 (0xEC48) and ZZAPPA (0xEC05), the active/reactive/apparent power of Phase B should be cleared for calculating the power on the overall system.

15.21. Calibration

15.21.1. Calibration Flow

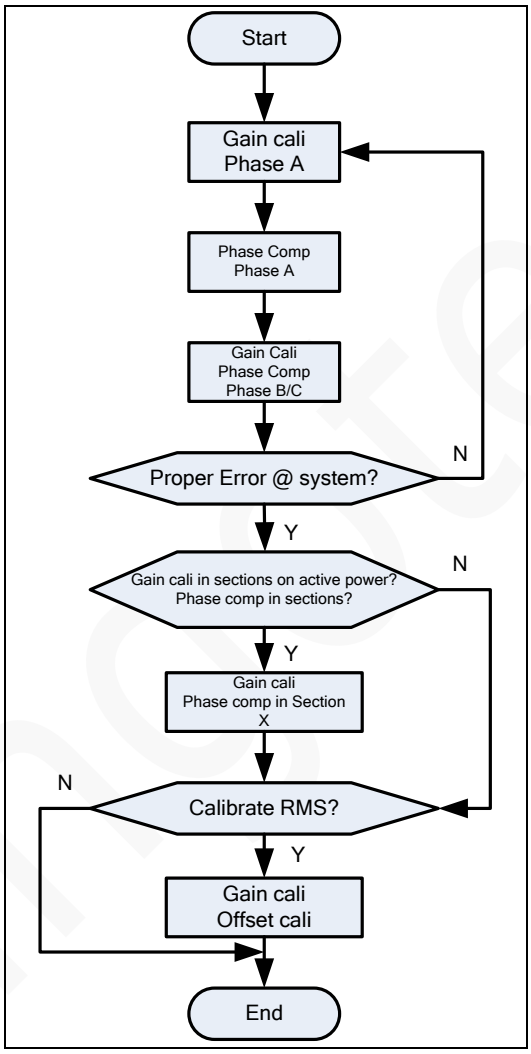


Figure 15-17 Calibration Flow

15.21.2. Equations for Calibration

All the equations in this section are suitable for both total and fundamental signal processing.

1. Equation for current/voltage RMS registers.

$$Value = V \times G \times K \qquad \text{Equation 15-21}$$

Where, V is the RMS of the input signal (mV); G is the gain; and K is a constant, 2.5×10^6.

2. Equation for power registers.

$$Value = Vi \times Gi \times Vv \times Gv \times K \times \cos\theta \times p \qquad \text{Equation 15-22}$$

Where, Vi and Vv are the input current and voltage; Gi and Gv are the gains for current and voltage respectively; cosθ is the power factor; p is the number of phase; K is a coefficient, 750 for 4-wire service, and 650 for 3-wire service.

3. Equation for ratio factor of RMS and power.

The value acquired by Equation 15-21 or Equation 15-22 is the theoretical value of the register of the RMS or power. It must be divided by a ratio factor to get the actual value.

$$Ivalue = \frac{Value}{D} \qquad \text{Equation 15-23}$$

Where, Value is the content of the register acquired by Equation 15-21 or Equation 15-22; D is the ratio factor; and Ivalue is the actual value.

Take the total current RMS of Phase A for example,

Firstly, the content of the register is acquired as follows:

$$Value = V \times G \times K$$
$$= 20 \times 4 \times 2.5 \times 10^6 = 200000000 = 0xBEBC200;$$

Secondly, the ratio factor is acquired if the actual current is 1.5000A

$$15000 = \frac{200000000}{D}$$
$$D = \frac{200000000}{15000} = 13333$$

Then, D is used as the ratio factor. Users can get the actual current RMS by dividing the content of the register by the ratio factor. By default, current RMS is accurate to the 4th decimal place.

4. Equation for line frequency registers.

$$f = \frac{3276800}{FRQ} \qquad \text{Equation 15-24}$$

Where, f is the line frequency to be measured; FRQ is the content of the registers for line frequency of each phase, in the address range of 0xC008~0xC00A, in the form of decimal.

5. Equation for power factor registers.

$$\cos\theta = \frac{Value}{2^{31}} \qquad \text{Equation 15-25}$$

Where, Value is content of the power factor registers; cosθ is the actual power factor.

6. Equation for energy accumulation threshold.

$$PGAT = P \times T \times 6.25 \qquad \text{Equation 15-26}$$

Where, P is the value of registers for the total or fundamental active power on the overall system when rate voltage/current is applied;

T is the time constant, acquired via the equation:

$$T = \frac{3600 \times 1000}{PulseConstant \times U_n \times I_n \times PhaseNumber}$$ Equation 15-27

7. Equation for the calibration registers.

$$S = 2^{31}(\frac{1}{1+e} - 1) + S_1(\frac{1}{1+e})$$ Equation 15-28

Where, S is the content of the registers for the gain calibration of the total/fundamental active/reactive and current/voltage RMS, in the form of 2's complement; S_1 is the original gain calibration; e is the error.

8. Equation for registers for phase compensation.

Please note that phase compensation must be executed after power calibration.

At a lower power factor (PF), the phase angle error can cause greater energy metering error. So generally, the phase angle error is calibrated at PF=0.5L to ensure the metering accuracy. When PF=0.5L, the phase angle between current and voltage is $-\frac{\pi}{3}$. According to Equation 15-2, a relationship between E and N depicted by the following equation is reached.

$$N = Round(\frac{1}{\pi} \times \frac{f_{smpl}}{100} \times \left\{-arccos[0.5 \times (1+E)] + \frac{\pi}{3}\right\})$$ Equation 15-29where,

N is the value, signed, to be set to the phase compensation control registers to correct the phase angle error. A positive N indicates that current signal must be delayed, so "0" must be set to the sign bit; a negative N indicates that the voltage signal must be delayed, so "1" must be set to the sign bit;

E is the energy metering error displayed in LCD screen of the calibration equipment;

f_{smpl} is the sampling frequency of the phase compensation circuit, Hz.

Equation 15-29 can be used to calculate the value N over the full range. But in practice, users can use another method to simplify the calculation.

The minimum correction range is ±1.4°, and when x is in a small range, the curve for function y=cosx is approximate to a line. So when PF is equal to 0.5L and x is over the range of $[-\frac{\pi}{3} - \frac{1.4\times\pi}{180}, -\frac{\pi}{3} + \frac{1.4\times\pi}{180}]$, users can use a simple equation as follows to calculate the value N.

$$N = Round(-\frac{3011}{2} \times E \times \frac{f_{smpl}}{819200})$$

However, please note that Equation 15-30 is only an approximate equation. Beyond a certain range of E, Equation 15-29 and Equation 15-30 may lead to different results. If they are not equal to each other, users must use Equation 15-29 to correct the phase angle error.

10. Equation for registers for current threshold for phase compensation or gain calibration of total active power in sections.

$$Value = ValueI \times K$$ Equation 15-31

ValueI is the content of the current RMS register calculated by Equation 15-21 when rate current is applied; K is the section points in the form of the percentage of the rate current, for example, 15%.

16. Interrupt

The interrupt system manages the interrupt sources and outputs two interrupt pulses (IRQ0 and IRQ1).

Two interrupt enable registers, IRQEN0 (0xA000) and IRQEN1 (0xA001), can enable or disable the interrupts and its output on the pin IRQ0 and IRQ1 respectively, and the interrupt flag register IRQFLAG (0xA002) sets flag bit for each interrupt that is occurring.

16.1. Interrupt Registers

Table 16-1 IRQ0 Interrupt Enable Register (0xA000, IRQEN0)

0xA000, R/W, IRQ0 Interrupt Enable Register, IRQEN0				
Bit		Default Value	Function Description	
bit[31:17]	Reserved	0		
bit16	PD	0	To enable power-down interrupt, high-level triggered.	1, enable; 0, disable.
bit15	SPI	0	To enable SPI communication error interrupt, rising edge triggered.	1, enable; 0, disable.
bit14	PSE	0	To enable phase sequence error interrupt, rising edge triggered.	1, enable; 0, disable.
bit13	EXIIC	0	To enable current detection interrupt of Channel IC, level triggered.	1, enable; 0, disable.
bit12	EXIIB	0	To enable current detection interrupt of Channel IB, level triggered.	1, enable; 0, disable.
bit11	EXIIA	0	To enable current detection interrupt of Channel IA, level triggered.	1, enable; 0, disable.
bit10	CF3	0	To enable the pulse output interrupt on the pin CF3, rising edge triggered.	1, enable; 0, disable.
bit9	CF2	0	To enable the pulse output interrupt on the pin CF2, rising edge triggered.	1, enable; 0, disable.
bit8	CF1	0	To enable the pulse output interrupt on the pin CF1, rising edge triggered.	1, enable; 0, disable.
bit7	CF0	0	To enable the pulse output interrupt on the pin CF0, rising edge triggered.	1, enable; 0, disable.
bit[6:4]	Reserved	0		
bit3	ZXUC	0	To enable the interrupt by negative to positive	1, enable; 0,

0xA000, R/W, IRQ0 Interrupt Enable Register, IRQEN0				
Bit		Default Value	Function Description	
			zero-crossing of Channel UC, edge triggered.	disable.
bit2	ZXUB	0	To enable the interrupt by negative to positive zero-crossing of Channel UB, edge triggered.	1, enable; 0, disable.
bit1	ZXUA	0	To enable the interrupt by negative to positive zero-crossing of Channel UA, edge triggered.	1, enable; 0, disable.
bit0	CHK	0	To enable system configuration error interrupt, high-level triggered.	This interrupt is forced to be enabled even though this bit is set to 0.
The configuration of this register can be read out of the register ZZIRQ0 (0xEC20) which is accessed as a 32-bit register with the 15 most significant bits padded with 0s and is used to calculate the checksum for system check.				

Table 16-2 IRQ1 Interrupt Enable Register (0xA001, IRQEN1)

0xA001, R/W, IRQ1 Interrupt Enable Register, IRQEN1				
Bit		Default Value	Function Description	
bit[31:17]	Reserved	0		
bit16	PD	0	To enable power-down interrupt, high-level triggered.	1, enable; 0, disable.
bit15	SPI	0	To enable SPI communication error interrupt, rising edge triggered.	1, enable; 0, disable.
bit14	PSE	0	To enable phase sequence error interrupt, rising edge triggered.	1, enable; 0, disable.
bit13	EXIIC	0	To enable current detection interrupt of Channel IC, level triggered.	1, enable; 0, disable.
bit12	EXIIB	0	To enable current detection interrupt of Channel IB, level triggered.	1, enable; 0, disable.
bit11	EXIIA	0	To enable current detection interrupt of Channel IA, level triggered.	1, enable; 0, disable.
bit10	CF3	0	To enable the pulse output interrupt on the pin CF3, rising edge triggered.	1, enable; 0, disable.
bit9	CF2	0	To enable the pulse output interrupt on the pin CF2, rising edge triggered.	1, enable; 0, disable.

0xA001, R/W, IRQ1 Interrupt Enable Register, IRQEN1				
Bit		Default Value	Function Description	
bit8	CF1	0	To enable the pulse output interrupt on the pin CF1, rising edge triggered.	1, enable; 0, disable.
bit7	CF0	0	To enable the pulse output interrupt on the pin CF0, rising edge triggered.	1, enable; 0, disable.
bit[6:4]	Reserved	0		
bit3	ZXUC	0	To enable the interrupt by negative to positive zero-crossing of Channel UC, edge triggered.	1, enable; 0, disable.
bit2	ZXUB	0	To enable the interrupt by negative to positive zero-crossing of Channel UB, edge triggered.	1, enable; 0, disable.
bit1	ZXUA	0	To enable the interrupt by negative to positive zero-crossing of Channel UA, edge triggered.	1, enable; 0, disable.
bit0	CHK	0	To enable system configuration error interrupt, high-level triggered.	1, enable; 0, disable.
The configuration of this register can be read out of the register ZZIRQ1 (0xEC21) which is accessed as a 32-bit register with the 15 most significant bits padded with 0s and is used to calculate the checksum for system check.				

Table 16-3 Interrupt Flag Register (0xA002, IRQFLAG)

0xA002, R/W, Interrupt Flag Register, IRQFLAG				
bit		Default Value	Function Description	
bit[31:17]	Reserved	0		
bit16	PD	0	To indicate a power-down interrupt occurs.	1, the interrupt occurs.
bit15	SPI	0	To indicate an SPI communication error interrupt occurs.	1, the interrupt occurs.
bit14	PSE	0	To indicate a phase sequence error interrupt occurs.	1, the interrupt occurs.
bit13	EXIIC	0	To indicate a current detection interrupt of Channel IC occurs.	1, the interrupt occurs.
bit12	EXIIB	0	To indicate a current detection interrupt of Channel IB occurs.	1, the interrupt

0xA002, R/W, Interrupt Flag Register, IRQFLAG				
bit		Default Value	Function Description	
				occurs.
bit11	EXIIA	0	To indicate a current detection interrupt of Channel IA occurs.	1, the interrupt occurs.
bit10	CF3	0	To indicate a pulse output interrupt on pin CF3 occurs.	1, the interrupt occurs.
bit9	CF2	0	To indicate a pulse output interrupt on pin CF2 occurs.	1, the interrupt occurs.
bit8	CF1	0	To indicate a pulse output interrupt on pin CF1 occurs.	1, the interrupt occurs.
bit7	CF0	0	To indicate a pulse output interrupt on pin CF0 occurs.	1, the interrupt occurs.
bit[6:4]	Reserved	0		
bit3	ZXUC	0	To indicate an interrupt by negative to positive zero-crossing of Channel UC occurs.	1, the interrupt occurs.
bit2	ZXUB	0	To indicate an interrupt by negative to positive zero-crossing of Channel UB occurs.	1, the interrupt occurs.
bit1	ZXUA	0	To indicate an interrupt by negative to positive zero-crossing of Channel UA occurs.	1, the interrupt occurs.
bit0	CHK	0	To indicate a system configuration error interrupt occurs.	1, the interrupt occurs.

16.2. System Configuration Error Interrupt

In the V9203, the configuration of the ZZPARA3 (0xEC2A) and the other 109 registers listed in the following table must be summed up for system configuration checksum calculation, and the checksum must be 0xFFFFFFFF. The checksum is calculated once every 640ms. If the checksum is 0xFFFFFFFF, it means the configuration is right; otherwise, a system configuration error occurs.

When a system configuration error occurs, the system configuration interrupt generated, and a high

logic is output on the pin IRQ0 whatever bit0 of IRQEN0 register (0xA000) is set. But, if bit0 of IRQEN1 register (0xA001) is cleared, this interrupt output is disabled on the pin IRQ1.

Table 16-4 Registers for System Configuration Checksum Calculation

No.	Address	Register		R/W	Bits for Checksum Calculation	Default Value
1	0xE954	WAEC0	To set phase compensation in Section 0.	R/W	32-bit	0
2	0xE955	WAEC1	To set phase compensation in Section 1.	R/W	32-bit	0
3	0xE956	WAEC2	To set phase compensation in Section 2.	R/W	32-bit	0
4	0xE957	WAEC3	To set phase compensation in Section 3.	R/W	32-bit	0
5	0xE958	WAEC4	To set phase compensation in Section 4.	R/W	32-bit	0
6	0xE95A	WAPTAK0	To set gain calibration in Section 0 of the total active power of Phase A.	R/W	32-bit	0
7	0xE95B	WAPTAK1	To set gain calibration in Section 1 of the total active power of Phase A.	R/W	32-bit	0
8	0xE95C	WAPTAK2	To set gain calibration in Section 2 of the total active power of Phase A.	R/W	32-bit	0
9	0xE95E	WAPTBK0	To set gain calibration in Section 0 of the total active power of Phase B.	R/W	32-bit	0
10	0xE95F	WAPTBK1	To set gain calibration in Section 1 of the total active power of Phase B.	R/W	32-bit	0
11	0xE960	WAPTBK2	To set gain calibration in Section 2 of the total active power of Phase B.	R/W	32-bit	0
12	0xE962	WAPTCK0	To set gain calibration in Section 0 of the total active power of Phase C.	R/W	32-bit	0
13	0xE963	WAPTCK1	To set gain calibration in Section 1 of the total active power of Phase C.	R/W	32-bit	0
14	0xE964	WAPTCK2	To set gain calibration in Section 2 of the total active power of Phase C.	R/W	32-bit	0
15	0xE965	WAQTA	To set gain calibration of the total reactive power of Phase A.	R/W	32-bit	0
16	0xE966	WAQTB	To set gain calibration of the total reactive power of Phase B.	R/W	32-bit	0

No.	Address	Register		R/W	Bits for Checksum Calculation	Default Value
17	0xE967	WAQTC	To set gain calibration of the total reactive power of Phase C.	R/W	32-bit	0
18	0xE968	WARTIA	To set gain calibration of the total current RMS of Phase A.	R/W	32-bit	0
19	0xE969	WARTIB	To set gain calibration of the total current RMS of Phase B.	R/W	32-bit	0
20	0xE96A	WARTIC	To set gain calibration of the total current RMS of Phase C.	R/W	32-bit	0
21	0xE96B	WARTIN	To set gain calibration of the total current RMS of Channel IN.	R/W	32-bit	0
22	0xE96C	WARTUA	To set gain calibration of the total voltage RMS of Phase A.	R/W	32-bit	0
23	0xE96D	WARTUB	To set gain calibration of the total voltage RMS of Phase B.	R/W	32-bit	0
24	0xE96E	WARTUC	To set gain calibration of the total voltage RMS of Phase C.	R/W	32-bit	0
25	0xE96F		It is recommended to write of 0s.	R/W	32-bit	0
26	0xE970	WBPTA	To set gain calibration of the fundamental active power of Phase A.	R/W	32-bit	0
27	0xE971	WBPTB	To set gain calibration of the fundamental active power of Phase B.	R/W	32-bit	0
28	0xE972	WBPTC	To set gain calibration of the fundamental active power of Phase C.	R/W	32-bit	0
29	0xE973	WBQTA	To set gain calibration of the fundamental reactive power of Phase A.	R/W	32-bit	0
30	0xE974	WBQTB	To set gain calibration of the fundamental reactive power of Phase B.	R/W	32-bit	0
31	0xE975	WBQTC	To set gain calibration of the fundamental reactive power of Phase C.	R/W	32-bit	0
32	0xE976	WBRTIA	To set gain calibration of the fundamental current RMS of Phase A.	R/W	32-bit	0
33	0xE977	WBRTIB	To set gain calibration of the fundamental current RMS of Phase B.	R/W	32-bit	0
34	0xE978	WBRTIC	To set gain calibration of the fundamental current RMS of Phase C.	R/W	32-bit	0

No.	Address	Register		R/W	Bits for Checksum Calculation	Default Value
35	0xE979	WBRTUA	To set gain calibration of the fundamental voltage RMS of Phase A.	R/W	32-bit	0
36	0xE97A	WBRTUB	To set gain calibration of the fundamental voltage RMS of Phase B.	R/W	32-bit	0
37	0xE97B	WBRTUC	To set gain calibration of the fundamental voltage RMS of Phase C.	R/W	32-bit	0
38	0xE97C	WTPA0A	To set Current Threshold 0 for phase compensation in sections of Phase A.	R/W	32-bit	0
39	0xE97D	WTPA0B	To set Current Threshold 0 for phase compensation in sections of Phase B.	R/W	32-bit	0
40	0xE97E	WTPA0C	To set Current Threshold 0 for phase compensation in sections of Phase C.	R/W	32-bit	0
41	0xE97F	WTPA1A	To set Current Threshold 1 for phase compensation in sections of Phase A.	R/W	32-bit	0
42	0xE980	WTPA1B	To set Current Threshold 1 for phase compensation in sections of Phase B.	R/W	32-bit	0
43	0xE981	WTPA1C	To set Current Threshold 1 for phase compensation in sections of Phase C.	R/W	32-bit	0
44	0xE982	WTPA2A	To set Current Threshold 2 for phase compensation in sections of Phase A.	R/W	32-bit	0
45	0xE983	WTPA2B	To set Current Threshold 2 for phase compensation in sections of Phase B.	R/W	32-bit	0
46	0xE984	WTPA2C	To set Current Threshold 2 for phase compensation in sections of Phase C.	R/W	32-bit	0
47	0xE985	WTPA3A	To set Current Threshold 3 for phase compensation in sections of Phase A.	R/W	32-bit	0
48	0xE986	WTPA3B	To set Current Threshold 3 for phase compensation in sections of Phase B.	R/W	32-bit	0
49	0xE987	WTPA3C	To set Current Threshold 3 for phase compensation in sections of Phase C.	R/W	32-bit	0
50	0xE988	WTPP0A	To set Current Threshold 0 for calibrating the total active power of Phase A.	R/W	32-bit	0
51	0xE989	WTPP0B	To set Current Threshold 0 for calibrating the total active power of	R/W	32-bit	0

No.	Address	Register		R/W	Bits for Checksum Calculation	Default Value
			Phase B.			
52	0xE98A	WTPP0C	To set Current Threshold 0 for calibrating the total active power of Phase C.	R/W	32-bit	0
53	0xE98B	WTPP1A	To set Current Threshold 1 for calibrating the total active power of Phase A.	R/W	32-bit	0
54	0xE98C	WTPP1B	To set Current Threshold 1 for calibrating the total active power of Phase B.	R/W	32-bit	0
55	0xE98D	WTPP1C	To set Current Threshold 1 for calibrating the total active power of Phase C.	R/W	32-bit	0
56	0xE98E	WWAPTA	To set offset calibration of the total active power of Phase A.	R/W	32-bit	0
57	0xE98F	WWAPTB	To set offset calibration of the total active power of Phase B.	R/W	32-bit	0
58	0xE990	WWAPTC	To set offset calibration of the total active power of Phase C.	R/W	32-bit	0
59	0xE991	WWAQTA	To set offset calibration of the total reactive power of Phase A.	R/W	32-bit	0
60	0xE992	WWAQTB	To set offset calibration of the total reactive power of Phase B.	R/W	32-bit	0
61	0xE993	WWAQTC	To set offset calibration of the total reactive power of Phase C.	R/W	32-bit	0
62	0xE994	WWARTIA	To set offset calibration of the total current RMS of Phase A.	R/W	32-bit	0
63	0xE995	WWARTIB	To set offset calibration of the total current RMS of Phase B.	R/W	32-bit	0
64	0xE996	WWARTIC	To set offset calibration of the total current RMS of Phase C.	R/W	32-bit	0
65	0xE997	WWARTIN	To set offset calibration of the total current RMS of Channel IN.	R/W	32-bit	0
66	0xE998	WWARTUA	To set offset calibration of the total voltage RMS of Phase A.	R/W	32-bit	0
67	0xE999	WWARTUB	To set offset calibration of the total	R/W	32-bit	0

No.	Address	Register		R/W	Bits for Checksum Calculation	Default Value
			voltage RMS of Phase B.			
68	0xE99A	WWARTUC	To set offset calibration of the total voltage RMS of Phase C.	R/W	32-bit	0
69	0xE99B		Reserved. It is recommended to write of 0s.	R/W	32-bit	0
70	0xE99C	WWBPTA	To set offset calibration of the fundamental active power of Phase A.	R/W	32-bit	0
71	0xE99D	WWBPTB	To set offset calibration of the fundamental active power of Phase B.	R/W	32-bit	0
72	0xE99E	WWBPTC	To set offset calibration of the fundamental active power of Phase C.	R/W	32-bit	0
73	0xE99F	WWBQTA	To set offset calibration of the fundamental reactive power of Phase A.	R/W	32-bit	0
74	0xE9A0	WWBQTB	To set offset calibration of the fundamental reactive power of Phase B.	R/W	32-bit	0
75	0xE9A1	WWBQTC	To set offset calibration of the fundamental reactive power of Phase C.	R/W	32-bit	0
76	0xE9A2	WWBRTIA	To set offset calibration of the fundamental current RMS of Phase A.	R/W	32-bit	0
77	0xE9A3	WWBRTIB	To set offset calibration of the fundamental current RMS of Phase B.	R/W	32-bit	0
78	0xE9A4	WWBRTIC	To set offset calibration of the fundamental current RMS of Phase C.	R/W	32-bit	0
79	0xE9A5	WWBRTUA	To set offset calibration of the fundamental voltage RMS of Phase A.	R/W	32-bit	0
80	0xE9A6	WWBRTUB	To set offset calibration of the fundamental voltage RMS of Phase B.	R/W	32-bit	0
81	0xE9A7	WWBRTUC	To set offset calibration of the fundamental voltage RMS of Phase C.	R/W	32-bit	0
82	0xEC01	ZZANA0	Analog Control Register 0, is read out as the configuration of ANCtrl0 (0x8000).	R	32-bit	0
83	0xEC02	ZZANA1	Analog Control Register 1, is read out as the configuration of ANCtrl1 (0x8001).	R	32-bit	0

No.	Address	Register		R/W	Bits for Checksum Calculation	Default Value
84	0xEC03	ZZANA2	Analog Control Register 2, is read out as the configuration of ANCtrl2 (0x8002).	R	32-bit	0
85	0xEC04	ZZANA3	Analog Control Register 3, is read out as the configuration of ANCtrl3 (0x8003).	R	32-bit	0
86	0xEC05	ZZAPPA	To select the mode for total/fundamental apparent power on the overall system calculation.	R/W	As a 32-bit register with 29 most significant bits padded with 0s.	0
87	0xEC16	ZZDCIA	To preset the bias current for the current of Phase A.	R/W	As a 32-bit register with bit23 being the sign bit and with sign extended to 32 bits.	0
88	0xEC17	ZZDCIB	To preset the bias current for the current of Phase B.	R/W	As a 32-bit register with bit23 being the sign bit and with sign extended to 32 bits.	0
89	0xEC18	ZZDCIC	To preset the bias current for the current of Phase C.	R/W	As a 32-bit register with bit23 being the sign bit and with sign extended to 32 bits.	0
90	0xEC19	ZZDCIN	To preset the bias current for the current of Channel IN.	R/W	As a 32-bit register with bit23 being the sign bit and with sign extended to 32 bits.	0

No.	Address	Register		R/W	Bits for Checksum Calculation	Default Value
91	0xEC1A	ZZDCUA	To preset the bias current for the voltage of Phase A.	R/W	As a 32-bit register with bit23 being the sign bit and with sign extended to 32 bits.	0
92	0xEC1B	ZZDCUB	To preset the bias current for the voltage of Phase B.	R/W	As a 32-bit register with bit23 being the sign bit and with sign extended to 32 bits.	0
93	0xEC1C	ZZDCUC	To preset the bias current for the voltage of Phase C.	R/W	As a 32-bit register with bit23 being the sign bit and with sign extended to 32 bits.	0
94	0xEC1D	ZZDCUM	To set the threshold for current detection.	R/W	As a 32-bit register with bit23 being the sign bit and with sign extended to 32 bits.	0
95	0xEC1E	ZZEGYTHH	To set the higher 32 bits of the energy threshold.	R/W	As a 32-bit register with 14 most significant bits padded with 0s.	0
96	0xEC1F	ZZEGYTHL	To set the lower 32 bits of the energy threshold.	R/W	32-bit	0
97	0xEC20	ZZIRQ0	IRQ0 interrupt enable register is read out as the configuration of IRQEN0 (0xA000).	R	As a 32-bit register with the 15 most significant bits	0

No.	Address	Register		R/W	Bits for Checksum Calculation	Default Value
					padded with 0s.	
98	0xEC21	ZZIRQ1	IRQ1 interrupt enable register is read out as the configuration of IRQEN1 (0xA001).	R	As a 32-bit register with the 15 most significant bits padded with 0s.	0
99	0xEC23	ZZPA0	To select the power source for the total/fundamental active power on the overall system in Calculation Mode 0.	R/W	As a 32-bit register with the 26 most significant bits padded with 0s.	0
100	0xEC24	ZZPA1	To select the power source for the total/fundamental active power on the overall system in Calculation Mode 1.	R/W	As a 32-bit register with the 26 most significant bits padded with 0s.	0
101	0xEC27	ZZPARA0	Metering control register 0 is read out as the configuration of MTPARA0 (0xC000).	R	32-bit	0
102	0xEC28	ZZPARA1	Metering control register 1 is read out as the configuration of MTPARA1 (0xC001).	R	32-bit	0
103	0xEC29	ZZPARA2	Metering control register 2 is read out as the configuration of MTPARA2 (0xC002).	R	32-bit	0
104	0xEC2A	ZZPARA3	Metering control register 3 is read out as the configuration of MTPARA3 (0xC003).	R	32-bit	0
105	0xEC34	ZZPCF0A	To select the source for CF pulse.	R/W	As a 32-bit register with the 26 most significant bits padded with 0s.	0
106	0xEC47	ZZQA0	To select the power source for the	R/W	As a 32-bit	0

No.	Address	Register		R/W	Bits for Checksum Calculation	Default Value
			total/fundamental reactive power on the overall system in Calculation Mode 0.		register with the 26 most significant bits padded with 0s.	
107	0xEC48	ZZQA1	To select the power source for the total/fundamental reactive power on the overall system in Calculation Mode 1.	R/W	As a 32-bit register with the 26 most significant bits padded with 0s.	0
108						
109						
110						

16.3. Zero-Crossing Interrupts

The V9203 supports to output the sign bit of the fundamental voltage of each phase on the pins ZX0 ~ ZX2: UA on ZX0 (Pin 34), UB on ZX1 (Pin 33), and UC on ZX2 (Pin 32). When a high logic (1) is output on the pins, it indicates the sign is negative; when a low logic (0) is output on the pins, it indicates the sign is positive; when a high-to-low transition is output on the pins, it indicates a zero-crossing from negative to positive is occurring.

When some bits of bit[3:1] are set to 1s, the zero-crossing interrupt is enabled when a zero-crossing from negative to positive is occurring, the flag bits are set to 1s, and high logics are output on the pin IRQ0 /IRQ1 to generate an interrupt to the master MCU.

The interrupt flags can be cleared via SPI communication.

16.4. CF Pulse Output Interrupt

When the CF pulse is output on the pins CF0~CF3, the low-to-high pulse transition can trigger an interrupt on the pin IRQ0 or/and IRQ1 if it is enabled.

The interrupt flag can be cleared via SPI communication.

16.5. Current Detection Interrupt

The current detection circuit in the V9203 supports full wave rectification to the raw waveform of the current output from the DMA_SPI interfaces. And the sampling frequency is 6.4kHz.

If 5 continuous samples of the current wave are higher than the pre-set threshold for current detection in ZZDCUM register (0xEC1D), a current signal is caught, and a current detection interrupt is generated if it was enabled via setting some bits of bit[13:11] to 1s in IRQEN0 (0xA000) or IRQEN1 (0xA001). When the samples of the current wave are lower than the threshold, the interrupt is cleared automatically.

This interrupt can be used to fast detect the current signal in OPM1 (power-off/no-voltage pre-detection mode) and OPM2 (RMS mode).

16.6. Phase Sequence Error Interrupt

The V9203 supports phase sequence detection based on the sequence of the zero-crossing of phase voltage from negative to positive. If the sequence is not from Phase A, to Phase B, and then to Phase C, it indicates a phase sequence error interrupt is occurring. If bit15 of IRQEN0 (0xA000) or IRQEN1 (0xA001) is set to 1, the flag bit is set to "1" when the interrupt is occurring, and an interrupt pulse is output on the pin IRQ0 or IRQ1.

The interrupt flag can be cleared via SPI communication.

This interrupt must be disabled in the 3-phase, 3-wire application.

16.7. SPI Communication Interrupt

When an error occurs on the communication between the V9203 and the master MCU via the SPI interfaces, the SPI communication interrupt is triggered.

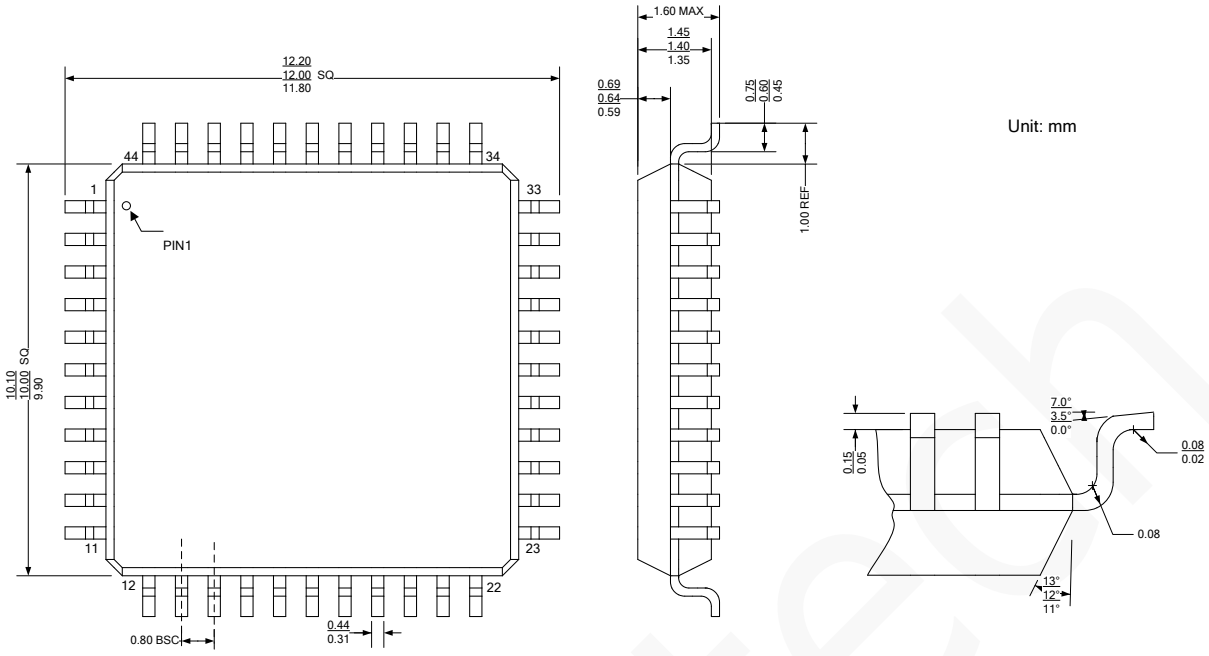
The interrupt flag can be cleared via SPI communication.

16.8. Power-Down Interrupt

When the input on the pin VDCIN is less than 1V, the power supply monitor circuit outputs logic 1 signaling the master MCU that the V9203 has been powered down.

When bit16 of IRQEN0 (0xA000) or IRQEN1 (0xA001) is set to 1, bit16 of IRQFLAG (0xA002) is set bit when the power-down interrupt is triggered, an interrupt is generated to the master MCU, and a high logic is output on the pin IRQ0 (Pin30) or IRQ1 (Pin31).

17. Outline Dimensions



Revision History

Date	Version	Description
2023-12-14	V3.7	Modify the Figure 15-8 Modes for Raw Waveform Output
2023-7-11	V3.6	Supplement the full wave current RMS algebra and register MUN description Delete the zero-crossing output function of the current signal Add SPI mode description Modify the equation for phase compensation
2022-08-13	V3.5	Correct Table 14-15 When the clock frequency of electric energy measurement is 819.2khz, the update time is 160ms; Stabilization time: 1200ms. Delete no-load contents.
2021-07-05	V3.4	Update IEC standard
2019-09-30	V3.3	Modify the energy pulse counter to 32 bits. Modifying the Formula of Phase Measurement.
2019-02-27	V3.2	Delete temperature measurement function.
2018-08-27	V3.1	Add temperature measurement function. Modify the power input voltage to 2.6~3.6V. Modify DVCC output voltage distribution to 2.2~2.7V
2018-07-09	V3.0	Modified the storage Temperature. Modified the power supply management. Modified the pin21(TYPE), must hold high logic for proper operation. Add absolution maximum ratings of analog current input and analog valtage input.
2014-06-23	V2.0	Modified the function description of bit[15:11] of ANCtrl2 (0x8002). Modified the description of phase compensation.
2013-05-10	V1.0	Initial release.