VANGO TECHNOLOGIES, INC.

V85XX
Datasheet

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Revision History

Table1. Document Version History

Date	Revision	Description
2023.03.01	V1.0	Initial Version;
2023.07.13	V1.1	Modify Functional Block Diagram of GPIO Controller. Modify MISC2_EPUCLKCTRL register name. Modify introduction of Comparator Controller. Modify the description about MODE of CRYPT_CTRL register. Modify CAN chapter description.
2024.01.25	V2.0	Modify resistor of EXTRSTN pin to 51K ohm. Modify the description about ACT of CRYPT_CTRL register. Delete CAN. Modify the default value of CRYPT_PRIME register. Modify the default value of FLASH_CSEADDR register. Modify the bit width of the RTC_ACTI register. Modify the description about MISC_HIADDR register. Modify the description about MISC_PIADDR register. Add SPI3 and SPI4. Modify the default value of MISC2_PCLKEN register. Add ANA_REG10 and ANA_REG11 register. Modify the description of ANA_REG4. Modify the description of power
2024.03.22	V3.0	Add V8520
2024.05.31	V3.1	Delete V8520
2024.07.23	V3.2	Update GPIO chapter layout.
2024.11.07	V3.3	Delete the deep sleep function; Delete the RTC automatic temperature compensation function; Correct the electrical characteristic parameters.

General Description

The V85XX series is a highly integrated 32-bit MCU which is suitable for multifunctional and Ultra-low-power IoT product. It is integrated with Cortex-M0 MCU, 256KB Flash, 32KB SRAM, UART/SPI/I2C interface, EPU, RNG, LCD, WDT and RTC. The V85XX series also supports kinds of low-power mode.

Features

- Working voltage: 2.2V ~ 5.5V.
- Working Current:
  - Normal mode: 1.64 mA @6.5536MHz
  - Idle mode: 0.28 mA @6.5536MHz
  - Sleep mode (LCD active, RTC_PSCA=0, VDD=3.3V, AVCCLDO power down): 8.76μA
  - Sleep mode (LCD inactive, RTC_PSCA=0, VDD=3.3V, AVCCLDO power down): 2.89μA
- Package:
  - LQFP100 (V8500)
  - LQFP80 (V8531)
  - LQFP64 (V8510)
- Operation Temperature: -40~+85℃
- Storage Temperature: -55~+150℃
- MCU
  - 32 bits Cortex-M0 with maximum 26.2144MHz operation speed.
  - Single cycle multiplier.
  - Standard 2-wires SWD debug interface.
  - 256KB FLASH with write protect, support both IAP and ISP.
  - 32K bytes SRAM with parity check and data retention under sleep mode.
  - Support abort exception detection including FLASH check-sum error, SRAM parity error, memory address error and memory align error.
- Interface Controller
  - Maximum 6 UART controllers with parity check.
  - Each UART TX channel can be coupled with IR carrier for IR transmission.
  - Maximum 2 ISO7816 controllers.
  - Maximum 4 SPI master/slave controllers.
  - Maximum 1 I2C master/slave controller.
  - 4 32 bits timers.
  - 4 16 bits PWM timers.
  - 4 channels DMA controller.
  - 1 RNG
  - 1 EPU controller with 2 high-speed energy accumulators and 6 low-speed energy

accumulators, support 2-way CF output
- 128/192/256 bits AES CODEC.
- ECC encrypt/decrypt accelerated engine.
- Dual frame buffer LCD controller
  - ✓ V8500: 4COM/6COM/8COM.
  - ✓ V8531: 4COM/6COM/8COM.
  - ✓ V8510: 4COM/6COM/8COM.
  - ✓ 1/3 or 1/4 bias.
  - ✓ Support multi-kinds of scan frequency.
  - ✓ LCD voltage: The default output is about 3.3V. Adjustment range: 2.7~3.6V, 0.06V per step.
- Watch dog timers with programmable period.
- Support multiple wake-up sources under each mode.
- Maximum 82 GPIOs.
- Maximum 16 GPIOs can be external interrupt and wakeup sources under all modes.

- Analog Controller
  - 16bits ADC with 10Ksps.
  - Maximum 8 external input.
  - ADC supports manual sample mode or auto sample mode.
  - Maximum 2 comparators with single end input or differential input.
  - Embedded 32KHz and 6.5MHz RCO.
  - Embedded 2 PLLs.
  - Support external 32.768KHz crystal or 6.5536MHz crystal (optional).
  - Support crystal absent detect for both 32.768KHz and 6.5536MHz crystal.
  - Each clock can be selected to be system clock.
  - Support digital clock divider up-to 1/256.
  - Support low voltage detection with programmable level.
  - Support power-on reset for both AVCC and DVCC.
  - Support VDD, VDCIN, VDD, BATRTC, AVCC, DVCC voltage detection.

Table2. V85XX series product

	V8500	V8531	V8510
ADC channel	8	8	4
UART	6	6	5
UART32K	2	2	2
ISO7816	2	2	2
SPI	4	4	4
I2C	1	1	1
Comparator	2	2	1
GPIO	82	71	53
External interrupt IO	16	16	15
32-bit Timer	4	4	4
16-bit PWM Timer	4	4	4
PWM out	4	4	4
DMA channel	4	4	4
RNG	1	1	1
EPU	1	1	1
LCD	76x4, 74x6, 72x8	65x4, 63x6, 61x8	49x4, 47x6, 45x8
FLASH	256KB	256KB	256KB
SRAM	32KB	32KB	32KB
Package type	100-LQFP	80-LQFP	64-LQFP

1 Electrical Characteristics

Unless otherwise specified, all voltages are referenced to V_{SS}.

1.1 Absolute Maximum Ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table3. Absolute Maximum Ratings

Symbol	Ratings	Min	Max	Unit
V_{VDD}-V_{SS}	External supply voltage	-0.3	+5.8	V
V_{IN}-V_{SS}	External signal input to GPIO pins.	-0.3	+5.8	V
S_{VDD}	VDD power-on speed	5V/sec	1V/usec	--
I_{INJ_PAD}	Single pin input injection current	-10	+10	mA
I_{INJ_SUM}	Sum of all input injected current	-50	+40	mA
T_W	Working temperature range	-40	+85	℃
T_S	Storage temperature	-55	+150	℃
T_J	PN junction temperature	-40	+125	℃

1.2 Normal Operating Voltage

Table4. Operating Voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IN,VDD}$	Input voltage range of VDD		2.2	3.3/5	5.5	V

1.3 Driving Capability Characteristics

Table5. Driving Condition of Power PINs

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{DRV,VDD}$	Driving Capability of VDD				40 (1)	mA
$I_{DRV,AVCC}$	Driving Capability of AVCC				30	mA
$I_{DRV,DVCC}$	Driving Capability of DVCC				35	mA
$I_{DRV,AVCCOUT}$	Driving Capability of AVCC_OUT				20 (2)	mA

Note1: Driving current of VDD include peripheral loads and loads at AVCC, DVCC and AVCC_OUT.

Note2: The sum of the driving capability of AVCC pin and AVCC_OUT pin cannot exceed 30mA.

1.4 Switching resistance of Power PIN

Table6. Switching Resistance of Power PIN

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{on,\ VDD2AVCC}$	Switch-on Resistance between VDD and AVCC when power down AVCCLDO	VDD=3.3V, IL (1) <30mA	6.5	7.3	9.0	ohm

Note1: Load current on AVCC.

1.5 Power consumption

Table7. General Operating Conditions

Symbol	Parameter	Conditions (CRPTY off, VDD=3.3V, AVCCLDO power off)	Min	Typ	Max	Unit
I_{ACTIVE}	Active current.	26.2144MHz system clock		4750		μA
		13.1072MHz system clock		2640		
		6.5536MHz system clock		1510		
		3.2768MHz system clock		960		
		1.6384MHz system clock		680		
		819.2kHz system clock		530		
		409.6kHz system clock		440		
		204.8kHz system clock		400		
		32K RC system clock (FLASH deep-standby)		14.9		
		32K RC system clock (power on FLASH)		85.0		
I_{IDLE}	Idle current.	26.2144MHz system clock		779		μA
		13.1072MHz system clock		470		
		6.5536MHz system clock		286		
		3.2768MHz system clock		223		
		1.6384MHz system clock		182		
		819.2kHz system clock		162		
		409.6kHz system clock		152		
		204.8kHz system clock		127		
		32K RC system clock		3.65		
I_{SLP1}	Sleep current at LCD off.	RTCCLK no frequency division		2.89		μA
		RTCCLK 4 frequency		2.7		

		division				
I_{SLP2}	Sleep current at LCD on.	RTCCLK no frequency division		8.76		μA
		RTCCLK 4 frequency division		8.5		

Table8. Power Consumption of Each Module

module	Power consumption(μA)	State (25℃, VDD=3.3V)
CMP 1/2	0.08	IT_CMP=00(Bias current=20nA)
	0.4	IT_CMP=01(Bias current=100nA)
	2	IT_CMP=1*(Bias current=500nA)
VDD/BATRTC voltage detection	1.5	
BGP	108	
ADC	230	
Temp sensor	370	
LCD	5	LCD driving res=600k
	9.9	LCD driving res=300k
	14.5	LCD driving res=200k
	19	LCD driving res=150k
32768 XTAL	0.6	ANA_REG4 = 1 ANA_REG10 &= ~0x80
32K RC	0.2	
6.5M RC	80	
6.5M XTAL	120	
PLL_L	20	
PLL_H	40	
AVCCLDO	1	

1.6 Embedded Reset and Power Control Block Characteristics

Table9. Embedded Reset and Power Control Block Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{RST}	Reset de-bounce time.			20		μS
V_{PORH}	PORH detect voltage (AVCCLDO).		1.9	2.1	2.2	V
V_{VDCIN}	V_{TH+}	Operating temperature	1.5			V
	V_{TH-}	Operating temperature			1.19	
V_{AVCCLV}	AVCCLV detect		2.2	2.5	2.7	V

	level.					
$V_{VDDALRAM}$	VDD supervisor voltage threshold	V_{TH} configurable, V_{TH}=2.9V;	2.73	2.9	3.02	V
AVCC	AVCC voltage		3.1	3.3	3.4	V
LCDLDO	LCDLDO voltage		3.2	3.3	3.4	V

Table10. Hysteresis Voltage Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PORH_HTRES}	PORH detect hysteresis voltage.			66.5		mV
V_{VDCIN_HTRES}	VDCIN detect hysteresis voltage.			42.0		mV
V_{AVCCLV_HTRES}	AVCCLV detect hysteresis voltage.			42.0		mV
$V_{VDDALRAM\_HTRES}$	VDD supervisor hysteresis voltage.	$V_{TH\_VDDALARM}$ = 4.5 V		142.5		mV
		$V_{TH\_VDDALARM}$ = 4.2V		133.0		mV
		$V_{TH\_VDDALARM}$ = 3.9 V		123.5		mV
		$V_{TH\_VDDALARM}$ = 3.6V		114.0		mV
		$V_{TH\_VDDALARM}$ = 3.2 V		101.4		mV
		$V_{TH\_VDDALARM}$ = 2.9 V		91.9		mV
		$V_{TH\_VDDALARM}$ = 2.6 V		82.4		mV
		$V_{TH\_VDDALARM}$ = 2.3 V		72.9		mV

1.7 GPIO Characteristics

Table11. GPIO Characteristics

Symbol	Parameter	V_{VDD}	Conditions	Min	Max	Unit
V_{IH}	Input high voltage	5V		0.7*V_{DD}		V
		3.3V		2		
V_{IL}	Input low voltage	5V			0.3* V_{VDD}	V
		3.3V			0.3* V_{VDD}	V
V_{HSYS}	Schmitt trigger hysteresis	5V		0.1* V_{VDD}		V
		3.3V				
I_{IH}	Input high current	5V			+2	μA
		3.3V				
I_{IL}	Input low current	5V		-2		μA
		3.3V				
V_{OH}	Output high voltage	5V	10mA	V_{VDD} -0.8	V_{VDD}	V
		3.3V	5mA	2.4	V_{VDD}	V

V_{OL}	Output low voltage	5V	10mA		0.5	V
		3.3V	5mA		0.4	V
C_{IN}	Input capacitance	5V			10	pF
		3.3V				

1.8 ADC Characteristics

Table12. ADC Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
BGPREF	BGP Voltage		1.18	1.2	1.22	V
PSRR	Power Supply Rejection Ratio of BGP			-55		dB
V_{ADC}	ADC operation voltage		2.7	3.3	3.6	V
I_{ADC}	ADC operation current.		170	230	350	μA
f_{ADCLK}	ADC sampling clock.			1.6384		MHz
C_{ADC}	Internal sample and hold capacitance.			1		pF
INL	Integral Nonlinearity			2		LSB
DNL	Differential Nonlinearity			1		LSB
Offset	Offset error			5		mV
$V_{WITHSTAND}$	Withstand voltage (input of ADC Channel)		-0.3		VDD	V

1.9 Comparator Characteristics

Table13. Comparator Characteristics

Symbol	Parameter	Conditions (25℃)	Min	Typ	Max	Unit
V_{CMP}	Comparator operation voltage (AVCC)		2.2	3.3	3.6	V
I_{CMP}	Comparator operation current.	Input bias current 20nA, input 50kHz square wave.		0.08		μA
		Input bias current 100nA, input 50kHz square wave.		0.4		μA
		Input bias current 500nA, input 50kHz square wave.		2		μA
td	Propagation delay	Input bias current 20nA, input 50kHz square wave.		1.6		μS

		Input bias current 100nA, input 50kHz square wave.		0.63		μS
		Input bias current 500nA, input 50kHz square wave.		0.27		μS
V_{CMPIN}	Comparator input voltage range.		0.8		VDD-0.3	V
V_{CMPREF}	Comparator reference voltage	Reference voltage is VREF	1.222	1.3	1.352	V
		Reference voltage is BGPREF	1.18	1.2	1.22	V
V_{HTRES}	Comparator hysteresis voltage		20.0	25.0	30.0	mV

1.10 Clock and PLL Characteristics

Table14. Clock and PLL Characteristics

Symbol	Parameter	Conditions (-40~85 ℃)	Min	Typ	Max	Unit
V_{DDPLLL}	PLLL operating voltage (DVCC)		1.35	1.5	1.65	V
$I_{VDDPLLL}$	PLLL operating current			30		μA
V_{DDPLLH}	PLLH operating voltage (DVCC)		1.35	1.5	1.65	V
$I_{VDDPLLH}$	PLLH operating current			40		μA
V_{DDRCL}	RCL operating voltage (AVCC)		2.2	3.3	3.6	V
I_{VDDRCL}	RCL operating current			0.2		μA
f_{RCL}	RCL frequency.		29.7	32	35.5	kHz
V_{DDRCH}	RCH operating voltage (AVCC)		2.2	3.3	3.6	V
I_{VDDRCH}	RCH operating current			45		μA
f_{RCH}	RCH frequency.		6.357	6.5	6.75	MHz
V_{DDXOH}	XOH operating voltage (AVCC)		2.2	3.3	3.6	V
I_{VDDXOH}	XOH operating current			150		μA

f_{XOH}	XOH frequency.			6.5536		MHz

1.11 FLASH and SRAM Characteristics

Table15. FLASH and SRAM Characteristics

Parameter	Conditions	Min	Typ	Max	Unit
FLASH word read access time.		38			ns
FLASH program time	-40~85℃	20000			time
FLASH data retention time	-40~85℃	20			year
FLASH byte program time		6		7.5	μS
FLASH page erase time (512 bytes)		4		5	ms
FLASH chip erase time		30		40	ms
FLASH active read current	26MHz access.		2.5	3.5	mA
FLASH active program current				3.5	mA
FLASH active erase current				2	mA
FLASH standby current			80	150	μA
FLASH deep standby current			0.1	6	μA
SRAM data retention voltage (DVCC)	-40~85℃	1.35	1.5	1.65	V

1.12 ESR Characteristics of Crystal Oscillator

Table16. ESR Characteristics of Crystal Oscillator

Parameter	Conditions (-40~85℃)	Min	Typ	Max	Unit
ESR of 6.5536M crystal oscillator				40	Ω
ESR of 32768K crystal oscillator				50	KΩ

Note1: *ESR (Equivalent series resistance)*

1.13 Stabilization Time of Clock and Wake up Time

Table17. Stabilization Time of Clock and Wake-up Time

Parameter	Conditions (-40~85℃)	Min	Typ	Max	Unit
PLLL lock time				1	ms
PLLH lock time				15	μS
Stabilization time of RCL				200	μS
Stabilization time of RCH				5	μS
Stabilization time of BGP				10	μS
Wake up time from sleep mode when RCH as system clock			18.4		μS
Wake up time from sleep mode when PLLL as system clock			1.03		mS
Wake up time from sleep mode			22.8		μS

when PLLH as system clock					
Interrupt response time in IDLE mode when RCH as system clock			6		μS
Interrupt response time in IDLE mode when PLLL as system clock			1.6		μS
Interrupt response time in IDLE mode when PLLH as system clock			1.6		μS

1.14 ADC Conversion Time

ADC clock frequency, CIC down sampling rate and CIC output skip point number influence the ADC conversion time. Please refer the following tables for the details:

Table18. ADC Conversion Time (ADC clock frequency and CIC down sampling rate are variable)

ADCLK/MHz / CIC down Sample rate / ADC Conversion time/ms	6.5536	3.2768	1.6384	0.8192	0.4096
1/512	0.937	0.937	1.875	3.750	7.500
1/256	0.468	0.468	0.937	1.875	3.750
1/128	0.234	0.234	0.468	0.937	1.875
1/64	0.117	0.117	0.234	0.468	0.937

Other parameter configuration: CICSKIP=6, CIC output skip first two points.

Note1: CIC is 3 order filter in this file, the data is stable when the first two sampling points is ignored.

Note2: $T_{ADC\_CONVERSION} = \frac{1}{\left(R_{CIC\_DownSample} * \frac{f_{ADC}}{2}\right)} * N_{Sample\_Point}$

(except ADC clock equal 6.5536MHz). Example, CIC down sample is 1/512, ADCLK is 3.2768MHz, and skip first two points, then

$T_{ADC\_CONVERSION} = \frac{1}{\left(\frac{1}{512} * \frac{3.2768MHz}{2}\right)} * 3 = 0.937ms$

Table19. ADC Conversion Time (CIC output skip point number is variable)

Parameter	CIC output skip point number	ADC Conversion time	Unit
MADC conversion time	2	1.875	mS
	3	2.520	mS
	4	3.150	mS
	5	3.780	mS
	6	4.410	mS

	7	5.040	mS
Other parameter configuration: CIC down sample is 1/512, ADCLK is 1.6384MHz			

1.15 ESD handling ratings

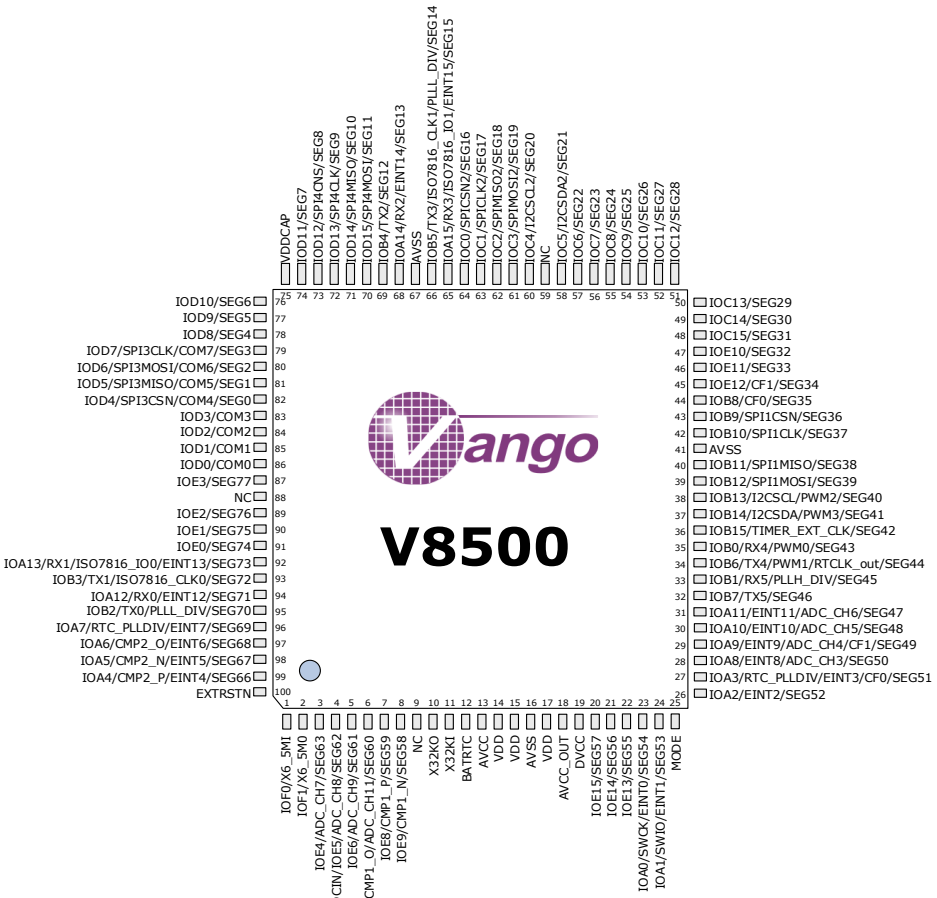
Table20. ESD handling ratings

Parameter	Conditions	Min	Max
HBM	Mil-Std-883J Method 3015.9	-4KV	+4KV
MM	EDEC EIA/JESD22-A115	-300V	+300V
LATCH-UP	JEDEC EIA/JESD78E	-200mA	+200mA

2 Pin Assignments

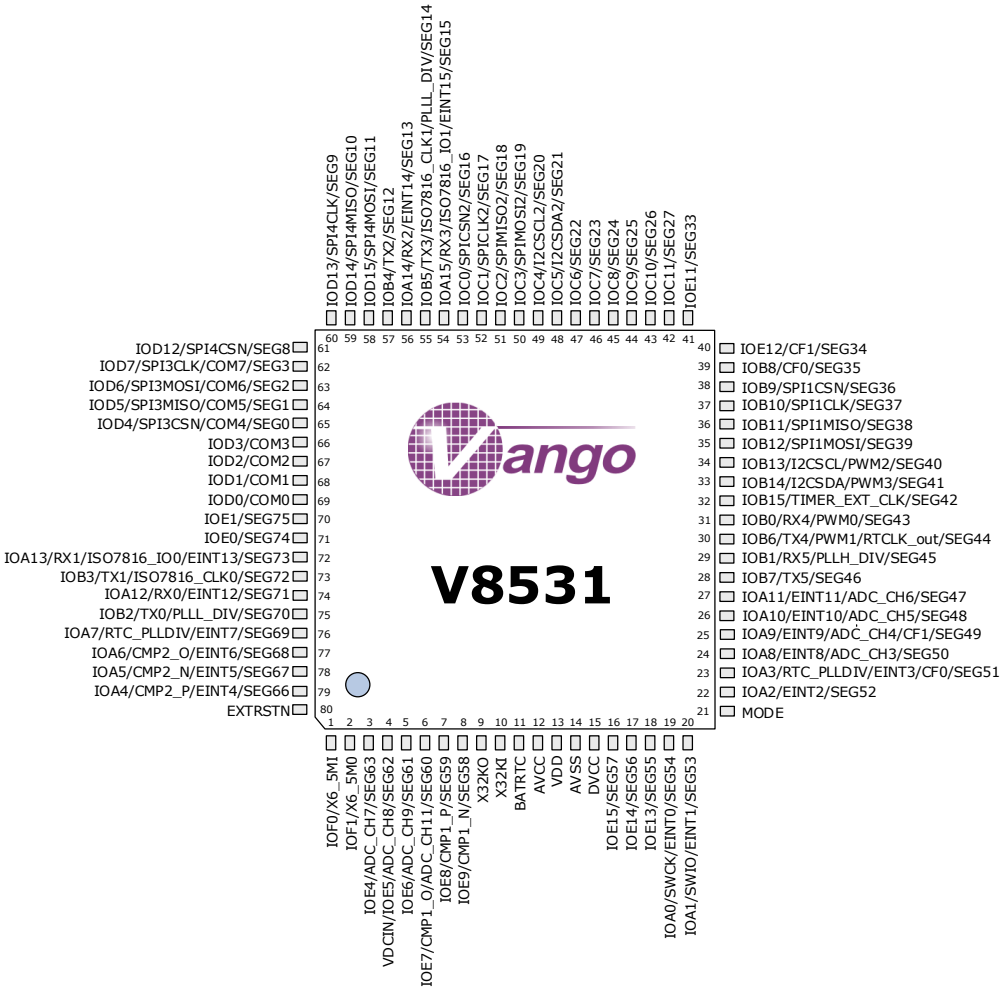
2.1 V8500 Pin Assignments

Figure1. V8500 Pin Assignments



2.2 V8531 Pin Assignments

Figure2. V8531 Pin Assignments



2.3 V8510 Pin Assignments

Figure3. V8510 Pin Assignments

2.4 V85XX Pin Descriptions

Table21. V85XX Pin Descriptions

Pin Number			Pin Name	Type	Description
V8500	V8531	V8510			
1	1		IOF0	I/O	Default: IOF0 Function 1: 6.5536M crystal input
2	2		IOF1	I/O	Default: IOF1 Function 1: 6.5536M crystal output
3	3		IOE4	I/O	Default: IOE4 Function 1: ADC_CH7 input Function 2: SEG63
4	4	2	IOE5	I/O	Default: VDCIN input. Function 1: ADC_CH8 input Function 2: IOE5 Function 3: SEG62
5	5		IOE6	I/O	Default: IOE6 Function 1: ADC_CH9 input Function 2: SEG61
6	6		IOE7	I/O	Default: IOE7 Function 1: Comparator 1 output Function 2: ADC_CH11 input Function 3: SEG60
7	7	3	IOE8	I/O	Default: IOE8 Function 1: Comparator 1 P input Function 2: SEG59
8	8		IOE9	I/O	Default: IOE9 Function 1: Comparator 1 N input Function 2: SEG58
9			NC		No connected.
10	9	4	X32KO	O	32768hz crystal output pin. The internal matching capacitance is 12pF.
11	10	5	X32KI	I	32768hz crystal input pin
12	11	6	BATRTC	I	Input of ADC channel 2 for battery voltage measurement. Positive signal input for comparator.
13	12	7	AVCC	O/P	AVCC output pin, user should connect a 0.1uF and 10uF de-couple capacitor at this pin.
14	13	8	VDD	P	Main VDD power input. User should connect a 0.1uF de-couple capacitor at this pin.
15		9	VDD	P	Main VDD power input

16	14	10	AVSS	G	Analog ground
17		11	VDD	I	Input of ADC channel 1 for battery voltage measurement. Positive signal input for comparator.
18			AVCC_OUT	O	AVCC voltage output pin. This pin has the same electrical level as AVCC, user can be used to drive small power modules.
19	15	12	DVCC	O/P	DVCC output pin, user should connect a 0.1uF and 10uF de-couple capacitor at this pin.
20	16	13	IOE15	I/O	Default: IOE15 Function 2: SEG57
21	17	14	IOE14	I/O	Default: IOE14 Function 2: SEG56
22	18	15	IOE13	I/O	Default: IOE13 Function 2: SEG55
23	19	16	IOA0	I/O	Default: IOA0 (MODE=1), SWCLK(MODE=0) Function 1: EINT0 Function 2: SEG54
24	20	17	IOA1	I/O	Default: IOA1 (MODE=1), SWDIO(MODE=0) Function 1: EINT1 Function 2: SEG53
25	21	18	MODE	I	Debug mode or normal mode selection. 0: Debug mode 1: Normal mode The signal level of this pin should be the same as VDD, and the state of this IO should not change during normal or debug operation.
26	22	19	IOA2	I/O	Default: IOA2 Function 1: EINT2 Function 2: SEG52
27	23	20	IOA3	I/O	Default: IOA3 Function 1: Second pulse output (RTC_PLLDIV output) Function 2: EINT3 Function 3: CF0 Function 4: SEG51
28	24	21	IOA8	I/O	Default: IOA8 Function 1: EINT8 Function 2: ADC_CH3 input Function 3: SEG50
29	25	22	IOA9	I/O	Default: IOA9

					Function 1: EINT9 Function 2: ADC_CH4 input Function 3: CF1 Function 4: SEG49
30	26	23	IOA10	I/O	Default: IOA10 Function 1: EINT10 Function 2: ADC_CH5 input Function 3: SEG48
31	27		IOA11	I/O	Default: IOA11 Function 1: EINT11 Function 2: ADC_CH6 input Function 3: SEG47
32	28		IOB7	I/O	Default: IOB7 Function 1: UART TXD 5 Function 2: SEG46
33	29	24	IOB1	I/O	Default: IOB1 Function 1: UART RXD 5 Function 3: PLLH divider output Function 4: SEG45
34	30	25	IOB6	I/O	Default: IOB6 Function 1: UART TXD 4 Function 2: PWM1 In/Out line Function 3: RTCCLK output Function 4: SEG44
35	31	26	IOB0	I/O	Default: IOB0 Function 1: UART RXD4 Function 2: PWM0 In/Out line Function 3: SEG43
36	32	27	IOB15	I/O	Default: IOB15 Function 1: Timer external clock input Function 2: SEG42
37	33	28	IOB14	I/O	Default: IOB14 Function 1: I2C SDA Function 2: PWM3 In/Out line Function 3: SEG41
38	34	29	IOB13	I/O	Default: IOB13 Function 1: I2C SCL Function 2: PWM2 In/Out line Function 3: SEG40
39	35	30	IOB12	I/O	Default: IOB12 Function 1: SPI1 MOSI Function 2: SEG39
40	36	31	IOB11	I/O	Default: IOB11

					Function 1: SPI1 MISO Function 2: SEG38
41			AVSS	G	Analog ground
42	37	32	IOB10	I/O	Default: IOB10 Function 1: SPI1 CLK Function 2: SEG37
43	38	33	IOB9	I/O	Default: IOB9 Function 1: SPI1 CSN Function 2: SEG36
44	39	34	IOB8	I/O	Default: IOB8 Function 1: CF0 Function 2: SEG35
45	40		IOE12	I/O	Default: IOE12 Function 1: CF1 Function 2: SEG34
46	41		IOE11	I/O	Default: IOE11 Function 1: SEG33
47			IOE10	I/O	Default: IOE10 Function 1: SEG32
48			IOC15	I/O	Default: IOC15 Function 1: SEG31
49			IOC14	I/O	Default: IOC14 Function 1: SEG30
50			IOC13	I/O	Default: IOC13 Function 1: SEG29
51			IOC12	I/O	Default: IOC12 Function 1: SEG28
52	42		IOC11	I/O	Default: IOC11 Function 1: SEG27
53	43		IOC10	I/O	Default: IOC10 Function 1: SEG26
54	44		IOC9	I/O	Default: IOC9 Function 1: SEG25
55	45		IOC8	I/O	Default: IOC8 Function 1: SEG24
56	46		IOC7	I/O	Default: IOC7 Function 1: SEG23
57	47		IOC6	I/O	Default: IOC6 Function 1: SEG22
58	48	35	IOC5	I/O	Default: IOC5 Function 1: I2C SDA (2) Function 2: SEG21
59			NC		No connected.

60	49	36	IOC4	I/O	Default: IOC4 Function 1: I2C SCL (2) Function 2: SEG20
61	50	37	IOC3	I/O	Default: IOC3 Function 1: SPI2 MOSI Function 2: SEG19
62	51	38	IOC2	I/O	Default: IOC2 Function 1: SPI2 MISO Function 2: SEG18
63	52	39	IOC1	I/O	Default: IOC1 Function 1: SPI2 CLK Function 2: SEG17
64	53	40	IOC0	I/O	Default: IOC0 Function 1: SPI2 CSN Function 2: SEG16
65	54	41	IOA15	I/O	Default: IOA15 Function 1: UART RXD 3 Function 2: ISO7816 I/O1 Function 3: EINT15 Function 4: SEG15
66	55	42	IOB5	I/O	Default: IOB5 Function 1: UART TXD 3 Function 2: ISO7816 CLK1 Function 3: PLLL_DIV Function 4: SEG14
67			AVSS	G	Analog ground.
68	56	43	IOA14	I/O	Default: IOA14 Function 1: UART RXD 2 Function 2: EINT14 Function 3: SEG13
69	57	44	IOB4	I/O	Default: IOB4 Function 1: UART TXD 2 Function 2: SEG12
70	58	45	IOD15	I/O	Default: IOD15 Function 1: SEG11 Function 1: SPI4MOSI
71	59	46	IOD14	I/O	Default: IOD14 Function 1: SEG10 Function 1: SPI4MISO
72	60	47	IOD13	I/O	Default: IOD13 Function 1: SEG9 Function 1: SPI4CLK

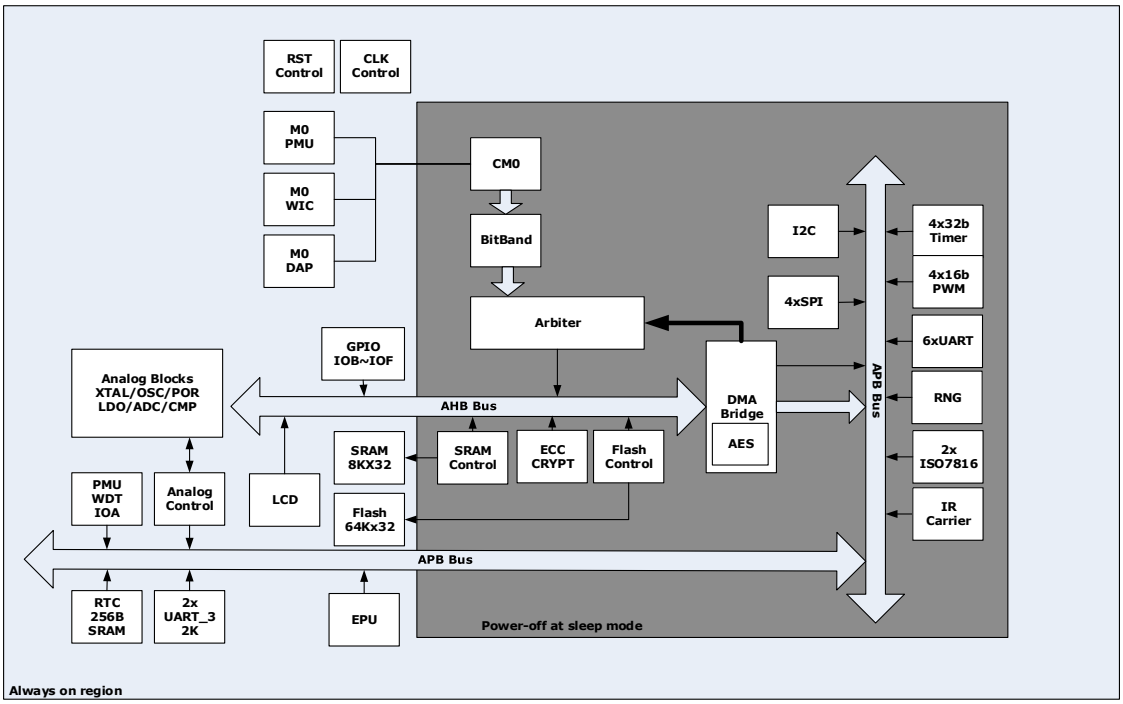
73	61	48	IOD12	I/O	Default: IOD12 Function 1: SEG8 Function 1: SPI4CSN
74			IOD11	I/O	Default: IOD11 Function 1: SEG7
75			VDDCAP	P	Main power supply decoupling pin. It is recommended to connect an external 0.1uF capacitor.
76			IOD10	I/O	Default: IOD10 Function 1: SEG6
77			IOD9	I/O	Default: IOD9 Function 1: SEG5
78			IOD8	I/O	Default: IOD8 Function 1: SEG4
79	62	49	IOD7	I/O	Default: IOD7 Function 1: COM7/SEG3 Function 1: SPI3CLK
80	63	50	IOD6	I/O	Default: IOD6 Function 1: COM6/SEG2 Function 1: SPI3MOSI
81	64	51	IOD5	I/O	Default: IOD5 Function 1: COM5/SEG1 Function 1: SPI3MISO
82	65	52	IOD4	I/O	Default: IOD4 Function 1: COM4/SEG0 Function 1: SPI3CSN
83	66	53	IOD3	I/O	Default: IOD3 Function 1: COM3
84	67	54	IOD2	I/O	Default: IOD2 Function 1: COM2
85	68	55	IOD1	I/O	Default: IOD1 Function 1: COM1
86	69	56	IOD0	I/O	Default: IOD0 Function 1: COM0
87			IOE3	I/O	Default: IOE3 Function 1: SEG77
88			NC		No connected.
89			IOE2	I/O	Default: IOE2 Function 1: SEG76
90	70		IOE1	I/O	Default: IOE1 Function 2: SEG75
91	71		IOE0	I/O	Default: IOE0 Function 2: SEG74

92	72	57	IOA13	I/O	Default: IOA13 Function 1: UART RXD 1 Function 2: ISO7816 I/O 0 Function 3: EINT13 Function 4: SEG73
93	73	58	IOB3	I/O	Default: IOB3 Function 1: UART TXD 1 Function 2: ISO7816 CLK 0 Function 3: SEG72
94	74	59	IOA12	I/O	Default: IOA12 Function 1: UART RXD 0 Function 2: EINT12 Function 3: SEG71
95	75	60	IOB2	I/O	Default: IOB2 Function 1: UART TXD 0 Function 2: PLLL devider output Function 3: SEG70
96	76	61	IOA7	I/O	Default: IOA7 Function 1: Second pulse output (RTC_PLLDIV output) Function 2: EINT7 Function 3: SEG69
97	77	62	IOA6	I/O	Default: IOA6 Function 1: Comparator 2 output Function 2: EINT6 Function 3: SEG68
98	78	63	IOA5	I/O	Default: IOA5 Function 1: Comparator 2 N input Function 2: EINT5 Function 3: SEG67
99	79	64	IOA4	I/O	Default: IOA4 Function 1: Comparator 2 P input Function 2: EINT4 Function 3: SEG66
100	80	1	EXTRSTN	I	External reset pin, low active. It is recommended to connect 51 K ohm resistor and 1 uF capacitor for RC filter circuit.

3 Functional Block Diagram

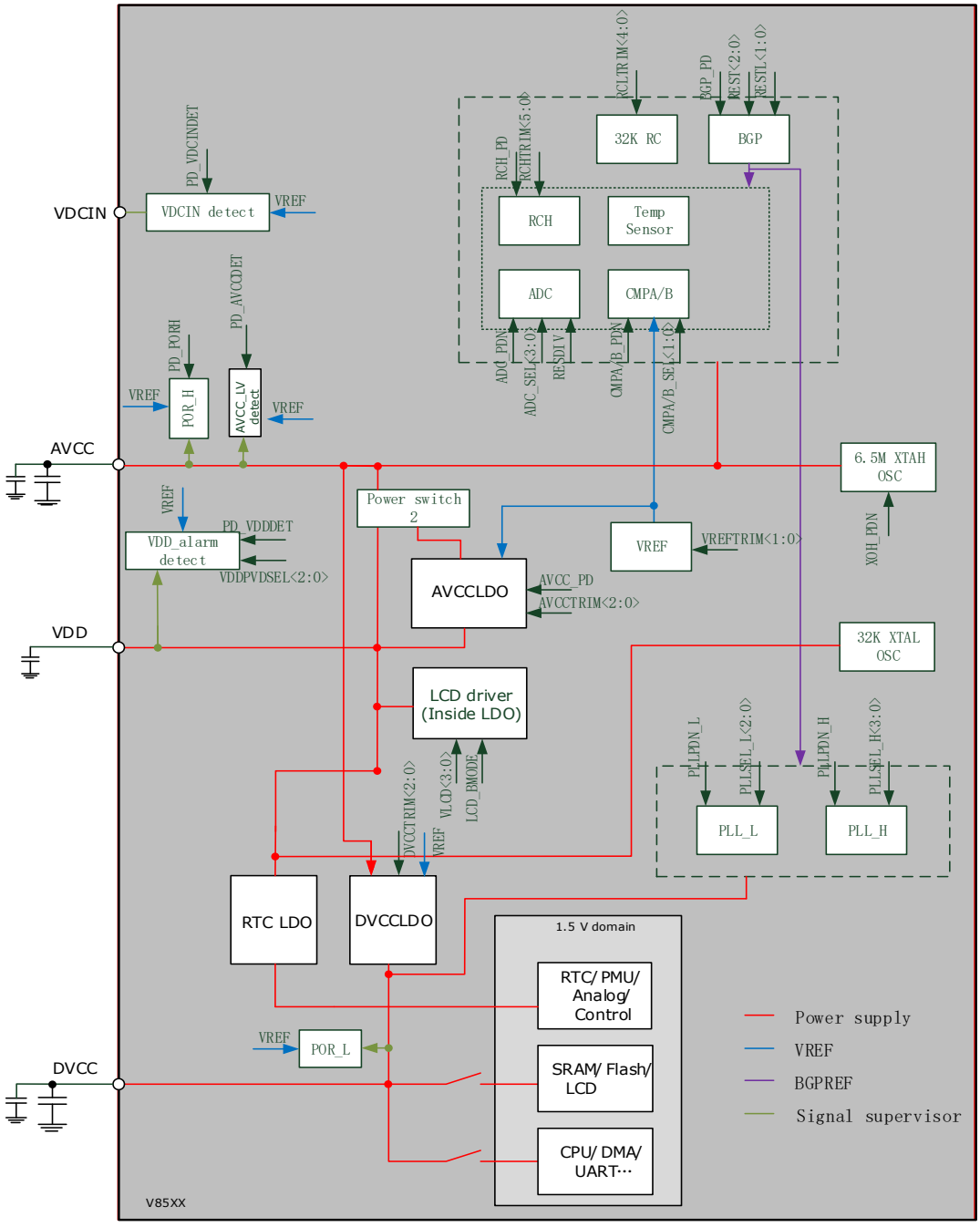
3.1 Functional Block Diagram

Figure4. V85XX Functional Block Diagram



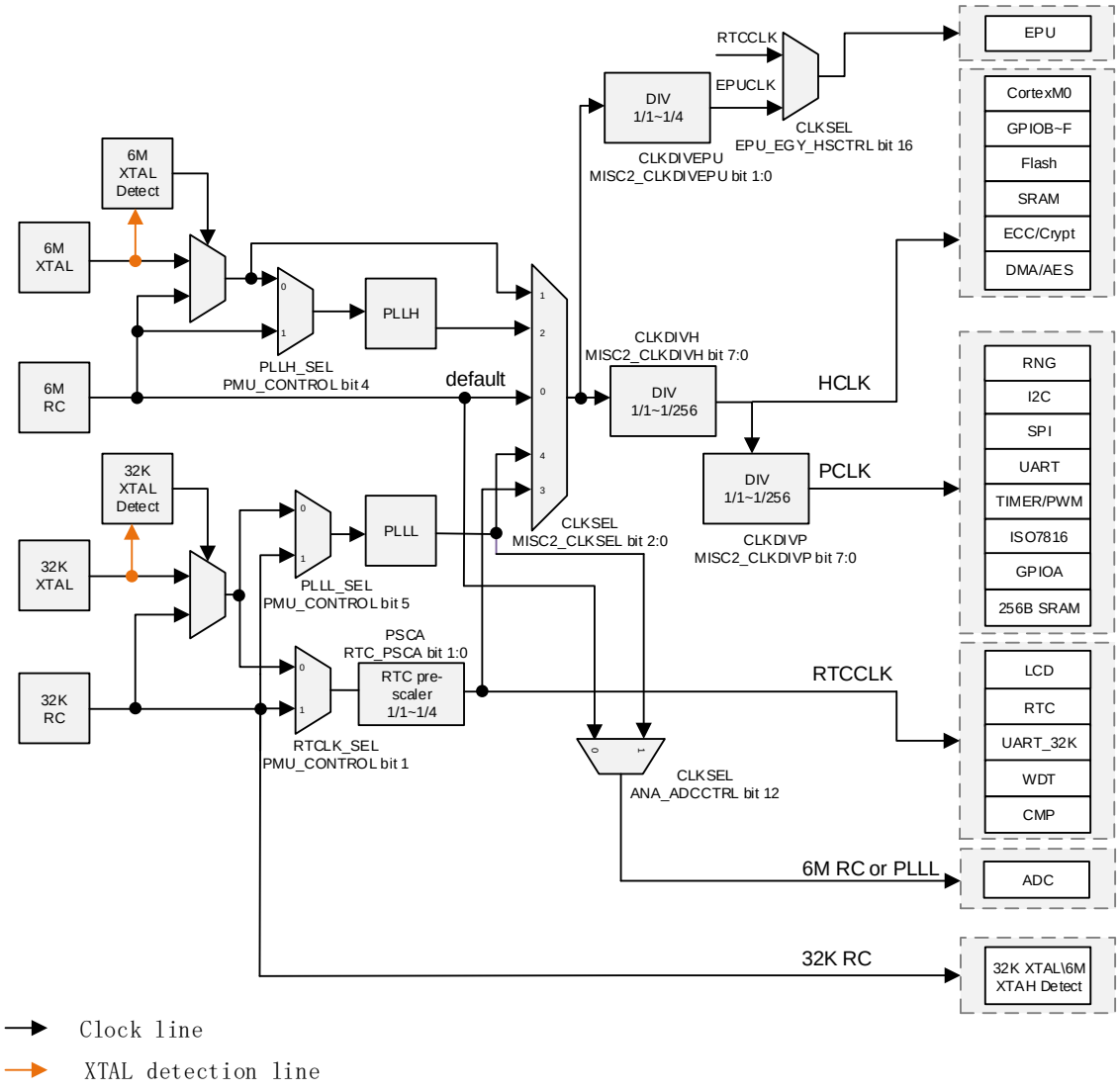
3.2 Power System Block Diagram

Figure5. V85XX Power System Block Diagram



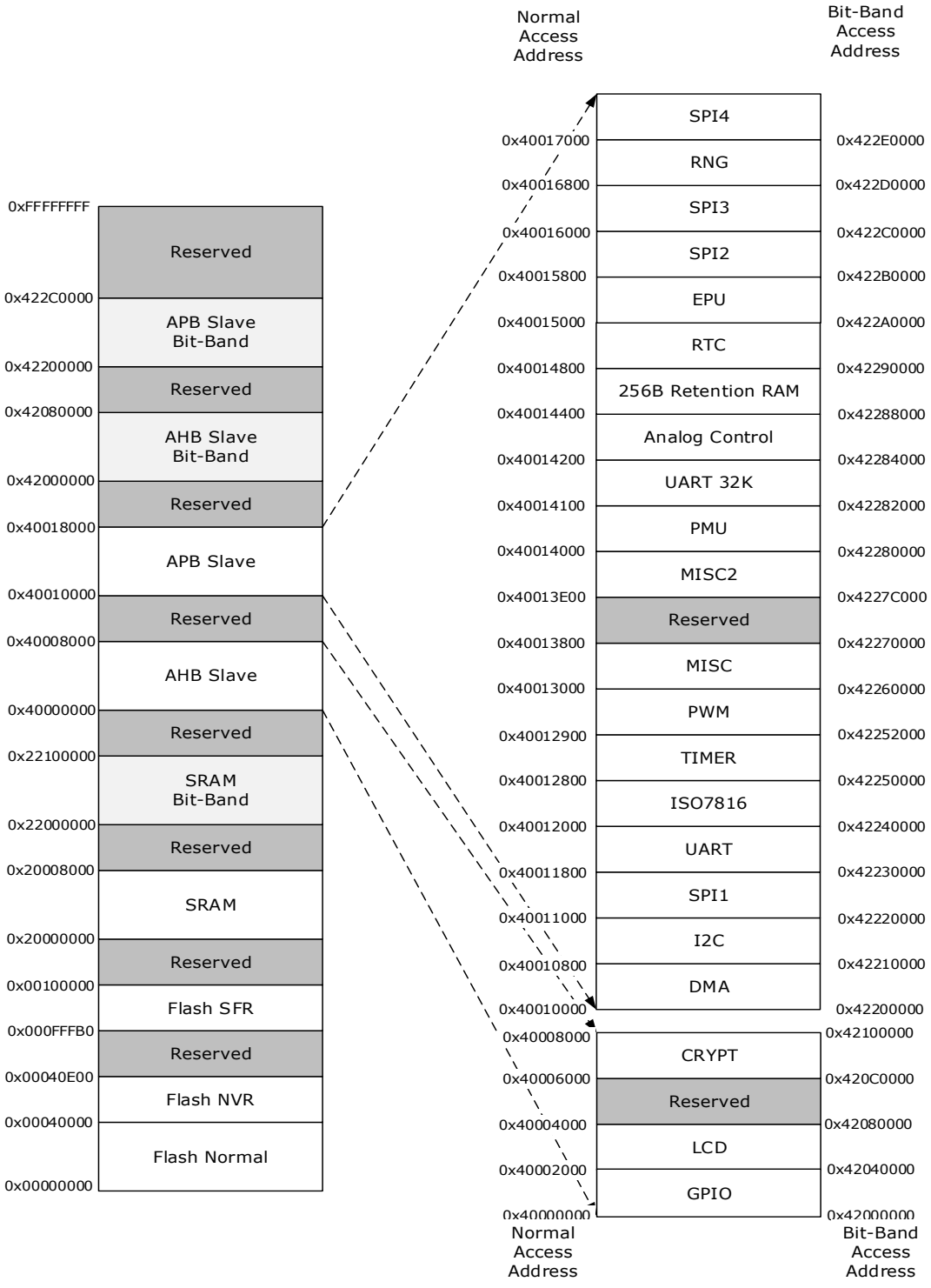
3.3 Clock Block Diagram

Figure6. V85XX Clock Block Diagram



4 Memory Maps

Figure7. V85XX Memory Maps



The bit-band region can only be accessed by Cortex-M0. The DMA controller can't access these regions. For all other regions, they can be accessed by both Cortex-M0 and DMA controller.

Table22. System Memory Map

Address Aread Start	Address Aread End	Size	Peripherals
0x0000_0000	0x0003_FFFF	256K	Flash Normal
0x0004_0000	0x0004_0FFF	4K	FLASH_NVR
0x000F_FF00	0x000F_FFFF	256B	FLASH
0x2000_0000	0x2000_7FFF	32K	SRAM
0x2200_0000	0x220F_FFFF	1M	SRAM Bit-Band
0x4000_0020	0x4000_003F	32B	GPIOB
0x4000_0040	0x4000_005F	32B	GPIOC
0x4000_0060	0x4000_007F	32B	GPIOD
0x4000_0080	0x4000_009F	32B	GPIOE
0x4000_00A0	0x4000_00BF	32B	GPIOF
0x4000_00C0	0x4000_00FF	64B	GPIOAF
0x4000_2000	0x4000_3FFF	8K	LCD
0x4000_6000	0x4000_7FFF	8K	CRYPT
0x4001_0000	0x4001_07FF	2K	DMA
0x4001_0800	0x4001_0FFF	2K	I2C
0x4001_1000	0x4001_17FF	2K	SPI1
0x4001_1800	0x4001_181F	32B	UART0
0x4001_1820	0x4001_183F	32B	UART1
0x4001_1840	0x4001_185F	32B	UART2
0x4001_1860	0x4001_187F	32B	UART3
0x4001_1880	0x4001_189F	32B	UART4
0x4001_18A0	0x4001_18BF	32B	UART5
0x4001_2000	0x4001_203F	64B	ISO78160
0x4001_2040	0x4001_207F	64B	ISO78161
0x4001_2800	0x4001_281F	32B	TMR0
0x4001_2820	0x4001_283F	32B	TMR1
0x4001_2840	0x4001_285F	32B	TMR2
0x4001_2860	0x4001_287F	32B	TMR3
0x4001_2900	0x4001_291F	32B	PWM0
0x4001_2920	0x4001_293F	32B	PWM1
0x4001_2940	0x4001_295F	32B	PWM2
0x4001_2960	0x4001_297F	32B	PWM3
0x4001_29F0	0x4001_29FF	16B	PWMMUX
0x4001_3000	0x4001_37FF	2K	MISC
0x4001_3E00	0x4001_3FFF	512B	MISC2
0x4001_4000	0x4001_40FF	256B	PMU
0x4001_4100	0x4001_417F	128B	U32K0
0x4001_4180	0x4001_41FF	128B	U32K1
0x4001_4200	0x4001_43FF	512B	ANA
0x4001_4400	0x4001_44FF	256B	RETRAM

0x4001_4800	0x4001_4FFF	2K	RTC
0x4001_5000	0x4001_57FF	2K	EPU
0x4001_5800	0x4001_5FFF	2K	SPI2
0x4001_6800	0x4001_6FFF	2K	RNG

4.1 Register Location

4.1.1 PMU Register Location

Table23. Register Location of the PMU Controller (PMU Base: 0x40014000)

Name	Type	Address	Description	Default
PMU_CONTROL	rw	0x0008	PMU control register	0x0000
PMU_STS	rc_w1	0x000C	PMU Status register	0x0000074
PMU_IOAOEN	rw	0x0010	IOA output enable register	0xFFFF
PMU_IOAIE	rw	0x0014	IOA input enable register	0xFFFF
PMU_IOADAT	rw	0x0018	IOA data register	0x0000
PMU_IOAATT	rw	0x001C	IOA attribute register	0x0000
PMU_IOAWKUEN	rw	0x0020	IOA wake-up enable register	0x00000000
PMU_IOASTS	r	0x0024	IOA input status register	--
PMU_IOAINTSTS	rc_w1	0x0028	IOA interrupt status register	0x0000
PMU_IOASEL	rw	0x0038	IOA special function select register	0x0000
VERSIONID	r	0x003C	Version ID of V85XX	--
PMU_WDTPASS	rw	0x0040	Watch dog timing unlock register	0x00000000
PMU_WDTEN	rw	0x0044	Watch dog timer enable register	0x1
PMU_WDTCLR	w	0x0048	Watch dog timer clear register	0x0000
PMU_IOANODEG	rw	0x0050	IOA no-deglitch control register.	0x0000
PMU_WDTSTS	rc_w1	0x0060	Watch dog timer status register.	0x00

Table24. Register Location of the PMU Controller (PMU Retention RAM Base: 0x40014400)

Name	Type	Address	Description	Default
PMU_RAM0	rw	0x0000	PMU 32 bits Retention RAM 0	--
PMU_RAM1	rw	0x0004	PMU 32 bits Retention RAM 1	--
PMU_RAM2	rw	0x0008	PMU 32 bits Retention RAM 2	--
…	…	…	…	
PMU_RAM63	rw	0x00FC	PMU 32 bits Retention RAM 63	--

4.1.2 ANA Register Location

Table25. Register Location of ANA Controller (ANA Base: 0x40014200)

Name	Type	Address	Description	Default
ANA_REG0	rw	0x0000	Analog register 0	0x00
ANA_REG1	rw	0x0004	Analog register 1	0x00
ANA_REG2	rw	0x0008	Analog register 2	0x00
ANA_REG3	rw	0x000C	Analog register 3	0x00
ANA_REG4	rw	0x0010	Analog register 4	0x00
ANA_REG5	rw	0x0014	Analog register 5	0x00
ANA_REG6	rw	0x0018	Analog register 6	0x00
ANA_REG7	rw	0x001C	Analog register 7	0x00
ANA_REG8	rw	0x0020	Analog register 8	0x00
ANA_REG9	rw	0x0024	Analog register 9	0x00
ANA_REGA	rw	0x0028	Analog register 10	0x00
ANA_REGB	rw	0x002C	Analog register 11	From FLASH
ANA_REGC	rw	0x0030	Analog register 12	From FLASH
ANA_REGD	rw	0x0034	Analog register 13	From FLASH
ANA_REGE	rw	0x0038	Analog register 14	From FLASH
ANA_REGF	rw	0x003C	Analog register 15	0x00
ANA_REG10	rw	0x0040	Analog register 16	From FLASH
ANA_REG11	rw	0x0044	Analog register 17	From FLASH
ANA_CTRL	rw	0x0050	Analog control register	0x0000000
ANA_CMPOUT	r	0x0054	Comparator result register	0x0030
ANA_INTSTS	rc_w1	0x0060	Analog interrupt status register	0x0000
ANA_INTEN	rw	0x0064	Analog interrupt enable register	0x0000
ANA_ADCCTRL	rw	0x0068	ADC control register	0x00000000
ANA_ADCDATA0	r	0x0070	ADC channel 0 data register	--
ANA_ADCDATA1	r	0x0074	ADC channel 1 data register	--
ANA_ADCDATA2	r	0x0078	ADC channel 2 data register	--
ANA_ADCDATA3	r	0x007C	ADC channel 3 data register	--
ANA_ADCDATA4	r	0x0080	ADC channel 4 data register	--
ANA_ADCDATA5	r	0x0084	ADC channel 5 data register	--
ANA_ADCDATA6	r	0x0088	ADC channel 6 data register	--
ANA_ADCDATA7	r	0x008C	ADC channel 7 data register	--
ANA_ADCDATA8	r	0x0090	ADC channel 8 data register	--
ANA_ADCDATA9	r	0x0094	ADC channel 9 data register	--
ANA_ADCDATAA	r	0x0098	ADC channel 10 data register	--
ANA_ADCDATAB	r	0x009C	ADC channel 11 data register	--
ANA_CMPCNT1	rc_w1	0x00B0	Comparator 1 counter	0x00000000
ANA_CMPCNT2	rc_w1	0x00B4	Comparator 2 counter	0x00000000

4.1.3 RTC Register Location

Table26. Register Location of RTC Controller (RTC Base: 0x40014800)

Name	Type	Address	Description	Default	Write Protect	Read Protect
RTC_SEC	rw	0x0000	RTC second register	--	V	V
RTC_MIN	rw	0x0004	RTC minute register	--	V	V
RTC_HOUR	rw	0x0008	RTC hour register	--	V	V
RTC_DAY	rw	0x000C	RTC day register	--	V	V
RTC_WEEK	rw	0x0010	RTC week-day register	--	V	V
RTC_MON	rw	0x0014	RTC month register	--	V	V
RTC_YEAR	rw	0x0018	RTC year register	--	V	V
RTC_WKUSEC	rw	0x0020	RTC wake-up second register	0x00	V	
RTC_WKUMIN	rw	0x0024	RTC wake-up minute register	0x00	V	
RTC_WKUHOUR	rw	0x0028	RTC wake-up hour register	0x00	V	
RTC_WKUCNT	rw	0x002C	RTC wake-up counter register	0x0000000	V	
RTC_CAL	rw	0x0030	RTC calibration register	--	V	
RTC_DIV	rw	0x0034	RTC PLL divider register	0x0000000		
RTC_CTL	rw	0x0038	RTC PLL divider control register	0x0		
RTC_PWD	rw	0x0044	RTC password control register	0x00000000		
RTC_CE	rw	0x0048	RTC write enable control register	0x0		
RTC_LOAD	rw	0x004C	RTC read enable control register	--		
RTC_INTSTS	rw	0x0050	RTC interrupt status control register	0x000		
RTC_INTEN	rw	0x0054	RTC interrupt enable control register	0x000		
RTC_PSCA	rw	0x0058	RTC clock pre-scaler control register	0x0	V	
RTC_ACTI	rw	0x0084	RTC calibration center temperature control register	0x1800	V	
RTC_ACF200	rw	0x0088	RTC calibration 200*frequency control register	0x640000	V	

RTC_ACADCW	rw	0x008C	RTC calibration manual ADC value control register	0x0000	V	
RTC_ACP0	rw	0x0090	RTC calibration parameter 0 control register	0x0000	V	
RTC_ACP1	rw	0x0094	RTC calibration parameter 1 control register	0x0000	V	
RTC_ACP2	rw	0x0098	RTC calibration parameter 2 control register	0x0000	V	
RTC_ACP3	r	0x009C	RTC calibration parameter 3 control register	0x0000		
RTC_ACP4	rw	0x00A0	RTC calibration parameter 4 control register	0x0000	V	
RTC_ACP5	rw	0x00A4	RTC calibration parameter 5 control register	0x0000	V	
RTC_ACP6	rw	0x00A8	RTC calibration parameter 6 control register	0x0000	V	
RTC_ACP7	rw	0x00AC	RTC calibration parameter 7 control register	0x0000	V	
RTC_ACK1	rw	0x00B0	RTC calibration parameter k1 control register	0x0000	V	
RTC_ACK2	rw	0x00B4	RTC calibration parameter k2 control register	0x0000	V	
RTC_ACK3	rw	0x00B8	RTC calibration parameter k3 control register	0x0000	V	
RTC_ACK4	rw	0x00BC	RTC calibration parameter k4 control register	0x0000	V	
RTC_ACK5	rw	0x00C0	RTC calibration parameter k5 control register	0x0000	V	
RTC_ACTEMP	r	0x00C4	RTC calibration	0x0000	V	

			calculated temperature register			
RTC_ACPPM	r	0x00C8	RTC calibration calculated PPM register	0x0000	V	
RTC_WKUCNTR	r	0x00CC	This register is used to represent the current WKUCNT value	0x000000	V	
RTC_ACKTEMP	rw	0x00D0	RTC calibration k temperature section control register	0x3C2800EC	V	

4.1.4 FLASH Register Location

Table27. Register Location of FLASH Controller (FLASH Controller Base: 0x00000000)

Name	Type	Address	Description	Default
FLASH_STS	r	0xFFFBC	FLASH programming status register	0x00
FLASH_INT	rc_w1	0xFFFCC	FLASH Checksum interrupt status	0x0
FLASH_CSSADDR	rw	0xFFFD0	FLASH Checksum start address	0x00000
FLASH_CSEADDR	rw	0xFFFD4	FLASH Checksum end address	0x3FFFC
FLASH_CSVALUE	r	0xFFFD8	FLASH Checksum value register	--
FLASH_CSCVALUE	rw	0xFFFDC	FLASH Checksum compare value register	0x00000000
FLASH_PASS	rw	0xFFFE0	FLASH password register	0x00000000
FLASH_CTRL	rw	0xFFFE4	FLASH control register	0x0
FLASH_PGADDR	rw	0xFFFE8	FLASH program address register	0x00000
FLASH_PGDATA	rw	0xFFFEC	FLASH program word data register	--
FLASH_PGB0	rw	0xFFFEC	FLASH program byte data register 0	--
FLASH_PGB1	rw	0xFFFED	FLASH program byte data register 1	--
FLASH_PGB2	rw	0xFFFEE	FLASH program byte data register 2	--
FLASH_PGB3	rw	0xFFFEF	FLASH program byte data register 3	--
FLASH_PGHW0	rw	0xFFFEC	FLASH program half-word data register 0	--
FLASH_PGHW1	rw	0xFFFEE	FLASH program half-word data register 1	--
FLASH_SERASE	rw	0xFFFF4	FLASH sector erase control register	0x00000000
FLASH_CERASE	rw	0xFFFF8	FLASH chip erase control register	0x00000000
FLASH_DSTB	rw	0xFFFFC	FLASH deep standby control register	0x00000000

4.1.5 GPIO Register Location

Table28. Register Location of GPIO Controller (GPIO Base: 0x40000000)

Name	Type	Address	Description	Default

IOB_OEN	rw	0x0020	IOB output enable register	0xFFFF
IOB_IE	rw	0x0024	IOB input enable register	0xFFFF
IOB_DAT	rw	0x0028	IOB data register	0x0000
IOB_ATT	rw	0x002C	IOB attribute register	0x0000
IOB_STS	r	0x0030	IOB input status register	--
IOC_OEN	rw	0x0040	IOC output enable register	0xFFFF
IOC_IE	rw	0x0044	IOC input enable register	0xFFFF
IOC_DAT	rw	0x0048	IOC data register	0x0000
IOC_ATT	rw	0x004C	IOC attribute register	0x0000
IOC_STS	r	0x0050	IOC input status register	--
IOD_OEN	rw	0x0060	IOD output enable register	0xFFFF
IOD_IE	rw	0x0064	IOD input enable register	0xFFFF
IOD_DAT	rw	0x0068	IOD data register	0x0000
IOD_ATT	rw	0x006C	IOD attribute register	0x0000
IOD_STS	r	0x0070	IOD input status register	--
IOE_OEN	rw	0x0080	IOE output enable register	0xFFFF
IOE_IE	rw	0x0084	IOE input enable register	0xFFFF
IOE_DAT	rw	0x0088	IOE data register	0x0000
IOE_ATT	rw	0x008C	IOE attribute register	0x0000
IOE_STS	r	0x0090	IOE input status register	--
IOF_OEN	rw	0x00A0	IOF output enable register	0x1F
IOF_IE	rw	0x00A4	IOF input enable register	0x1F
IOF_DAT	rw	0x00A8	IOF data register	0x0
IOF_ATT	rw	0x00AC	IOF attribute register	0x0
IOF_STS	r	0x00B0	IOF input status register	--
IOB_SEL	rw	0x00C0	IOB special function select register	0x00
IOE_SEL	rw	0x00CC	IOE special function select register	0x00
IO_MISC	rw	0x00E0	IO misc. control register	0x00

4.1.6 DMA Register Location

Table29. Register Location of DMA Controller (DMA Base: 0x40010000)

Name	Type	Address	Description	Default
DMA_IE	rw	0x0000	DMA interrupt enable register	0x000
DMA_STS	rw	0x0004	DMA status register	0x0000
DMA_C0CTL	rw	0x0010	DMA channel 0 control register	0x00000000
DMA_C0SRC	rw	0x0014	DMA channel 0 source register	0x00000000
DMA_C0DST	rw	0x0018	DMA channel 0 destination register	0x00000000
DMA_C0LEN	r	0x001C	DMA channel 0 transfer length register	0x0000
DMA_C1CTL	rw	0x0020	DMA channel 1 control register	0x00000000

DMA_C1SRC	rw	0x0024	DMA channel 1 source register	0x00000000
DMA_C1DST	rw	0x0028	DMA channel 1 destination register	0x00000000
DMA_C1LEN	r	0x002C	DMA channel 1 transfer length register	0x0000
DMA_C2CTL	rw	0x0030	DMA channel 2 control register	0x00000000
DMA_C2SRC	rw	0x0034	DMA channel 2 source register	0x00000000
DMA_C2DST	rw	0x0038	DMA channel 2 destination register	0x00000000
DMA_C2LEN	r	0x003C	DMA channel 2 transfer length register	0x0000
DMA_C3CTL	rw	0x0040	DMA channel 3 control register	0x00000000
DMA_C3SRC	rw	0x0044	DMA channel 3 source register	0x00000000
DMA_C3DST	rw	0x0048	DMA channel 3 destination register	0x00000000
DMA_C3LEN	r	0x004C	DMA channel 3 transfer length register	0x0000
DMA_AESCTL	rw	0x0050	DMA AES control register	0x00000000
DMA_AESKEY0	rw	0x0060	DMA AES key 0 register	0x00000000
DMA_AESKEY1	rw	0x0064	DMA AES key 1 register	0x00000000
DMA_AESKEY2	rw	0x0068	DMA AES key 2 register	0x00000000
DMA_AESKEY3	rw	0x006C	DMA AES key 3 register	0x00000000
DMA_AESKEY4	rw	0x0070	DMA AES key 4 register	0x00000000
DMA_AESKEY5	rw	0x0074	DMA AES key 5 register	0x00000000
DMA_AESKEY6	rw	0x0078	DMA AES key 6 register	0x00000000
DMA_AESKEY7	rw	0x007C	DMA AES key 7 register	0x00000000

4.1.7 UART Register Location

Table30. Register Location of UART Controller (UART Base: 0x40011800)

Name	Type	Address	Description	Default
UART0_DATA	rw	0x0000	UART0 data register	0x00
UART0_STATE	rc_w1	0x0004	UART0 status register	0x00
UART0_CTRL	rw	0x0008	UART0 control register	0x000
UART0_INTSTS	rc_w1	0x000C	UART0 interrupt status register	0x00
UART0_BAUDDIV	rw	0x0010	UART0 baud rate divide register	0x00000
UART0_CTRL2	rw	0x0014	UART0 control register 2	0x0
UART1_DATA	rw	0x0020	UART1 data register	0x00
UART1_STATE	rc_w1	0x0024	UART1 status register	0x00
UART1_CTRL	rw	0x0028	UART1 control register	0x000
UART1_INTSTS	rc_w1	0x002C	UART1 interrupt status register	0x00
UART1_BAUDDIV	rw	0x0030	UART1 baud rate divide register	0x00000

UART1_CTRL2	rw	0x0034	UART1 control register 2	0x0
UART2_DATA	rw	0x0040	UART2 data register	0x00
UART2_STATE	rc_w1	0x0044	UART2 status register	0x00
UART2_CTRL	rw	0x0048	UART2 control register	0x000
UART2_INTSTS	rc_w1	0x004C	UART2 interrupt status register	0x00
UART2_BAUDDIV	rw	0x0050	UART2 baud rate divide register	0x00000
UART2_CTRL2	rw	0x0054	UART2 control register 2	0x0
UART3_DATA	rw	0x0060	UART3 data register	0x00
UART3_STATE	rc_w1	0x0064	UART3 status register	0x00
UART3_CTRL	rw	0x0068	UART3 control register	0x000
UART3_INTSTS	rc_w1	0x006C	UART3 interrupt status register	0x00
UART3_BAUDDIV	rw	0x0070	UART3 baud rate divide register	0x00000
UART3_CTRL2	rw	0x0074	UART3 control register 2	0x0
UART4_DATA	rw	0x0080	UART4 data register	0x00
UART4_STATE	rc_w1	0x0084	UART4 status register	0x00
UART4_CTRL	rw	0x0088	UART4 control register	0x000
UART4_INTSTS	rc_w1	0x008C	UART4 interrupt status register	0x00
UART4_BAUDDIV	rw	0x0090	UART4 baud rate divide register	0x00000
UART4_CTRL2	rw	0x0094	UART4 control register 2	0x0
UART5_DATA	rw	0x00A0	UART5 data register	0x00
UART5_STATE	rc_w1	0x00A4	UART5 status register	0x00
UART5_CTRL	rw	0x00A8	UART5 control register	0x000
UART5_INTSTS	rc_w1	0x00AC	UART5 interrupt status register	0x00
UART5_BAUDDIV	rw	0x00B0	UART5 baud rate divide register	0x00000
UART5_CTRL2	rw	0x00B4	UART5 control register 2	0x0

4.1.8 UART 32K Register Location

Table31. Register Location of UART 32K Controller (UART 32K 0 Base: 0x40014100)

Name	Type	Address	Description	Default
U32K0_CTRL0	rw	0x0000	UART 32K 0 control register 0	0x00
U32K0_CTRL1	rw	0x0004	UART 32K 0 control register 1	0x00
U32K0_PHASE	rw	0x0008	UART 32K 0 baud rate control register	0x4B00
U32K0_DATA	r	0x000C	UART 32K 0 receive data buffer	--
U32K0_STS	rc_w1	0x0010	UART 32K 0 interrupt status register	0x00
U32K1_CTRL0	rw	0x0080	UART 32K 1 control register 0	0x00
U32K1_CTRL1	rw	0x0084	UART 32K 1 control register 1	0x00
U32K1_PHASE	rw	0x0088	UART 32K 1 baud rate control register	0x4B00
U32K1_DATA	r	0x008C	UART 32K 1 receive data buffer	--
U32K1_STS	rc_w1	0x0090	UART 32K 1 interrupt status register	0x00

4.1.9 ISO7816 Register Location

Table32. Register Location of ISO7816 Controller (ISO7816 Base: 0x40012000)

Name	Type	Address	Description	Default
ISO78160_BAUDDIVL	rw	0x0004	ISO78160 baud-rate low byte register	0x00
ISO78160_BAUDDIVH	rw	0x0008	ISO78160 baud-rate high byte register	0x00
ISO78160_DATA	rw	0x000C	ISO78160 data register	0x00
ISO78160_INFO	rc_w1	0x0010	ISO78160 information register	0x00
ISO78160_CFG	rw	0x0014	ISO78160 control register	0x00
ISO78160_CLK	rw	0x0018	ISO78160 clock divider control register	0x00
ISO78161_BAUDDIVL	rw	0x0044	ISO78161 baud-rate low byte register	0x00
ISO78161_BAUDDIVH	rw	0x0048	ISO78161 baud-rate high byte register	0x00
ISO78161_DATA	rw	0x004C	ISO78161 data register	0x00
ISO78161_INFO	rc_w1	0x0050	ISO78161 information register	0x00
ISO78161_CFG	rw	0x0054	ISO78161 control register	0x00
ISO78161_CLK	rw	0x0058	ISO78161 clock divider control register	0x00

4.1.10 TIMER/PWM Register Location

Table33. Register Location of 32b TIMER Controller (32b TIMER Base: 0x40012800)

Name	Type	Address	Description	Default
TMR0_CTRL	rw	0x0000	Timer 0's control register	0x0
TMR0_VALUE	rw	0x0004	Timer 0's current count register	0x00000000
TMR0_RELOAD	rw	0x0008	Timer 0's reload register	0x00000000
TMR0_INT	rc_w1	0x000C	Timer 0's interrupt status register	0x0
TMR1_CTRL	rw	0x0020	Timer 1's control register	0x0
TMR1_VALUE	rw	0x0024	Timer 1's current count register	0x00000000
TMR1_RELOAD	rw	0x0028	Timer 1's reload register	0x00000000
TMR1_INT	rc_w1	0x002C	Timer 1's interrupt status register	0x0
TMR2_CTRL	rw	0x0040	Timer 2's control register	0x0
TMR2_VALUE	rw	0x0044	Timer 2's current count register	0x00000000
TMR2_RELOAD	rw	0x0048	Timer 2's reload register	0x00000000
TMR2_INT	rc_w1	0x004C	Timer 2's interrupt status register	0x0
TMR3_CTRL	rw	0x0060	Timer 3's control register	0x0
TMR3_VALUE	rw	0x0064	Timer 3's current count register	0x00000000
TMR3_RELOAD	rw	0x0068	Timer 3's reload register	0x00000000

TMR3_INT	rc_w1	0x006C	Timer 3's interrupt status register	0x0

Table34. Register Location of 16b PWM TIMER Controller (16-bit PWM TIMER Base: 0x40012900)

Name	Type	Address	Description	Default
PWM0_CTL	rw	0x0000	PWM Timer 0's control register	0x00
PWM0_TAR	r	0x0004	PWM Timer 0's current count register	0x0000
PWM0_CCTL0	rw	0x0008	PWM Timer 0's compare control register 0	0x000
PWM0_CCTL1	rw	0x000C	PWM Timer 0's compare control register 1	0x000
PWM0_CCTL2	rw	0x0010	PWM Timer 0's compare control register 2	0x000
PWM0_CCR0	rw	0x0014	PWM Timer 0's compare data register 0	0x0000
PWM0_CCR1	rw	0x0018	PWM Timer 0's compare data register 1	0x0000
PWM0_CCR2	rw	0x001C	PWM Timer 0's compare data register 2	0x0000
PWM1_CTL	rw	0x0020	PWM Timer 1's control register	0x00
PWM1_TAR	r	0x0024	PWM Timer 1's current count register	0x0000
PWM1_CCTL0	rw	0x0028	PWM Timer 1's compare control register 0.	0x000
PWM1_CCTL1	rw	0x002C	PWM Timer 1's compare control register 1	0x000
PWM1_CCTL2	rw	0x0030	PWM Timer 1's compare control register 2	0x000
PWM1_CCR0	rw	0x0034	PWM Timer 1's compare data register 0	0x0000
PWM1_CCR1	rw	0x0038	PWM Timer 1's compare data register 1	0x0000
PWM1_CCR2	rw	0x003C	PWM Timer 1's compare data register 2	0x0000
PWM2_CTL	rw	0x0040	PWM Timer 2's control register	0x00
PWM2_TAR	r	0x0044	PWM Timer 2's current count register	0x0000
PWM2_CCTL0	rw	0x0048	PWM Timer 2's compare control register 0	0x000
PWM2_CCTL1	rw	0x004C	PWM Timer 2's compare control register 1	0x000
PWM2_CCTL2	rw	0x0050	PWM Timer 2's compare control register 2	0x000
PWM2_CCR0	rw	0x0054	PWM Timer 2's compare data register 0	0x0000
PWM2_CCR1	rw	0x0058	PWM Timer 2's compare data register 1	0x0000
PWM2_CCR2	rw	0x005C	PWM Timer 2's compare data register 2	0x0000
PWM3_CTL	rw	0x0060	PWM Timer 3's control register	0x00
PWM3_TAR	r	0x0064	PWM Timer 3's current count register	0x0000
PWM3_CCTL0	rw	0x0068	PWM Timer 3's compare control register 0	0x000
PWM3_CCTL1	rw	0x006C	PWM Timer 3's compare control register	0x000

			1	
PWM3_CCTL2	rw	0x0070	PWM Timer 3's compare control register 2	0x000
PWM3_CCR0	rw	0x0074	PWM Timer 3's compare data register 0	0x0000
PWM3_CCR1	rw	0x0078	PWM Timer 3's compare data register 1	0x0000
PWM3_CCR2	rw	0x007C	PWM Timer 3's compare data register 2	0x0000
PWM_O_SEL	rw	0x00F0	PWM output selection register	0xDB51

4.1.11 LCD Register Location

Table35. Register Location of LCD Controller (LCD Base: 0x40002000)

Name	Type	Address	Description	Default
LCD_FB00	rw	0x0000	LCD Frame buffer 0 register	--
LCD_FB01	rw	0x0004	LCD Frame buffer 1 register	--
LCD_FB02	rw	0x0008	LCD Frame buffer 2 register	--
LCD_FB03	rw	0x000C	LCD Frame buffer 3 register	--
LCD_FB04	rw	0x0010	LCD Frame buffer 4 register	--
LCD_FB05	rw	0x0014	LCD Frame buffer 5 register	--
LCD_FB06	rw	0x0018	LCD Frame buffer 6 register	--
LCD_FB07	rw	0x001C	LCD Frame buffer 7 register	--
LCD_FB08	rw	0x0020	LCD Frame buffer 8 register	--
LCD_FB09	rw	0x0024	LCD Frame buffer 9 register	--
LCD_FB0A	rw	0x0028	LCD Frame buffer 10 register	--
LCD_FB0B	rw	0x002C	LCD Frame buffer 11 register	--
LCD_FB0C	rw	0x0030	LCD Frame buffer 12 register	--
LCD_FB0D	rw	0x0034	LCD Frame buffer 13 register	--
LCD_FB0E	rw	0x0038	LCD Frame buffer 14 register	--
LCD_FB0F	rw	0x003C	LCD Frame buffer 15 register	--
LCD_FB10	rw	0x0040	LCD Frame buffer 16 register	--
LCD_FB11	rw	0x0044	LCD Frame buffer 17 register	--
LCD_FB12	rw	0x0048	LCD Frame buffer 18 register	--
LCD_FB13	rw	0x004C	LCD Frame buffer 19 register	--
LCD_FB14	rw	0x0050	LCD Frame buffer 20 register	--
LCD_FB15	rw	0x0054	LCD Frame buffer 21 register	--
LCD_FB16	rw	0x0058	LCD Frame buffer 22 register	--
LCD_FB17	rw	0x005C	LCD Frame buffer 23 register	--
LCD_FB18	rw	0x0060	LCD Frame buffer 24 register	--
LCD_FB19	rw	0x0064	LCD Frame buffer 25 register	--
LCD_FB1A	rw	0x0068	LCD Frame buffer 26 register	--
LCD_FB1B	rw	0x006C	LCD Frame buffer 27 register	--
LCD_FB1C	rw	0x0070	LCD Frame buffer 28 register	--
LCD_FB1D	rw	0x0074	LCD Frame buffer 29 register	--

LCD_FB1E	rw	0x0078	LCD Frame buffer 30 register	--
LCD_FB1F	rw	0x007C	LCD Frame buffer 31 register	--
LCD_FB20	rw	0x0080	LCD Frame buffer 32 register	--
LCD_FB21	rw	0x0084	LCD Frame buffer 33 register	--
LCD_FB22	rw	0x0088	LCD Frame buffer 34 register	--
LCD_FB23	rw	0x008C	LCD Frame buffer 35 register	--
LCD_FB24	rw	0x0090	LCD Frame buffer 36 register	--
LCD_FB25	rw	0x0094	LCD Frame buffer 37 register	--
LCD_FB26	rw	0x0098	LCD Frame buffer 38 register	--
LCD_FB27	rw	0x009C	LCD Frame buffer 39 register	--
LCD_CTRL	rw	0x0100	LCD control register	0x00
LCD_CTRL2	rw	0x0104	LCD control register 2	0x0000
LCD_SEGCTRL0	rw	0x0108	LCD segment enable control register 0	0x00000000
LCD_SEGCTRL1	rw	0x010C	LCD segment enable control register 1	0x00000000
LCD_SEGCTRL2	rw	0x0110	LCD segment enable control register 2	0x00000000

4.1.12 SPI Register Location

Table36. Register Location of SPI1 Controller (SPI1 Base: 0x40011000)

Name	Type	Address	Description	Default
SPI1_CTRL	rw	0x0000	SPI1 Control Register	0x0000
SPI1_TXSTS	rw	0x0004	SPI1 Transmit Status Register	0x8200
SPI1_TXDAT	rw	0x0008	SPI1 Transmit FIFO register	--
SPI1_RXSTS	rw	0x000C	SPI1 Receive Status Register	0x0000
SPI1_RXDAT	r	0x0010	SPI1 Receive FIFO Register	--
SPI1_MISC	rw	0x0014	SPI1 Misc. Control Register	0x0003

Table37. Register Location of SPI2 Controller (SPI2 Base: 0x40015800)

Name	Type	Address	Description	Default
SPI2_CTRL	rw	0x0000	SPI2 Control Register	0x0000
SPI2_TXSTS	rw	0x0004	SPI2 Transmit Status Register	0x8200
SPI2_TXDAT	rw	0x0008	SPI2 Transmit FIFO register	--
SPI2_RXSTS	rw	0x000C	SPI2 Receive Status Register	0x0000
SPI2_RXDAT	r	0x0010	SPI2 Receive FIFO Register	--
SPI2_MISC	rw	0x0014	SPI2 Misc. Control Register	0x0003

Table38. Register Location of SPI3 Controller (SPI3 Base: 0x40016000)

Name	Type	Address	Description	Default
SPI3_CTRL	rw	0x0000	SPI3 Control Register	0x0000
SPI3_TXSTS	rw	0x0004	SPI3 Transmit Status Register	0x8200
SPI3_TXDAT	rw	0x0008	SPI3 Transmit FIFO register	--

SPI3_RXSTS	rw	0x000C	SPI3 Receive Status Register	0x0000
SPI3_RXDAT	r	0x0010	SPI3 Receive FIFO Register	--
SPI3_MISC	rw	0x0014	SPI3 Misc. Control Register	0x0003

Table39. Register Location of SPI4 Controller (SPI4 Base: 0x40017000)

Name	Type	Address	Description	Default
SPI4_CTRL	rw	0x0000	SPI4 Control Register	0x0000
SPI4_TXSTS	rw	0x0004	SPI4 Transmit Status Register	0x8200
SPI4_TXDAT	rw	0x0008	SPI4 Transmit FIFO register	--
SPI4_RXSTS	rw	0x000C	SPI4 Receive Status Register	0x0000
SPI4_RXDAT	r	0x0010	SPI4 Receive FIFO Register	--
SPI4_MISC	rw	0x0014	SPI4 Misc. Control Register	0x0003

4.1.13 I2C Register Location

Table40. Register Location of I2C Controller (I2C Base: 0x40010800)

Name	Type	Address	Description	Default
I2C_DATA	rw	0x0000	I2C data register	0x00
I2C_ADDR	rw	0x0004	I2C address register	0x00
I2C_CTRL	rw	0x0008	I2C control/status register	0x00
I2C_STS	rw	0x000c	I2C status register	0xF8
I2C_CTRL2	rw	0x0018	I2C interrupt enable register	0x0

4.1.14 MISC Register Location

Table41. Register Location of MISC Controller (MISC Base: 0x40013000)

Name	Type	Address	Description	Default
MISC_SRAMINT	rc_w1	0x0000	SRAM parity error Interrupt	0x00
MISC_SRAMINIT	rw	0x0004	SRAM initialize register	0x01
MISC_PARERR	r	0x0008	SRAM parity error address register	0x0000
MISC_IREN	rw	0x000C	IR enable control register	0x00
MISC_DUTYL	rw	0x0010	IR duty low pulse control register	0x0000
MISC_DUTYH	rw	0x0014	IR Duty high pulse control register	0x0000
MISC_IRQLAT	rw	0x0018	Cortex-M0 IRQ latency control register	0x00
MISC_HIADDR	r	0x0020	AHB invalid access address	--
MISC_PIADDR	r	0x0024	APB invalid access address	--

Table42. Register Location of MISC2 Controller (MISC2 Base: 0x40013E00)

Name	Type	Address	Description	Default
MISC2_FLASHWC	rw	0x0000	FLASH wait cycle register	0x2100
MISC2_CLKSEL	rw	0x0004	Clock selection register	0x0

MISC2_CLKDIVH	rw	0x0008	AHB clock divider control register	0x00
MISC2_CLKDIVP	rw	0x000C	APB clock divider control register	0x01
MISC2_HCLKEN	rw	0x0010	AHB clock enable control register	0x1FF
MISC2_PCLKEN	rw	0x0014	APB clock enable control register	0xF83FFFFF
MISC2_EPUCLKCTRL	rw	0x0020	EPU clock control register	0x0
MISC2_RSTEPU	rw	0x0024	EPU reset control register	0x0

4.1.15 CRYPT Register Location

Table43. Register Location of CRYPT Controller (MISC Base: 0x40006000)

Name	Type	Address	Description	Default
CRYPT_CTRL	rw	0x0000	CRYPT control register	0x0000
CRYPT_PTRA	rw	0x0004	CRYPT pointer A	0x0000
CRYPT_PTRB	rw	0x0008	CRYPT pointer B	0x0000
CRYPT_PTRO	rw	0x000C	CRYPT pointer O	0x0000
CRYPT_CARRY	r	0x0010	CRYPT carry/borrow bit register	0x0
CRYPT_PRIME0	rw	0x0020	The Prime number for modular calculation	0xFFFFFFFF
CRYPT_PRIME1	rw	0x0024	The Prime number for modular calculation	0xFFFFFFFF
CRYPT_PRIME2	rw	0x0028	The Prime number for modular calculation	0xFFFFFFFF
CRYPT_PRIME3	rw	0x002C	The Prime number for modular calculation	0x0000
CRYPT_PRIME4	rw	0x0030	The Prime number for modular calculation	0x0000
CRYPT_PRIME5	rw	0x0034	The Prime number for modular calculation	0x0000
CRYPT_PRIME6	rw	0x0038	The Prime number for modular calculation	0x0001
CRYPT_PRIME7	rw	0x003C	The Prime number for modular calculation	0xFFFFFFFF

4.1.16 EPU Register Location

Table44. Register Location of EPU Controller (EPU Base: 0x40015000)

Name	Type	Address	Description	Default
EPU_CFCTRL	rw	0x0008	CF output control register	0x0
EPU_HSCTRL	rw	0x000C	High-speed energy accumulators control register	0x0606
EPU_LSCTRL	rw	0x 0010	Low-speed energy accumulators	0x6666

			control register	
EPU_CLR	rw	0x0014	Energy accumulators clear register	0x0
EPU_CRPTH	rw	0x0018	Anti-creep threshold for energy accumulator register	0x0
EPU_PWRTH0	rw	0x001C	Accumulation threshold for energy accumulator register 0	0x0
EPU_PWRTH1	rw	0x0020	Accumulation threshold for energy accumulator register 1	0x0
EPU_INTEN	rw	0x0024	EPU interrupt enable register	0x0
EPU_INTSTS	rc_w1	0x0028	EPU interrupt status register	0x0
EPU_STS	r	0x002C	EPU status register	0x0
EPU_CONST0	rw	0x0034	Energy accumulator 0 accumulating constant register	0x0(32-bit Complement Code)
EPU_OUTL0	r	0x0038	Energy accumulator 0 accumulating low bit register	0x0
EPU_OUTH0	r	0x003C	Energy accumulator 0 accumulating high bit register	0x0
EPU_CFCNT0	r	0x0040	Energy accumulator 0 pulse counter register	0x0
EPU_CONST1	rw	0x0048	Energy accumulator 1 accumulating constant register	0x0
EPU_OUTL1	r	0x004C	Energy accumulator 1 accumulating low bit register	0x0
EPU_OUTH1	r	0x0050	Energy accumulator 1 accumulating high bit register	0x0
EPU_CFCNT1	r	0x0054	Energy accumulator 1 pulse counter register	0x0
EPU_CONSTx(x=2-7)	rw	0x0070+（x-2）*12	Energy accumulator x's accumulating constant register	0x0
EPU_OUTx(n=2-7)	r	0x0074+（x-2）*12	Energy accumulator x's accumulating register	0x0
EPU_CFCNTx(n=2-7)	r	0x0078+（x-2）*12	Energy accumulator x's pulse counter register	0x0

4.1.17 RNG Register Location

Table45. Register Location of RNG Controller (RNG Base: 0x40016800)

Name	Type	Address	Description	Default
RNG_IMR	rw	0x0100	RNG interrupt mask register	0x0000

RNG_ISR	rw	0x0104	RNG interrupt status register	0x0000
RNG_ICR	rw	0x0108	RNG interrupt clear register	0x0000
RNG_CFG	rw	0x010C	RNG configure register	0x0000
RNG_DATA0	rw	0x0114	RNG data register 0	0x0000
RNG_DATA1	rw	0x0118	RNG data register 1	0x0000
RNG_DATA2	rw	0x011C	RNG data register 2	0x0000
RNG_DATA3	rw	0x0120	RNG data register 3	0x0000
RNG_DATA4	rw	0x0124	RNG data register 4	0x0000
RNG_DATA5	rw	0x0128	RNG data register 5	0x0000
RNG_CMD	rw	0x012C	RNG source enable register	0x0000
RNG_CNT	rw	0x0130	RNG sample counter register	0x0000
RNG_BYPASS	rw	0x0138	RNG testing bypass register	0x0000

4.1.18 Info Information Register

The analog trim data and boot option is stored in Info Sector 6 (0x40C00); the RTC calibration data is stored in Info Sector 4 (0x40800). The address 0x40800 ~ 0x409FF data is written by downloading tool (offline download and RTC calibration). Other data is written before leaving factory. The following table shows the details of this information.

Info Sector data can only be read and cannot be written. All information has a backup. The first data in the form is expressed in 1, and second copies in 2. Each data has a checksum data. Checksum algorithm: add up each data, and reverse the result.

Table46. Info Information Register

Address	Sign	Data	Description
0x00040800	P4	RTC normal temperature offset 1	Load low 16 bits to RTC_ACP4 register, such as 0. (Unit: 0.1ppm).
0x00040804		Check sum 1	INV (SUM (0x40800, 0x40800))
0x00040808	P4	RTC normal temperature offset 2	Load low 16 bits to RTC_ACP4 register, such as 0. (Unit: 0.1ppm).
0x0004080C		Check sum 2	INV (SUM (0x40808, 0x40808))
0x00040810	K1	Crystal secondary calibration coefficient K1 1	Load to RTC_ACK1 register. K1 is calculated as follows: K1=B1/1000000*65536, B1 is the segment factor of crystal oscillator' quadratic curve. For example, the value of K1 is 20827.
0x00040814	K2	Crystal secondary calibration coefficient K2 1	Load to RTC_ACK2 register. K2 is calculated as follows:

			K2=B2/1000000*65536, B2 is the segment factor of crystal oscillator' quadratic curve. For example, the value of K2 is 21496.
0x00040818	K3	Crystal secondary calibration coefficient K3 1	Load to RTC_ACK3 register. K3 is calculated as follows: K3=B3/1000000*65536, B3 is the segment factor of crystal oscillator' quadratic curve. For example, the value of K3 is 22020.
0x0004081C	K4	Crystal secondary calibration coefficient K4 1	Load to RTC_ACK4 register. K4 is calculated as follows: K4=B4/1000000*65536, B4 is the segment factor of crystal oscillator' quadratic curve. For example, the value of K4 is 24517.
0x00040820	K5	Crystal secondary calibration coefficient K5 1	Load to RTC_ACK5 register. K5 is calculated as follows: K5=B5/1000000*65536, B5 is the segment factor of crystal oscillator' quadratic curve. For example, the value of K5 is 25257.
0x00040824		Check sum 1	INV (SUM (0x40810, 0x40820))
0x00040828	K1	Crystal secondary calibration coefficient K1 2	Load to RTC_ACK1 register. K1 is calculated as follows: K1=B1/1000000*65536, B1 is the segment factor of crystal oscillator' quadratic curve. For example, the value of K1 is 20827.
0x0004082C	K2	Crystal secondary calibration coefficient K2 2	Load to RTC_ACK2 register. K2 is calculated as follows: K2=B2/1000000*65536, B2 is the segment factor of crystal oscillator' quadratic curve. For example, the value of K2 is 21496.
0x00040830	K3	Crystal secondary calibration coefficient K3 2	Load to RTC_ACK3 register. K3 is calculated as follows: K3=B3/1000000*65536, B3 is

			the segment factor of crystal oscillator' quadratic curve. For example, the value of K3 is 22020.
0x00040834	K4	Crystal secondary calibration coefficient K4 2	Load to RTC_ACK4 register. K4 is calculated as follows: K4=B4/1000000*65536, B4 is the segment factor of crystal oscillator' quadratic curve. For example, the value of K4 is 24517.
0x00040838	K5	Crystal secondary calibration coefficient K5 2	Load to RTC_ACK5 register. K5 is calculated as follows: K5=B5/1000000*65536, B5 is the segment factor of crystal oscillator' quadratic curve. For example, the value of K5 is 25257.
0x0004083C		Check sum 2	INV (SUM (0x40828, 0x40838))
0x00040840	ACTI	Fixed point temperature of crystal 1	Load to RTC_ACTI register, such as 0x1800
0x00040844		Check sum 1	INV (SUM (0x40840, 0x40840))
0x00040848	ACTI	Fixed point temperature of crystal 2	Load to RTC_ACTI register, such as 0x1800
0x0004084C		Check sum 2	INV (SUM (0x40848, 0x40848))
0x00040850	KTEMPx(x=4~1)	Temperature section division settings 1	Load to RTC_ACKTEMP register, such as 0x3C2800EC
0x00040854		Check sum 1	INV (SUM (0x40850, 0x40850))
0x00040858	KTEMPx(x=4~1)	Temperature section division settings 2	Load to RTC_ACKTEMP register, such as 0x3C2800EC
0x0004085C		Check sum 2	INV (SUM (0x40858, 0x40858))
…			Reserved.
0x00040CE0		BAT_R offset 1	(3.6-BAT measure result) * 1000, resister division
0x00040CE4		BAT_C offset 1	(3.6-BAT measure result) * 1000, cap division
0x00040CE8		Check sum 1	INV (SUM (0x40CE0, 0x40CE4))
0x00040CEC			Reserved.
0x00040CF0		BAT_R offset 2	(3.6-BAT measure result) * 1000, resister division
0x00040CF4		BAT_C offset 2	(3.6-BAT measure result) * 1000, cap division

0x00040CF8		Check sum 2	INV (SUM (0x40CF0, 0x40CF4))
0x00040CFC			Reserved.
0x00040D00	P1/P0	RTC_ACP1/0 set 1	Load the high 16 bits to RTC_ACP1 register, such as 1060; Load the low 16 bits to RTC_ACP0, such as -214.
0x00040D04	P2’	RTC_ACP2 set 1	The value in this register is recorded as P2’, such as -19746971. According to the formula P2=P2’+(Tr-Tm)*256 to calculate P2, and load P2 to RTC_ACP2 register.
0x00040D08	P5	RTC_ACP5 set 1	Load the high 16 bits to RTC_ACP5 register, such as 6444 and the low 16 bits are abandoned.
0x00040D0C	P7/P6’	RTC_ACP 7/6 set 1	Load the high 16 bits to RTC_ACP7 register, such as 0. Load the low 16 bits to P6’ register, such as 1342. According to the formula: P6=a*P6’ to calculate P6, where a=PCLK/6553600.
0x00040D10		Check Sum set 1	INV (SUM (0x40DE0, 0x40DEC))
0x00040D14	P1/P0	RTC_ACP1/0 set 2	Load the high 16 bits to RTC_ACP1 register, such as 1060; Load the low 16 bits to RTC_ACP0, such as -214.
0x00040D18	P2’	RTC_ACP2 set 2	The value in this register is recorded as P2’, such as -19746971. According to the formula P2=P2’+(Tr-Tm)*256 to calculate P2, and load P2 to RTC_ACP2 register.
0x00040D1C	P5	RTC_ACP5 set 2	Load the high 16 bits to RTC_ACP5 register, such as 6444 and the low 16 bits are abandoned.
0x00040D20	P7/P6’	RTC_ACP 7/6 set 2	Load the high 16 bits to RTC_ACP7 register, such as 0; Load the low 16 bits to P6’ register, such as 1342.

			According to the formula: P6=a*P6' to calculate P6, where a=PCLK/6553600.
0x00040D24		Check Sum set 2	INV (SUM (0x40DF4, 0x40E00))
0x00040D28		AVCC gain 1	Pre-trim result/3.3 * 10000
0x00040D2C		DVCC gain 1	Pre-trim result/3.3 * 10000
0x00040D30		BGP gain 1	Pre-trim result/1.2 * 10000
0x00040D34		RCL gain 1	Pre-trim result/32768 * 10000
0x00040D38		RCH gain 1	Pre-trim result/6553600 * 10000
0x00040D3C		Check sum 1	INV(SUM(0x40D28, 0x40D38))
0x00040D40		AVCC gain 2	Pre-trim result/3.3 * 10000
0x00040D44		DVCC gain 2	Pre-trim result/3.3 * 10000
0x00040D48		BGP gain 2	Pre-trim result/1.2 * 10000
0x00040D4C		RCL gain 2	Pre-trim result/32768 * 10000
0x00040D50		RCH gain 2	Pre-trim result/6553600 * 10000
0x00040D54		Check sum 2	INV(SUM(0x40D40, 0x40D50))
0x00040D58		ID word 0, Backup 1	
0x00040D5C		ID word 1, Backup 1	
0x00040D60		ID Check sum 1	INV (SUM (0x40D58, 0x40D5C))
0x00040D64		ID word 0, Backup 2	
0x00040D68		ID word 1, Backup 2	
0x00040D6C		ID Check sum 2	INV (SUM (0x40D64, 0x40D68))
0x00040D70	Tr	Real Temperature 1 (from tmp275)	According to the formula P2=P2'+(Tr-Tm)*256 to calculate P2, and load P2 to RTC_ACP2 register.
0x00040D74	Tm	Measure Temperature 1 (from ADC)	
0x00040D78		Temp Check sum 1	INV(SUM(0x40D70, 0x40D74))
0x00040D7C	Tr	Real Temperature 2 (from tmp275)	According to the formula P2=P2'+(Tr-Tm)*256 to calculate P2, and load P2 to RTC_ACP2 register.
0x00040D80	Tm	Measure Temperature 2 (from ADC)	
0x00040D84		Temp Check sum 2	INV (SUM (0x40D7C, 0x40D80))
0x00040D88			Reserved.
0x00040D8C			Reserved.
0x00040D90		Measure LCD LDO gain 1	Pre-trim result/3.3 * 10000
0x00040D94		VLCD setting 1	
0x00040D98		LCD LDO Check sum 1	INV (SUM (0x40D90, 0x40D94))
0x00040D9C		Measure LCD LDO gain 2	Pre-trim result/3.3 * 10000
0x00040DA0		VLCD setting 2	
0x00040DA4		LCD LDO Check sum 2	INV (SUM (0x40D9C, 0x40DA0))
0x00040DC0		Analog trim data1	Program during CP flow for analog parameter
0x00040DC4		0xFFFFFFFF	

0x00040DC8		0xFFFFFFFF	
0x00040DCC		Checksum1	INV(SUM(0x40DC0, 0x40DC8)), the data of 0x00040DC8 address cannot be read, and it is replaced by 0xFFFFFFFF.
0x00040DD0		Analog trim data2.	Program during CP flow for analog parameter
0x00040DD4		0xFFFFFFFF	
0x00040DD8		0xFFFFFFFF	
0x00040DDC		Checksum2	INV(SUM(0x40DD0, 0x40DD8)), the data of 0x00040DD8 address cannot be read, and it is replaced by 0xFFFFFFFF.
…			
0x00040400	a1	ADC coefficient 1 of ADC_CHx channel in 3.3V system under no divider mode condition	Vdc=a1/100000000*X+b1/100000000 (32 bits complement)
0x00040404	b1		
0x00040408	a2	ADC coefficient 1 of ADC_CHx channel in 3.3V system under resistive divider mode condition	Vdc=a2/100000000*X+b2/100000000 (32 bits complement)
0x0004040C	b2		
0x00040410	a3	ADC coefficient 1 of ADC_CHx channel in 3.3V system under capacitive divider mode condition	Vdc=a3/100000000*X+b3/100000000 (32 bits complement)
0x00040414	b3		
0x00040418	a4	ADC coefficient 1 of VDD channel in 3.3V system under resistive divider mode condition	Vdc=a4/100000000*X+b4/100000000 (32 bits complement)
0x0004041C	b4		
0x00040420	a5	ADC coefficient 1 of VDD channel in 3.3V system under capacitive divider mode condition	Vdc=a5/100000000*X+b5/100000000 (32 bits complement)
0x00040424	b5		
0x00040428	a6	ADC coefficient 1 of BATRTC channel in 3.3V system under resistive divider mode condition	Vdc=a6/100000000*X+b6/100000000 (32 bits complement)
0x0004042C	b6		
0x00040430	a7	ADC coefficient 1 of BATRTC channel in 3.3V system under capacitive divider mode condition	Vdc=a7/100000000*X+b7/100000000 (32 bits complement)
0x00040434	b7		
0x00040438		Checksum1	INV(SUM(0x00040400,

			0x00040434))
0x0004043C			Reserved.
0x00040440	a1	ADC coefficient 2 of ADC_CHx channel in 3.3V system under no divider mode condition	Vdc=a1/100000000*X+b1/10000 0000 (32 bits complement)
0x00040444	b1		
0x00040448	a2	ADC coefficient 2 of ADC_CHx channel in 3.3V system under resistive divider mode condition	Vdc=a2/100000000*X+b2/10000 0000 (32 bits complement)
0x0004044C	b2		
0x00040450	a3	ADC coefficient 2 of ADC_CHx channel in 3.3V system under capacitive divider mode condition	Vdc=a3/100000000*X+b3/10000 0000 (32 bits complement)
0x00040454	b3		
0x00040458	a4	ADC coefficient 2 of VDD channel in 3.3V system under resistive divider mode condition	Vdc=a4/100000000*X+b4/10000 0000 (32 bits complement)
0x0004045C	b4		
0x00040460	a5	ADC coefficient 2 of VDD channel in 3.3V system under capacitive divider mode condition	Vdc=a5/100000000*X+b5/10000 0000 (32 bits complement)
0x00040464	b5		
0x00040468	a6	ADC coefficient 2 of BATRTC channel in 3.3V system under resistive divider mode condition	Vdc=a6/100000000*X+b6/10000 0000 (32 bits complement)
0x0004046C	b6		
0x00040470	a7	ADC coefficient 2 of BATRTC channel in 3.3V system under capacitive divider mode condition	Vdc=a7/100000000*X+b7/10000 0000 (32 bits complement)
0x00040474	b7		
0x00040478		Checksum2	INV(SUM(0x00040440, 0x00040474))
0x0004047C			Reserved.
0x00040480	A1	ADC coefficient 1 of ADC_CHx channel in 5V system under no divider mode condition	Vdc=A1/100000000*X+B1/10000 0000 (32 bits complement)
0x00040484	B1		
0x00040488	A2	ADC coefficient 1 of ADC_CHx channel in 5V system under resistive divider mode condition	Vdc=A2/100000000*X+B2/10000 0000 (32 bits complement)
0x0004048C	B2		
0x00040490	A3	ADC coefficient 1 of ADC_CHx channel in 5V	Vdc=A3/100000000*X+B3/10000 0000 (32 bits complement)
0x00040494	B3		

		system under capacitive divider mode condition	
0x00040498	A4	ADC coefficient 1 of VDD channel in 5V system under resistive divider mode condition	Vdc=A4/100000000*X+B4/10000 0000 (32 bits complement)
0x0004049C	B4		
0x000404A0	A5	ADC coefficient 1 of VDD channel in 5V system under capacitive divider mode condition	Vdc=A5/100000000*X+B5/10000 0000 (32 bits complement)
0x000404A4	B5		
0x000404A8	A6	ADC coefficient 1 of BATRTC channel in 5V system under resistive divider mode condition	Vdc=A6/100000000*X+B6/10000 0000 (32 bits complement)
0x000404AC	B6		
0x000404B0	A7	ADC coefficient 1 of BATRTC channel in 5V system under capacitive divider mode condition	Vdc=A7/100000000*X+B7/10000 0000 (32 bits complement)
0x000404B4	B7		
0x000404B8		Checksum1	INV(SUM(0x00040480, 0x000404B4))
0x000404BC			Reserved.
0x000404C0	A1	ADC coefficient 2 of ADC_CHx channel in 5V system under no divider mode condition	Vdc=A1/100000000*X+B1/10000 0000 (32 bits complement)
0x000404C4	B1		
0x000404C8	A2	ADC coefficient 2 of ADC_CHx channel in 5V system under resistive divider mode condition	Vdc=A2/100000000*X+B2/10000 0000 (32 bits complement)
0x000404CC	B2		
0x000404D0	A3	ADC coefficient 2 of ADC_CHx channel in 5V system under capacitive divider mode condition	Vdc=A3/100000000*X+B3/10000 0000 (32 bits complement)
0x000404D4	B3		
0x000404D8	A4	ADC coefficient 2 of VDD channel in 5V system under resistive divider mode condition	Vdc=A4/100000000*X+B4/10000 0000 (32 bits complement)
0x000404DC	B4		
0x000404E0	A5	ADC coefficient 2 of VDD channel in 5V system under capacitive divider mode condition	Vdc=A5/100000000*X+B5/10000 0000 (32 bits complement)
0x000404E4	B5		
0x000404E8	A6	ADC coefficient 2 of BATRTC channel in 5V	Vdc=A6/100000000*X+B6/10000 0000 (32 bits complement)
0x000404EC	B6		

		system under resistive divider mode condition	
0x000404F0	A7	ADC coefficient 2 of BATRTC channel in 5V system under capacitive divider mode condition	Vdc=A7/100000000*X+B7/100000000 (32 bits complement)
0x000404F4	B7		
0x000404F8		Checksum2	INV(SUM(0x000404C0, 0x000404F4))

5 Interrupt Controller

5.1 Introduction

Any interrupt can wake up the system from IDLE, some of them can wake up the system from sleep.

5.2 Interrupt Sources

Table47. Interrupt Sources Table

Item	Vector address	Interrupt Nom.	Description	Enable bit of peripheral event	Flag of peripheral event	Wake-up source
						Sleep
NMI	00000008h	-14	NMI			
HardFault	0000000Ch	-13	HardFault			
SVCall	0000002Ch	-5	SVCall			
PendSV	00000038h	-2	PendSV			
SysTick	0000003Ch	-1	SysTick			
PMU	00000040h	0	IOA0~15	PMU_CONTROL.0 and PMU_IOAWKUEN.0~15	PMU_IOAINTSTS.0~15	V
			32K crystal is removed or broken	PMU_CONTROL.2	PMU_STS.0	V
			6M crystal is removed or broken	PMU_CONTROL.3	PMU_STS.1	
RTC	00000044h	1	Reserved.	RTC_INTEN.0	RTC_INTSTS.0	V
			illegal time format	RTC_INTEN.1	RTC_INTSTS.1	V
			multi-second period is reach	RTC_INTEN.2	RTC_INTSTS.2	V

			multi-minute period is reach	RTC_INTEN.3	RTC_INTSTS.3	V
			multi-hour period is reach	RTC_INTEN.4	RTC_INTSTS.4	V
			mid-night (00:00) is reach	RTC_INTEN.5	RTC_INTSTS.5	V
			32K counter period is reach	RTC_INTEN.6	RTC_INTSTS.6	V
			-	-	-	-
			illegal write to CE register	RTC_INTEN.8	RTC_INTSTS.8	
U32K0	0000004 8h	2	Receiver data input	U32K0_CTRL1.0	U32K0_STS.0	V
			Receive parity error	U32K0_CTRL1.1	U32K0_STS.1	V
			Receive buffer overrun	U32K0_CTRL1.2	U32K0_STS.2	V
U32K1	0000004 Ch	3	Same as U32K0			
I2C	0000005 0h	4	Serial Interrupt	I2C_CTRL2.0	I2C_CTRL.3	
SPI1	0000005 4h	5	SPI1 Transmit	SPI1_TXSTS.14	SPI1_TXSTS.15	
			SPI1 Receive	SPI1_RXSTS.14	SPI1_RXSTS.15	
SPI2	000000A Ch	27	Same as SPI1			
UART0	0000005 8h	6	Receive	UART0_CTRL.3	UART0_INTSTS.1	
			Transmit overrun	UART0_CTRL.4	UART0_INTSTS.2	
			Receive overrun	UART0_CTRL.5	UART0_INTSTS.3	
			Receive parity error	UART0_CTRL.7	UART0_INTSTS.4	
			Transmit done	UART0_CTRL.8	UART0_INTSTS.5	
UART1	0000005 Ch	7	Same as UART0			
UART2	0000006 0h	8	Same as UART0			
UART3	0000006 4h	9	Same as UART0			
UART4	0000006 8h	10	Same as UART0			
UART5	0000006 Ch	11	Same as UART0			
ISO781 60	0000007 0h	12	Receive	ISO78160_CFG.5	ISO78160_INFO. 5	
			Transmit	ISO78160_CFG.6	ISO78160_INFO. 6	
			Receive overrun	ISO78160_CFG.7	ISO78160_INFO. 7	

ISO78161	00000074h	13	Same as ISO78160			
TMR0	00000078h	14	Timer 0 overflow	TMR0_CTRL.3	TMR0_INT.0	
TMR1	0000007Ch	15	Same as TMR0			
TMR2	00000080h	16	Same as TMR0			
TMR3	00000084h	17	Same as TMR0			
PWM0	00000088h	18	PWM timer overflow	PWM0_CTL.1	PWM0_CTL.0	
			Compare 0	PWM0_CCTL0.4	PWM0_CCTL0.0	
			Compare 1	PWM0_CCTL1.4	PWM0_CCTL1.0	
			Compare 2	PWM0_CCTL2.4	PWM0_CCTL2.0	
PWM1	0000008Ch	19	Same as PWM0			
PWM2	00000090h	20	Same as PWM0			
PWM3	00000094h	21	Same as PWM0			
DMA	00000098h	22	Channel 0 package end	DMA_IE.0	DMA_STS.0	
			Channel 1 package end	DMA_IE.1	DMA_STS.1	
			Channel 2 package end	DMA_IE.2	DMA_STS.2	
			Channel 3 package end	DMA_IE.3	DMA_STS.3	
			Channel 0 frame end	DMA_IE.4	DMA_STS.4	
			Channel 1 frame end	DMA_IE.5	DMA_STS.5	
			Channel 2 frame end	DMA_IE.6	DMA_STS.6	
			Channel 3 frame end	DMA_IE.7	DMA_STS.7	
			Channel 0 data abort	DMA_IE.8	DMA_STS.8	
			Channel 1 data abort	DMA_IE.9	DMA_STS.9	
			Channel 2 data abort	DMA_IE.10	DMA_STS.10	
			Channel 3 data abort	DMA_IE.11	DMA_STS.11	
FLASH	0000009Ch	23	checksum error	FLASH_CTRL.2	FLASH_INT.0	
ANA	000000A0h	24	manual ADC conversion done	ANA_INTEN.0	ANA_INTSTS.0	
			auto ADC conversion done	ANA_INTEN.1	ANA_INTSTS.1	
			COMP1 rising or falling	ANA_INTEN.2	ANA_INTSTS.2	V
			COMP2 rising or falling	ANA_INTEN.3	ANA_INTSTS.3	V
			VDDALARM rising or falling	ANA_INTEN.7	ANA_INTSTS.7	V
			VDCIN rising or falling	ANA_INTEN.8	ANA_INTSTS.8	V

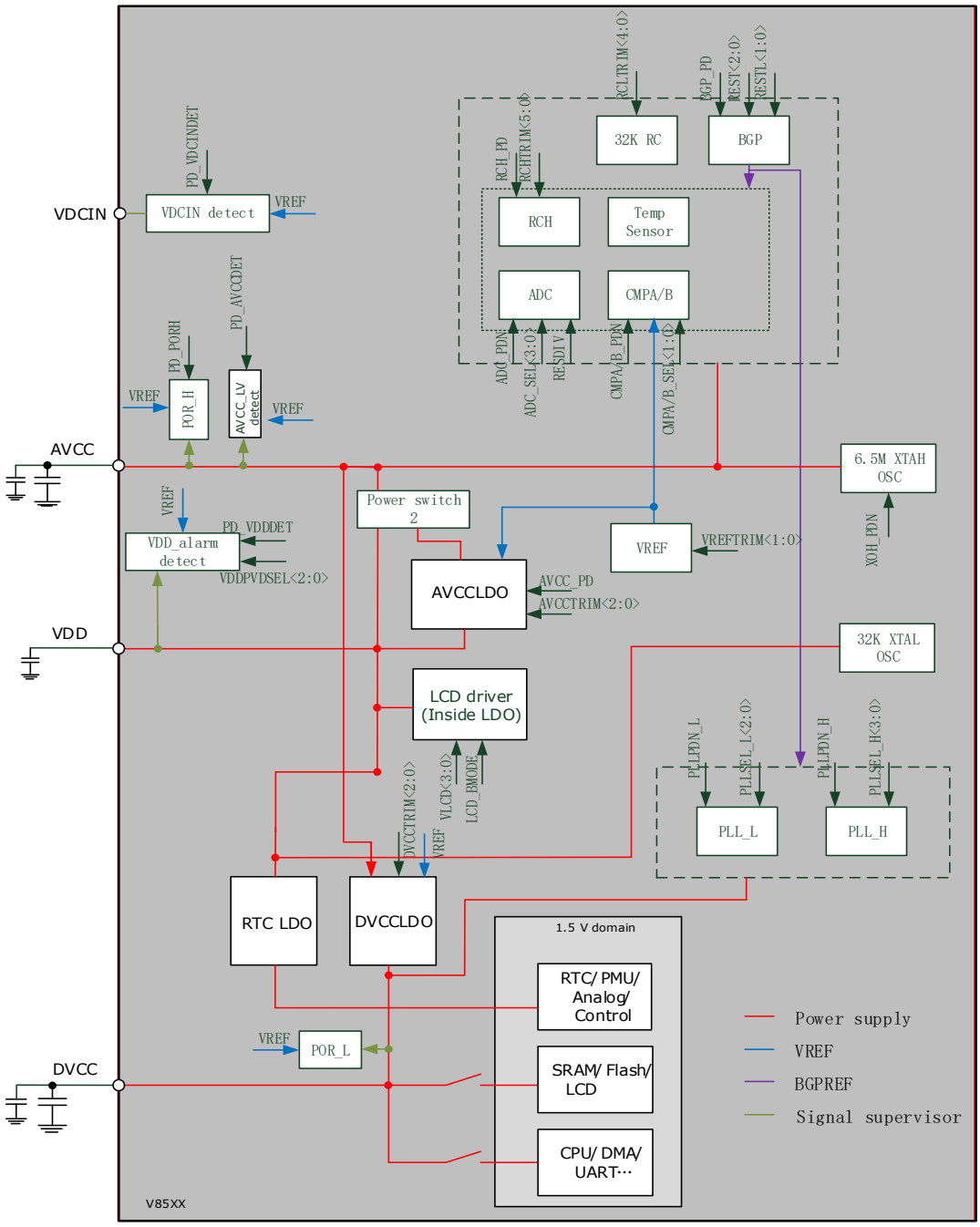
			AVCCLV rising or falling	ANA_INTEN.10	ANA_INTSTS.10	V
			VDCINDROP is 0 and the entry of sleep modes are detected	ANA_INTEN.11	ANA_INTSTS.11	V
			ANA_REGx error	ANA_INTEN.12	ANA_INTSTS.12	V
			TADC change over threshold	ANA_INTEN.13	ANA_INTSTS.13	V
EPU	000000B0h	28	Correctly receive 0xA5 frame	EPU_INTEN.12	EPU_INTSTS.12	
			Receive byte timeout	EPU_INTEN.11	EPU_INTSTS.11	
			Receive checksum error	EPU_INTEN.10	EPU_INTSTS.10	
			Receive parity error	EPU_INTEN.9	EPU_INTSTS.9	
			Correctly receive	EPU_INTEN.8	EPU_INTSTS.8	
			EGY7 overflow	EPU_INTEN.7	EPU_INTSTS.7	
			EGY6 overflow	EPU_INTEN.6	EPU_INTSTS.6	
			EGY5 overflow	EPU_INTEN.5	EPU_INTSTS.5	
			EGY4 overflow	EPU_INTEN.4	EPU_INTSTS.4	
			EGY3 overflow	EPU_INTEN.3	EPU_INTSTS.3	
			EGY2 overflow	EPU_INTEN.2	EPU_INTSTS.2	
			EGY1 overflow	EPU_INTEN.1	EPU_INTSTS.1	V
			EGY0 overflow	EPU_INTEN.0	EPU_INTSTS.0	V
RNG	000000BCh	31	Von Neumann error	RNG_IMR.3	RNG_ISR.3	
			CRNG error	RNG_IMR.2	RNG_ISR.2	
			AUTOCORR error	RNG_IMR.1	RNG_ISR.1	
			Data valid	RNG_IMR.0	RNG_ISR.0	

6 Power system

V85XX power supply has the following features:

- Supporting 5.5V and 3.3V power supply;
- The GPIO ports are powered by VDD.
- The analog circuitry inside the chip is powered by AVCC;
- The digital circuitry inside the chip and PLL circuitry are powered by DVCC;
- Supporting low voltage monitoring and real-time monitoring battery voltage.

Figure8. V85XX Power System Block Diagram



6.1 Register Location

Table48. Register Location of ANA Controller for Power (ANA Base: 0x40014200)

Name	Type	Address	Description	Default
ANA_REG5	rw	0x0014	Analog register 5	0x00
ANA_REG6	rw	0x0018	Analog register 6	0x00
ANA_REG7	rw	0x001C	Analog register 7	0x00
ANA_REG8	rw	0x0020	Analog register 8	0x00
ANA_REGA	rw	0x0028	Analog register 10	0x00
ANA_REGF	rw	0x003C	Analog register 15	0x00
ANA_CTRL	rw	0x0050	Analog control register	0x0000000
ANA_CMPOUT	r	0x0054	Comparator result register	0x0030
ANA_INTSTS	rc_w1	0x0060	Analog interrupt status register	0x0000
ANA_INTEN	rw	0x0064	Analog interrupt enable register	0x0000

6.2 Register Definition

6.2.1 ANA_REG5 Register

Table49. Description of Each Bit in ANA_REG5 for Power

Bit	Name	Type	Description
6	PD_AVCCDET	rw	Power down AVCC low voltage detector. 0: Power-up AVCC LV detector. 1: Power-down detector.

6.2.2 ANA_REG6 Register

Table50. Description of Each Bit in ANA_REG6 for Power

Bit	Name	Type	Description
6	VDDDISC	rw	Discharge the VDD battery. Discharge resistance is 1.7k, and the discharge current is V_{VDD} / 1.7k. 1: enable 1.7k resistor from VDD to GND
7	BATRTCDISC	rw	Discharge the BATRTC battery. Discharge resistance is 1.7k, and the discharge current is V_{BATRTC} / 1.7k. 1: enable 1.7k resistor from BATRTC to GND

6.2.3 ANA_REG7 Register

Table51. Description of Each Bit in ANA_REG7 for Power

Bit	Name	Type	Description
7:0	Rsvd	-	Reserved.

6.2.4 ANA_REG8 Register

Table52. Description of Each Bit in ANA_REG8 for Power

Bit	Name	Type	Description
7	PD_AVCCLDO	rw	AVCCLDO control register, and control power-down or power-up of LDO. 0: Power up LDO, Voltage of AVCC pin is 3.3V. 1: Power down LDO, AVCC connect to VDD through a switch AVCCLDO can be power down only when power supply less than 3.6V.
6:4	VDDPVDSEL	rw	Voltage selection of VDD power detector, the setting in this register will affect the status of VDDALARM. 000: 4.5V 001: 4.2V 010: 3.9V 011: 3.6V 100: 3.2V 101: 2.9V 110: 2.6V 111: 2.3V

6.2.5 ANA_REG9 Register

Table53. Description of Each Bit in ANA_REG9 for Power

Bit	Name	Type	Description
7	PD_VDDDET	rw	Power down VDD input VDDALARM detector This module powered by VDD. 0: Power up. 1: Power down.

6.2.6 ANA_REGA Register

Table54. Description of Each Bit in ANA_REGA for Power

Bit	Name	Type	Description

7	PD_VDCINDET	rw	PD VDCIN detector 0: Power up 1: Power down
6:0	Rsvd	-	Default value is 0x00, and must be set to 0x0A.

6.2.7 ANA_REGF Register

Table55. Description of Each Bit in ANA_REGF for Power

Bit	Name	Type	Description
2	AVCCO_EN	rw	Power on AVCC_OUT pin 0: Power down 1: Power up

6.2.8 ANA_CMPOUT Register

Table56. Description of ANA_CMPOUT Register for Power

Bit	Name	Type	Description
10	AVCCLV	r	AVCC low power status. And hysteresis voltage of AVCCLV is 20mV~30mV. 0: AVCC is higher than 2.5V. 1: AVCC is lower than 2.5V.
8	VDCINDROP	r	VDCIN drop status 0: VDCIN is not drop (VDCIN higher than threshold). 1: VDCIN is drop (i.e. VDCIN lower than threshold).
7	VDDALARM	r	This bit shows the output of VDDALARM. 0: Voltage of VDD is higher than voltage setting by VDDPVDSEL. 1: Voltage of VDD is lower than voltage setting by VDDPVDSEL.

6.2.9 ANA_INSTS Register

Table57. Description of ANA_INTSTS Register for Power

Bit	Name	Type	Description
11	INTSTS11	rc_w1	Interrupt flag of sleep mode entry under VDCINDROP is 0(i.e. VDCIN higher than threshold), this interrupt will be generated when VDCINDROP is 0 and the entry of sleep modes are detected. Programmer can enable this interrupt to force CPU wake-up from sleep mode when VDCINDROP is 0. Read 0: No Sleep mode entry interrupt. Read 1: Sleep mode entry interrupt is happened.

			Write 0: No effect. Write 1: clear this bit.
10	INTSTS10	rc_w1	Interrupt flag of AVCCLV (AVCC low power status), this interrupt will be generated when AVCCLV rising or falling. Read 0: No AVCCLV interrupt. Read 1: AVCCLV interrupt is happened. Write 0: No effect. Write 1: clear this bit.
8	INTSTS8	rc_w1	Interrupt flag of VDCINDROP (VDCIN status), this interrupt will be generated when VDCINDROP rising or falling. Read 0: No VDCINDROP interrupt. Read 1: VDCINDROP interrupt is happened. Write 0: No effect. Write 1: clear this bit.
7	INTSTS7	rc_w1	Interrupt flag of VDDALARM (VDD status), this interrupt will be generated when VDDALARM rising or falling. Read 0: No VDDALARM interrupt. Read 1: VDDALARM interrupt is happened. Write 0: No effect. Write 1: clear this bit.

6.2.10 ANA_INTEN Register

Table58. Description of ANA_INTEN Register for Power

Bit	Name	Type	Description
11	INTEN11	rw	Interrupt and wake-up enable control of sleep mode entry, when VDCINDROP is 0(i.e. VDCIN higher than threshold). Programmer can enable this interrupt to force CPU wake-up from sleep mode when VDCINDROP is 0 and the entry of sleep modes are detected. 0: Disable Sleep mode entry interrupt and wake-up. 1: Enable Sleep mode entry interrupt and wake-up.
10	INTEN10	rw	Interrupt and wake-up enable control of AVCCLV. 0: Disable AVCCLV interrupt and wake-up. 1: Enable AVCCLV interrupt and wake-up.
8	INTEN8	rw	Interrupt and wake-up enable control of VDCINDROP. 0: Disable VDCINDROP interrupt and wake-up. 1: Enable VDCINDROP interrupt and wake-up.
7	INTEN7	rw	Interrupt and wake-up enable control of VDDALARM. 0: Disable VDDALARM interrupt and wake-up. 1: Enable VDDALARM interrupt and wake-up.

6.3 3.3V Regulator Circuit (AVCC)

In V85XX, the analog circuit is powered by the 3.3V regulator circuit (AVCC). AVCC is controlled via the bit 'PD_AVCCLDO' (bit [7] of ANA_REG8). AVCCLDO can be power down only when power supply less than 3.6V.

AVCC has a driving capability of 30 mA.

AVCC can output from AVCC_OUT, and is controlled by the bit 'AVCCO_EN' (bit [2] of ANA_REGF). When AVCCO_EN=1, AVCC_OUT will output AVCC level. Otherwise, it will be in high-z state. AVCC_OUT has a driving capability of 20mA. The sum of the driving capability of AVCC pin and AVCC_OUT pin cannot exceed 30mA.

It is recommended to externally decouple the pin 'AVCC' with a 10uF capacitor in parallel with a 0.1-uF capacitor.

Figure9. AVCCLDO Output and VDD Power Input

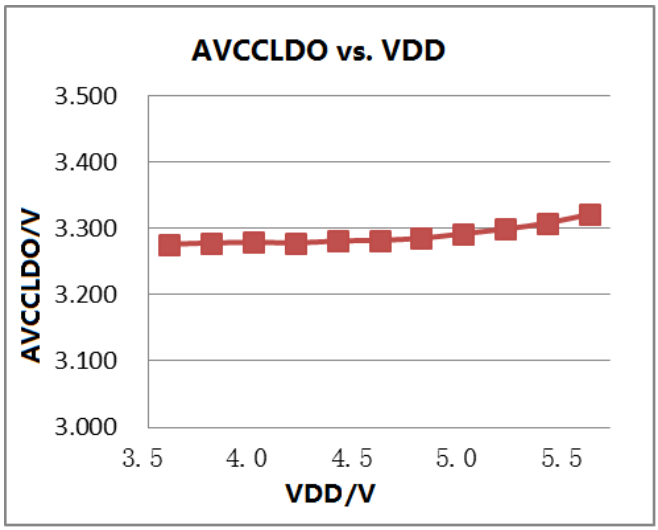
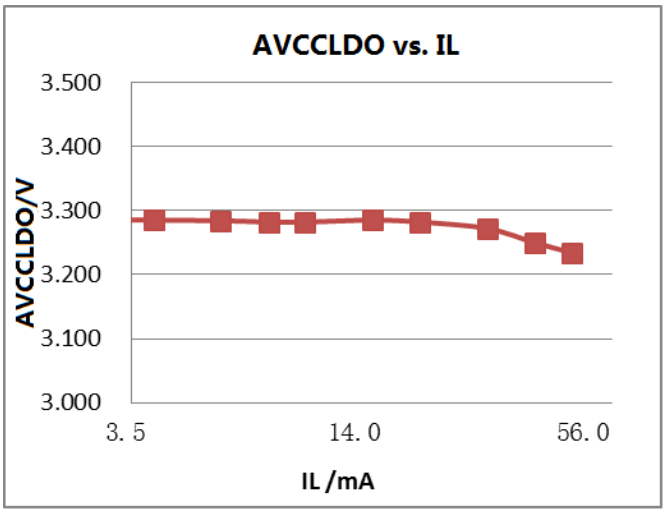


Figure10. AVCCLDO Output and The Load Current



6.4 Digital Power Supply (DVCC)

In V85XX, PLL clock generation circuit and core digital blocks are powered by the digital power supply circuit. This circuit will output a stable voltage (DVCC, i.e. 1.5V) when power input (AVCC) is higher than 1.7V.

The digital power supply circuit has a driving capability of 35mA. When the load current through the circuits is less than 35mA, the digital power supply will be stable; when the load current is higher than 35mA, the higher the load current is, the lower the digital power supply will be.

This power supply circuit will not stop working until the system is powered off.

It is recommended to externally decouple the pin ‘DVCC’ with a 10uF capacitor in parallel with a 0.1-uF capacitor.

Figure11. DVCCLDO Output and VDD Power Input

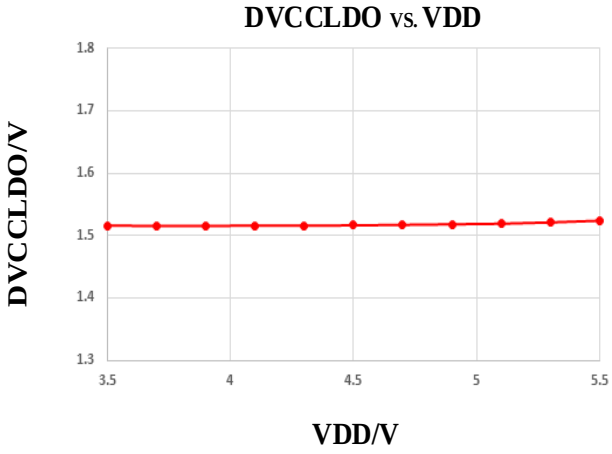
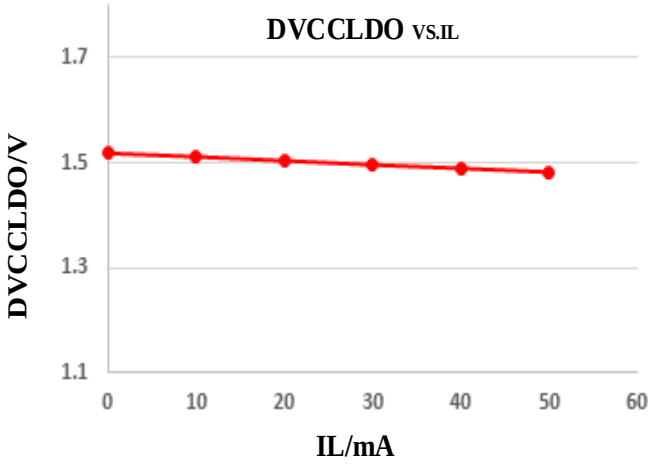


Figure12. DVCCLDO Output and The Load Current Power Supply Supervisor



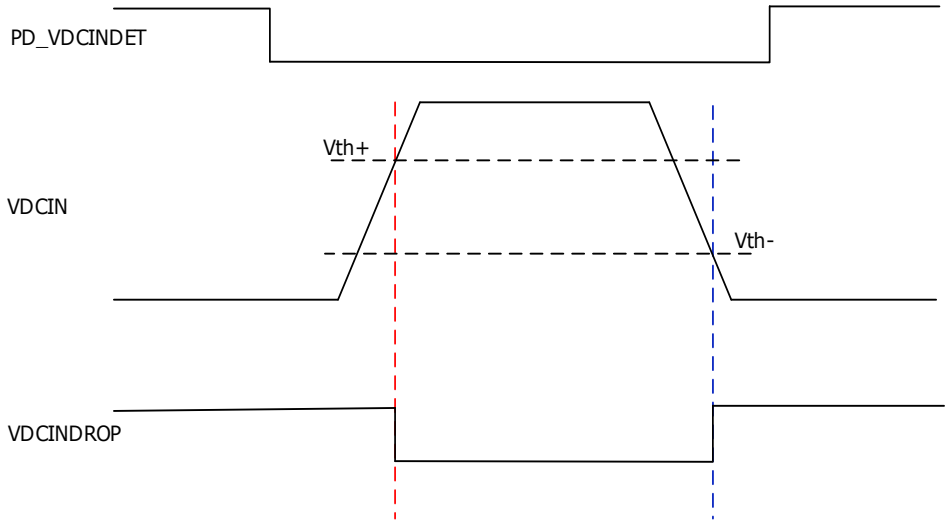
6.5 Power Supervisor

6.5.1 VDCIN Supervisor

In V85XX, the main power is input into the pin 'VDCIN' after a resistive divider. The input voltage on the pin 'VDCIN' is monitored continuously by the power supply supervisor.

When the 'VDCIN' voltage drops below Vth -, the flag bit VDCINDROP (ANACMP_OUT bit 8) will be set to 1 and a power-down interrupt will be generated to MCU. When the 'VDCIN' voltage rises above Vth+, the flag bit VDCINDROP (ANACMP_OUT bit 8) will be cleared to 0 and a power-up interrupt will be generated to MCU. The VDCIN voltage monitoring function is enabled by default. When not in use, you can set the BIT7 (PD_VDCINDET) of ANA_REGA register to 1.

Figure13. Relation Between VDCIN Input Signal and States of Flag Bits VDCINDROP



6.5.2 VDD Supervisor

Power alarm detector is designed to supervise the power state of VDD. When VDD is lower than the specified voltage threshold defined by VDDPVDSEL<2:0> in ANA_REG8, the power alarm signal will inform MCU by interrupt.

VDDPVDSEL<2:0>	Voltage selection of power detector	000: 4.5V; 001:4.2V; 010: 3.9V; 011: 3.6V; 100: 3.2V; 101: 2.9V; 110: 2.6V; 111: 2.3V

6.5.3 AVCC Supervisor

AVCCLV module is designed to supervise the power state of AVCC. When AVCC is lower than 2.5V, an LV signal will inform MCU by interrupt, in this situation, the ADC precision will be degraded much, so do not use ADC to measure any signal.

6.6 Power Switch

6.6.1 Power Switch 2

Power switch 3 is designed to select AVCC voltage input source. When PD_AVCCLDO (ANA_REG8 bit 7) is set to 0, Voltage of AVCC pin is 3.3V. When PD_AVCCLDO (ANA_REG8 bit 7) is set to 1, AVCC connect to VDD through a switch, and the switch resistor refer to table 1-4.

AVCCLDO can be power down only when power supply less than 3.6V.

7 PMU Controller

7.1 Introduction

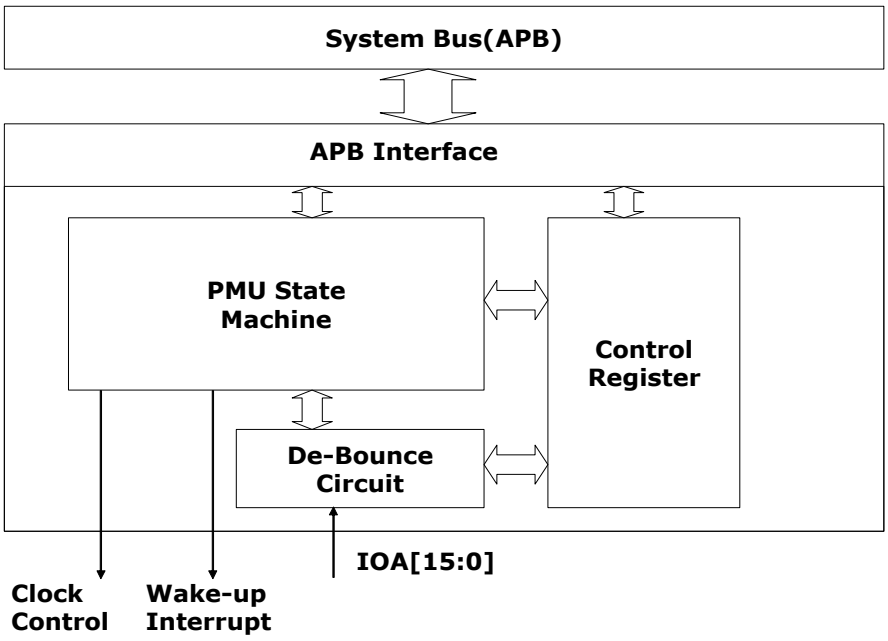
The PMU controller is used to control the sleep mode of V85XX. There are 16 IOs integrated inside the PMU controller which can wake-up the chip from sleep mode. Only RTC, analog controller and UART 32K module will be alive under this mode.

7.2 Features

- 16 GPIOs with wake-up and interrupt function.
- Interrupt generation.
- When entry sleep mode, system clock will power down. When MCU wake up from sleep mode, hardware will switch the system clock to the setting before entry sleep mode.
- Crystal absent detect and interrupt.

7.3 Functional Block Diagram

Figure14. Functional Block Diagram of PMU Controller



7.4 PMU Register Location

Table59. PMU Registers Map

Register Name	Offset	Type	Reset Value	Description
PMU_CONTROL	0x0008	rw	0x0000_0000	PMU control register
PMU_STS	0x000C	rc_w1	0x0000_0074	PMU Status register
PMU_IOAOEN	0x0010	rw	0x0000_FFFF	IOA output enable register
PMU_IOAIE	0x0014	rw	0x0000_FFFF	IOA input enable register
PMU_IOADAT	0x0018	rw	0x0000_0000	IOA data register
PMU_IOAATT	0x001C	rw	0x0000_0000	IOA attribute register
PMU_IOAWKUEN	0x0020	rw	0x0000_0000	IOA wake-up enable register
PMU_IOASTS	0x0024	r	0x0000_0000	IOA input status register
PMU_IOAINTSTS	0x0028	rc_w1	0x0000_0000	IOA interrupt status register
PMU_IOASEL	0x0038	rw	0x0000_0000	IOA special function select register
PMU_WDTPASS	0x0040	rw	0x0000_0000	Watch dog timing unlock register
PMU_WDTEN	0x0044	rw	0x0000_0001	Watch dog timer enable register
PMU_WDTCLR	0x0048	w	0x0000_0000	Watch dog timer clear register
PMU_IOANODEG	0x0050	rw	0x0000_0000	IOA no-deglitch control register.
PMU_WDTSTS	0x0060	rc_w1	0x0000_0000	Watch dog timer status register.

7.5 Register Definitions

7.5.1 PMU_CONTROL Register

Table60. PMU_CONTROL Register Description

Bit	Name	Type	Description
31:16	Rsvd	-	Reserved.
15:8	PWUPCYC	rw	Power-up cycle count, this register controls the power-up wait time when a wake-up even is received. The unit is 32K clock period.
5	PLLL_SEL	rw	Low speed PLL input clock selection. 0: 32K XTAL 1: 32K RC.
4	PLLH_SEL	rw	High speed PLL input clock selection. 0: 6.5MHz RC 1: 6.5536MHz XTAL
3	INT_6M_EN	rw	6.5536M XTAL absent interrupt enable register. This bit is used to control the interrupt signal output to CPU. When this bit is set to 1, if 6.5536M crystal is removed or broken, an interrupt will be issued to CPU. And if this event is happened during sleep, CPU will be waked up.
2	INT_32K_EN	rw	32K XTAL absent interrupt enable register. This bit is used to control the interrupt signal output to CPU. When this bit is set to 1, if 32K crystal is removed or broken, an interrupt will be issued to CPU. And if this event is

			happened during sleep, CPU will be waked up.
1	RTCCLK_SEL	rw	RTC Clock selection. 0: 32K XTAL 1: 32K RC
0	INT_IOA_EN	rw	IOA0~15 interrupt enable register. This bit is used to control the interrupt signal output to CPU. User can set some of the IO pins as wake-up source during sleep.

7.5.2 PMU_STS Register

Table61. PMU_STS Register Description

Bit	Name	Type	Description
31:25	Rsvd	-	Reserved.
24	MODE	r	This register shows the current status of MODE pin. 0: Debug mode. 1: Normal mode.
6	DPORST	rc_w1	This bit indicated if the last reset is caused by internal digital power-on reset signal, and this bit is set to 1 only when the chip power supply first time. Write 1 to clear this bit.
5	PORST	rc_w1	This bit indicated if the last reset is caused by PORH reset or PORL reset. PORH reset is caused when AVCCLDO voltage is lower than 2.08V. PORL reset is caused when DVCCLDO voltage is lower than 1.3V. Write 1 to clear this bit.
4	EXTRST	rc_w1	This bit indicated if the last interrupt is cause by external reset signal. Write 1 to clear this bit.
3	EXIST_6M	r	6.5536M XTAL exist status register. This bit represents 6.5536M XTAL is existed or absent. After 6.5536MHz XTAL (BIT7 of ANA_REG3 is configured as 1) is turned on, the state bit will refresh, otherwise it will remain in its previous state. 0: 6.5536M crystal is absent. 1: 6.5536M crystal is existed.
2	EXIST_32K	r	32K XTAL exist status register. This bit represents 32K XTAL is existed or absent. 0: 32K crystal is absent. 1: 32K crystal is existed.
1	INT_6M	rc_w1	This bit represents the 6.5536M crystal absent interrupt status. When this bit is set to 1, it means the 6.5536M crystal is removed or broken. When the EXIST_6M state goes from 1 to 0, the state position is 1.

			Write 1 to this bit can clear this flag to 0.
0	INT_32K	rc_w1	This bit represents the 32K crystal absent interrupt status. When this bit is set to 1, it means the 32K crystal is removed or broken. When the EXIST_32K state goes from 1 to 0, the state position is 1. Write 1 to this bit can clear this flag to 0.

7.5.3 PMU_IOAOEN Register

Table62. PMU_IOAOEN Register Description

Bit	Name	Type	Description
31:16	Rsvd	-	Reserved.
15:0	IOAOEN	rw	Each bit controls the IOA output enable signal Referred to Table213 for detail of IO state. 0: Enable IO's output function. 1: Disable IO's output function.

7.5.4 PMU_IOAIE Register

Table63. PMU_IOAIE Register Description

Bit	Name	Type	Description
31:16	Rsvd	-	Reserved.
15:0	IOAIE	rw	Each bit controls the IOA input enable signal Referred to Table213 for detail of IO state. 0: Disable IO's input function. 1: Enable IO's input function.

7.5.5 PMU_IOADAT Register

Table64. PMU_IOADAT Register Description

Bit	Name	Type	Description
31:16	Rsvd	-	Reserved.
15:0	IOADAT	rw	Each bit controls the IOA output data and pull low/high function Referred to Table213 for detail of IO state.

7.5.6 PMU_IOAATT Register

Table65. PMU_IOAATT Register Description

Bit	Name	Type	Description

31:16	Rsvd	-	Reserved.
15:0	IOAATT	rw	Each bit controls the IOA attribute Referred to Table213 for detail of IO state. When an IO is set to output mode (GPIO or special function), this bit is used to control the CMOS or open drain mode of the IO pad. 0: CMOS mode. 1: Open drain mode (disable PMOS output).

Table66. IO Status under Different Kind of Setting

IOx Setting			IO Status
IOxOEN	IOxDAT	IOxATT	
1	0	0	Disable output function.
1	1	0	Disable output function.
1	0	1	Disable output function.
1	1	1	Disable output function.
0	0	0	Output low
0	1	0	Output high
0	0	1	Open drain output low.
0	1	1	Open drain pull-high

7.5.7 PMU_IOAWKUEN Register

Table67. PMU_IOAWKUEN Register Description

Bit	Name	Type	Description
31:0	IOAWKUEN	rw	Every 2 bits control the IOA wake up or interrupt enable function. Bit [1:0]: IOA0WKUEN[1:0] Bit [3:2]: IOA1WKUEN[1:0] …… Bit [31:30]: IOA15WKUEN[1:0] Refer to Table214 for detail of each wake-up mode.

Table68. Description of each IO wake-up mode

IOAyWKUEN[1：0]	IOAyDAT	Wake-up Event
0	X	Disable wake-up function
1	0	Rising edge
	1	Falling Edge
2	0	High Level
	1	Low level
3	X	Rising or falling edge

Which y=0 ... 15, indicating an IO port.

For rising edge or falling edge wake-up source, since the H/W will use the final latch IO status before entering sleep mode, so the programmer needs to wait until the IO status change back to normal state. For example, when rising edge mode is chosen, the programmer should wait until the IO status back to low state to ensure the rising edge can be detected correctly. For high level or low level source, IO have no debounce in normal interrupt or wake up from sleep mode, but IO have four RTCCLK clock cycles debounce When CPU wake up from sleep mode.

7.5.8 PMU_IOASTS Register

Table69. PMU_IOASTS Register Description

Bit	Name	Type	Description
31:16	Rsvd	-	Reserved.
15:0	IOASTS	r	Each bit represents the current IOA input data value.

7.5.9 PMU_IOAINTSTS Register

Table70. PMU_IOAINTSTS Register Description

Bit	Name	Type	Description
31:16	Rsvd	-	Reserved.
15:0	IOAINTSTS	rc_w1	Each bit represents the IOA interrupt status. The corresponded bit will be set to 1 when corresponded wake-up event is detected. This register can be clear to 0 by writing corresponded bit to 1.

7.5.10 PMU_WDTPASS Register

Table71. PMU_WDTPASS Register Description

Bit	Name	Type	Description
31:1	Rsvd	-	Reserved.
0	UNLOCK	r	This bit indicates the watch dog timer enable register has been unlocked and is ready to change the watch dog enable control register. To set this bit to 1, programmer should write 0xAA5555AA to this register. This bit will be cleared immediately after any register write to any PMU control register, including ICE write, so programmer should set the PMU_WDTEN immediately after the UNLOCK bit is set to 1, otherwise the UNLOCK procedure should start again.

7.5.11 PMU_WDTEN Register

Table72. PMU_WDTEN Register Description

Bit	Name	Type	Description
31:5	Rsvd	-	Reserved.
4:2	WDTSEL	rw	This register is used to control the WDT counting period. 0: 2 secs 1: 1 sec 2: 0.5 secs 3: 0.25 secs 4: 512s 5: 256 secs 6: 128 secs 7: 64 secs To change the value of this register, UNLOCK bit of PMU_WDTPASS should be set to 1 first.
0	WDTEN	rw	This bit indicates the watch dog timer is enable. To change the value of this register, UNLOCK bit of PMU_WDTPASS should be set to 1 first.

7.5.12 PMU_WDTCLR Register

Table73. PMU_WDTCLR Register Description

Bit	Name	Type	Description
31:24	Rsvd	-	Reserved.
23:0	WDTCNT	rc_w1	This register shows the current counter value of wat dog timer. When this timer count to limit value set by WDTSEL, the WDT will issue a system reset. So programmer should clear this timer in a regulator time to avoid WDT reset. To clear this timer programmer should write 0x55AAAA55 to this register. During debug mode, this register will be cleared to 0 automatically and no WDT reset will be issued under the debug mode.

7.5.13 PMU_WDTSTS Register

Table74. PMU_WDTSTS Register Description

Bit	Name	Type	Description
31:1	Rsvd	-	Reserved.
0	WDTSTS	rc_w1	This register indicates that a WDT reset has happened. Programmer can read this bit to know if this time is the WDT reset. Write 1 to this bit can clear this flag.

7.5.14 PMU_IOASEL Register

Table75. PMU_IOASEL Register Description

Bit	Name	Type	Description
31:10	Rsvd	-	Reserved.
9	IOA_SEL9	rw	IOA9 special function select register. 0: GPIO 1: Special function 1 (CF1), only valid when CF1 enable.
7	IOA_SEL7	rw	IOA7 special function select register. 0: GPIO 1: Special function 1 (RTC_PLLDIV).
6	IOA_SEL6	rw	IOA6 special function select register. 0: GPIO 1: Special function 2 (CMP2_O).
3	IOA_SEL3	rw	IOA3 special function select register. 0: GPIO 1: Special function 1 or 2 (RTC_PLLDIV or CF0). Only valid when each funciton enable. RTC_PLLDIV has higher priority.
2:0	Rsvd	-	Reserved.

7.5.15 PMU_IOANODEG Register

Table76. PMU_IOANODEG Register Description

Bit	Name	Type	Description
31:16	Rsvd	-	Reserved.
15:0	IOANODEG	rw	Each bit control if the IOA wake-up signal will go through de-glitch circuit or not. If set this bit to 1, the corresponded IOA wake-up signal will not go through de-glitch circuit which can have a faster wake-up time. This bit affect the edge wake-up signal under sleep mode. 0: IOA wake-up signal will go through de-glitch circuit. 1: IOA wake-up signal will not go through de-glitch circuit.

7.6 RETRAM Register Location

Table77. RETRAM Registers Map

Register Name	Offset	Type	Reset Value	Description
RETRAM_RAMx[0..63,0x4]	0x0000	rw	0x0000_0000	PMU retention RAMx

7.6.1 RETRAM_RAMx Register

Table78. RETRAM_RAMx Register Description

Bit	Name	Type	Description
31:0	RAM	rw	There is a 256 bytes (64x32) SRAM is embedded in the PMU controller. Only word access is allowed to these ports.

7.7 Reset

After exit from each mode, some of the hardware module will be reset automatically, the following table shows the detail of reset of each module.

Table79. Reset of Each Module under Different Events

Module	External Reset	Power-on Reset	Watch-dog Reset	M0-soft Reset	Wake up from	
					sleep	idle
Cortex-M0	V	V	V	V	-	-
System SRAM	-	-	-	-	-	-
Retention SRAM	-	-	-	-	-	-
PMU (IOA)	V	V	V	-	-	-
WDT	V	V	V	-	-	-
RTC	V*	V*	V*	-	-	-
UART 32K 0	V	V	V	-	-	-
UART 32K 1	V	V	V	-	-	-
Analog Controller	V	V	V	-	-	-
LCD	V	V	V	V	-	-
GPIO (IOB~IOF)	V	V	V	V	-	-
MISC2	V	V	V	V	-	-
MISC	V	V	V	V	V	-
I2C	V	V	V	V	V	-
SPI1/SPI2	V	V	V	V	V	-
UART	V	V	V	V	V	-
ISO7816	V	V	V	V	V	-
TIMER	V	V	V	V	V	-
PWM	V	V	V	V	V	-
DMA	V	V	V	V	V	-
RNG	V	V	V	V	V	-
EPU	V	V	V	V	-	-
SRAM Controller	V	V	V	V	V	-
FLASH Controller	V	V	V	V	V	-

Note1: ***(V*)****: RTC registers without write protection can be reset under external reset or power-on reset or watch-dog reset, other registers cannot be reset under one of reset external reset or watch-dog reset events. RTC*

registers with write protection(except RTC_SEC、RTC_MIN、RTC_HOUR、RTC_DAY、RTC_WEEK、RTC_MON、RTC_YEAR、RTC_CAL) can be reset under power-on reset

For different mode, the enable or disable of clock generated module will be controlled by hardware or software, the following tables shows the detail of clock status under each mode.

Table80. Clock Source Enable or Disable in Different Modes

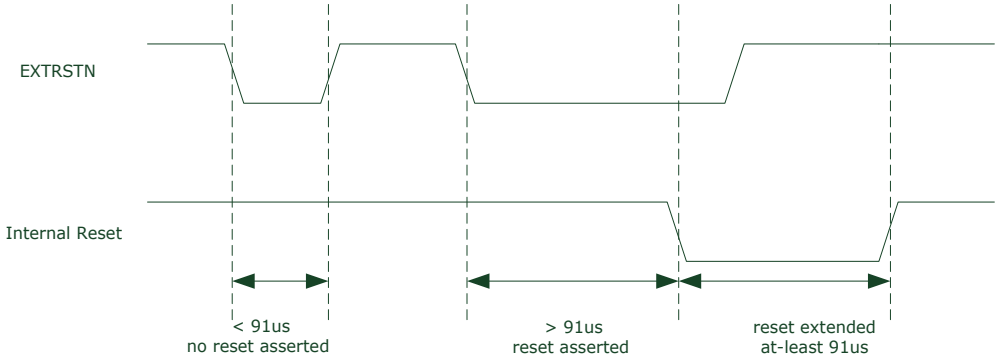
Clock Source	mode		
	Sleep	IDLE	Active
6.5536M RC	OFF	Controlled by RCHPD	
6.5536M XTAL	OFF	Controlled by XOHPDN	
PLLH	OFF	Controlled by PLLHPDN	
PLLL	OFF	Controlled by PLLLPDN	
32K RC	ON	ON	
32K XTAL	ON	ON	

Clock Source	Wake up from different modes	
	Sleep	IDLE
6.5536M RC	Controlled by RCHPD	
6.5536M XTAL	Controlled by XOHPDN	
PLLH	Controlled by PLLHPDN	
PLLL	Controlled by PLLLPDN	
32K RC	ON	
32K XTAL	ON	

7.7.1 External Reset

The external reset pin (EXTRSTN) can reset most of the modules inside V85XX. In order to prevent the external noise couple into this pin, a de-glitch circuit is embedded in V85XX. The following diagram shows an example of how this de-glitch circuit works. The deglitch time will increase accordingly when the RTCCLK pre-scaler is set to a non-zero value. For example, when RTCCLK pre-scaler is set to 1/4, the de-glitch time will be increased to 91*4 = 364 μs.

Figure15. External Reset De-glitch Timing



7.7.2 WDT Reset

WDT's reset level is the same as POR.

7.7.3 POR Reset

The POR module can provide chip's internal reset, should work with external reset together.

7.7.4 M0-soft Reset

M0-soft reset instruction can reset the most modules in V85XX, details please refer to Table79.

7.7.5 Wake up from sleep/ IDLE

Any interrupt can wake up the system from IDLE, some of them can wake up the system from sleep.

Table81. Interrupt Sources

Item	Vector address	Interrupt Nom.	Description	Enable bit of peripheral event	Flag of peripheral event	Wake-up source
						Sleep
NMI	00000008h	-14	NMI			
HardFault	0000000Ch	-13	HardFault			
SVCall	0000002Ch	-5	SVCall			
PendSV	00000038h	-2	PendSV			
SysTick	0000003Ch	-1	SysTick			
PMU	00000040h	0	IOA0~15	PMU_CONTROL.0 and PMU_IOAWKUEN.0 ~15	PMU_IOAINTSTS.0~15	V
			32K crystal is removed or broken	PMU_CONTROL.2	PMU_STS.0	V
			6M crystal is removed or broken	PMU_CONTROL.3	PMU_STS.1	
RTC	00000044h	1	Reserved.	RTC_INTEN.0	RTC_INTSTS.0	V

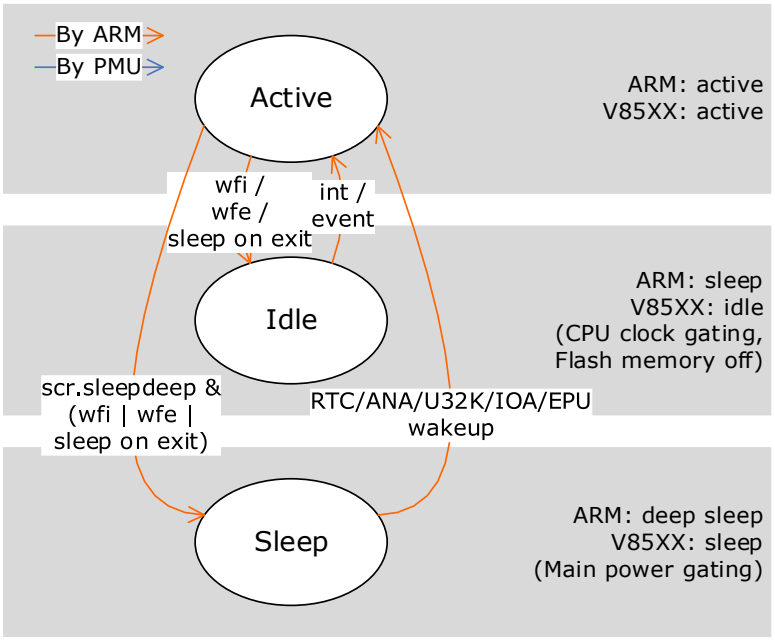
			illegal time format	RTC_INTEN.1	RTC_INTSTS.1	V
			multi-second period is reach	RTC_INTEN.2	RTC_INTSTS.2	V
			multi-minute period is reach	RTC_INTEN.3	RTC_INTSTS.3	V
			multi-hour period is reach	RTC_INTEN.4	RTC_INTSTS.4	V
			mid-night (00:00) is reach	RTC_INTEN.5	RTC_INTSTS.5	V
			32K counter period is reach	RTC_INTEN.6	RTC_INTSTS.6	V
			-	-	-	-
			illegal write to CE register	RTC_INTEN.8	RTC_INTSTS.8	
U32K0~1	00000048h 0000004Ch	2\3	Receiver data input	U32Kx_CTRL1.0	U32Kx_STS.0	V
			Receive parity error	U32Kx_CTRL1.1	U32Kx_STS.1	V
			Receive buffer overrun	U32Kx_CTRL1.2	U32Kx_STS.2	V
I2C	00000050h	4	Serial Interrupt	I2C_CTRL2.0	I2C_CTRL.3	
SPI1~4	00000054h \000000Ach \000000A8h \000000A4h	5\27\26\25	SPI Transmit	SPIx_TXSTS.14	SPIx_TXSTS.15	
			SPI Receive	SPIx_RXSTS.14	SPIx_RXSTS.15	
UART0~5	00000058h ~ 0000006Ch	6\7\8\ 9\10\11	Receive	UARTx_CTRL.3	UARTx_INTSTS.1	
			Transmit overrun	UARTx_CTRL.4	UARTx_INTSTS.2	
			Receive overrun	UARTx_CTRL.5	UARTx_INTSTS.3	
			Receive parity error	UARTx_CTRL.7	UARTx_INTSTS.4	
			Transmit done	UARTx_CTRL.8	UARTx_INTSTS.5	
ISO78160~1	00000070h ~ 00000074h	12\13	Receive	ISO7816x_CFG.5	ISO7816x_INFO.5	
			Transmit	ISO7816x_CFG.6	ISO7816x_INFO.6	
			Receive overrun	ISO7816x_CFG.7	ISO7816x_INFO.7	
Timer0~3	00000078h ~ 00000084h	14\15\ 16\17	Timer x overflow	TMRx_CTRL.3	TMRx_INT.0	
PWM0~3	00000088h ~000094h	18\19\ 20\21	PWM timer overflow	PWMx_CTL.1	PWMx_CTL.0	
			Compare 0	PWMx_CCTL0.4	PWMx_CCTL0.0	
			Compare 1	PWMx_CCTL1.4	PWMx_CCTL1.0	
			Compare 2	PWMx_CCTL2.4	PWMx_CCTL2.0	
DMA	00000098h	22	Channel 0 package end	DMA_IE.0	DMA_STS.0	
			Channel 1 package end	DMA_IE.1	DMA_STS.1	
			Channel 2 package end	DMA_IE.2	DMA_STS.2	
			Channel 3 package end	DMA_IE.3	DMA_STS.3	
			Channel 0 frame end	DMA_IE.4	DMA_STS.4	
			Channel 1 frame end	DMA_IE.5	DMA_STS.5	
			Channel 2 frame end	DMA_IE.6	DMA_STS.6	
			Channel 3 frame end	DMA_IE.7	DMA_STS.7	
			Channel 0 data abort	DMA_IE.8	DMA_STS.8	
			Channel 1 data abort	DMA_IE.9	DMA_STS.9	
			Channel 2 data abort	DMA_IE.10	DMA_STS.10	
			Channel 3 data abort	DMA_IE.11	DMA_STS.11	

FLASH	0000009Ch	23	checksum error	FLASH_CTRL.2	FLASH_INT.0	
ANA	000000A0h	24	manual ADC conversion done	ANA_INTEN.0	ANA_INTSTS.0	
			auto ADC conversion done	ANA_INTEN.1	ANA_INTSTS.1	
			COMP1 rising or falling	ANA_INTEN.2	ANA_INTSTS.2	V
			COMP2 rising or falling	ANA_INTEN.3	ANA_INTSTS.3	V
			VDDALARM rising or falling	ANA_INTEN.7	ANA_INTSTS.7	V
			VDCIN rising or falling	ANA_INTEN.8	ANA_INTSTS.8	V
			AVCCLV rising or falling	ANA_INTEN.10	ANA_INTSTS.10	V
			VDCINDROP is 0 and the entry of sleep modes are detected	ANA_INTEN.11	ANA_INTSTS.11	V
			ANA_REGx error	ANA_INTEN.12	ANA_INTSTS.12	V
			TADC change over threshold	ANA_INTEN.13	ANA_INTSTS.13	V
EPU	000000B0h	28	Correctly receive 0xA5 frame	EPU_INTEN.12	EPU_INTSTS.12	
			Receive byte timeout	EPU_INTEN.11	EPU_INTSTS.11	
			Receive checksum error	EPU_INTEN.10	EPU_INTSTS.10	
			Receive parity error	EPU_INTEN.9	EPU_INTSTS.9	
			Correctly receive	EPU_INTEN.8	EPU_INTSTS.8	
			EGY7 overflow	EPU_INTEN.7	EPU_INTSTS.7	
			EGY6 overflow	EPU_INTEN.6	EPU_INTSTS.6	
			EGY5 overflow	EPU_INTEN.5	EPU_INTSTS.5	
			EGY4 overflow	EPU_INTEN.4	EPU_INTSTS.4	
			EGY3 overflow	EPU_INTEN.3	EPU_INTSTS.3	
			EGY2 overflow	EPU_INTEN.2	EPU_INTSTS.2	
			EGY1 overflow	EPU_INTEN.1	EPU_INTSTS.1	V
			EGY0 overflow	EPU_INTEN.0	EPU_INTSTS.0	V
RNG	000000BCh	31	Von Neumann error	RNG_IMR.3	RNG_ISR.3	
			CRNG error	RNG_IMR.2	RNG_ISR.2	
			AUTOCORR error	RNG_IMR.1	RNG_ISR.1	
			Data valid	RNG_IMR.0	RNG_ISR.0	

7.8 Working Model

The following diagram shows the power state machine of V85XX.

Figure16. Power State Flow Chart of V85XX



According to the diagram above, idle mode or sleep is controlled by CPU directly, and the programmer only needs to execute corresponded instruction (WFI or WFE) to enter these two modes. The following shows the wake-up source under each mode.

Note1: *It should be noted that MCU could enter sleep mode mode only when MODE=1. If MCU execute instruction for entry sleep mode when MODE=0, MCU will enter idle mode.*

Note2: *When MCU wake up from sleep mode, hardware will switch the system clock to the setting before entry sleep mode. For example, the system clock is PLLL before entry sleep mode, the hardware will switch the system clock to PLLL when wake up from sleep mode. Before entry IDLE mode and wake up from IDLE mode, the hardware does not change the system clock automatically.*

Note3: *If user enables RTC automatic temperature compensation, user can't select RCH as system clock before entry sleep mode. If user disables RTC automatic temperature compensation, user can select RCH as system clock before entry sleep mode. System clock source control by CLKSEL (MISC2_CTRL bit2:0).*

Note4: *User can't select RTCCLK as system clock before entry sleep mode. System clock source control by CLKSEL (MISC2_CTRL bit2:0).*

Note5: *When wake up from sleep mode, PLLL lock time is 1ms, and PLLH lock time is 15μs.*

Table82. Wake-up Source under Each Mode

INT Number	Source	Wake up from	
		sleep	idle
Event	-	-	-
NMI	SRAM Parity Error	-	V
0	PMU (Ext Int)	V	V
1	RTC	V	V
2	UART 32K 0	V	V

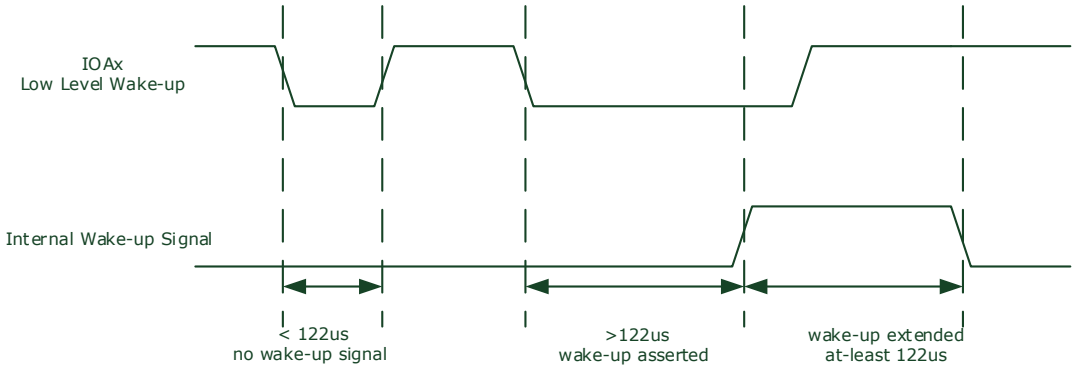
3	UART 32K 1	V	V
4	I2C	-	V
5	SPI1	-	V
6	UART0	-	V
7	UART1	-	V
8	UART2	-	V
9	UART3	-	V
10	UART4	-	V
11	UART5	-	V
12	ISO78160	-	V
13	ISO78161	-	V
14	TIMER0	-	V
15	TIMER1	-	V
16	TIMER2	-	V
17	TIMER3	-	V
18	PWM0	-	V
19	PWM1	-	V
20	PWM2	-	V
21	PWM3	-	V
22	DMA	-	V
23	FLASH	-	V
24	ANA	V	V
25	SPI4	-	V
26	SPI3	-	V
27	SPI2	-	V
28	EPU	V	V
31	RNG	-	V

7.9 Application Note

7.9.1 External IO Wake-up

All 16 IOAs can wake-up the system from sleep mode. In order to prevent some glitches on these signal to unexpected wake-up the system, a de-glitch circuit is embedded in V85XX. The following diagram shows an example of how this de-glitch circuit works. The de-glitch time will increase accordingly when the RTCCLK pre-scaler is set to a non-zero value. For example, when RTCCLK pre-scaler is set to 1/4, the de-glitch time will be increased to122*4=488μs. The de-glitch time only affects the wake-up signal under sleep mode.

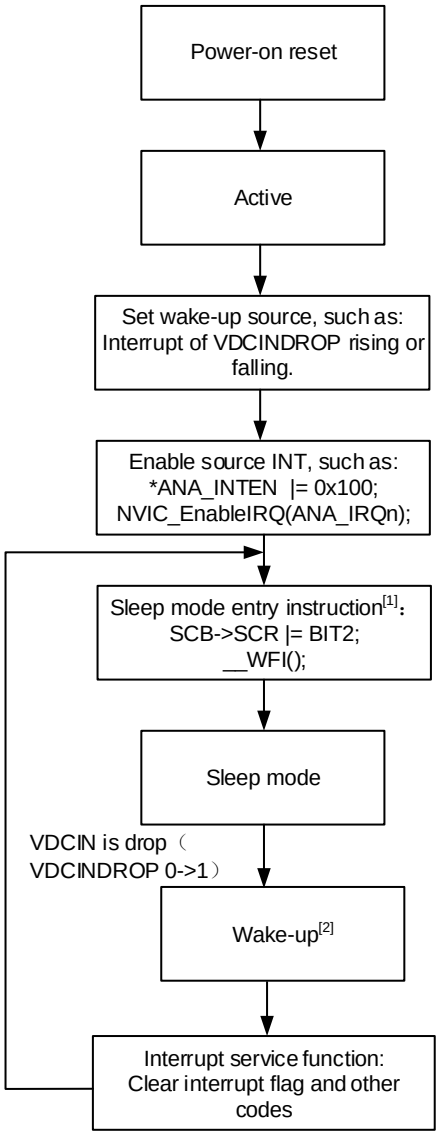
Figure17. External Wake-up Example



7.9.2 Sleep Entry Procedure

The following figure shows an example of sleep mode entry procedure.

Figure18. Sleep Mode Entry Flow

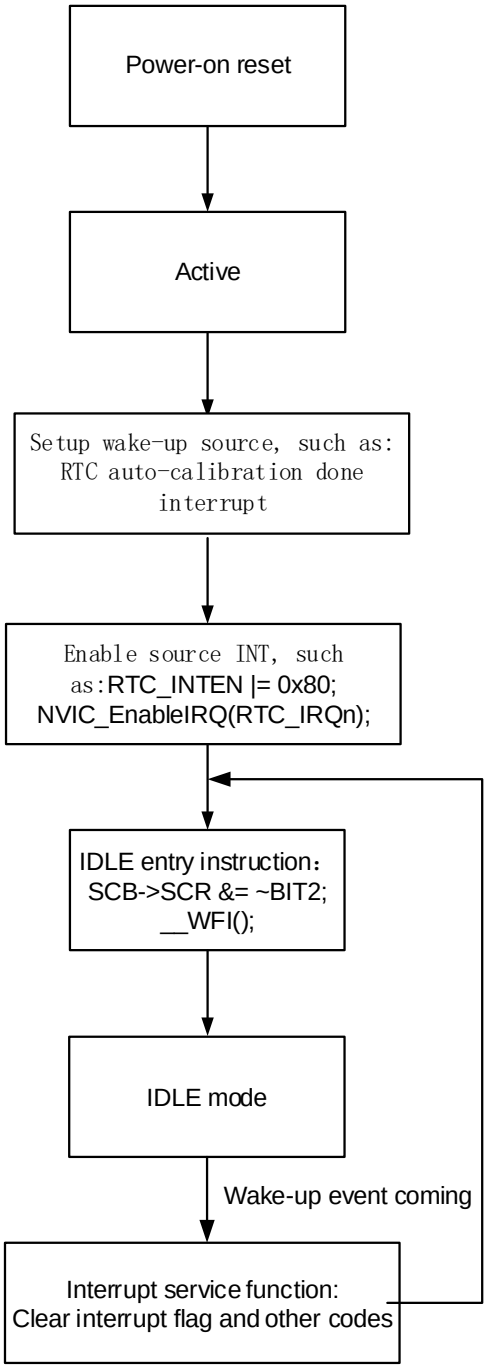


[1]: It should be noted that MCU could enter sleep mode only when MODE=1. If MCU executes instruction for entry sleep mode when MODE=0, MCU will entry IDLE mode.
[2]: When MCU is waken up from sleep mode, hardware will switch the system clock to the state of entry sleep mode. For example, the system clock is PLLL before entering sleep mode, the hardware will switch the system clock to PLLL when waking up from sleep mode.
Note: User should not select RTCCLK as system clock before entering sleep mode. System clock source is controlled by CLKSEL(MISC2_CTRL bit2:0).

7.9.3 IDLE Entry Procedure

The following figure shows an example of idle mode entry procedure.

Figure19. IDLE Mode Entry Flow



[1]:Any interrupt can wake up the system from IDLE.
Before entry IDLE mode and wake up from IDLE mode, the hardware does not change the system clock automatically.
WDT state is controlled by software when wake up from IDLE mode.

8 Clock Controller

8.1 Introduction

The settings in clock controller will be reset after wake-up from system reset.

In the V85XX, there are four clock sources:

- The 32K RC oscillator circuit, to generate a 32.768K RC clock (32K RC). This circuit is running always. 32k RC can trimming from RCLTRIM [4:0] (ANA_REGB).
- The 32K crystal oscillator circuit, to generate a 32.768K XTAL clock (32K XTAL). This circuit is monitored by the 32K XTAL monitoring circuit that is sourced by 32K RC clock. When this oscillator circuit stops running, 32K RC clock will replace 32K XTAL, and the monitoring circuit will stimulate the crystal oscillator circuit until it runs again.
- The 6M RC oscillator circuit, to generate a 6.5536M RC clock (6M RC). This circuit can stop running by user register control. This circuit starts running from chip reset.
- The 6M XTAL oscillator circuit, to generate a 6.5536M XTAL clock (6M XTAL). This circuit can stop running by user register control.

In the V85XX, there are three clock domains:

- HCLK is generated by one of the 6.5536M XTAL\6.5536M RC\32.768K XTAL\32.768K RC or multiply of them. HCLK provides clock pulses for the CPU\FLASH\SRAM\DMA\GPIO\LCD\CRYPT.
- PCLK is divided from HCLK. PCLK provides clock pulses for the slow peripheral.
- RTCCLK provides clock pulses for the RTC\ WDT\ UART32K\LCD.

For different mode, the enable or disable of clock generated module will be controlled by hardware or software, the following tables shows the detail of clock status under each mode.

Table83. Clock Source Enable or Disable in Different Modes

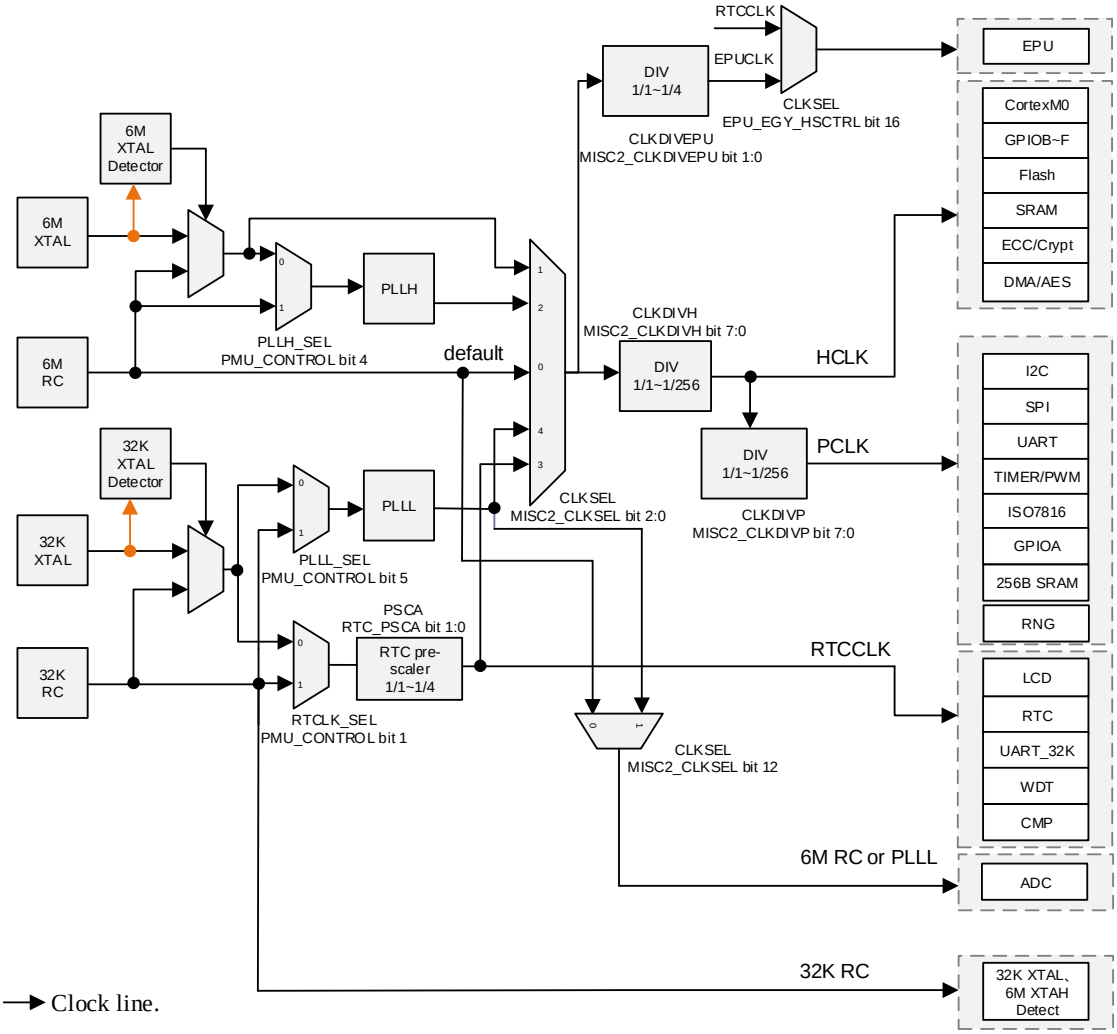
Clock Source	Power modes		
	Sleep	IDLE	Active
6.5536M RC	OFF	Controlled by RCHPD	
6.5536M XTAL	OFF	Controlled by XOHPDN	
PLLH	OFF	Controlled by PLLHPDN	
PLLL	OFF	Controlled by PLLLPDN	
32K RC	ON	ON	
32K XTAL	ON	ON	

Clock Source	Wake up from different modes

	Sleep	IDLE
6.5536M RC	Controlled by RCHPD	
6.5536M XTAL	Controlled by XOHPDN	
PLLH	Controlled by PLLHPDN	
PLLL	Controlled by PLLLPDN	
32K RC	ON	
32K XTAL	ON	

8.2 Block Diagram

Figure20. V85XX Clock Block Diagram



8.3 Feature

- Clock control of each sub-module
- Clock divider of AHBCLK and APBCLK.

8.4 Register Location

Table84. Register Location of ANA Controller for CLOCK (ANA Base: 0x40014200)

Name	Type	Address	Description	Default
ANA_REG2	rw	0x0008	Analog control register 2	0x00
ANA_REG3	rw	0x000C	Analog control register 3	0x00
ANA_REG4	rw	0x0010	Analog control register 4	0x00
ANA_REG9	rw	0x0024	Analog control register 9	0x00
ANA_REGB	rw	0x002C	Analog control register 11	From FLASH
ANA_REGC	rw	0x0030	Analog control register 12	From FLASH
ANA_REG10	rw	0x0040	Analog register 16	From FLASH
ANA_REG11	rw	0x0044	Analog register 17	From FLASH
ANA_CMPOUT	r	0x0054	Comparator result register	0x0030

Table85. Register Location of the PMU Controller (PMU Base: 0x40014000)

Name	Type	Address	Description	Default
PMU_CONTROL	rw	0x0008	PMU control register	0x0000
PMU_STS	rc_w1	0x000C	PMU Status register	0x0000074

Table86. Register Location of MISC2 Controller (MISC2 Base: 0x40013E00)

Name	Type	Address	Description	Default
MISC2_CLKSEL	rw	0x0004	Clock selection register	0x0
MISC2_CLKDIVH	rw	0x0008	AHB clock divider control register	0x00
MISC2_CLKDIVP	rw	0x000C	APB clock divider control register	0x01
MISC2_HCLKEN	rw	0x0010	AHB clock enable control register	0x1FF
MISC2_PCLKEN	rw	0x0014	APB clock enable control register	0xF83FFFFF
MISC2_EPUCLKCTRL	rw	0x0020	EPU clock control register	0x0

8.5 Register Definition

8.5.1 ANA_REG2 Register

Table87. Description of ANA_REG2

Bit	Name	Function	Notes
7	XOLPD	32K crystal pad (XOL) power	0: XOL power on.

		down control.	1: XOL power down.

8.5.2 ANA_REG3 Register

Table88. Description of ANA_REG3

Bit	Name	Function	Notes
3	BGPPD	BGP power down control signal.	0: Power-up BGP. 1: Power-down BGP.
4	RCHPD	RCH (6.5536M RC) power down control signal.	0: Power-up RCH. 1: Power-down RCH.
5	PLLLPDN	PLLL (32768Hz input PLL) power up control signal.	0: Power-down PLLL. 1: Power-up PLLL.
6	PLLHPDN	PLLH (6.5536MHz input PLL) power up control signal.	0: Power-down PLLH. 1: Power-up PLLH.
7	XOHPDN	6.5536M crystal power up control signal.	0: Power-down XOH. 1: Power-up XOH.

Note1: RCH and PLL and ADC are related to BGP, must power-up BGP before power-up RCH or PLL or ADC. User can power down BGP by set BGPPD to 1 when BGP was not used in program. User could not power down BGP by set BGPPD to 1 when BGP was used in program, because the system has a protection function to ensure reliability. User can power down BGP in sleep mode whether BGP is used or not.

8.5.3 ANA_REG4 Register

Table89. Description of ANA_REG2

Bit	Name	Function	Notes
7:2	Rsvd	-	Default: 0x00, must be set to 0x00 by user.
1:0	XRSEL	XOL pull-down resistor selection	XOL crystal oscillator pull-down resistor selection. 00: Enable pull-down resistor 210K 01: Enable pull-down resistor 105K 10/11: Bypass pull-down resistor Selection of XOL crystal pull-up resistance, see ANA_REG10 for details.

8.5.4 ANA_REG9 Register

Table90. Description of ANA_REG9

Bit	Name	Function	Notes
2:0	PLLLSEL	Frequency selection of PLLL.	000: 26.2144MHz 001: 13.1072MHz 010: 6.5536MHz 011: 3.2768MHz 100: 1.6384MHz 101: 0.8192MHz 110: 0.4096MHz 111: 0.2048MHz
6:3	PLLHSEL	Frequency selection of PLLH. The PLLH's frequency is the multiply of external XOH or internal RCH.	1000~1011: Reserved. 1100: 2 x Input clock 1101: 2.5 x Input clock 1110: 3 x Input clock 1111: 3.5 x Input clock 0000: 4 x Input clock 0001: 4.5 x Input clock 0010: 5 x Input clock 0011: 5.5 x Input clock 0100: 6 x Input clock 0101: 6.5 x Input clock 0110: 7 x Input clock 0111: 7.5 x Input clock

8.5.5 ANA_REGB Register

Table91. Description of ANA_REGB

Bit	Name	Function	Notes
4:0	RCLTRIM[4:0]	Trimming of 32kHz RC.	00000~01111: increased by 4% for each step; 10000~11111: decreased by 4% for each step;
Note: Users must not modify the configuration of ANA_REGx(x=B~E), it can be loaded from FLASH automatically.			

8.5.6 ANA_REGC Register

Table92. Description of ANA_REGC

Bit	Name	Function	Notes
5:0	RCHTRIM[5:0]	Trimming of 6.5536MHz RC	000000~011111: increased by 1.25% for each step; 100000~111111: decreased by 1.25% for each step;

Note: Users must not modify the configuration of ANA_REGx(x=B~E), it can be loaded from FLASH automatically.

8.5.7 ANA_REG10 Register

Table93. Description of ANA_REG10

Bit	Name	Function	Notes
7	XOL_LP	rw	Selection of pull-up resistance for XOL crystals 0: 5.3M Ω 1: 450K Ω XOL crystal pull-down resistor selection, see ANA_ REG4 for details.
6:0	Rsvd	-	Reserved.

8.5.8 ANA_REG11 Register

Table94. Description of ANA_REG11

Bit	Name	Function	Notes
7	Rsvd	-	Reserved.
6:0	PLLL_X_SEL	rw	PLLL doubling selection 0: x 1 1: x 1.2

8.5.9 ANA_CMPOUT Register

Table95. Description of ANA_CMPOUT Register

Bit	Name	Type	Description	Default
1	LOCKL	r	PLLL lock status. It takes about 1ms until PLLL locked. 0: PLLL is not lock. 1: PLLL is lock.	0x0
0	LOCKH	r	PLLH lock status. It takes about 15μs until PLLH locked. 0: PLLH is not lock. 1: PLLH is lock.	0x0

8.5.10 PMU_CONTROL Register

Table96. Description of PMU_CONTROL Register

Bit	Name	Type	Description	Default
5	PLLL_SEL	rw	Low speed PLL input clock selection. 0: 32KXTAL 1: 32K RC	0x0
4	PLLH_SEL	rw	High speed PLL input clock selection. 0: 6.5MHz RC 1: 6.5536MHz XTAL	0x0
3	INT_6M_EN	rw	6.5536M XTAL absent interrupt enable register. This bit is used to control the interrupt signal output to CPU. When this bit is set to 1, if 6.5536M crystal is removed or broken, an interrupt will be issued to CPU.	0x0
2	INT_32K_EN	rw	32K XTAL absent interrupt enable register. This bit is used to control the interrupt signal output to CPU. When this bit is set to 1, if 32K crystal is removed or broken, an interrupt will be issued to CPU. And if this event is happened during sleep, CPU will be waked up.	0x0
1	RTCCLK_SEL	rw	RTC Clock selection. 0: 32K XTAL 1: 32K RC	0x0

8.5.11 PMU_STS Register

Table97. Description of PMU_STS Register

Bit	Name	Type	Description	Default
3	EXIST_6M	r	6.5536M XTAL exist status register. This bit represents 6.5536M XTAL is existed or absent. After 6.5536MHz XTAL (BIT7 of ANA_REG3 is configured as 1) is turned on, the state bit will refresh, otherwise it will remain in its previous state. 0: 6.5536M crystal is absent. 1: 6.5536M crystal is existed.	0x0
2	EXIST_32K	r	32K XTAL exist status register. This bit represents 32K XTAL is existed or absent. 0: 32K crystal is absent. 1: 32K crystal is existed.	0x1
1	INT_6M	rc_w1	This bit represents the 6.5536M crystal absent interrupt status. When this bit is set to 1, it means the 6.5536M crystal is removed or broken. When the EXIST_6M state goes from 1 to 0, the	0x0

			state position is 1. Write 1 to this bit can clear this flag to 0.	
0	INT_32K	rc_w1	This bit represents the 32K crystal absent interrupt status. When this bit is set to 1, it means the 32K crystal is removed or broken. When the EXIST_32K state goes from 1 to 0, the state position is 1. Write 1 to this bit can clear this flag to 0.	0x0

8.5.12 MISC2_CLKSEL Register

Table98. Description of MISC2_CLKSEL Register

Bit	Name	Type	Description	Default
31:3	Rsvd	-	Reserved.	0
2:0	CLKSEL	rw	This register is used to control AHB clock source. 0: RCH (6.5MHz RC) 1: XOH (6.5536MHz XTAH). 2: PLLH. 3: RTCCLK (controlled by RTCCLK_SEL in PMU_CONTROL register). 4: PLLL. Before clock select to one of the clock source, programmer should enable the corresponded module first by setting PMU_CONTROL register.	0x0

8.5.13 MISC2_CLKDIVH Register

Table99. Description of MISC2_CLKDIVH Register

Bit	Name	Type	Description	Default
31:8	Rsvd	-	Reserved.	0
7:0	CLKDIVH	rw	This register is used to control AHB clock divider. 0: Clock source divide by 1 1: Clock source divide by 2. 2: Clock source divide by 3. …. 255: Clock source divide by 256.	0x00

8.5.14 MISC2_CLKDIVP Register

Table100. Description of MISC2_CLKDIVP Register

Bit	Name	Type	Description	Default
31:8	Rsvd	-	Reserved.	0
7:0	CLKDIVP	rw	This register is used to control APB clock divider. 0: AHB clock divide by 1. 1: AHB clock divide by 2. 2: AHB clock divide by 3. …. 255: AHB clock divide by 256.	0x01

8.5.15 MISC2_HCLKEN Register

Table101. Description of MISC2_HCLKEN Register

Bit	Name	Type	Description	Default
31:9	Rsvd	-	Reserved.	0
8:0	HCLKEN	rw	This register is used to control clock enable of each AHB module. The corresponded module can be turned-off only when its function is not been used. Refer to Table102 for detail about each module. 0: Disable. 1: Enable.	0x1FF

Table102. HCLK clock enable of each module

Bit	Module	Note
0	--	
1	Arbiter & Bus Matrix	Shouldn’t off when CPU or DMA is active.
2	FLASH Controller	Shouldn’t off.
3	SRAM Controller	Shouldn’t off.
4	DMA Controller	
5	GPIO Controller	
6	LCD Controller	
7	--	
8	CRYPT Controller	

8.5.16 MISC2_PCLKEN Register

Table103. Description of MISC2_PCLKEN Register

Bit	Name	Type	Description	Default
31:0	PCLKEN	rw	This register is used to control clock enable of each APB module. The corresponded module	0xF83FFFFF

			can be turned-off only when its function is not been used. Refer to Table104 for detail about each module. 0: Disable. 1: Enable.	

Table104. PCLK Clock Enable of Each Module

Bit	Module	Note
0	AHB2APB Bridge	Shouldn't off.
1	DMA Controller	
2	I2C	
3	SPI1	
4	UART0	
5	UART1	
6	UART2	
7	UART3	
8	UART4	
9	UART5	
10	ISO78160	
11	ISO78161	
12	Timer	
13	MISC	
14	MISC2	
15	PMU	
16	RTC	
17	ANA	
18	U32K 0	
19	U32K 1	
20	Reserved.	
21	SPI2.	
22	EPU	
23	RNG	
24	SPI4	
25	Reserved.	
26	SPI3	
31:27	Reserved.	

8.5.17 MISC2_EPUCLKCTRL Register

Table105. Description of MISC2_ EPUCLKCTRL Register

Bit	Name	Type	Description	Default

31:5	Rsvd	-	Reserved.	0
4	EPUCLKEN	rw	EPU function clock enable. 1: enable 0: disable	0x00
1:0	CLKDIVEPU	rw	EPU clock divider. (EPU clock source is same to HCLK clock source) 0: Clock source divide by 1. 1: Clock source divide by 2. 2: Clock source divide by 3. 3: Clock source divide by 4. Note: EPU work at 6.5536MHz clock.	0x00

9 Analog Controller

9.1 Introduction

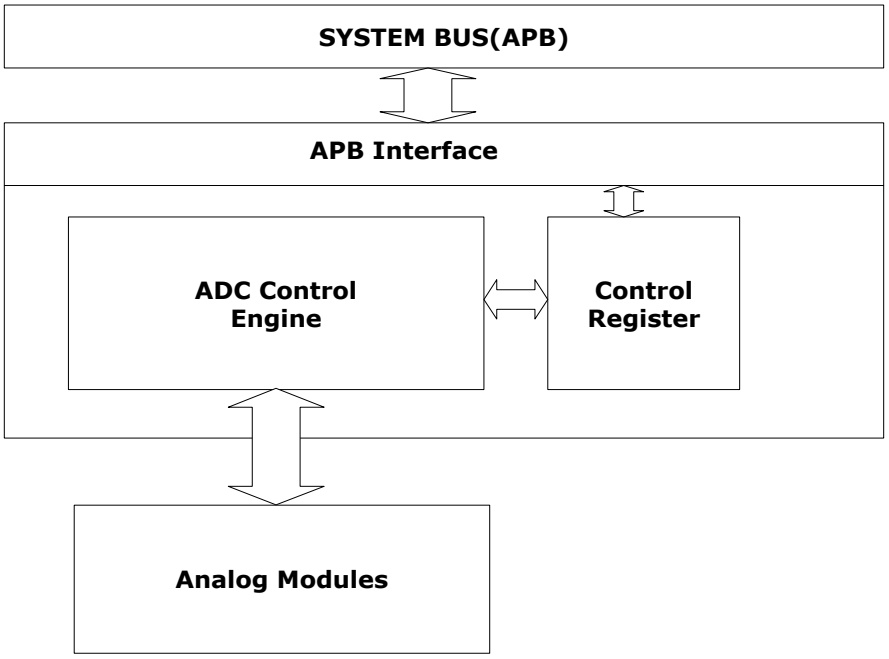
The Analog controller is used to control the analog function of V85XX. All the analog related control like ADC, comparator and other analog flag detection are controlled by this module.

9.2 Feature

- Interrupt/wake-up signal generated for analog detect flag.
- Comparator interrupt generation.
- Comparator counter.
- ADC manual and auto sample mode.
- ADC interrupt generation.

9.3 Block Diagram

Figure21. Functional Block Diagram of Analog Controller



9.4 Register Location

Table106. ANA Registers Map

Register Name	Offset	Type	Reset Value	Description

ANA_REG0	0x0000	rw	0x0000_0000	Analog register 0
ANA_REG1	0x0004	rw	0x0000_0000	Analog register 1
ANA_REG2	0x0008	rw	0x0000_0000	Analog register 2
ANA_REG3	0x000C	rw	0x0000_0000	Analog register 3
ANA_REG4	0x0010	rw	0x0000_0000	Analog register 4
ANA_REG5	0x0014	rw	0x0000_0000	Analog register 5
ANA_REG6	0x0018	rw	0x0000_0000	Analog register 6
ANA_REG7	0x001C	rw	0x0000_0000	Analog register 7
ANA_REG8	0x0020	rw	0x0000_0000	Analog register 8
ANA_REG9	0x0024	rw	0x0000_0000	Analog register 9
ANA_REGA	0x0028	rw	0x0000_0000	Analog register 10
ANA_REGB	0x002C	rw	0x0000_0000	Analog register 11
ANA_REGC	0x0030	rw	0x0000_0000	Analog register 12
ANA_REGD	0x0034	rw	0x0000_0000	Analog register 13
ANA_REGE	0x0038	rw	0x0000_0000	Analog register 14
ANA_REGF	0x003C	rw	0x0000_0000	Analog register 15
ANA_REG10	0x0040	rw	0x0000_0000	Analog register 16
ANA_REG11	0x0044	rw	0x0000_0000	Analog register 17
ANA_CTRL	0x0050	rw	0x0000_0000	Analog control register
ANA_CMPOUT	0x0054	r	0x0000_0030	Comparator result register
ANA_INTSTS	0x0060	rc_w1	0x0000_0000	Analog interrupt status register
ANA_INTEN	0x0064	rw	0x0000_0000	Analog interrupt enable register
ANA_ADCCTRL	0x0068	rw	0x0000_0000	ADC control register
ANA_ADCDATAx[0..11,0x4]	0x0070	r	0x0000_0000	ADC channel x data register
ANA_CMPCNTx[1..2,0x4]	0x00B0	rc_w1	0x0000_0000	Comparator 1 counter

9.5 Register Definition

9.5.1 ANA_REG0 Register

Table107. ANA_REG0 Register Description

Bit	Name	Type	Description
7:0	REG0_RSVD	rw	Reserved.

9.5.2 ANA_REG1 Register

Table108. ANA_REG1 Register Description

Bit	Name	Type	Description
7:6	Rsvd	-	Reserved.
5	GDE4	w	Enable cap division for M ADC input signal 0: Disable

			1: Enable 1/4 cap division
4	RESDIV	rw	Enable resistor division for M ADC input signal 0: Disable 1: Enable 1/4 resistor division
3:0	Rsvd	-	Reserved.

9.5.3 ANA_REG2 Register

Table109. ANA_REG2 Register Description

Bit	Name	Type	Description
7:6	Rsvd	-	Reserved.
5	REFSEL_CMP2	rw	REF selection of CMP2 0: VREF 1: BGPREF.
4	REFSEL_CMP1	rw	REF selection of CMP1 0: VREF 1: BGPREF.
3:2	CMP2_SEL	rw	Signal source selection of comparator B 00: CMP2_P to REF 01: CMP2_N to REF 1*: CMP2_P to CMP2_N
1:0	CMP1_SEL	rw	Signal source selection of comparator A 00: CMP1_P to REF 01: CMP1_N to REF 1*: CMP1_P to CMP1_N

9.5.4 ANA_REG3 Register

Table110. ANA_REG3 Register Description

Bit	Name	Type	Description
7	XOHPDN	rw	6.5536M crystal power up control signal. 0: Power-down XOH 1: Power-up XOH
6	PLLHPDN	rw	PLLH (6.5536MHz input PLL) power up control signal. 0: Power-down PLLH 1: Power-up PLLH
5	PLLLPDN	rw	PLLL (32768Hz input PLL) power up control signal. 0: Power-down PLLL 1: Power-up PLLL
4	RCHPD	rw	RCH (6.5536M RC) power down control signal 0: Power-up RCH 1: Power-down RCH

3	BGPPD	rw	BGP power down control signal. 0: Power-up BGP 1: Power-down BGP
2	CMP2PDN	rw	CMP2 power up control signal 0: Power-down CMP2 1: Power-up CMP2
1	CMP1PDN	rw	CMP1 power up control signal 0: Power-down CMP1 1: Power-up CMP1
0	ADCPDN	rw	ADC power up control signal. ADC automatic conversion should be disabled before ADC is powered down. 0: Power-down ADC 1: Power-up ADC

Note1: RCH and PLL and ADC are related to BGP, must power-up BGP before power-up RCH or PLL or ADC. User can power down BGP by set BGPPD to 1 when BGP was not used in program. User could not power down BGP by set BGPPD to 1 when BGP was used in program, because the system has a protection function to ensure reliability. User can power down BGP in sleep mode whether BGP is used or not.

9.5.5 ANA_REG4 Register

Table111. ANA_REG4 Register Description

Bit	Name	Type	Description
7:2	Rsvd	-	Default: 0x00, must be set to 0x00 by user.
1:0	XRSEL	rw	XOL crystal oscillator pull-down resistor selection. 00: Enable pull-down resistor 210K 01: Enable pull-down resistor 105K 10/11: Bypass pull-down resistor Selection of XOL crystal pull-up resistance, see ANA_REG10 for details.

9.5.6 ANA_REG5 Register

Table112. ANA_REG5 Register Description

Bit	Name	Type	Description
7	Rsvd	-	Reserved.
6	PD_AVCCDET	rw	Power down AVCC low voltage detector. 0: Power-up AVCC LV detector. 1: Power-down detector.
3:2	IT_CMP2	rw	Bias current selection of CMP2 00: 20nA; 01: 100nA;

			1*: 500nA;
1:0	IT_CMP1	rw	Bias current selection of CMP1 00: 20nA; 01: 100nA; 1*: 500nA;

9.5.7 ANA_REG6 Register

Table113. ANA_REG6 Register Description

Bit	Name	Type	Description
7	BATRTCDISC	rw	Discharge the BATRTC battery. Discharge resistance is 1.7k, and the discharge current is V_{BATRTC} / 1.7k. 1: enable 1.7k resistor from BATRTC to GND
6	VDDDISC	rw	Discharge the VDD battery. Discharge resistance is 1.7k, and the discharge current is V_{VDD} / 1.7k. 1: enable 1.7k resistor from VDD to GND
5	Rsvd	-	Reserved.
4:1	VLCD	rw	LCD driving voltage VLCD=0: default VLCD=0~5: adjust range =+60mV*VLCD VLCD=6~15: adjust range =-60mV*(VLCD-5)
0	LCD_BMODE	rw	LCD BIAS mode selection 0: 1/3 bias; 1: 1/4 bias.

9.5.8 ANA_REG7 Register

Table114. ANA_REG7 Register Description

Bit	Name	Type	Description
7:0	Rsvd	-	Reserved.

9.5.9 ANA_REG8 Register

Table115. ANA_REG8 Register Description

Bit	Name	Type	Description
7	PD_AVCCLDO	rw	AVCCLDO control register, and control power-down or power-up of LDO. 0: Power up LDO, Voltage of AVCC pin is 3.3V. 1: Power down LDO, AVCC connect to VDD through a switch, and the switch resistor refer to table 1-4.

			AVCCLDO can be power down only when power supply less than 3.6V.
6:4	VDDPVDSEL	rw	Voltage selection of VDD power detector, the setting in this register will affect the status of VDDALARM. 000: 4.5V 001: 4.2V 010: 3.9V 011: 3.6V 100: 3.2V 101: 2.9V 110: 2.6V 111: 2.3V
3:0	Rsvd	-	Reserved.

9.5.10 ANA_REG9 Register

Table116. ANA_REG9 Register Description

Bit	Name	Type	Description
7	PD_VDDDET	rw	Power down VDD input VDDALARM detector This module powered by VDD. 0: Power up. 1: Power down.
6:3	PLLHSEL	rw	Frequency selection of PLLH The PLLH's frequency is the multiply of external XOH or internal RCH. 1000~1011: Reserved. 1100: 2 x Input clock 1101: 2.5 x Input clock 1110: 3 x Input clock 1111: 3.5 x Input clock 0000: 4 x Input clock 0001: 4.5 x Input clock 0010: 5 x Input clock 0011: 5.5 x Input clock 0100: 6 x Input clock 0101: 6.5 x Input clock 0110: 7 x Input clock 0111: 7.5 x Input clock
2:0	PLLLSEL	rw	Frequency selection of PLLL 000: 26.2144MHz 001: 13.1072MHz 010: 6.5536MHz 011: 3.2768MHz

			100: 1.6384MHz 101: 0.8192MHz 110: 0.4096MHz 111: 0.2048MHz

9.5.11 ANA_REGA Register

Table117. ANA_REGA Register Description

Bit	Name	Type	Description
7	PD_VDCINDET	rw	PD VDCIN detector 0: Power up 1: Power down
6:0	Rsvd	-	Default value is 0x00, and must be set to 0x0A.

9.5.12 ANA_REGB Register

Table118. ANA_REGB Register Description

Bit	Name	Type	Description
7:5	VREFTRIM	rw	Trimming of VREF, which will affect DVCC/AVCC's output by same ratio 011: +9%; 010: +6%; 001: +3%; 000: 0%; 100: -3%; 101: -6%; 110: -9%; 111: -12%;
4:0	RCLTRIM	rw	Trimming of 32kHz RC. 00000~01111: increased by 4% for each step; 10000~11111: decreased by 4% for each step;

Note1: Users must not modify the configuration of ANA_REGx(x=B~E), it can be loaded from FLASH automatically.

9.5.13 ANA_REGC Register

Table119. ANA_REGC Register Description

Bit	Name	Type	Description
7:6	Rsvd	-	Reserved.
5:0	RCHTRIM	rw	Trimming of 6.5536MHz RC 000000~011111: increased by 1.25% for each step; 100000~111111: decreased by 1.25% for each step;

Note1: Users must not modify the configuration of ANA_REGx(x=B~E), it can be loaded from FLASH automatically.

9.5.14 ANA_REGD Register

Table120. ANA_REGD Register Description

Bit	Name	Type	Description
7:0	REGD_RSVD	rw	Reserved.

Note1: Users must not modify the configuration of ANA_REGx (x=B~E), it can be loaded from FLASH automatically.

9.5.15 ANA_REGE Register

Table121. ANA_REGE Register Description

Bit	Name	Type	Description
7:0	REGE_RSVD	rw	Reserved.

Note1: Users must not modify the configuration of ANA_REGx (x=B~E), it can be loaded from FLASH automatically.

9.5.16 ANA_REGF Register

Table122. ANA_REGF Register Description

Bit	Name	Type	Description
7	COMP2P_SEL	rw	0: Determined by CMP2_SEL 1: Determined by BAT_SEL
6	COMP1P_SEL	rw	0: Determined by CMP1_SEL 1: Determined by BAT_SEL
5:4	BATVOL_SEL	rw	BAT voltage selection 00: 2.6V 01: 2.4V 10: 2.2V 11: 2.0V
3	BAT_SEL	rw	BAT selection 0: VDD 1: BATRTC
2	AVCCO_EN	rw	Power on AVCC_OUT pin 0: Power down 1: Power up
1:0	Rsvd	-	Reserved.

9.5.17 ANA_REG10 Register

Table123. ANA_REG10 Register Description

Bit	Name	Type	Description

7	XOL_LP	rw	Selection of pull-up resistance for XOL crystals 0: 5.3M Ω 1: 450K Ω XOL crystal pull-down resistor selection, see ANA_ REG4 for details.
6:0	Rsvd	-	Reserved.

9.5.18 ANA_REG11 Register

Table124. ANA_REG11 Register Description

Bit	Name	Type	Description
7	PLLL_X_SEL	rw	PLLL doubling selection 0: x 1 1: x 1.2
6:0	Rsvd	-	Reserved.

9.5.19 ANA_CTRL Register

Table125. ANA_CTRL Register Description

Bit	Name	Type	Description
31:26	Rsvd	-	Reserved.
25:24	VDCINDEB	rw	VDCIN de-bounce control register. 0: No de-bounce. 1: 2 RTCCLK de-bounce. 2: 3 RTCCLK de-bounce. 3: 4 RTCCLK de-bounce. When de-bounce is enabled, the input signal is valid only when the signal isn't change in multi-cycles of RTCCLK clock. And, the response time of the wake-up and interrupt will be delayed until the signal is valid. This circuit can work under all mode.
23:22	CMP2DEB	rw	Comparator 2 de-bounce control register. 0: No de-bounce. 1: 2 RTCCLK de-bounce. 2: 3 RTCCLK de-bounce. 3: 4 RTCCLK de-bounce. When de-bounce is enabled, the input signal is valid only when the signal isn't change in multi-cycles of RTCCLK clock. And, the response time of the wake-up and interrupt will be delayed until the signal is valid. This circuit can work under all mode.
21:20	CMP1DEB	rw	Comparator 1 de-bounce control register.

			0: No de-bounce. 1: 2 RTCCLK de-bounce. 2: 3 RTCCLK de-bounce. 3: 4 RTCCLK de-bounce. When de-bounce is enabled, the input signal is valid only when the signal isn't change in multi-cycles of RTCCLK clock. And, the response time of the wake-up and interrupt will be delayed until the signal is valid. This circuit can work under all mode.
15:8	RCHTGT	rw	This register is used to store the target value of RCH. When the target frequency is 6.5536MHz, user should fill 6553600/32768 = 200 to this register.
7:4	Rsvd	-	Reserved.
3:2	COMP2_SEL	rw	This register is used to control the interrupt and wake-up signal generation of COMP2. 0: Off. 1: Rising edge of COMP2. 2: Falling edge of COMP2. 3: Change of COMP2.
1:0	COMP1_SEL	rw	This register is used to control the interrupt and wake-up signal generation of COMP1. 0: Off. 1: Rising edge of COMP1. 2: Falling edge of COMP1. 3: Change of COMP1.

9.5.20 ANA_CMPOUT Register

Table126. ANA_CMPOUT Register Description

Bit	Name	Type	Description
31:11	Rsvd	-	Reserved.
10	AVCCLV	r	AVCC low power status. And hysteresis voltage of AVCCLV is 20mV~30mV. 0: AVCC is higher than 2.5V. 1: AVCC is lower than 2.5V.
8	VDCINDROP	r	VDCIN drop status 0: VDCIN is not drop (VDCIN higher than threshold). 1: VDCIN is drop (i.e. VDCIN lower than threshold).
7	VDDALARM	r	This bit shows the output of VDDALARM. 0: Voltage of VDD is higher than voltage setting by VDDPVDSEL. 1: Voltage of VDD is lower than voltage setting by VDDPVDSEL.

3	COMP2	r	This bit shows the output of comparator 2.
2	COMP1	r	This bit shows the output of comparator 1.
1	LOCKL	r	PLLL lock status. It takes about 1ms until PLLL locked. 0: PLLL is not lock. 1: PLLL is lock.
0	LOCKH	r	PLLH lock status. It takes about 15μs until PLLH locked. 0: PLLH is not lock. 1: PLLH is lock.

9.5.21 ANA_INSTS Register

Table127. ANA_INTSTS Register Description

Bit	Name	Type	Description
31:13	Rsvd	-	Reserved.
12	INTSTS12	rc_w1	ANA_REGx error flag. This interrupt is used to detect the error status of ANA_REGx, an automatically check0sum and parity check is applied to ANA_REGx, when external noise cause by ESD or other problem affect the setting of ANA_REGx, this interrupt will be asserted and programmer can use this flag to determine if it is necessary to recover the setting in the ANA_REGx. Read 0: No ANA_REGx error interrupt. Read 1: ANA_REGx error is happened. Write 0: No effect. Write 1: clear this bit.
11	INTSTS11	rc_w1	Interrupt flag of sleep mode entry under VDCINDROP is 0(i.e. VDCIN higher than threshold), this interrupt will be generated when VDCINDROP is 0 and the entry of sleep modes are detected. Programmer can enable this interrupt to force CPU wake-up from sleep mode when VDCINDROP is 0. Read 0: No Sleep mode entry interrupt. Read 1: Sleep mode entry interrupt is happened. Write 0: No effect. Write 1: clear this bit.
10	INTSTS10	rc_w1	Interrupt flag of AVCCLV (AVCC low power status), this interrupt will be generated when AVCCLV rising or falling. Read 0: No AVCCLV interrupt. Read 1: AVCCLV interrupt is happened. Write 0: No effect. Write 1: clear this bit.
8	INTSTS8	rc_w1	Interrupt flag of VDCINDROP (VDCIN status), this interrupt will be generated when VDCINDROP rising or

			falling. Read 0: No VDCINDROP interrupt. Read 1: VDCINDROP interrupt is happened. Write 0: No effect. Write 1: clear this bit.
7	INTSTS7	rc_w1	Interrupt flag of VDDALARM (VDD status), this interrupt will be generated when VDDALARM rising or falling. Read 0: No VDDALARM interrupt. Read 1: VDDALARM interrupt is happened. Write 0: No effect. Write 1: clear this bit.
6:4	Rsvd	-	Reserved.
3	INTSTS3	rc_w1	Interrupt flag of COMP2, the interrupt generate condition is controlled by COMP2_SEL. Read 0: No COMP2 interrupt. Read 1: COMP2 interrupt is happened. Write 0: No effect. Write 1: clear this bit.
2	INTSTS2	rc_w1	Interrupt flag of COMP1, the interrupt generate condition is controlled by COMP1_SEL. Read 0: No COMP1 interrupt. Read 1: COMP1 interrupt is happened. Write 0: No effect. Write 1: clear this bit.
1	INTSTS1	rc_w1	Interrupt flag of auto ADC conversion done. Read 0: Auto ADC conversion not complete. Read 1: Auto ADC conversion has done. Write 0: No effect. Write 1: clear this bit.
0	INTSTS0	rc_w1	Interrupt flag of manual ADC conversion done. Read 0: Manual ADC conversion not complete. Read 1: Manual ADC conversion has done. Write 0: No effect. Write 1: clear this bit.

9.5.22 ANA_INTEN Register

Table128. ANA_INTEN Register Description

Bit	Name	Type	Description
31:13	Rsvd	-	Reserved.
12	INTEN12	rw	Interrupt and wake-up enable control of ANA_REGx error. 0: Disable ANA_REGx error interrupt and wake-up. 1: Enable ANA_REGx error interrupt and wake-up.

11	INTEN11	rw	Interrupt and wake-up enable control of sleep mode entry, when VDCINDROP is 0(i.e. VDCIN higher than threshold). Programmer can enable this interrupt to force CPU wake-up from sleep mode when VDCINDROP is 0 and the entry of sleep modes are detected. 0: Disable Sleep mode entry interrupt and wake-up. 1: Enable Sleep mode entry interrupt and wake-up.
10	INTEN10	rw	Interrupt and wake-up enable control of AVCCLV. 0: Disable AVCCLV interrupt and wake-up. 1: Enable AVCCLV interrupt and wake-up.
8	INTEN8	rw	Interrupt and wake-up enable control of VDCINDROP. 0: Disable VDCINDROP interrupt and wake-up. 1: Enable VDCINDROP interrupt and wake-up.
7	INTEN7	rw	Interrupt and wake-up enable control of VDDALARM. 0: Disable VDDALARM interrupt and wake-up. 1: Enable VDDALARM interrupt and wake-up.
6:4	Rsvd	-	Reserved.
3	INTEN3	rw	Interrupt and wake-up enable control of COMP2. 0: Disable COMP2 interrupt and wake-up. 1: Enable COMP2 interrupt and wake-up.
2	INTEN2	rw	Interrupt and wake-up enable control of COMP1. 0: Disable COMP1 interrupt and wake-up. 1: Enable COMP1 interrupt and wake-up.
1	INTEN1	rw	Interrupt enable control of auto ADC conversion done. 0: Disable auto ADC conversion interrupt. 1: Enable auto ADC conversion interrupt.
0	INTEN0	rw	Interrupt enable control of manual ADC conversion done. 0: Disable manual ADC conversion interrupt. 1: Enable manual ADC conversion interrupt.

9.5.23 ANA_ADCCTRL Register

Table129. ANA_ADCCTRL Register Description

Bit	Name	Type	Description
31	MTRIG	rw	Manual ADC trigger. Write 0: No effect. Write 1: Start a manual ADC conversion. Read 0: Current manual ADC conversion is done. Read 1: Current manual ADC conversion is ongoing.
29	CICAON	rw	CIC filter always on control register. 0: CIC filter will be disabled when no ADC sample process is ongoing. 1: CIC filter will be enabled for all the time.

28	CICINV	rw	CIC filter input inversion. 0: No invert CIC filter input. 1: Invert CIC filter input.
27	CICSCA	rw	CIC output scale-down selection. 0: No scale down CIC filter's output. 1: Scale down CIC filter's output to 1/2.
26:24	CICSKIP	rw	CIC output skip control register. This register is used to control how many samples will be skipped at the beginning of ADC sample. If CICAON is 1 and the ADC channel is not changed, the CIC output will not be skipped by the ADC controller, this can be used for high speed capture to single channel. 0: Skip first 4 samples. 1: Skip first 5 samples. 2: Skip first 6 samples. 3: Skip first 7 samples. 4: No skip any sample. 5: Skip first 1 sample. 6: Skip first 2 samples. 7: Skip first 3 samples.
23:22	DSRSEL	rw	CIC down sampling rate control register. The higher down-sampling rate, the higher output data stability, and lower sampling rate. 0: 1/512 down-sampling rate. 1: 1/256 down-sampling rate. 2: 1/128 down-sampling rate. 3: 1/64 down-sampling rate.
21	AMODE	rw	Auto ADC mode control. 0: Capture single channel specified by ACH. 1: Capture multiple channels (0~11 channels) at one time.
20	MMODE	rw	Manual ADC mode control. 0: Capture single channel specified by MCH. 1: Capture multiple channels (0~11 channels) at one time.
18:16	AEN	rw	Auto ADC conversion enable control register. 0: Auto ADC conversion is off. 4: Auto ADC will be triggered by timer 0's overflow. 5: Auto ADC will be triggered by timer 1's overflow. 6: Auto ADC will be triggered by timer 2's overflow. 7: Auto ADC will be triggered by timer 3's overflow.
12	CLKSEL	rw	ADC clock source selection. 0: 6.5M RCH 1: PLLL

11:8	CLKDIV	rw	The ADC clock source is internal 6.5M RCH or PLLL. The typical ADC main clock is 1.6384MHz, if ADC clock source is 6.5M RCH, CLKDIV is calculated such as: CLKDIV=6.5536/1.6384-1=3.
7:4	ACH	rw	Auto ADC channel control. 0: Auto ADC capture ADC channel 0. 1: Auto ADC capture ADC channel 1. …. 11: Auto ADC capture ADC channel 11. 12~15: Reserved. This register is valid only when AMODE is 0.
3:0	MCH	rw	Manual ADC channel control. 0: Manual ADC capture ADC channel 0. 1: Manual ADC capture ADC channel 1. …. 11: Auto ADC capture ADC channel 11. 12~15: Reserved. This register is valid only when MMODE is 0.

9.5.24 ANA_ADCDATAx Register

Table130. ANA_ADCDATAx Register Description

Bit	Name	Type	Description
31:16	Rsvd	-	Reserved.
15:0	ADCDATAx	r	The result of ADC conversion will be stored in these registers. DATA0: Store conversion result of ADC channel 0. DATA1: Store conversion result of ADC channel 1. … DATA11: Store conversion result of ADC channel 11. For single channel conversion (MMODE is 0 or AMODE is 0), only the channel specified by MCH or ACH will be updated. For multi-channels conversion (MMODE is 1 or AMODE is 1), DATA0~DATA11 will be updated.

9.5.25 ANA_CMPCNTx Register

Table131. ANA_CMPCNTx Register Description

Bit	Name	Type	Description
31:0	CNTx	rc_w1	This register stores the happen times of comparator x according to the setting in COMPx_SEL. For example, when COMPx_SEL is set to 1, then this counter will increase 1 when the COMPx is rising. This register can

			be cleared by writing 0 to this register, but this operation is valid only when corresponded CMPPDNx is set to 1 (when the corresponded comparator is enabled).

10 ADC Controller

10.1 Introduction

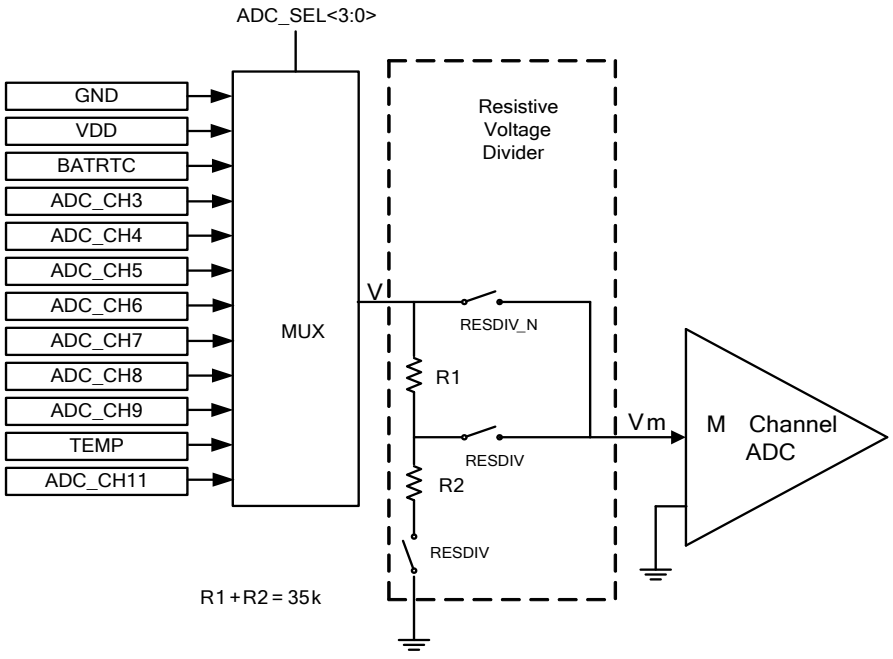
One second-order Σ-ΔADC is designed in 12 channels of the V85XX for analog-to-digital conversion, and their full measurement scale is 0~1.2V if no voltage division. After set voltage division, when main power supply is 3.3V, the measurement scale is 0~3.6V. When main power supply is 5V, the measurement scale is 0~4.6V in cap division mode, and the measurement scale is 0~5.2V in resistor division mode. The ADC can be used to measure the ground, temperature, VDD, BATRTC voltage and external voltage signals. The clock source is 6.5536M RC or PLLL.

10.2 Feature

- ADC manual and auto sample mode.
- ADC interrupt generation.

10.3 Block Diagram

Figure22. ADC Architecture



10.4 Register Location

Table132. Register Location of ANA Controller for ADC (ANA Base: 0x40014200)

Name	Type	Address	Description	Default
ANA_REG0	rw	0x0000	Analog register 0	0x00
ANA_REG1	rw	0x0004	Analog register 1	0x00
ANA_REG3	rw	0x000C	Analog register 3	0x00
ANA_INTSTS	rc_w1	0x0060	Analog interrupt status register	0x0000
ANA_INTEN	rw	0x0064	Analog interrupt enable register	0x0000
ANA_ADCCTRL	rw	0x0068	ADC control register	0x00000000
ANA_ADCDATA0	r	0x0070	ADC channel 0 data register	--
ANA_ADCDATA1	r	0x0074	ADC channel 1 data register	--
ANA_ADCDATA2	r	0x0078	ADC channel 2 data register	--
ANA_ADCDATA3	r	0x007C	ADC channel 3 data register	--
ANA_ADCDATA4	r	0x0080	ADC channel 4 data register	--
ANA_ADCDATA5	r	0x0084	ADC channel 5 data register	--
ANA_ADCDATA6	r	0x0088	ADC channel 6 data register	--
ANA_ADCDATA7	r	0x008C	ADC channel 7 data register	--
ANA_ADCDATA8	r	0x0090	ADC channel 8 data register	--
ANA_ADCDATA9	r	0x0094	ADC channel 9 data register	--
ANA_ADCDATAA	r	0x0098	ADC channel 10 data register	--
ANA_ADCDATAB	r	0x009C	ADC channel 11 data register	--

10.5 Register Definition

10.5.1 ANA_REG1 Register

Table133. Description of each bit in ANA_REG1 of ADC

Bit	Name	Function	Notes
3:0	Rsvd	-	0
4	RESDIV	Enable resistor division for M ADC input signal	0: Disable 1: Enable 1/4 resistor division
5	GDE4	Enable cap division for M ADC input signal	0: Disable 1: Enable 1/4 cap division
7:6	Rsvd	-	0

10.5.2 ANA_REG3 Register

Table134. Description of each bit in ANA_REG3 of ADC

Bit	Name	Function	Notes
0	ADCPDN	ADC power up control signal. ADC automatic conversion should be disabled before ADC is powered down.	0: Power-down ADC 1: Power-up ADC
3	BGPPD	BGP power down control signal.	0: Power-up BGP 1: Power-down BGP
4	RCHPD	RCH (6.5536M RC) power down control signal	0: Power-up RCH 1: Power-down RCH
Note: RCH and PLL and ADC are related to BGP, must power-up BGP before power-up RCH or PLL or ADC. User can power down BGP by set BGPPD to 1 when BGP was not used in program. User could not power down BGP by set BGPPD to 1 when BGP was used in program, because the system has a protection function to ensure reliability. User can power down BGP in sleep mode whether BGP is used or not.			

10.5.3 ANA_INSTS Register

Table135. Description of ANA_INTSTS Register for ADC

Bit	Name	Type	Description	Default
1	INTSTS1	rc_w1	Interrupt flag of auto ADC conversion done. Read 0: Auto ADC conversion not complete. Read 1: Auto ADC conversion has done. Write 0: No effect. Write 1: clear this bit.	0x0
0	INTSTS0	rc_w1	Interrupt flag of manual ADC conversion done. Read 0: Manual ADC conversion not complete. Read 1: Manual ADC conversion has done. Write 0: No effect. Write 1: clear this bit.	0x0

10.5.4 ANA_INTEN Register

Table136. Description of ANA_INTEN Register for ADC

Bit	Name	Type	Description	Default
1	INTEN1	rw	Interrupt enable control of auto ADC conversion done. 0: Disable auto ADC conversion interrupt. 1: Enable auto ADC conversion interrupt.	0x0
0	INTEN0	rw	Interrupt enable control of manual ADC conversion done. 0: Disable manual ADC conversion interrupt.	0x0

			1: Enable manual ADC conversion interrupt.	

10.5.5 ANA_ADCCTRL Register

Table137. Description of ANA_ADCCTRL Register

Bit	Name	Type	Description	Default
31	MTRIG	rw	Manual ADC trigger. Write 0: No effect. Write 1: Start a manual ADC conversion. Read 0: Current manual ADC conversion is done. Read 1: Current manual ADC conversion is ongoing.	0x0
30	Rsvd	-	Reserved.	0
29	CICAON	rw	CIC filter always on control register. 0: CIC filter will be disabled when no ADC sample process is ongoing. 1: CIC filter will be enabled for all the time.	0x0
28	CICINV	rw	CIC filter input inversion. 0: No invert CIC filter input. 1: Invert CIC filter input.	0x0
27	CICSCA	rw	CIC output scale-down selection. 0: No scale down CIC filter's output. 1: Scale down CIC filter's output to 1/2.	0x0
26:24	CICSKIP	rw	CIC output skip control register. This register is used to control how many samples will be skipped at the beginning of ADC sample. If CICAON is 1 and the ADC channel is not changed, the CIC output will not be skipped by the ADC controller, this can be used for high speed capture to single channel. 0: Skip first 4 samples. 1: Skip first 5 samples. 2: Skip first 6 samples. 3: Skip first 7 samples. 4: No skip any sample. 5: Skip first 1 sample. 6: Skip first 2 samples. 7: Skip first 3 samples.	0x0
23:22	DSRSEL	rw	CIC down sampling rate control register. The higher down-sampling rate, the higher output data stability, and lower sampling rate. 0: 1/512 down-sampling rate. 1: 1/256 down-sampling rate.	0x0

			2: 1/128 down-sampling rate. 3: 1/64 down-sampling rate.	
21	AMODE	rw	Auto ADC mode control. 0: Capture single channel specified by ACH. 1: Capture multiple channels (0~11 channels) at one time.	0x0
20	MMODE	rw	Manual ADC mode control. 0: Capture single channel specified by MCH. 1: Capture multiple channels (0~11 channels) at one time.	0x0
19	Rsvd	-	Reserved.	0
18:16	AEN	rw	Auto ADC conversion enable control register. 0: Auto ADC conversion is off. 4: Auto ADC will be triggered by timer 0's overflow. 5: Auto ADC will be triggered by timer 1's overflow. 6: Auto ADC will be triggered by timer 2's overflow. 7: Auto ADC will be triggered by timer 3's overflow. Others: Reserved.	0x0
15:13	Rsvd	-	Reserved.	0
12	CLKSEL	rw	ADC clock source selection. 0: 6.5M RCH 1: PLLL	0x0
11:8	CLKDIV	rw	The ADC clock source is internal 6.5M RCH or PLLL. The typical ADC main clock is 1.6384MHz, if ADC clock source is 6.5M RCH, CLKDIV is calculated such as: CLKDIV=6.5536/1.6384-1=3.	0x0
7:4	ACH	rw	Auto ADC channel control. 0: Auto ADC capture ADC channel 0. 1: Auto ADC capture ADC channel 1. …. 11: Auto ADC capture ADC channel 11. 12~15: Reserved. This register is valid only when AMODE is 0. The ADC sampling channels show as the following table.	0x0
3:0	MCH	rw	Manual ADC channel control. 0: Manual ADC capture ADC channel 0. 1: Manual ADC capture ADC channel 1. …. 11: Auto ADC capture ADC channel 11.	0x0

			12~15: Reserved. This register is valid only when MMODE is 0. The ADC sampling channels show as the following table.	

Table138. The ADC Sampling Channels

Bit	Name	value
7:4	ACH	0000: GND; 0001: VDD 0010: BATRTC; 0011: ADC_CH3 0100: ADC_CH4; 0101: ADC_CH5 0110: ADC_CH6; 0111: ADC_CH7 1000: ADC_CH8; 1001: ADC_CH9 1010: TEMP; 1011: ADC_CH11 1100~1111: Reserved.
3:0	MCH	

10.5.6 ANA_ADCDATAx Register

Table139. Description of ANA_ADCDATAx Register

Bit	Name	Type	Description	Default
31:16	Rsvd	-	Reserved.	0
15:0	ADCDATAx	r	The result of ADC conversion will be stored in these registers. DATA0: Store conversion result of ADC channel 0. DATA1: Store conversion result of ADC channel 1. … DATA11: Store conversion result of ADC channel 11. For single channel conversion (MMODE is 0 or AMODE is 0), only the channel specified by MCH or ACH will be updated. For multi-channels conversion (MMODE is 1 or AMODE is 1), DATA0~DATA11 will be updated.	0x--

10.6 Measuring Battery Voltage and External Voltage

In the V85XX, ADC can be used to measure external voltage signals by ADC_CHx, and can be used to measure VDD/BATRTC signals.

ADC channel mode: single channel; multi-channel.

ADC trigger mode: auto triggered by timer; manual trigger.

Divider mode: no divider; resistive divider; capacitive divider. Resistance voltage divider has extra power consumption. Because there are 35kΩ resistors in the internal resistive divider network, this network consumes power:

$$P = U_D \times I_D = V \times \frac{V}{R_1 + R_2} = \frac{V^2}{35} \qquad \text{Equation 9-1}$$

The voltage of ordinary channels (ADC_CHx): channel 3, 4, 5, 6, 7, 8, 9 and 11.

The voltage of VDD channels: channel 1.

The voltage of BATRTC channels: channel 2.

User needs to check whether a and b (A and B) parameters of storage area used to store ADC coefficients are legal. If so, the data of the storage area is used for calculation; if not, the ADC coefficient is used for calculation with fixed parameters. The calculation formula is shown in Table46, voltage measuring range and formula. A and b (a and b) of ADC coefficients are shown in Table46.

Table140. Voltage measurement range and formula

Power	Channel	Divider Mode	Signal range (V)	Formula
3.3V	ADC_CHx	No divider	-0.2~1.2	If a and b parameters of ADC are valid, $V_{DC} = a1 \div 100000000 * X + b1 \div 100000000$ else $V_{DC} = 0.00003680 * X + 0.00205011$
		Resistive	-0.2~3.6	If a and b parameters of ADC are valid, $V_{DC} = a2 \div 100000000 * X + b2 \div 100000000$ else $V_{DC} = 0.00016425*X+0.03739179$
		Capacitive	-0.2~3.6	If a and b parameters of ADC are valid, $V_{DC} = a3 \div 100000000 * X + b3 \div 100000000$ else $V_{DC} = 0.00014051*X-0.00023322$
	VDD	Resistive	2.5~4.8	If a and b parameters of ADC are valid,

	channels			$V_{DC} = a4 \div 100000000 * X + b4 \div 100000000$ else $V_{DC} = 0.00015392*X+0.06667986+OffsetBatl \div 1000$
		Capacitive	2.5~4.6	If a and b parameters of ADC are valid, $V_{DC} = a5 \div 100000000 * X + b5 \div 100000000$ else $V_{DC} = 0.00014107*X-0.00699515+OffsetBatC \div 1000$
	BATRTC channels	Resistive	0.7~4.8	If a and b parameters of ADC are valid, $V_{DC} = a6 \div 100000000 * X + b6 \div 100000000$ else $V_{DC} = 0.00015392*X+0.06667986+OffsetBatl \div 1000$
		Capacitive	0.7~4.6	If a and b parameters of ADC are valid, $V_{DC} = a7 \div 100000000 * X + b7 \div 100000000$ else $V_{DC} = 0.00014107*X-0.00699515+OffsetBatC \div 1000$
5V	ADC_CHx	No divider	-0.2~1.2	If A and B parameters of ADC are valid, $V_{DC} = A1 \div 100000000 * X + B1 \div 100000000$ else $V_{DC} = 0.00003678 * X + 0.00235783$
		Resistive	-0.2~4.8	If A and B parameters of ADC are valid, $V_{DC} = A2 \div 100000000 * X + B2 \div 100000000$ else $V_{DC} = 0.00016129*X + 0.00673599$
		Capacitive	-0.2~4.6	If A and B parameters of ADC are valid, $V_{DC} = A3 \div 100000000 * X + B3 \div 100000000$ else $V_{DC} = 0.00014076*X-0.00753319$
	VDD channels	Resistive	2.5~4.8	If A and B parameters of ADC are valid, $V_{DC} = A4 \div 100000000 * X + B4 \div 100000000$ else

				$V_{DC} = 0.00015392*X+0.06667986+OffsetBatI \div 1000$
		Capacitive	2.5~4.6	If A and B parameters of ADC are valid, $V_{DC} = A5 \div 100000000 * X + B5 \div 100000000$ else $V_{DC} = 0.00014107*X-0.00699515+OffsetBatC \div 1000$
	BATRTC channels	Resistive	0.7~4.8	If A and B parameters of ADC are valid, $V_{DC} = A6 \div 100000000 * X + B6 \div 100000000$ else $V_{DC} = 0.00015392*X+0.06667986+OffsetBatI \div 1000$
		Capacitive	0.7~4.6	If A and B parameters of ADC are valid, $V_{DC} = A7 \div 100000000 * X + B7 \div 100000000$ else $V_{DC} = 0.00014107*X-0.00699515+OffsetBatC \div 1000$

In the above equations,

X=ADC_DATAx Equation 9-2

Where:

ADC_DATAx is the content of bytes located at addresses (0x40014270+4x), x is channel 0~11.

10.7 Measuring Temperature

When the ADC channel you choose is TEMPERATURE (CH10), you should not set capacitive division. The temperature measurement range is over -40~+85˚C.

It is recommended to measure temperature following steps:

1. Set ADC to start working.
   Users must set ADC CLK to 1.6384 MHz, and set DSRSEL to 1/512 down-sampling rate, with no voltage division or resistor division, then start ADC conversion.
2. Wait for read 1 from ANAINSTS (0x40014260)(ANAINTSTS0(bit 0)/ANAINSTS1(bit 1) in auto/manual mode), and then read the register ADC_DATAA (0x40014298).
3. Calibrate temperature T: (in unit of 8.8 format °C). The format of T is 16-bit signed value, including 8 bits integer and 8 bits fraction signed value. The actual temperature is equal to T/256.0. For example, 0x1880 means 24.5 °C.

$$T = \left(\left(P0 * \left((X * X) >> 16\right)\right) + P1 * X + P2\right) >> 8 \quad \text{Equation 9-3}$$

where X is the reading of register ADC_DATAA(in hexadecimal);

where P0 is the content of bytes located at addresses 0x40D00(16bit);

where P1 is the content of bytes located at addresses 0x40D02(16bit);

where P2 is calculated by the following equation:

$$P2 = P2' + (Tr - Tm) * 256 \qquad \text{Equation 9-4}$$

where P2' is the content of bytes located at addresses 0x40D04(32bit);

where Tr is the content of bytes located at addresses 0x40D70(32bit);

where Tm is the content of bytes located at addresses 0x40D74(32bit).

Note1: To enhance ADC data quality in the channel 10 for the temperature sensor, four-sample moving average is implemented. The four buffers used to average are first-in first-out queues, which are reset to zero by DPOR. Every time a user makes an ADC conversion, the hardware writes a data to the buffer, and calculates the average value of the data of the four buffers inside, and puts it in the register of ADC_DATAA. Therefore, in order to get the exact temperature value of a certain temperature, users need to convert ADC four times continuously and take the last ADC_DATAA register data as ADC data.

10.8 ADC Precautions

1. ADC auto trigger conversion process

   Turn on auto trigger ADC conversion steps: turn on ADC, configure and turn on timer.
   Turn off the auto trigger ADC conversion step: turn off the timer, and then turn off the ADC.

2. ADC related ANA_ ADCCTRL register write operation

   Before the register ANA_ ADCCTRL is written, it is necessary to ensure that the value read back by bit31 (mtrig) is 0, that is, the current ADC manual conversion has been completed.

11 Comparator Controller

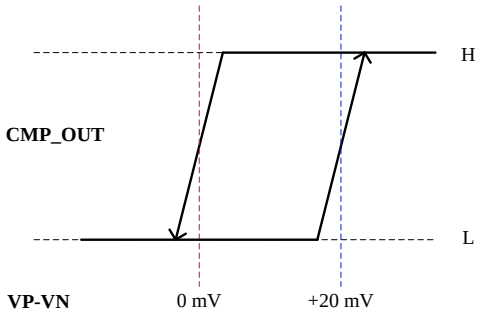
11.1 Introduction

The V85XX integrates two comparators to compare the analog signals. Three patterns can be selected as input sources:

- Positive signal input on pin CMP_P and negative signal input on pin CMP_N;
- Positive signal input on pin CMP_P and negative signal from BGPREF or VREF;
- Positive signal input on pin CMP_N and negative signal from BGPREF or VREF;
- Positive signal from VDD or BATRTC and negative signal from BGPREF or VREF.

Each comparator have hysteresis voltage of 20mV.

Figure23. hysteresis Window of CMP Controller

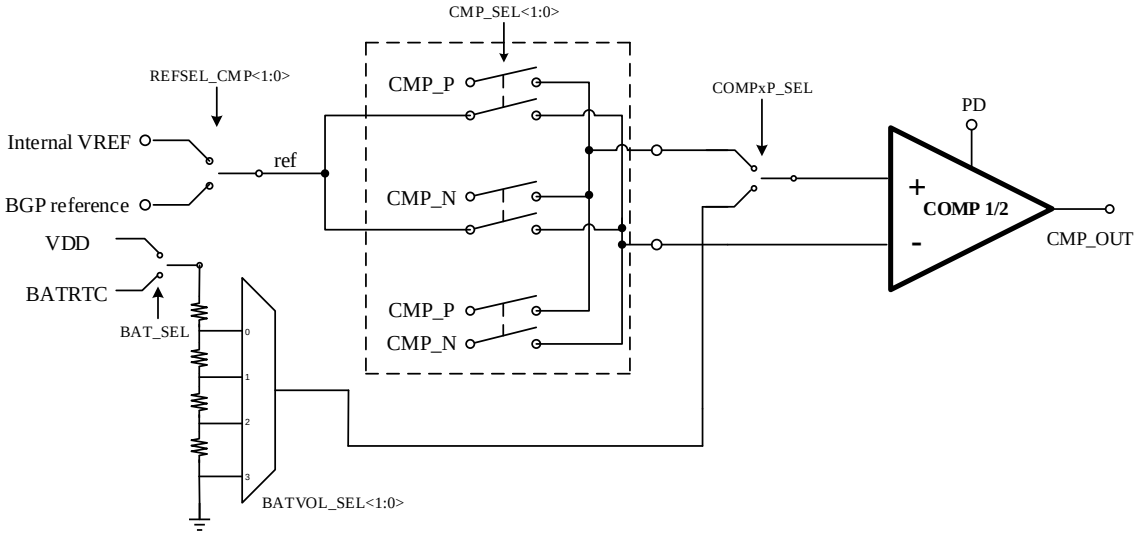


11.2 Feature

- Interrupt/wake-up signal generated for analog detect flag.
- Comparator interrupt generation.
- Comparator counter.

11.3 Block Diagram

Figure24. Functional Block Diagram of CMP Controller



11.4 Register Location

Table141. Register Location of ANA Controller for CMP (ANA Base: 0x40014200)

Name	Type	Address	Description	Default
ANA_REG2	rw	0x0008	Analog register 2	0x00
ANA_REG3	rw	0x000C	Analog register 3	0x00
ANA_REG5	rw	0x0014	Analog register 5	0x00
ANA_REGF	rw	0x003C	Analog register 15	0x00
ANA_CTRL	rw	0x0050	Analog control register	0x0000000
ANA_CMPOUT	r	0x0054	Comparator result register	0x0030
ANA_INTSTS	rc_w1	0x0060	Analog interrupt status register	0x0000
ANA_INTEN	rw	0x0064	Analog interrupt enable register	0x0000
ANA_CMPCNT1	rc_w1	0x00B0	Comparator 1 counter	0x00000000
ANA_CMPCNT2	rc_w1	0x00B4	Comparator 2 counter	0x00000000

11.5 Register Definition

11.5.1 ANA_REG2 Register

Table142. Description of each bit in ANA_REG2 for CMP

Bit	Name	Function	Notes
1:0	CMP1_SEL	Signal source selection of comparator 1	00：CMP1_P to REF 01: CMP1_N to REF 1*: CMP1_P to CMP1_N
3:2	CMP2_SEL	Signal source selection of comparator 2	00: CMP2_P to REF 01: CMP2_N to REF

			1*: CMP2_P to CMP2_N
4	REFSEL_CMP1	REF selection of CMP1	0: VREF 1: BGPREF.
5	REFSEL_CMP2	REF selection of CMP2	0: VREF 1: BGPREF.

11.5.2 ANA_REG3 Register

Table143. Description of each bit in ANA_REG3 for CMP

Bit	Name	Function	Notes
1	CMP1PDN	CMP1 power up control signal	0: Power-down CMP1 1: Power-up CMP1
2	CMP2PDN	CMP2 power up control signal	0: Power-down CMP2 1: Power-up CMP2
3	BGPPD	BGP power down control signal.	0: Power-up BGP 1: Power-down BGP
Note: RCH and PLL and ADC are related to BGP, You must power-up BGP before you power-up RCH or PLL or ADC. User can power down BGP by set BGPPD to 1 when BGP was not used in program. User could not power down BGP by set BGPPD to 1 when BGP was used in program, because the system has a protection function to ensure reliability. User can power down BGP in sleep mode whether BGP is used or not.			

11.5.3 ANA_REG5 Register

Table144. Description of each bit in ANA_REG5 for CMP

Bit	Name	Function	Notes
1:0	IT_CMP1	Bias current selection of CMP1	00: 20nA; 01: 100nA; 1*: 500nA;
3:2	IT_CMP2	Bias current selection of CMP2	00: 20nA; 01: 100nA; 1*: 500nA;
Note: The smaller the CMP bias current, the lower the power consumption and the longer the propagation delay time; the higher the CMP bias current, the higher the power consumption and the shorter the propagation delay time.			

11.5.4 ANA_REGF Register

Table145. Description of each bit in ANA_REGF for CMP

Bit	Name	Function	Notes
3	BAT_SEL	BAT selection of CMP	BAT selection 0: BTA1

			1: BATRTC
5:4	BATVOL_SEL	BAT voltage selection	BAT voltage selection 00: 2.6V 01: 2.4V 10: 2.2V 11: 2.0V
6	COMP1P_SEL	Positive signal selection of COMP1	0: Determined by CMP1_SEL 1: Determined by BAT_SEL
7	COMP2P_SEL	Positive signal selection of COMP2	0: Determined by CMP2_SEL 1: Determined by BAT_SEL

11.5.5 ANA_CTRL Register

Table146. Description of ANA_CTRL Register for CMP

Bit	Name	Type	Description	Default
23:22	CMP2DEB	rw	Comparator 2 de-bounce control register. 0: No de-bounce. 1: 2 RTCCLK de-bounce. 2: 3 RTCCLK de-bounce. 3: 4 RTCCLK de-bounce. When de-bounce is enabled, the input signal is valid only when the signal isn't change in multi-cycles of RTCCLK clock. And, the response time of the wake-up and interrupt will be delayed until the signal is valid. This circuit can work under all mode including sleep.	0x0
21:20	CMP1DEB	rw	Comparator 1 de-bounce control register. 0: No de-bounce. 1: 2 RTCCLK de-bounce. 2: 3 RTCCLK de-bounce. 3: 4 RTCCLK de-bounce. When de-bounce is enabled, the input signal is valid only when the signal isn't change in multi-cycles of RTCCLK clock. And, the response time of the wake-up and interrupt will be delayed until the signal is valid. This circuit can work under all mode including sleep mode.	0x0
19:18	Rsvd	-	Reserved.	0
3:2	COMP2_SEL	rw	This register is used to control the interrupt and wake-up signal generation of COMP2. 0: Off 1: Rising edge of COMP2. 2: Falling edge of COMP2.	0x0

			3: Change of COMP2.	
1:0	COMP1_SEL	rw	This register is used to control the interrupt and wake-up signal generation of COMP1. 0: Off 1: Rising edge of COMP1. 2: Falling edge of COMP1. 3: Change of COMP1.	0x0

11.5.6 ANA_CMPOUT Register

Table147. Description of ANA_CMPOUT Register for CMP

Bit	Name	Type	Description	Default
3	COMP2	r	This bit shows the output of comparator 2.	0x0
2	COMP1	r	This bit shows the output of comparator 1.	0x0

11.5.7 ANA_INSTS Register

Table148. Description of ANA_INTSTS Register for CMP

Bit	Name	Type	Description	Default
3	INTSTS3	rc_w1	Interrupt flag of COMP2, the interrupt generate condition is controlled by COMP2_SEL. Read 0: No COMP2 interrupt. Read 1: COMP2 interrupt is happened. Write 0: No effect. Write 1: Clear this bit.	0x0
2	INTSTS2	rc_w1	Interrupt flag of COMP1, the interrupt generate condition is controlled by COMP1_SEL. Read 0: No COMP1 interrupt. Read 1: COMP1 interrupt is happened. Write 0: No effect. Write 1: Clear this bit.	0x0

11.5.8 ANA_INTEN Register

Table149. Description of ANA_INTEN Register for CMP

Bit	Name	Type	Description	Default
3	INTEN3	rw	Interrupt and wake-up enable control of COMP2. 0: Disable COMP2 interrupt and wake-up. 1: Enable COMP2 interrupt and wake-up.	0x0
2	INTEN2	rw	Interrupt and wake-up enable control of COMP1. 0: Disable COMP1 interrupt and wake-up. 1: Enable COMP1 interrupt and wake-up.	0x0

11.5.9 ANA_CMPCNTx Register

Table150. Description of ANA_CMPCNTx Register

Bit	Name	Type	Description	Default
31:0	CNTx	rc_w1	This register store the happen times of comparator x according to the setting in COMPx_SEL. For example, when COMPx_SEL is set to 1, then this counter will increase 1 when the COMPx is rising. This register can be cleared by writing 0 to this register, but this operation is valid only when corresponded CMPPDNx is set to 1 (when the corresponded comparator is enabled).	0x0000000

12 PMU_WDT Unit

12.1 Introduction

In the V85XX, the embedded 24-bit watchdog timer (WDT) counting pulses of the 32kHz RTCCLK clock.

When the program gets stuck somewhere, the timer overflows and reset the system to cause the program start from the beginning. WDT's reset level is the same as POR reset, it can provide chip's internal reset.

12.2 Features

- WDT counting period: 512s\256s\128s\64s\2s\1s\0.5s\0.25s.
- Password protection to avoid close WDT in un-expected event.

12.3 WDT State in Different Modes

For different mode, the enable or disable of WDT module will be controlled by hardware or software, the following table shows the detail of WDT status under each mode when MODE (PMU_STS register bit24) is 1. If MODE (PMU_STS register bit24) is 0, WDT is invalid in all modes.

Table151. WDT Enable or Disable in Different Modes (MODE=1)

WDT	Power modes		
	Sleep	IDLE	Active
State	ON (WDTEN = 1) OFF (WDTEN = 0)	ON (WDTEN = 1) OFF (WDTEN = 0)	ON (WDTEN = 1) OFF (WDTEN = 0)
WDT	**Wake up from different modes**		
	Sleep	**IDLE**	
State	ON	ON (WDTEN = 1) OFF (WDTEN = 0)	

12.4 PMU Register Location

Table152. Register Location of the PMU_WDT Controller (PMU Base: 0x40014000)

Name	Type	Address	Description	Default

PMU_WDTPASS	rw	0x0040	Watch dog timing unlock register	0x00000000
PMU_WDTEN	rw	0x0044	Watch dog timer enable register	0x1
PMU_WDTCLR	w	0x0048	Watch dog timer clear register	0x0000
PMU_WDTSTS	rc_w1	0x0060	Watch dog timer status register.	0x00

12.5 PMU Register Definitions

12.5.1 PMU_WDTPASS Register

Table153. Description of PMU_WDTPASS Register

Bit	Name	Type	Description	Default
31:1	Rsvd	-	Reserved.	0
0	UNLOCK	r	This bit indicates the watch dog timer enable register has been unlocked and is ready to change the watch dog enable control register. To set this bit to 1, programmer should write 0xAA5555AA to this register. This bit will be cleared immediately after any register write to any PMU control register, including ICE write, so programmer should set the PMU_WDTEN immediately after the UNLOCK bit is set to 1, otherwise the UNLOCK procedure should start again.	0x0

12.5.2 PMU_WDTEN Register

Table154. Description of PMU_WDTEN Register

Bit	Name	Type	Description	Default
31:5	Rsvd	-	Reserved.	0
4:2	WDTSEL	rw	This register is used to control the WDT counting period. 0: 2 secs 1: 1 sec 2: 0.5 secs 3: 0.25 secs 4: 512s 5: 256 secs 6: 128 secs 7: 64 secs	0x0

			To change the value of this register, UNLOCK bit of PMU_WDTPASS should be set to 1 first.	
1	Rsvd	-	Reserved.	0
0	WDTEN	rw	This bit indicates the watch dog timer is enable. To change the value of this register, UNLOCK bit of PMU_WDTPASS should be set to 1 first.	0x1

12.5.3 PMU_WDTCLR Register

Table155. Description of PMU_WDTCLR Register

Bit	Name	Type	Description	Default
31:24	Rsvd	-	Reserved.	0
23:0	WDTCNT	rc_w1	This register shows the current counter value of wat dog timer. When this timer count to limit value set by WDTSEL, the WDT will issue a system reset. So programmer should clear this timer in a regulator time to avoid WDT reset. To clear this timer programmer should write 0x55AAAA55 to this register. During debug mode, this register will be cleared to 0 automatically and no WDT reset will be issued under the debug mode.	0x0

12.5.4 PMU_WDTSTS Register

Table156. Description of PMU_WDTSTS Register

Bit	Name	Type	Description	Default
31:1	Rsvd	-	Reserved.	0
0	WDTSTS	rc_w1	This register indicates that a WDT reset has happened. Programmer can read this bit to know if this time is the WDT reset. Write 1 to this bit can clear this flag.	0x0

13 RTC Controller

13.1 Introduction

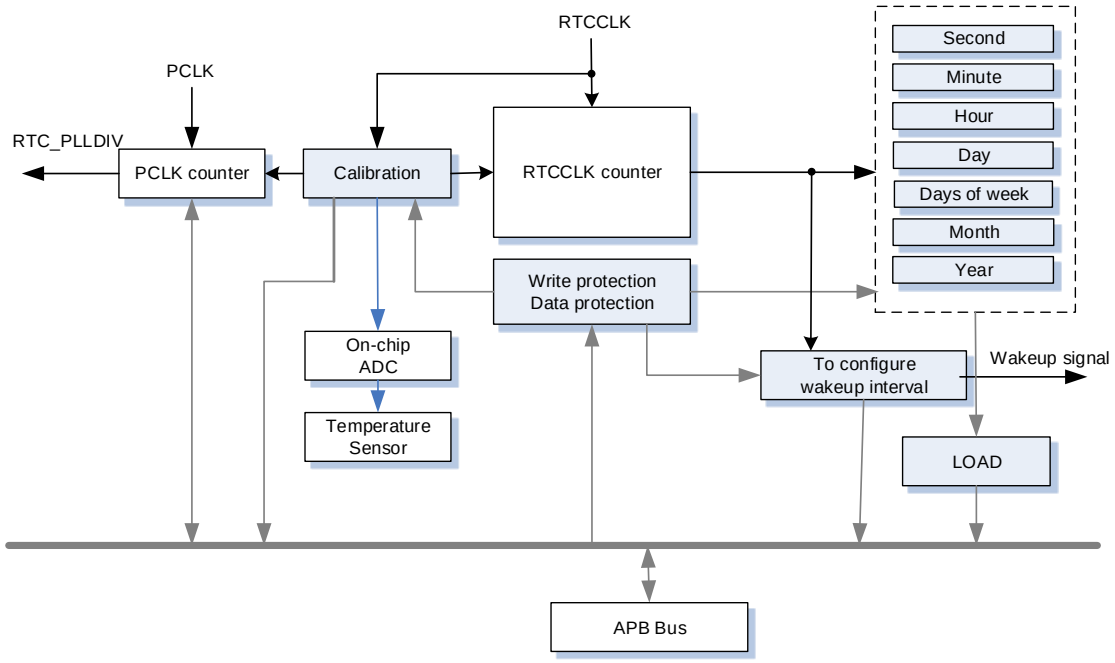
The RTC controller is used to control time calculation. The time calculation function can realize the year, month, week, day, hour, minute, second automatically calculation function and the leap year detection. There are also multi-second, multi-minutes, and multi-hours auto wake-up timer embedded in the RTC engine.

13.2 Feature

- BCD format Time Calculation from second to year.
- Automatically leap year detection.
- Automatic temperature detection.
- 32768 frequency compensation.
- Programmable multiple wake-up source.
- Initialize calibration engine for manufactory.
- RTC clock scaling for lower power consumption under sleep mode.

13.3 Block Diagram

Figure25. Functional Block Diagram of RTC Controller



13.4 Reading and Writing of RTC Register

13.4.1 Writing of RTC

In the V85XX, some RTC registers are protected by write protection, including RTC timing registers and RTC calibration registers and so on. For details, please refer to the Table157.

The MCU must write of these registers following steps as:

1. User must wait until BSY (bit1 of register RTC_CE) is 0, to ensure the state of RTC is idle;
2. Writing 0x5AA55AA5 to the register RTC_PWD to enable the RTC_CE port's access;
3. Writing 0xA55AA55B to the register RTC_CE to enable writing of write protection registers.
4. Configuring write protection registers. RTC_SEC ~ RTC_YEAR register should be configured together;
5. Writing 0x5AA55AA5 to the register RTC_PWD to enable the RTC_CE port's access;
6. Writing 0xA55AA55A to the register RTC_CE to clear CE (bit0 of register RTC_CE) flag, and BSY (bit1 of register RTC_CE) flag will be set immediately after the CE is cleared from 1 to 0. After CE is cleared to 0, the contents of write protection registers update to RTC core will be start. The update procedure take around 3 32K period, which is around 100us.
7. User must wait until BSY (bit1 of register RTC_CE) cleared to 0 automatically after sixth step configuration, to ensure RTC update is done.

The MCU can write a register that without write protection directly.

13.4.2 Reading of RTC

RTC timing registers are protected from reading. For details, please refer to Table157.

To read the timing registers, the MCU must read these registers following steps as:

1. User must wait until BSY (bit1 of register RTC_CE) is 0, to ensure the state of RTC is idle;
2. The MCU must read register RTC_LOAD firstly, BSY (bit1 of register RTC_CE) will be set immediately when RTC_LOAD port is read by MCU. BSY will be cleared automatically after the read procedure is done, the read procedure take around 3 32K period, which is around 100 μs;
3. After the read procedure of RTC_LOAD is done, the current timed will be latched and programmer can read data from RTC_SEC ~ RTC_YEAR register.

The MCU can read a register that without read protection directly.

13.5 Register Location

The following table shows the register location of each register. The column "Write Protect means the register can only be written when CE is set to 1, and will be updated to RTC core only when CE is cleared to 0. The column "Read protect" means the value in these registers will be updated only when RTC_LOAD port is read and BSY bit is cleared to 0.

Table157. RTC Registers Map

Register Name	Offset	Type	Reset Value	Description
RTC_SEC	0x0000	rw	0x0000_0000	RTC register in seconds
RTC_MIN	0x0004	rw	0x0000_0000	RTC register in minutes
RTC_HOUR	0x0008	rw	0x0000_0000	RTC register in hours
RTC_DAY	0x000C	rw	0x0000_0000	RTC register in days
RTC_WEEK	0x0010	rw	0x0000_0000	RTC register in weeks
RTC_MON	0x0014	rw	0x0000_0000	RTC register in months
RTC_YEAR	0x0018	rw	0x0000_0000	RTC register in years
RTC_WKUSEC	0x0020	rw	0x0000_0000	RTC second wake-up register
RTC_WKUMIN	0x0024	rw	0x0000_0000	RTC minute wake-up register
RTC_WKUHOUR	0x0028	rw	0x0000_0000	RTC hour wake-up register
RTC_WKUCNT	0x002C	rw	0x0000_0000	RTC counter wake-up register
RTC_CAL	0x0030	rw	0x0000_0000	RTC calibration register
RTC_DIV	0x0034	rw	0x0000_0000	RTC_PLLDIV division register
RTC_CTL	0x0038	rw	0x0000_0000	RTC_PLLDIV divide control register
RTC_PWD	0x0044	rw	0x0000_0000	RTC password control register
RTC_CE	0x0048	rw	0x0000_0000	RTC write enable control register
RTC_LOAD	0x004C	rw	0x0000_0000	RTC read enable control register
RTC_INTSTS	0x0050	rw	0x0000_0000	RTC interrupt status register
RTC_INTEN	0x0054	rw	0x0000_0000	RTC interrupt status register
RTC_PSCA	0x0058	rw	0x0000_0000	RTC clock pre-scaler control register
RTC_ACTI	0x0084	rw	0x0000_1800	Crytstal vertex temperature register
RTC_ACF200	0x0088	rw	0x0064_0000	RTC 200*frequency register
RTC_ACADCW	0x008C	rw	0x0000_0000	RTC manual ADC value control register
RTC_ACPx[0..7,0x4]	0x0090	rw	0x0000_0000	RTC parametric x register
RTC_ACKx[1..5,0x4]	0x00B0	rw	0x0000_0000	RTC parametric k x register
RTC_ACTEMP	0x00C4	r	0x0000_0000	RTC calculated temperature register
RTC_ACPPM	0x00C8	r	0x0000_0000	RTC calculated PPM register
RTC_WKUCNTR	0x00CC	r	0x0000_0000	Record the current WKUCNT value
RTC_ACKTEMP	0x00D0	rw	0x3C28_00EC	RTC control register for K coefficient temperature sections

RTC registers without write protection can be reset under external reset or power-on reset or watch-dog reset, other registers cannot be reset under one of reset external reset or watch-dog reset events. RTC registers with write protection(except RTC_SEC、RTC_MIN、RTC_HOUR、RTC_DAY、RTC_WEEK、RTC_MON、RTC_YEAR、RTC_CAL) can be reset under power-on reset

13.6 Register Definition

13.6.1 RTC_SEC/MIN/DAY/WEEK/MONTH/YEAR Register

The time register is following the BCD encode, where the bit 7~4 is represent the 10's digit and bit 3~0 is for 1's digit. The value in these registers can be set only when CE is high, and it will be update to RTC core only when the CE is cleared from 1 to 0. To read current time, programmer should process a read operation to RTC_LOAD register, and wait until the BSY bit is cleared. Otherwise, the register value will be invalid.

Table158. Description of RTC_SEC/MIN/DAY/WEEK/MONTH/YEAR Register

Register		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x0000	RTC_SEC, 0~59	-	S40	S20	S10	S8	S4	S2	S1
0x0004	RTC_MIN, 0~59	-	M40	M20	M10	M8	M4	M2	M1
0x0008	RTC_HOUR,0~23	-	-	H20	H10	H8	H4	H2	H1
0x000C	RTC_DAY, 1~31	-	-	D20	D10	D8	D4	D2	D1
0x0010	RTC_WEEK, 0~6	-	-	-	-	-	W4	W2	W1
0x0014	RTC_MON, 1~12	-	-	-	Mo10	Mo8	Mo4	Mo2	Mo1
0x0018	RTC_YEAR, 00~99	Y80	Y40	Y20	Y10	Y8	Y4	Y2	Y1
Default		X	X	X	X	X	X	X	X
"week" can only be set by user, RTC will not detect automatically. After initialize setting, RTC will increase the week count automatically. For example, when user set 2010/1/1 as Friday, RTC will detect 2010/01/02 as Saturday. W4/W2/W1:000, Sunday; 001, Monday; 010, Tuesday; 011, Wednesday; 100, Thursday; 101, Friday; 110, Saturday. System can only set the last two digit of year, for example, when setting year 2010, RTC_YEAR should be set as 0b00010000.									

13.6.2 RTC_SEC Register

Table159. RTC_SEC Register Description

Bit	Name	Type	Description
31:7	Rsvd	-	Reserved.
6:0	SEC	rw	RTC second register

13.6.3 RTC_MIN Register

Table160. RTC_MIN Register Description

Bit	Name	Type	Description
31:7	Rsvd	-	Reserved.
6:0	MIN	rw	RTC minute register

13.6.4 RTC_HOUR Register

Table161. RTC_HOUR Register Description

Bit	Name	Type	Description
31:6	Rsvd	-	Reserved.
5:0	HOUR	rw	RTC hour register

13.6.5 RTC_DAY Register

Table162. RTC_DAY Register Description

Bit	Name	Type	Description
31:6	Rsvd	-	Reserved.
5:0	DAY	rw	RTC day register

13.6.6 RTC_WEEK Register

Table163. RTC_WEEK Register Description

Bit	Name	Type	Description
31:3	Rsvd	-	Reserved.
2:0	WEEK	rw	RTC week register

13.6.7 RTC_MON Register

Table164. RTC_MON Register Description

Bit	Name	Type	Description
31:5	Rsvd	-	Reserved.
4:0	MON	rw	RTC month register

13.6.8 RTC_YEAR Register

Table165. RTC_YEAR Register Description

Bit	Name	Type	Description
31:8	Rsvd	-	Reserved.
7:0	YEAR	rw	RTC year register

13.6.9 RTC_WKUSEC Register

Table166. RTC_WKUSEC Register Description

Bit	Name	Type	Description
31:6	Rsvd	-	Reserved.

5:0	WKUSEC	rw	This register is used to control the multi-second wake-up function. The wake-up period is (WKUSEC + 1)*1 second. When the INTEN[2] is 1 and the internal wake-up second count is reach the target value, the INTSTS[2] will be set to 1 and wake-up signal will be asserted to PMU controller. For the first interrupt generated by WKUSEC, it may have < 1 sec error if the new WKUSEC number is not equal to current WKUSEC number. If the new WKUSEC is equal to current WKUSEC, the first interrupt time may have 0~(WKUSEC +1) variation. To avoid this problem, set an alternative value (like 0) to this register and update it with RTC_CE operation. Then set the correct value to it.

13.6.10 RTC_WKUMIN Register

Table167. RTC_WKUMIN Register Description

Bit	Name	Type	Description
31:6	Rsvd	-	Reserved.
5:0	WKUMIN	rw	This register is used to control the multi-minute wake-up function. The wake-up period is (WKUMIN + 1)*1 minute. When the INTEN[3] is 1 and the internal wake-up minute count is reach the target value, the INTSTS[3] will be set to 1 and wake-up signal will be asserted to PMU controller. For the first interrupt generated by WKUMIN, it may have < 1 minute error if the new WKUMIN number is not equal to current WKUMIN number. If the new WKUMIN is equal to current WKUMIN, the first interrupt time may have 0~(WKUMIN +1) variation. To avoid this problem, set an alternative value (like 0) to this register and update it with RTC_CE operation. Then set the correct value to it.

13.6.11 RTC_WKUHOUR Register

Table168. RTC_WKUHOUR Register Description

Bit	Name	Type	Description
31:5	Rsvd	-	Reserved.
4:0	WKUHOUR	rw	This register is used to control the multi-hour wake-up function. The wake-up period is (WKUHOUR + 1)*1 hour. When the INTEN[4] is 1 and the internal wake-up hour count is reach the target value, the INTSTS[4] will be set to 1 and wake-up signal will be asserted to PMU

			controller. For the first interrupt generated by WKUHOUR, it may have < 1 hour error if the new WKUHOUR number is not equal to current WKUHOUR number. If the new WKUHOUR is equal to current WKUHOUR, the first interrupt time may have 0~(WKUHOUR +1) variation. To avoid this problem, set an alternative value (like 0) to this register and update it with RTC_CE operation. Then set the correct value to it.

13.6.12 RTC_WKUCNT Register

Table169. RTC_WKUCNT Register Description

Bit	Name	Type	Description
31:26	Rsvd	-	Reserved.
25:24	CNTSEL	rw	This is register is used to set the counter clock of WKUCNT. When PSCA is 0. 0: Counter clock is 32768Hz 1: Counter clock is 2048Hz. 2: Counter clock is 512Hz 3: Counter clock is 128Hz When PSCA is 1. 0: Counter clock is 8192Hz 1: Counter clock is 2048Hz. 2: Counter clock is 512Hz 3: Counter clock is 128Hz
23:0	WKUCNT	rw	This register is used to control the 32K counter wake-up function. The wake-up period is (WKUCNT + 1)*Counter Clock Cycle. The counter clock is controlled by CNTSEL. When the INTEN[6] is 1 and the internal wake-up count is reach the target value, the INTSTS[6] will be set to 1 and wake-up signal will be asserted to PMU controller.

13.6.13 RTC_CAL Register

Table170. RTC_CAL Register Description

Bit	Name	Type	Description
31:14	Rsvd	-	Reserved.
13:0	CAL	rw	RTC 32768 calibration register, this register is a 14 bits signed value. The RTC engine will do calibration for every 30 seconds, the internal counter will count 32768 times during 1~29 second. At the 30 second, it will count [32768-(CAL-1)] for a second, so it can let the average 1

			second pulse in 30 seconds become an accurate 1 second pulse. The PPM resolution of the CAL register is 1.02ppm, and the adjustable range is ±8332.3ppm (±12 minutes/day).

13.6.14 RTC_DIV Register

Table171. RTC_DIV Register Description

Bit	Name	Type	Description
31:26	Rsvd	-	Reserved.
25:0	RTCDIV	rw	This register is used to generate divider output. The output frequency is PCLK/(2*(RTCDIV+1)).

13.6.15 RTC_CTL Register

Table172. RTC_CTL Register Description

Bit	Name	Type	Description
31:3	Rsvd	-	Reserved.
2	RTCPLLOE	rw	RTC_PLLDIV Divider output enable, this register is used to control the RTC_PLLDIV output. 0: Disable RTC_PLLDIV output. 1: Enable RTC_PLLDIV output. The RTC_PLLDIV output is at IOA[3] or IOA[7], the PMU_IOASEL bit 3 or 7 should also be set to 1 when RTC_PLLDIV output is enabled.
1:0	Rsvd	-	Reserved.

13.6.16 RTC_PWD Register

Table173. RTC_PWD Register Description

Bit	Name	Type	Description
31:1	Rsvd	-	Reserved.
0	PWDEN	r	This register is used to protect the RTC_CE port's access. Before access the RTC_CE, programmer should write 0x5AA55AA5 to this port, and the PWDEN will be set to 1. This bit will be cleared automatically after any write to RTC_CE port. Which means programmer should write to this port again before next access to RTC_CE port.

13.6.17 RTC_CE Register

Table174. RTC_CE Register Description

Bit	Name	Type	Description
31:2	Rsvd	-	Reserved.
1	BSY	r	This flag is used to indicate the RTC update procedure or RTC read procedure is ongoing. This bit will be set immediately after the CE is cleared from 1 to 0 or when RTC_LOAD port is read by CPU. This bit will be cleared automatically after the read or write procedure is done. Programmer can poll this bit to know if the RTC update is done or not. The update or read procedure take around 3 32K period, which is around 100 μS.
0	CE	r	This register is used to unlock the access to RTC register. This register can be only when PWDEN is set to 1 and 0xA55AA55B is written to this register. After this bit is set to 1, the RTC register can be programmed, but the actual update to RTC core will be start after this bit is cleared to 0. To clear this bit, the PWDEN should be set to 1 and 0xA55AA55A should be written to this register.

13.6.18 RTC_LOAD Register

Table175. RTC_LOAD Register Description

Bit	Name	Type	Description
31:0	LOAD	rw	This register is used to let RTC engine read data from RTC core. When programmer read from this port, the current time will be latched and programmer can read data from RTC_SEC ~ RTC_YEAR register. The read procedure will takes 3 RTCCLK cycles, programmer can check the BSY bit to know if the procedure is done. The read data from this port is invalid.

13.6.19 RTC_INTSTS Register

Table176. RTC_INTSTS Register Description

Bit	Name	Type	Description
31:9	Rsvd	-	Reserved.
8	INTSTS8	rc_w1	Interrupt status 8, this interrupt will be set when an illegal write to CE register is happened. The illegal write means the BSY bit is still 1 but CE is set to 1 again or RTC_LOAD port is read again. Write 1 to clear this bit.

7	Rsvd	-	Reserved.
6	INTSTS6	rc_w1	Interrupt status 6, this interrupt will be set when 32K counter interrupt period set by WKUCNT is reach. Write 1 to clear this bit.
5	INTSTS5	rc_w1	Interrupt status 5, this interrupt will be set when mid-night (00:00) is reach. Write 1 to clear this bit.
4	INTSTS4	rc_w1	Interrupt status 4, this interrupt will be set when multi-hour interrupt period set by WKUHOUR is reach. Write 1 to clear this bit.
3	INTSTS3	rc_w1	Interrupt status 3, this interrupt will be set when multi-minute interrupt period set by WKUMIN is reach. Write 1 to clear this bit.
2	INTSTS2	rc_w1	Interrupt status 2, this interrupt will be set when multi-second interrupt period set by WKUSEC is reach. Write 1 to clear this bit.
1	INTSTS1	rc_w1	Interrupt status 1, this interrupt will be set when illegal time format is written into RTC core. Write 1 to clear this bit.
0	Rsvd	-	Reserved.

13.6.20 RTC_INTEN Register

Table177. RTC_INTEN Register Description

Bit	Name	Type	Description
31:9	Rsvd	-	Reserved.
8	INTEN8	rw	Interrupt enable 8, when this bit is 1, the INTSTS8 interrupt will be asserted to CPU.
7	Rsvd	-	Reserved.
6	INTEN6	rw	Interrupt enable 6, when this bit is 1, the INTSTS6 interrupt will be asserted to CPU and wake-up signal will be asserted to PMU controller.
5	INTEN5	rw	Interrupt enable 5, when this bit is 1, the INTSTS5 interrupt will be asserted to CPU and wake-up signal will be asserted to PMU controller.
4	INTEN4	rw	Interrupt enable 4, when this bit is 1, the INTSTS3 interrupt will be asserted to CPU and wake-up signal will be asserted to PMU controller.
3	INTEN3	rw	Interrupt enable 3, when this bit is 1, the INTSTS3 interrupt will be asserted to CPU and wake-up signal will be asserted to PMU controller.
2	INTEN2	rw	Interrupt enable 2, when this bit is 1, the INTSTS2 interrupt will be asserted to CPU and wake-up signal will be asserted to PMU controller.

1	INTEN1	rw	Interrupt enable 1, when this bit is 1, the INTSTS1 interrupt will be asserted to CPU and wake-up signal will be asserted to PMU controller.
0	Rsvd	-	Reserved.

13.6.21 RTC_PSCA Register

Table178. RTC_PSCA Register Description

Bit	Name	Type	Description
31:2	Rsvd	-	Reserved.
1:0	PSCA	rw	This register is used to control the RTCCLK pre-scaler. When slow down the RTCCLK, it can significantly reduce the power under sleep mode. 0: No pre-scaler, RTC clock is 32768 Hz. 1: 1/4 pre-scaler, RTC clock is 8192 Hz. 2~3: Reserved. When this register is set, all modules which is using RTCCLK will be affected. The RTC time counter and LCD frame rate will be automatically adjusted by hardware, so no need to modify the setting. But the RTC_WKUCNT's input clock will be changed, so programmer should modify the corresponded setting. And the UART 32K baud rate register need to be re-calculated according to new RTCCLK speed.

13.6.22 RTC_ACTI Register

Table179. RTC_ACTI Register Description

Bit	Name	Type	Description
31:14	Rsvd	-	Reserved.
13:0	ACTI	rw	Ti control register. This register is used to store the Ti value which is used as the center temperature during calibration. This register is 8 bits integer and 8 bits fraction value. This register can be updated only when CE is 1, and should be a fixed value when ACEN is 1. For example, 0x1880 means 24.5 degree (24.5*256=6272=0x1880), 0xE780 means -24.5 degree(~0x1880+1=0xE780).

13.6.23 RTC_ACF200 Register

Table180. RTC_ACF200 Register Description

Bit	Name	Type	Description
31:26	Rsvd	-	Reserved.
25:0	F200	rw	This register is used to store the current PCLK speed value which is used for the calculation of PLLDIV value. This register is 26 bits integer. For example, when current PCLK speed is 6.5536MHz, then programmer should fill 6553600/2 = 0x320000 into this register. At the same time, the P6 should also be changed according to the following equation. P6 = 0.0004096 * F200. This register can be updated only when CE is 1, and should be fixed value when ACEN is 1.

13.6.24 RTC_ACADCW Register

Table181. RTC_ACADCW Register Description

Bit	Name	Type	Description
31:16	Rsvd	-	Reserved.
15:0	ADCW	rw	This register is used to store the manual ADC value which is used for the calculation for temperature. This register is 16 bits integer. This register is valid only when ADCSEL is set to 1.

13.6.25 RTC_ACPx Register

Table182. RTC_ACPx Register Description

Bit	Name	Type	Description
31:0	P0~P7	rw	The P0~P7 registers are used for calibration. Only P2 is 32 bits signed value, other P0~P7 is 16 bits signed value. P3 is read only and will be updated automatically according to calculated temperature. These registers can be updated only when CE is 1, and should be fixed value when ACEN is 1. Please refer to FLASH control section for detail.

13.6.26 RTC_ACKx Register

Table183. RTC_ACKx Register Description

Bit	Name	Type	Description
31:16	Rsvd	-	Reserved.
15:0	K1~K5	rw	The K1~K5 registers are used for calibration. These

			registers are 16 bits signed register. Hardware will auto select a suitable Kx according to calculated temperature T and update to RTC_ACP3 register. K1: T< KTEMP1. K2: KTEMP1≤T< KTEMP2. K3: KTEMP2≤T< KTEMP3. K4: KTEMP3≤T< KTEMP4. K5: T≥KTEMP4. These registers can be updated only when CE is 1, and should be fixed value when ACEN is 1.

13.6.27 RTC_ACKTEMP Register

Table184. RTC_ACKTEMP Register Description

Bit	Name	Type	Description
31:24	KTEMP4	rw	This register is used to control the section 4 temperature. This is a signed 8 bits value. This register can be updated only when CE is 1, and should be a fixed value when ACEN is 1.
23:16	KTEMP3	rw	This register is used to control the section 3 temperature. This is a signed 8 bits value. This register can be updated only when CE is 1, and should be a fixed value when ACEN is 1.
15:8	KTEMP2	rw	This register is used to control the section 2 temperature. This is a signed 8 bits value. This register can be updated only when CE is 1, and should be a fixed value when ACEN is 1.
7:0	KTEMP1	rw	This register is used to control the section 1 temperature. This is a signed 8 bits value. This register can be updated only when CE is 1, and should be a fixed value when ACEN is 1.

13.6.28 RTC_ACTEMP Register

Table185. RTC_ACTEMP Register Description

Bit	Name	Type	Description
31:16	Rsvd	-	Reserved.
15:0	TEMP	r	This register is used to store the calculated result of current temperature, and this is a 16 bits signed value. The format in this register is 8 bits integer and 8 bits fraction signed value. The actual temperature is equal to T/256.0. For example, 0x1880 means 24.5

			degree(24.5*256=6272=0x1880), 0xE780 means -24.5 degree(~0x1880+1=0xE780).

13.6.29 RTC_ACPPM Register

Table186. RTC_ACPPM Register Description

Bit	Name	Type	Description
31:16	Rsvd	-	Reserved.
15:0	PPM	r	This register is used to store the calculated result the offset of 32768 external crystal's current temperature. This register is a 16-bit signed value and the unit of this register is 0.1 PPM.

13.6.30 RTC_WKUCNTR Register

Table187. RTC_WKUCNTR Register Description

Bit	Name	Type	Description
31:24	Rsvd	-	Reserved.
23:0	WKUCNTR	r	This register is used to represent the current WKUCNT value. WKUCNTR increases from 0 to WKUCNT. Accumulating from 0, after reaching the WKUCNT setting value, continue to accumulate from 0 again.

13.7 Info information register（Related to RTC-Cal）

The RTC calibration data is stored in Info Sector 4 (0x40800). The address 0x40800 ~ 0x409FF data is written by downloading tool (offline download and RTC calibration). Other data is written before leaving factory. The following table shows the details of this information.

Info Sector data can only be read and cannot be written. All information has a backup. The first data in the form is expressed in 1, and second copies in 2. Each data has a checksum data. Checksum algorithm: add up each data, and reverse the result.

Table188. Info Information Register (Related to RTC-Cal)

Address	Sign	Data	Description
0x00040800	P4	RTC normal temperature offset 1	Load low 16 bits to RTC_ACP4 register, such as 0. unit(0.1ppm),
0x00040804		Check sum 1	INV(SUM(0x40800,0x40800))
0x00040808	P4	RTC normal temperature offset 2	Load low 16 bits to RTC_ACP4 register, such as 0. unit(0.1ppm),
0x0004080C		Check sum 2	INV(SUM(0x40808,0x40808))
0x00040810	K1	Crystal secondary	Load to RTC_ACK1 register. K1 is

		calibration coefficient K1 1	calculated as follows: K1=B1/1000000*65536, B1 is the segment factor of crystal oscillator' quadratic curve. For example, the value of K1 is 20827.
0x00040814	K2	Crystal secondary calibration coefficient K2 1	Load to RTC_ACK2 register. K2 is calculated as follows: K2=B2/1000000*65536, B2 is the segment factor of crystal oscillator' quadratic curve. For example, the value of K2 is 21496.
0x00040818	K3	Crystal secondary calibration coefficient K3 1	Load to RTC_ACK3 register. K3 is calculated as follows: K3=B3/1000000*65536, B3 is the segment factor of crystal oscillator' quadratic curve. For example, the value of K3 is 22020.
0x0004081C	K4	Crystal secondary calibration coefficient K4 1	Load to RTC_ACK4 register. K4 is calculated as follows: K4=B4/1000000*65536, B4 is the segment factor of crystal oscillator' quadratic curve. For example, the value of K4 is 24517.
0x00040820	K5	Crystal secondary calibration coefficient K5 1	Load to RTC_ACK5 register. K5 is calculated as follows: K5=B5/1000000*65536, B5 is the segment factor of crystal oscillator' quadratic curve. For example, the value of K5 is 25257.
0x00040824		Check sum 1	INV(SUM(0x40810, 0x40820))
0x00040828	K1	Crystal secondary calibration coefficient K1 2	Load to RTC_ACK1 register. K1 is calculated as follows: K1=B1/1000000*65536, B1 is the segment factor of crystal oscillator' quadratic curve. For example, the value of K1 is 20827.
0x0004082C	K2	Crystal secondary calibration coefficient K2 2	Load to RTC_ACK2 register. K2 is calculated as follows: K2=B2/1000000*65536, B2 is the segment factor of crystal oscillator' quadratic curve. For example, the value of K2 is 21496.
0x00040830	K3	Crystal secondary calibration coefficient K3	Load to RTC_ACK3 register. K3 is calculated as follows:

		2	K3=B3/1000000*65536, B3 is the segment factor of crystal oscillator' quadratic curve. For example, the value of K3 is 22020.
0x00040834	K4	Crystal secondary calibration coefficient K4 2	Load to RTC_ACK4 register. K4 is calculated as follows: K4=B4/1000000*65536, B4 is the segment factor of crystal oscillator' quadratic curve. For example, the value of K4 is 24517.
0x00040838	K5	Crystal secondary calibration coefficient K5 2	Load to RTC_ACK5 register. K5 is calculated as follows: K5=B5/1000000*65536, B5 is the segment factor of crystal oscillator' quadratic curve. For example, the value of K5 is 25257.
0x0004083C		Check sum 2	INV(SUM(0x40828, 0x40838))
0x00040840	ACTI	Fixed point temperature of crystal 1	Load to RTC_ACTI register, such as 0x1800
0x00040844		Check sum 1	INV(SUM(0x40840,0x40840))
0x00040848	ACTI	Fixed point temperature of crystal 2	Load to RTC_ACTI register, such as 0x1800
0x0004084C		Check sum 2	INV(SUM(0x40848,0x40848))
0x00040850	KTEMPx(x=4~1)	Temperature section division settings 1	Load to RTC_ACKTEMP register, such as 0x3C2800EC
0x00040854		Check sum 1	INV(SUM(0x40850,0x40850))
0x00040858	KTEMPx(x=4~1)	Temperature section division settings 2	Load to RTC_ACKTEMP register, such as 0x3C2800EC
0x0004085C		Check sum 2	INV(SUM(0x40858,0x40858))
0x00040D00	P1/P0	RTC_ACP1/0 set 1	Load the high 16 bits to RTC_ACP1 register, such as 1060; Load the low 16 bits to RTC_ACP0, such as -214.
0x00040D04	P2'	RTC_ACP2 set 1	The value in this register is recorded as P2', such as -19746971. According to the formula P2=P2'+(Tr-Tm)*256 to calculate P2, and load P2 to RTC_ACP2 register.
0x00040D08	P5	RTC_ACP5 set 1	Load the high 16 bits to RTC_ACP5 register, such as 6444, and the low 16

			bits be abandon.
0x00040D0C	P7/P6’	RTC_ACP 7/6 set 1	Load the high 16 bits to RTC_ACP7 register, such as 0; Load the low 16 bits to P6’ register, such as 1342. According to the formula: P6=a*P6’ to calculate P6, where a=PCLK/6553600.
0x00040D10		Check Sum set 1	INV(SUM(0x40DE0, 0x40DEC))
0x00040D14	P1/P0	RTC_ACP1/0 set 2	Load the high 16 bits to RTC_ACP1 register, such as 1060; Load the low 16 bits to RTC_ACP0, such as -214.
0x00040D18	P2’	RTC_ACP2 set 2	The value in this register is recorded as P2’, such as -19746971. According to the formula P2=P2’+(Tr-Tm)*256 to calculate P2, and load P2 to RTC_ACP2 register.
0x00040D1C	P5	RTC_ACP5 set 2	Load the high 16 bits to RTC_ACP5 register, such as 6444, and the low 16 bits be abandon.
0x00040D20	P7/P6’	RTC_ACP 7/6 set 2	Load the high 16 bits to RTC_ACP7 register, such as 0; Load the low 16 bits to P6’ register, such as 1342. According to the formula: P6=a*P6’ to calculate P6, where a=PCLK/6553600.
0x00040D24		Check Sum set 2	INV(SUM(0x40DF4, 0x40E00))
0x00040D70	Tr	Real Temperature 1 (from tmp275)	According to the formula P2=P2’+(Tr-Tm)*256 to calculate P2, and load P2 to RTC_ACP2 register.
0x00040D74	Tm	Measure Temperature 1 (from ADC)	
0x00040D78		Temp Check sum 1	INV(SUM(0x40D70, 0x40D74))
0x00040D7C	Tr	Real Temperature 2 (from tmp275)	According to the formula P2=P2’+(Tr-Tm)*256 to calculate P2, and load P2 to RTC_ACP2 register.
0x00040D80	Tm	Measure Temperature 2 (from ADC)	
0x00040D84		Temp Check sum 2	INV(SUM(0x40D7C, 0x40D80))

13.8 Application Note

13.8.1 Temperature Calibration

User can calculate temperature T according to the following formula, and T is 256 times larger than the actual temperature.

$$T = \left(\left(P0 * \left((X * X) >> 16\right)\right) + P1 * X + P2\right) >> 8$$

Where X is ADC sampling data, and X is 16 bits complement.

The P0~P2 is the value in RTC_ACP0~RTC_ACP2 registers, and P0~P2 is used to doing the temperature calibration.

The actual temperature is calculated as following.

$$T' = T/256$$

13.8.2 Frequency Error Calibration

1. User can calculate the frequency error of the chip as follows:

$$Delta = \left(P3 * ((T - Ti)^2 >> 16)\right) >> 16 + P4$$

Where Delta is the error rate in 0.1ppm unit of frequency deviation of 32768.

T = Actual temperature of the chip.

Ti= Setting value in RTC_ACTI register, which is the center temperature of the crystal during RTC calibration.

P4= The crystal deviation in normal temperature.

P3 is the K coefficient of the crystal for the current temperature. The hardware will select the K coefficient from Kx(x=1~5) according the actual temperature T, and update the K coefficient to the RTC_ACP3 register.

2. User can calculate the frequency correction value as follows:

$$RTC\_CAL = (Delta * P5) >> 16$$

P5 is the value in RTC_ACP5 register, or user can calculate P5 as follows:

$P5 = 65536/10/(1/30/32768/$RTCCLK prescaler），

and

$(1/30/32768/$RTCCLK prescaler) is PPM resolution of the RTC_CAL register.

3. User can calculate the PLL frequency division to output second pulse as follows:

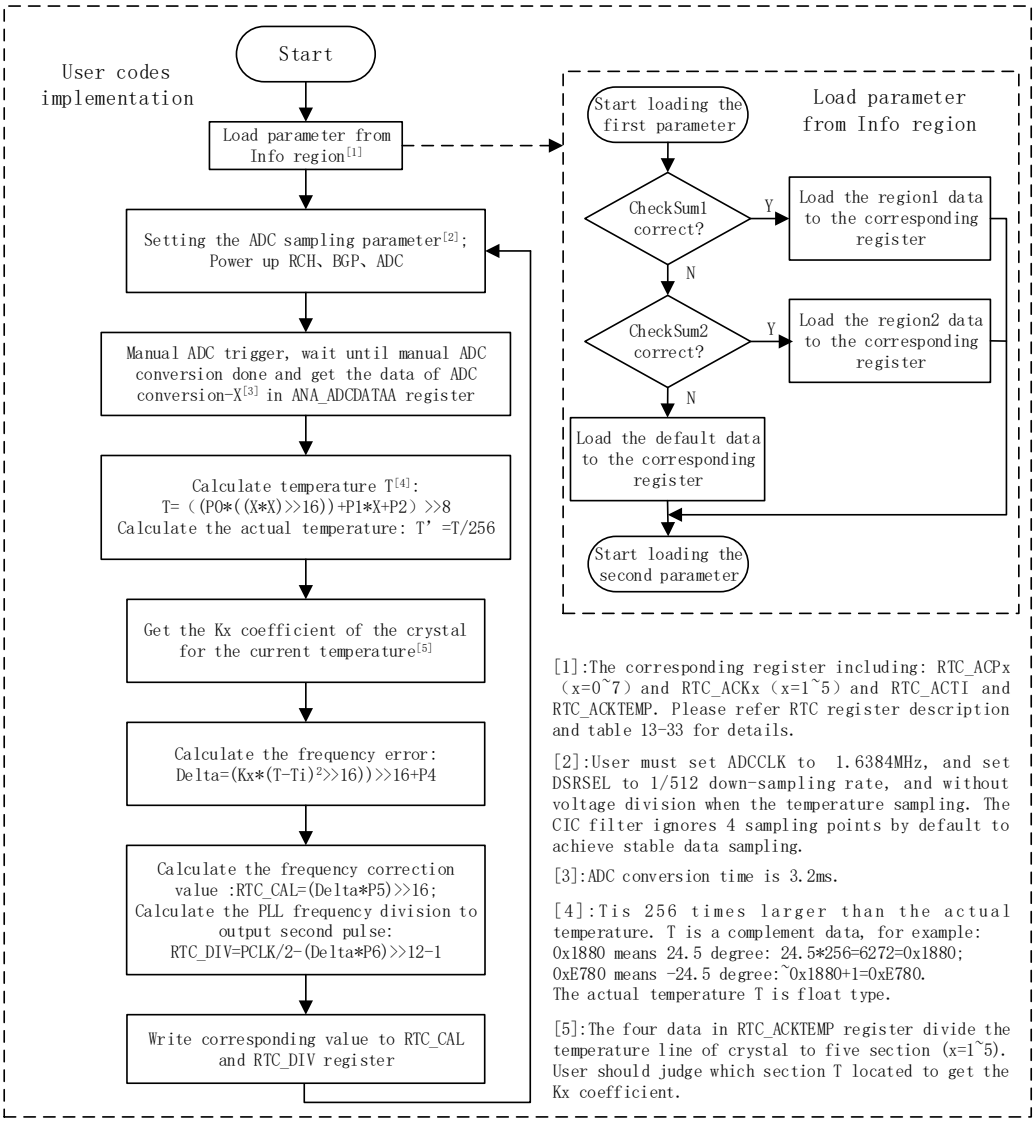
$$RTC\_DIV = PCLK/2 - (Delta * P6) >> 12 - 1$$

Where P6 is the value in RTC_ACP6 register, or user can calculate P6 as follows:

$$P6 = PCLK * 2.048*10^{-4}$$

13.8.3 RTC Manual Temperature Compensation

Figure26. RTC Manual Temperature Compensation Flow Chart



13.8.4 Notes on RTC calibration

The writing and reading operation in RTC register

Please extremely follow RTC reading and writing operation in user's manual.

14 FLASH Controller

14.1 Introduction

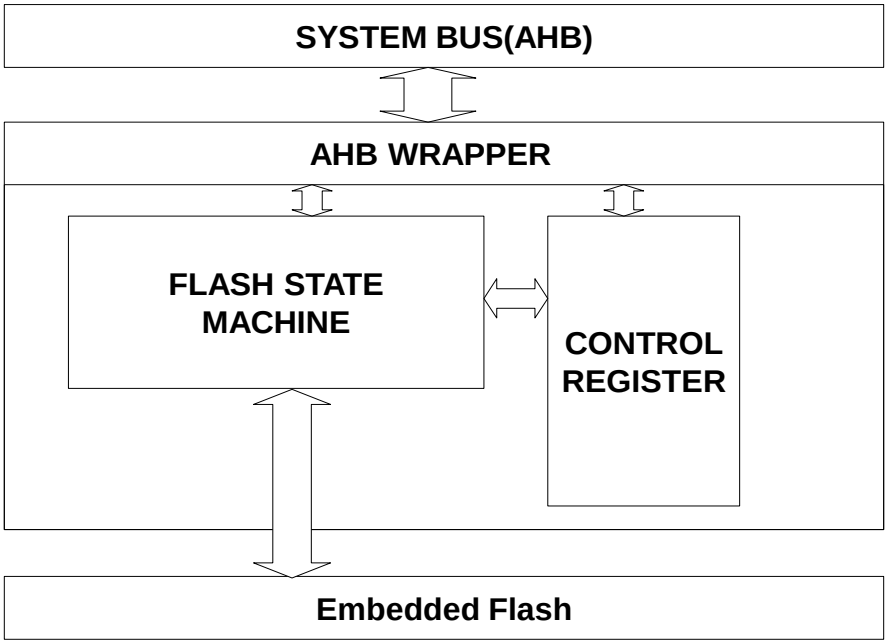
The FLASH controller is used to controller the read/write program of embedded FLASH. It supports byte/half-word/word program and sector/chip erase. Programmable timing can be controlled by 1 USCYCLE in MISC controller. It will automatically gate the external master access when FLASH is not ready, and always provide correct data with correct access timing. The setting in FLASH controller will be reset after wake-up from sleep mode, programmer should restore the setting manually after wake-up from sleep state.

14.2 Feature

- Support byte/half-word/word programming.
- Support sector/chip erase.
- Support standby mode. When MCU does not access flash, flash automatically enters standby mode. Any access to flash will wake the flash from standby with a wake-up time of 0.
- Support deep-standby mode. When MCU enters sleep mode, flash automatically enters deep-standby mode. At the same time, support the manual access to the deep-standby mode by configuration of flash FLASH_DSTB register. Any access to flash will cause flash to wake up from deep-standby with a wake-up time of 10*1ustick.
- Support automatically gate external master when FLASH is not ready.
- Support Info sector read.
- Support FLASH configuration register read/write.
- Programmable program speed.
- Support background checksum function and interrupt.

14.3 Block Diagram

Figure27. Functional Block Diagram of FLASH Controller



14.4 Register Location

Table189. FLASH Registers Map

Register Name	Offset	Type	Reset Value	Description
FLASH_STS	0x00BC	r	0x0000_0000	FLASH programming status register
FLASH_INT	0x00CC	rc_w1	0x0000_0000	FLASH Checksum interrupt status
FLASH_CSSADDR	0x00D0	rw	0x0000_0000	FLASH Checksum start address
FLASH_CSEADDR	0x00D4	rw	0x0003_FFFC	FLASH Checksum end address
FLASH_CSVALUE	0x00D8	r	0x0000_0000	FLASH Checksum value register
FLASH_CSCVALUE	0x00DC	rw	0x0000_0000	FLASH Checksum compare value register
FLASH_PASS	0x00E0	rw	0x0000_0000	FLASH password register
FLASH_CTRL	0x00E4	rw	0x0000_0000	FLASH control register
FLASH_PGADDR	0x00E8	rw	0x0000_0000	FLASH program address register
FLASH_PGDATA	0x00EC	rw	0x0000_0000	FLASH program word data register
FLASH_SERASE	0x00F4	rw	0x0000_0000	FLASH sector erase control register
FLASH_CERASE	0x00F8	rw	0x0000_0000	FLASH chip erase control register
FLASH_DSTB	0x00FC	rw	0x0000_0000	FLASH deep standby control register

Table190. Register Location of MISC2 Controller for FLASH

Name	Type	Address	Description	Default
MISC2_FLASHWC	rw	0x0000	FLASH wait cycle register	0x2100

14.5 Register Definition

14.5.1 FLASH_PASS Register

Table191. FLASH_PASS Register Description

Bit	Name	Type	Description
31:1	Rsvd	-	Reserved.
0	UNLOCK	r	The UNLOCK bit is used to indicate the FLASH program has been unlocked or not. To set this bit, programmer should write 0x55AAAA55 to this register. This bit will be kept high until programmer write any other value to this register. If the UNLOCK bit is 0, all FLASH program or erase or write configuration action will be disabled.

14.5.2 FLASH_CTRL Register

Table192. FLASH_CTRL Register Description

Bit	Name	Type	Description
31:3	Rsvd	-	Reserved.
2	CSINTEN	rw	This register is used to control the interrupt enable of checksum error. 0: Disable checksum error interrupt. 1: Enable checksum error interrupt.
1:0	CSMODE	rw	This register is used to control the checksum mode. 0: Disable checksum function. 1: Always-on checksum mode 2: Checksum start at overflow of timer 2. 3: Checksum start at rising edge of RTC second pulse.

14.5.3 FLASH_PGADDR Register

Table193. FLASH_PGADDR Register Description

Bit	Name	Type	Description
31:18	Rsvd	-	Reserved.
17:0	PGADDR	rw	This register is used to control the program address before doing program. This is byte address of FLASH IP, please refer to Table194 for detail about address under each mode. This address will increment automatically when a successful program is done.

Table194. Description of PGADDR and Write Data Port under Different Mode

Mode	PGADDR[17:2]	PGADDR[1:0]	Write Data Port
Normal Word Program	0x0000~0xFFFF	0	FLASH_PGDATA
Normal Byte Program	0x0000~0xFFFF	0	FLASH_PGB0
		1	FLASH_PGB1
		2	FLASH_PGB2
		3	FLASH_PGB3
Normal Half-Word Program	0x0000~0xFFFF	0	FLASH_PGHW0
		2	FLASH_PGHW1
Sector Erase	0x0000~0xFFFF	0	FLASH_SERASE

14.5.4 FLASH_PGDATA Register

Table195. FLASH_PGDATA Register Description

Bit	Name	Type	Description
31:0	PGDATA	rw	This register is used to control the program data. When UNLOCK is 1, write to this register will trigger a 4 bytes program automatically. Any access to FLASH IP during this period will be gated until the program is done. A two 32 bits FIFO is inside the FLASH controller, so programmer can do continuous program without interrupt. But if programmer needs to access FLASH IP, like execute program, during this period the FLASH program speed will become slower since more setup time is required for FLASH IP. It is suggested to put your programming program in SRAM, then the maximum program speed can be achieved. It is a must to do word write to this register to trigger a 4 bytes program, byte or half-word write will result-in single byte or two-bytes program.

14.5.4.1 FLASH_PGBx Register (x=0,1,2,3)

Table196. Description of FLASH_PGBx Register

Bit	Name	Type	Description
31:8	Rsvd	-	Reserved.
7:0	PGBx	rw	This register is used to control the program data. When UNLOCK is 1, write to this register will trigger one-byte program automatically. Any access to FLASH IP during this period will be gated until the program is done. A two 8 bits FIFO is inside the FLASH controller, so programmer can do continuous program without

			interrupt. But if programmer needs to access FLASH IP, like execute program, during this period the FLASH program speed will become slower since more setup time is required for FLASH IP. It is suggested to put your programming program in SRAM, then the maximum program speed can be achieved. It is a must to do byte write to this register to trigger a single byte program, word or half-word write will result-in 4 bytes or two-bytes program.

14.5.4.2 FLASH_PGHWx Register (x=0,1)

Table197. Description of FLASH_PGHWx Register

Bit	Name	Type	Description
31:16	Rsvd	-	Reserved.
15:0	PGHWx	rw	This register is used to control the program data. When UNLOCK is 1, write to this register will trigger a 2 bytes program automatically. Any access to FLASH IP during this period will be gated until the program is done. A two 16 bits FIFO is inside the FLASH controller, so programmer can do continuous program without interrupt. But if programmer needs to access FLASH IP, like execute program, during this period the FLASH program speed will become slower since more setup time is required for FLASH IP. It is suggested to put your programming program in SRAM, then the maximum program speed can be achieved. It is a must to do half-word write to this register to trigger a 2 bytes program, byte or word write will result-in single byte or 4-bytes program.

14.5.5 FLASH_SERASE Register

Table198. FLASH_SERASE Register Description

Bit	Name	Type	Description
31:1	Rsvd	-	Reserved.
0	SERASE	r	This bit is used to indicate if the sector erase is ongoing

			or not. This bit can be set when UNLOCK is 1 and programmer write 0xAA5555AA to this register, and it will be cleared automatically after the sector erase is done. The address of sector erase is controlled by PGADDR[17:2]. The sector erase time is 4000* 1us tick. One sector is 512 byte.

14.5.6 FLASH_CERASE Register

Table199. FLASH_CERASE Register Description

Bit	Name	Type	Description
31:1	Rsvd	-	Reserved.
0	CERASE	r	This bit is used to indicate if the chip erase is ongoing or not. This bit can be set when UNLOCK is 1 and programmer write 0xAA5555AA to this register, and it will be cleared automatically after the chip erase is done. The chip erase time is 30000* 1us tick.

14.5.7 FLASH_DSTB Register

Table200. FLASH_DSTB Register Description

Bit	Name	Type	Description
31:1	Rsvd	-	Reserved.
0	DSTB	r	This bit is used to indicate if the FLASH IP is entering deep standby. This bit can be set when UNLOCK is 1 and programmer write 0xAA5555AA to this register, and it will be cleared automatically after the FLASH IP wake-up from deep-standby mode. The deep standby mode can exit by any access to FLASH IP, but a 10 μS tick is required for the FLASH IP to back to normal state. During this period, the any access to FLASH will be gated until FLASH is ready.

14.5.8 FLASH_INT Register

Table201. FLASH_INT Register Description

Bit	Name	Type	Description
31:1	Rsvd	-	Reserved.
0	CSERR	rc_w1	Checksum error status bit. This flag is used to indicate the previous checksum operation has error, which means compare fail from CSVALUE to CSCVALUE. When CSINTEN is 1, an interrupt will be asserted to CPU. Write

			1 to clear this flag.

14.5.9 FLASH_CSSADDR Register

Table202. FLASH_CSSADDR Register Description

Bit	Name	Type	Description
31:18	Rsvd	-	Reserved.
17:0	CSSADDR	rw	Checksum start address register. This register is used to control the start address of checksum. The value in this register is byte address, but the LSB 2 bits are always 0.

14.5.10 FLASH_CSEADDR Register

Table203. FLASH_CSEADDR Register Description

Bit	Name	Type	Description
31:18	Rsvd	-	Reserved.
17:0	CSEADDR	rw	Checksum end address register. This register is used to control the end address of checksum. The value in this register is byte address, but the LSB 2 bits are always 0. The checksum range is (CSSADDR =< ADDR =< CSSADDR).

14.5.11 FLASH_CSVALUE Register

Table204. FLASH_CSVALUE Register Description

Bit	Name	Type	Description
31:0	CSVALUE	r	Checksum latched value register. This register is used to represent the checksum result of previous checksum operation.

14.5.12 FLASH_CSCVALUE Register

Table205. FLASH_CSCVALUE Register Description

Bit	Name	Type	Description
31:0	CSCVALUE	rw	Checksum compare value register. This register is used to store the expected checksum result. When the checksum is done but the calculated checksum value doesn't match CSCVALUE, the CSERR flag will be set. Calculating method of checksum compare value: accumulate all the values in this range (CSSADDR =< ADDR=< CSEADDR). The cumulative

			result is valid for 32 bits of data.

14.5.13 FLASH_STS Register

Table206. FLASH_STS Register Description

Bit	Name	Type	Description
31:5	Rsvd	-	Reserved.
4:0	STS	r	FLASH controller status register. 1: FLASH operation is done. Others: FLASH controller is in busy state or idle state. Programmer can poll this register to ensure all FLASH operation is done before disabling the FLASH_PASS register.

14.5.14 MISC2_FLASHWC Register

Table207. Description of MISC2_FLASHWC Register

Bit	Name	Type	Description	Default
31:14	Rsvd	-	Reserved.	0x0
13:8	1USCYCLE	rw	This register is used for FLASH controller to calculate 1ustick from AHB clock 1ustick = (AHB clock period)*(1USCYCLE+1) This setting is related to the wake-up time of FLASH, and the programming time of FLASH. FLASH wake-up time =1ustick *10. It must meet 1ustick >=1 μs. For example, the clock frequency of AHB is 26.2144MHz. In order to ensure the minimum wake-up time, 1USCYCLE should be set to 26. So, the wake-up time of FLASH is 27 / 26214400 * 10, which is about 10 μs. For example, the clock frequency of AHB is 32.768KHz. In order to ensure the minimum wake-up time, 1USCYCLE should be set to 0. So, the wake-up time of FLASH is 1 / 32768 * 10, which is about 305 μs.	0x21

15 GPIO Controller

15.1 Introduction

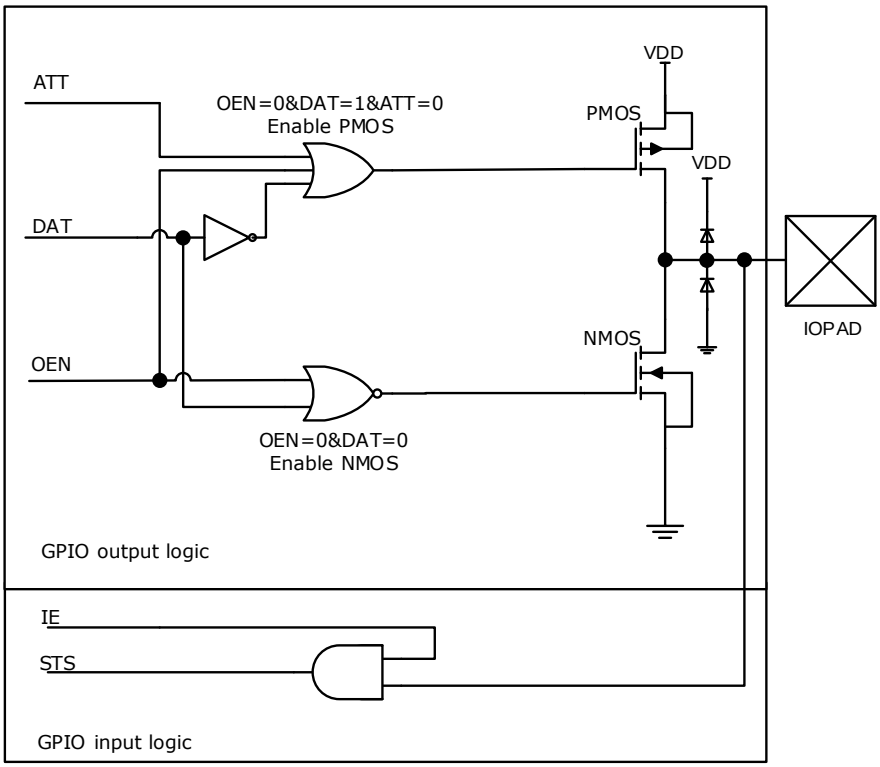
There total 82 IOs in V85XX and 16 IOs (GPIOA) are controlled by PMU controller with wake-up function. Other IOs (GPIOB~GPIOF) are controlled by GPIO controller which will keep their state at sleep mode.

15.2 Feature

- Each IO can be input or output mode.
- Each IO can be open drain mode.
- All pins have no pull-up and pull-down.
- GPIOA can wake up Sleep mode.

15.3 Block Diagram

Figure28. Functional Block Diagram of GPIO Controller



15.4 GPIOA Register Location

Table208. Register Location of the PMU_IOA Controller for GPIO

Register Name	Offset	Type	Reset Value	Description
PMU_IOAOEN	0x0010	rw	0x0000_FFFF	IOA output enable register
PMU_IOAIE	0x0014	rw	0x0000_FFFF	IOA input enable register
PMU_IOADAT	0x0018	rw	0x0000_0000	IOA data register
PMU_IOAATT	0x001C	rw	0x0000_0000	IOA attribute register
PMU_IOAWKUEN	0x0020	rw	0x0000_0000	IOA wake-up enable register
PMU_IOASTS	0x0024	r	--	IOA input status register
PMU_IOAINTSTS	0x0028	rc_w1	0x0000	IOA interrupt status register
PMU_IOASEL	0x0038	rw	0x0000	IOA special function select register
PMU_IOANODEG	0x0050	rw	0x0000	IOA no-deglitch control register.

15.5 GPIOA Register Definition

15.5.1 PMU_IOAOEN Register

Table209. Description of PMU_IOAOEN Register

Bit	Name	Type	Description
31:16	Rsvd	-	Reserved.
15:0	IOAOEN	rw	Each bit controls the IOA output enable signal Referred to Table213 for detail of IO state. 0: Enable IO's output function. 1: Disable IO's output function.

15.5.2 PMU_IOAIE Register

Table210. Description of PMU_IOAIE Register

Bit	Name	Type	Description
31:16	Rsvd	-	Reserved.
15:0	IOAIE	rw	Each bit controls the IOA input enable signal Referred to Table213 for detail of IO state. 0: Disable IO's input function. 1: Enable IO's input function.

15.5.3 PMU_IOADAT Register

Table211. Description of PMU_IOADAT Register

Bit	Name	Type	Description
31:16	Rsvd	-	Reserved.
15:0	IOADAT	rw	Each bit controls the IOA output data and pull low/high function Referred to Table213 for detail of IO state.

15.5.4 PMU_IOAATT Register

Table212. Description of PMU_IOAATT Register

Bit	Name	Type	Description
31:16	Rsvd	-	Reserved.
15:0	IOAATT	rw	Each bit controls the IOA attribute Referred to Table213 for detail of IO state. When an IO is set to output mode (GPIO or special function), this bit is used to control the CMOS or open drain mode of the IO pad. 0: CMOS mode. 1: Open drain mode (disable PMOS output).

Table213. IO Status under Different Kind of Setting

IOx Setting			IO Status
IOxOEN	IOxDAT	IOxATT	
1	0	0	Disable output function.
1	1	0	Disable output function.
1	0	1	Disable output function.
1	1	1	Disable output function.
0	0	0	Output low
0	1	0	Output high
0	0	1	Open drain output low.
0	1	1	Open drain pull-high

15.5.5 PMU_IOAWKUEN Register

Table214. Description of PMU_IOAWKUEN Register

Bit	Name	Type	Description
31:0	IOAWKUEN	rw	Every 2 bits control the IOA wake up or interrupt enable function. Bit [1:0]: IOA0WKUEN[1:0] Bit [3:2]: IOA1WKUEN[1:0] …… Bit [31:30]: IOA15WKUEN[1:0] Refer to Table214 for detail of each wake-up mode.

Table215. Description of each IO wake-up mode

IOAyWKUEN[1：0]	IOAyDAT	Wake-up Event
0	X	Disable wake-up function
1	0	Rising edge

	1	Falling Edge
2	0	High Level
	1	Low level
3	X	Rising or falling edge

Which y=0 ... 15, indicating an IO port.

For rising edge or falling edge wake-up source, since the H/W will use the final latch IO status before entering sleep mode, so the programmer needs to wait until the IO status change back to normal state. For example, when rising edge mode is chosen, the programmer should wait until the IO status back to low state to ensure the rising edge can be detected correctly. For high level or low level source, IO have no debounce in normal interrupt or wake up from sleep mode, but IO have four RTCCLK clock cycles debounce When CPU wake up from sleep mode.

15.5.6 PMU_IOASTS Register

Table216. Description of PMU_IOASTS Register

Bit	Name	Type	Description
31:16	Rsvd	-	Reserved.
15:0	IOASTS	r	Each bit represents the current IOA input data value.

15.5.7 PMU_IOAINTSTS Register

Table217. Description of PMU_IOAINTSTS Register

Bit	Name	Type	Description
31:16	Rsvd	-	Reserved.
15:0	IOAINTSTS	rc_w1	Each bit represents the IOA interrupt status. The corresponded bit will be set to 1 when corresponded wake-up event is detected. This register can be clear to 0 by writing corresponded bit to 1.

15.5.8 PMU_IOASEL Register

Table218. Description of PMU_IOASEL Register

Bit	Name	Type	Description
31:10	Rsvd	-	Reserved.
9	IOA_SEL9	rw	IOA9 special function select register. 0: GPIO 1: Special function 1 (CF1), only valid when CF1 enable.
7	IOA_SEL7	rw	IOA7 special function select register. 0: GPIO 1: Special function 1 (RTC_PLLDIV).
6	IOA_SEL6	rw	IOA6 special function select register.

			0: GPIO 1: Special function 2 (CMP2_O).
3	IOA_SEL3	rw	IOA3 special function select register. 0: GPIO 1: Special function 1 or 2 (RTC_PLLDIV or CF0). Only valid when each function enable. RTC_PLLDIV has higher priority.

15.5.9 PMU_IOANODEG Register

Table219. Description of PMU_IOANODEG Register

Bit	Name	Type	Description
31:16	Rsvd	-	Reserved.
15:0	IOANODEG	rw	Each bit control if the IOA wake-up signal will go through de-glitch circuit or not. If set this bit to 1, the corresponded IOA wake-up signal will not go through de-glitch circuit which can have a faster wake-up time. This bit effect the edge wake-up signal under sleep mode. 0: IOA wake-up signal will go through de-glitch circuit. 1: IOA wake-up signal will not go through de-glitch circuit.

15.6 GPIOB-F Register Location

Table220. GPIO Registers Map

Register Name	Offset	Type	Reset Value	Description
GPIO_OEN	0x0000	rw	0x0000_FFFF	IO output enable register
GPIO_IE	0x0004	rw	0x0000_FFFF	IO input enable register
GPIO_DAT	0x0008	rw	0x0000_0000	IO data register
GPIO_ATT	0x000C	rw	0x0000_0000	IO attribute register
GPIO_STS	0x0010	r	0x0000_0000	IO input status register

15.7 GPIOB~F Register Definition

15.7.1 GPIO_OEN Register

Table221. GPIO_OEN Register Description

Bit	Name	Type	Description
31:16	Rsvd	-	Reserved.
15:0	IOXOEN	rw	Each bit controls the IOx output enable signal Referred to Table213 for detail of IO state. 0: Enable IO's output function.

			1: Disable IO's output function.

15.7.2 GPIO_IE Register

Table222. GPIO_IE Register Description

Bit	Name	Type	Description
31:16	Rsvd	-	Reserved.
15:0	IOXIE	rw	Each bit controls the IOx input enable signal Referred to Table213 for detail of IO state. 0: Disable IO's input function. 1: Enable IO's input function.

15.7.3 GPIO_DAT Register

Table223. GPIO_DAT Register Description

Bit	Name	Type	Description
31:16	Rsvd	-	Reserved.
15:0	IOXDAT	rw	Each bit controls the IOx output data and pull low/high function Referred to Table213 for detail of IO state.

15.7.4 GPIO_ATT Register

Table224. GPIO_ATT Register Description

Bit	Name	Type	Description
31:16	Rsvd	-	Reserved.
15:0	IOXATT	rw	Each bit controls the IOx attribute Referred to Table213 for detail of IO state. When an IO is configured to a special mode, like UART or SPI, programmer can set the corresponded IOXATT to 1 to let it become open drain mode. Which means when output high, it will become input floating, when output low, it will keep the same output low behavior.

15.7.5 GPIO_STS Register

Table225. GPIO_STS Register Description

Bit	Name	Type	Description
31:16	Rsvd	-	Reserved.
15:0	IOXSTS	r	Each bit represents the current IOx input data value.

15.8 GPIOAF Register Location

Table226. GPIOAF Registers Map

Register Name	Offset	Type	Reset Value	Description
GPIOAF_IOBSEL	0x0000	rw	0x0000_0000	IOB special function select register
GPIOAF_IOESEL	0x000C	rw	0x0000_0000	IOE special function select register
GPIOAF_IOMISC	0x0020	rw	0x0000_0000	IO misc. control register

15.9 GPIOAF Register Definition

15.9.1 GPIOAF_IOBSEL Register

Table227. GPIOAF_IOBSEL Register Description

Bit	Name	Type	Description
31:9	Rsvd	-	Reserved.
8	IOB_SEL8	rw	IOB8 special function select register. 0: GPIO or special function 1 1: Special function 2 (CF0)
6	IOB_SEL6	rw	IOB6 special function select register 0: GPIO or special function 1/2 1: Special function 3(RTCCLK) when special function 1/2 is not enabled.
5	IOB_SEL5	rw	IOB5 special function select register. 0: GPIO or special function 1/2 1: Special function 3 (PLLL divider) when special function 1/2 is not enabled.
2	IOB_SEL2	rw	IOB2 special function select register 0: GPIO or special function 1/2 1: Special function 3 (PLLL divider) when special function 1/2 is not enabled.
1	IOB_SEL1	rw	IOB1 special function select register 0: GPIO or special function 1/2 1: Special function 3 (PLLH divider) when special function 1/2 is not enabled.
0	Rsvd	-	Reserved.

15.9.2 GPIOAF_IOESEL Register

Table228. GPIOAF_IOESEL Register Description

Bit	Name	Type	Description

31:13	Rsvd	-	Reserved.
12	IOE_SEL12	rw	IOE12 special function select register. 0: GPIO 1: Special function 1 (CF1).
11:8	Rsvd	-	Reserved.
7	IOE_SEL7	rw	IOE7 special function select register. 1: Special function 1 (CMP1_O).
6:0	Rsvd	-	Reserved.

15.9.3 GPIOAF_IOMISC Register

Table229. GPIOAF_IOMISC Register Description

Bit	Name	Type	Description
31:6	Rsvd	-	Reserved.
5	I2CIOC	rw	This register is used to control the I2C function is at IOB or IOC. 0: I2C is at IOB13~IOB14. 1: I2C is at IOC4~IOC5.
4:3	Rsvd	-	Reserved.
2:0	PLLHDIV	rw	When IOB1 is selected to special function 3 or IOB2 is selected to special function 3, or IOB5 is selected to special function 3, this register is used to control the divide ratio of PLLH and PLLL's output. 0: /1 1: /2 2: /4 3: /8 4: /16 Others: Reserved.

15.10 Special Function of IO

15.10.1 Special Function of IOA

The following table shows the special function of IOA, the special function will be turn-on when corresponded module is enabled.

Table230. Special Function of IOA

IO	Special Function 1	Special Function 2	Special Function 3	Special Function 4
IOA0	SWCLK (When MODE is 0)		LCDSEG54	

IOA1	SWDIO (When MODE is 0)		LCDSEG53	
IOA2			LCDSEG52	
IOA3	RTC_PLLDIV	CF0	LCDSEG51	
IOA4			LCDSEG66	CMP2_P
IOA5			LCDSEG67	CMP2_N
IOA6	CMP2_O		LCDSEG68	
IOA7	RTC_PLLDIV		LCDSEG69	
IOA8			LCDSEG50	ADC_CH3
IOA9	CF1		LCDSEG49	ADC_CH4
IOA10			LCDSEG48	ADC_CH5
IOA11			LCDSEG47	ADC_CH6
IOA12	UART RX0		LCDSEG71	
IOA13	UART RX1	ISO7816 RX0	LCDSEG73	
IOA14	UART RX2		LCDSEG13	
IOA15	UART RX3	ISO7816 RX1	LCDSEG15	

15.10.2 Special Function of IOB

The following table shows the special function of IOB, the special function will be turn-on when corresponded module is enabled. But when special function is LCD COM/SEG or ADC or CMP or X6_5M or VDCIN, programmer should disable GPIO input and disable GPIO output manually and disable other special function on this GPIO to ensure the correctness of these special functions.

Table231. Special function of IOB

IO	Special Function 1	Special Function 2	Special Function 3	Special Function 4
IOB0	UART RX4	PWM0		LCDSEG43
IOB1	UART RX5		PLLH divider	LCDSEG45
IOB2	UART TX0		PLLL divider	LCDSEG70
IOB3	UART TX1	ISO7816 CLK0		LCDSEG72
IOB4	UART TX2			LCDSEG12
IOB5	UART TX3	ISO7816 CLK1	PLLL divider	LCDSEG14
IOB6	UART TX4	PWM1	RTCCLK	LCDSEG44
IOB7	UART TX5			LCDSEG46
IOB8		CF0		LCDSEG35
IOB9	SPI1CSN			LCDSEG36
IOB10	SPI1CLK			LCDSEG37
IOB11	SPI1MISO			LCDSEG38
IOB12	SPI1MOSI			LCDSEG39
IOB13	I2CSCL (I2CIOC=0)	PWM2		LCDSEG40

IOB14	I2CSDA (I2CIOC=0)	PWM3		LCDSEG41
IOB15	TIMER EXT CLK			LCDSEG42

15.10.3 Special Function of IOC

The following table shows the special function of IOC, the special function will be turn-on when corresponded module is enabled. But when special function is LCD COM/SEG or ADC or CMP or X6_5M or VDCIN, programmer should disable GPIO input and disable GPIO output manually and disable other special function on this GPIO to ensure the correctness of these special functions.

Table232. Special function of IOC

IO	Special Function 1	Special Function 2	Special Function 3
IOC0	SPI2CSN		LCDSEG16
IOC1	SPI2CLK		LCDSEG17
IOC2	SPI2MISO		LCDSEG18
IOC3	SPI2MOSI		LCDSEG19
IOC4		I2CSCL (I2CIOC=1)	LCDSEG20
IOC5		I2CSDA (I2CIOC=1)	LCDSEG21
IOC6			LCDSEG22
IOC7			LCDSEG23
IOC8			LCDSEG24
IOC9			LCDSEG25
IOC10			LCDSEG26
IOC11			LCDSEG27
IOC12			LCDSEG28
IOC13			LCDSEG29
IOC14			LCDSEG30
IOC15			LCDSEG31

15.10.4 Special Function of IOD

The following table shows the special function of IOD, the special function will be turn-on when corresponded module is enabled. But when special function is LCD COM/SEG or ADC or CMP or X6_5M or VDCIN, programmer should disable GPIO input and disable GPIO output manually and disable other special function on this GPIO to ensure the correctness of these special functions.

Table233. Special function of IOD

IO	Special Function 1	Special Function 2	Special Function 3
IOD0	LCDCOM0		
IOD1	LCDCOM1		

IOD2	LCDCOM2		
IOD3	LCDCOM3		
IOD4	LCDCOM4	LCDSEG0	SPI3CSN
IOD5	LCDCOM5	LCDSEG1	SPI3MISO
IOD6	LCDCOM6	LCDSEG2	SPI3MOSI
IOD7	LCDCOM7	LCDSEG3	SPI3CLK
IOD8	LCDSEG4		
IOD9	LCDSEG5		
IOD10	LCDSEG6		
IOD11	LCDSEG7		
IOD12	LCDSEG8	SPI4CSN	
IOD13	LCDSEG9	SPI4CLK	
IOD14	LCDSEG10	SPI4MISO	
IOD15	LCDSEG11	SPI4MOSI	

15.10.5 Special Function of IOE

The following table shows the special function of IOE, the special function will be turn-on when corresponded module is enabled. But when special function is LCD COM/SEG or ADC or CMP or X6_5M or VDCIN, programmer should disable GPIO input and disable GPIO output manually and disable other special function on this GPIO to ensure the correctness of these special functions.

Table234. Special function of IOE

IO	Special Function 1	Special Function 2	Special Function 3
IOE0		LCDSEG74	
IOE1		LCDSEG75	
IOE2		LCDSEG76	
IOE3		LCDSEG77	
IOE4		LCDSEG63	ADC_CH7
IOE5		LCDSEG62	ADC_CH8
IOE6		LCDSEG61	ADC_CH9
IOE7	CMP1_O	LCDSEG60	ADC_CH11
IOE8		LCDSEG59	CMP1_P
IOE9		LCDSEG58	CMP1_N
IOE10		LCDSEG32	
IOE11		LCDSEG33	
IOE12	CF1	LCDSEG34	
IOE13		LCDSEG55	
IOE14		LCDSEG56	
IOE15		LCDSEG57	

15.10.6 Special Function of IOF

The following table shows the special function of IOF, the special function will be turn-on when corresponded module is enabled. But when special function is LCD COM/SEG or ADC or CMP or X6_5M or VDCIN, programmer should disable GPIO input and disable GPIO output manually and disable other special function on this GPIO to ensure the correctness of these special functions.

Table235. Special function of IOF

IO	Special Function 1
IOF0	X6_5MI
IOF1	X6_5MO

16 DMA Controller

16.1 Introduction

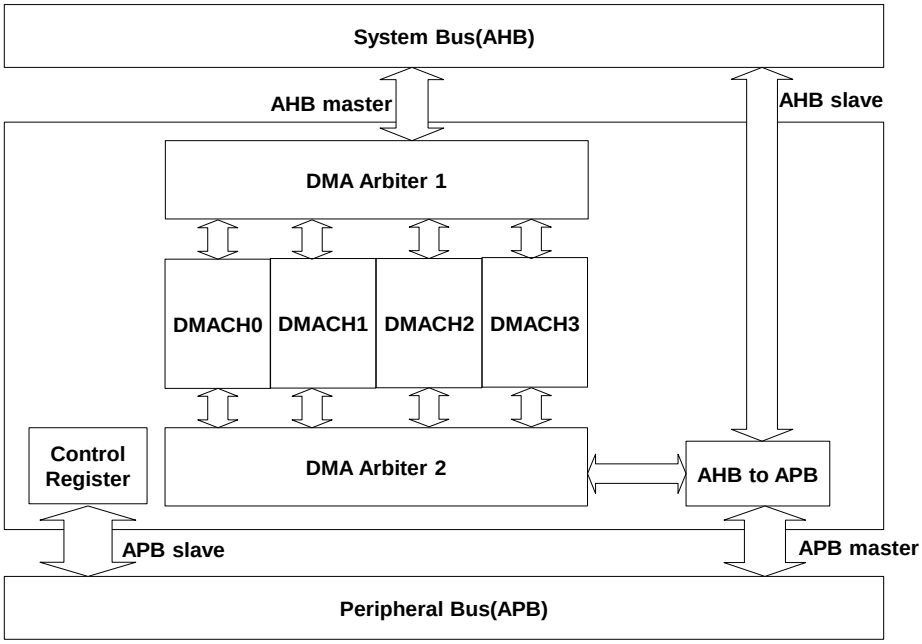
The DMA controller is used to transfer data from memory to memory or transfer data from memory to IO or from IO to memory. The DMA controller is also integrated with an AHB to APB bridge, so when DMA is doing APB transfer, the AHB performance will not be affected by slow peripheral. There are total 4 channels integrated in V85XX and each channel's priority is round-robin. The setting in DMA controller will be reset after wake-up from sleep mode, programmer should restore the setting manually after wake-up from sleep state.

16.2 Feature

- Memory to Memory Transfer
- Memory to IO Transfer
- IO to Memory Transfer
- Software mode or Hardware DMA request mode.
- Support Fix, Package Round or Frame Round Address mode
- Support Package/Frame/Data-abort IRQ generation.
- Support detection of data abort on bus.
- Integrated with AHB to APB Bridge.
- Support AES 128/192/256 encode/decode

16.3 Block Diagram

Figure29. Functional Block Diagram of DMA Controller



16.4 Register Location

Table236. DMA Registers Map

Register Name	Offset	Type	Reset Value	Description
DMA_IE	0x0000	rw	0x0000_0000	DMA interrupt enable register
DMA_STS	0x0004	rw	0x0000_0000	DMA status register
DMA_CxCTL[0..3,0x10]	0x0010	rw	0x0000_0000	DMA channel x control register
DMA_CxSRC[0..3,0x10]	0x0014	rw	0x0000_0000	DMA channel x source register
DMA_CxDST[0..3,0x10]	0x0018	rw	0x0000_0000	DMA channel x destination register
DMA_CxLEN[0..3,0x10]	0x001C	r	0x0000_0000	DMA channel x transfer length register
DMA_AESCTL	0x0050	rw	0x0000_0000	DMA AES control register
DMA_AESKEYx[0..7,0x4]	0x0060	rw	0x0000_0000	DMA AES key x register

16.5 Register Definition

16.5.1 DMA_IE Register

Table237. DMA_IE Register Description

Bit	Name	Type	Description
31:12	Rsvd	-	Reserved.
11	C3DAIE	rw	Channel 3 data abort interrupt enable 0: Disable

			1: Enable
10	C2DAIE	rw	Channel 2 data abort interrupt enable 0: Disable 1: Enable
9	C1DAIE	rw	Channel 1 data abort interrupt enable 0: Disable 1: Enable
8	C0DAIE	rw	Channel 0 data abort interrupt enable 0: Disable 1: Enable
7	C3FEIE	rw	Channel 3 frame end interrupt enable 0: Disable 1: Enable
6	C2FEIE	rw	Channel 2 frame end interrupt enable 0: Disable 1: Enable
5	C1FEIE	rw	Channel 1 frame end interrupt enable 0: Disable 1: Enable
4	C0FEIE	rw	Channel 0 frame end interrupt enable 0: Disable 1: Enable
3	C3PEIE	rw	Channel 3 package end interrupt enable 0: Disable 1: Enable
2	C2PEIE	rw	Channel 2 package end interrupt enable 0: Disable 1: Enable
1	C1PEIE	rw	Channel 1 package end interrupt enable 0: Disable 1: Enable
0	C0PEIE	rw	Channel 0 package end interrupt enable 0: Disable 1: Enable

16.5.2 DMA_STS Register

Table238. DMA_STS Register Description

Bit	Name	Type	Description
31:16	Rsvd	-	Reserved.
15	C3DA	rc_w1	Channel 3 data abort interrupt flag, write 1 to clear this flag.
14	C2DA	rc_w1	Channel 2 data abort interrupt flag, write 1 to clear this

			flag.
13	C1DA	rc_w1	Channel 1 data abort interrupt flag, write 1 to clear this flag.
12	C0DA	rc_w1	Channel 0 data abort interrupt flag, write 1 to clear this flag.
11	C3FE	rc_w1	Channel 3 frame end interrupt flag, write 1 to clear this flag.
10	C2FE	rc_w1	Channel 2 frame end interrupt flag, write 1 to clear this flag.
9	C1FE	rc_w1	Channel 1 frame end interrupt flag, write 1 to clear this flag.
8	C0FE	rc_w1	Channel 0 frame end interrupt flag, write 1 to clear this flag.
7	C3PE	rc_w1	Channel 3 package end interrupt flag, write 1 to clear this flag.
6	C2PE	rc_w1	Channel 2 package end interrupt flag, write 1 to clear this flag.
5	C1PE	rc_w1	Channel 1 package end interrupt flag, write 1 to clear this flag.
4	C0PE	rc_w1	Channel 0 package end interrupt flag, write 1 to clear this flag.
3	C3BUSY	r	DMA channel 3 busy register 0: Idle 1: Busy
2	C2BUSY	r	DMA channel 2 busy register. 0: Idle 1: Busy
1	C1BUSY	r	DMA channel 1 busy register. 0: Idle 1: Busy
0	C0BUSY	r	DMA channel 0 busy register. 0: Idle 1: Busy

16.5.3 DMA_CxCTL Register

Table239 shows the bit assignment of DMA_CxCTL register, the data in this register will be latched into DMA channel after the transfer is start, so any modification to this register won't affect the on-going DMA transfer. Only STOP bit can stop the DMA transfer immediately.

Table239. DMA_CxCTL Register Description

Bit	Name	Type	Description
31:24	FLEN	rw	Package number register, actual transfer package

			number is (FLEN + 1). Total length is (FLEN + 1) * (PLEN + 1).
23:16	PLEN	rw	Package length register, actual transfer package length is (PLEN + 1). Total length is (FLEN + 1) * (PLEN + 1).
15	STOP	rw	Force stop DMA transfer, write 1 to this bit will force the DMA channel back to idle state, programmer should clear this bit to 0 if another DMA transfer need to be assigned into the same channel. 0: Normal mode. 1: Force stop DMA transfer.
14	AESEN	rw	Enable AES encrypt/decrypt function of DMA channel. Only DMA channel 3 supports AES function. When AES function is enabled, the SIZE should be set to 32 bits mode and SMODE and TMODE should be set to 1 or 2. And package size should be multiply of 4. 0: Disable. 1: Enable.
13	CONT	rw	Continuous mode, DMA transfer will not stop until STOP bit is set to 1. Every time DMA complete all package and frame transfer, it will start from beginning and do the transfer continuously. 0: Discontinuous mode. 1: Continuous mode.
12	TMODE	rw	Transfer mode selection register. 0: One DMA request only transfers one single data. 1: One DMA request transfers one package data.
11:7	DMASEL	rw	DMA request source selection. Please refer to Table 16-5 of detail about each DMA
6:5	DMODE	rw	Destination address mode. 0: Fix. 1: Incremental but rounded at package end. 2: Incremental but rounded at frame end. 3: Reserved.
4:3	SMODE	rw	Source address mode. 0: Fix. 1: Incremental but rounded at package end. 2: Incremental but rounded at frame end. 3: Reserved.
2:1	SIZE	rw	Transfer size mode. 0: Byte (8 bits). 1: Half-word (16 bits) 2: Word (32 bits) 3: Reserved.

0	EN	rw	DMA channel enable register. 0: Disable DMA channel (no effect when CONT is 1) 1: Enable DMA channel. This bit will be cleared automatically by hardware when a DMA transfer is done at CONT is 0.

Table240. DMA Source Selection

DMASEL	Source	DMASEL	Source
0	Software	16	ISO78161 TX
1	-	17	ISO78161 RX
2	UART0 TX	18	TIMER 0
3	UART0 RX	19	TIMER 1
4	UART1 TX	20	TIMER 2
5	UART1 RX	21	TIMER 3
6	UART2 TX	22	SPI1 TX
7	UART2 RX	23	SPI1 RX
8	UART3 TX	24	UART 32K 0
9	UART3 RX	25	UART 32K 1
10	UART4 TX	26	CMP1
11	UART4 RX	27	CMP2
12	UART5 TX	28	SPI3 TX
13	UART5 RX	29	SPI3 RX
14	ISO78160 TX	30	SPI2 TX
15	ISO78160 RX	31	SPI2 RX

16.5.4 DMA_CxSRC Register

Table241. DMA_CxSRC Register Description

Bit	Name	Type	Description
31:0	SRC	rw	DMA source address register. When SIZE in DMA_CxCTL is 1, then this register must be half-word aligned. When SIZE in DMA_CxCTL is 2, then this register must be word aligned. When the SRC is set to 0x4001xxxx, then it will be switch to IO read automatically.

16.5.5 DMA_CxDST Register

Table242. DMA_CxDST Register Description

Bit	Name	Type	Description
31:0	DST	rw	DMA destination address register. When SIZE in DMA_CxCTL is 1, then this register must be half-word

			aligned. When SIZE in DMA_CxCTL is 2, then this register must be word aligned. When the DST is set to 0x4001xxxx, then it will be switch to IO write automatically.

16.5.6 DMA_CxLEN Register

Table243. DMA_CxLEN Register Description

Bit	Name	Type	Description
31:16	Rsvd	-	Reserved.
15:8	CFLEN	r	Current transferred package number. The total length of DMA transmission is CFLEN * (PLEN +1) + CPLEN. After all packages are transferred, it will be automatically cleared.
7:0	CPLEN	r	Current transferred package length. The total length of DMA transmission is CFLEN * (PLEN +1) + CPLEN. After all packages are transferred, it will be automatically cleared.

16.5.7 DMA_AESCTL Register

Table244. DMA_AESCTL Register Description

Bit	Name	Type	Description
31:4	Rsvd	-	Reserved.
3:2	MODE	rw	AES mode selection register. 0: AES128 1: AES192 2: AES256 3: Reserved.
0	ENC	rw	AES encode/decode selection register. 0: Decode 1: Encode

16.5.8 DMA_AESKEYx Register

Table245. DMA_AESKEYx Register Description

Bit	Name	Type	Description
31:0	KEYx	rw	AES KEY register. KEY0: bit 31~0 KEY1: bit 63~32 KEY2: bit 95~64 KEY3: bit 127~96

			KEY4: bit 159~128 KEY5: bit 191~160 KEY6: bit 223~192 KEY7: bit 255~224. When mode is AES128, only bit 127~0 is used. When mode is AES192, only bit 191~0 is used. When mode is AES256, bit 255~0 is used.

17 UART Controller

17.1 Introduction

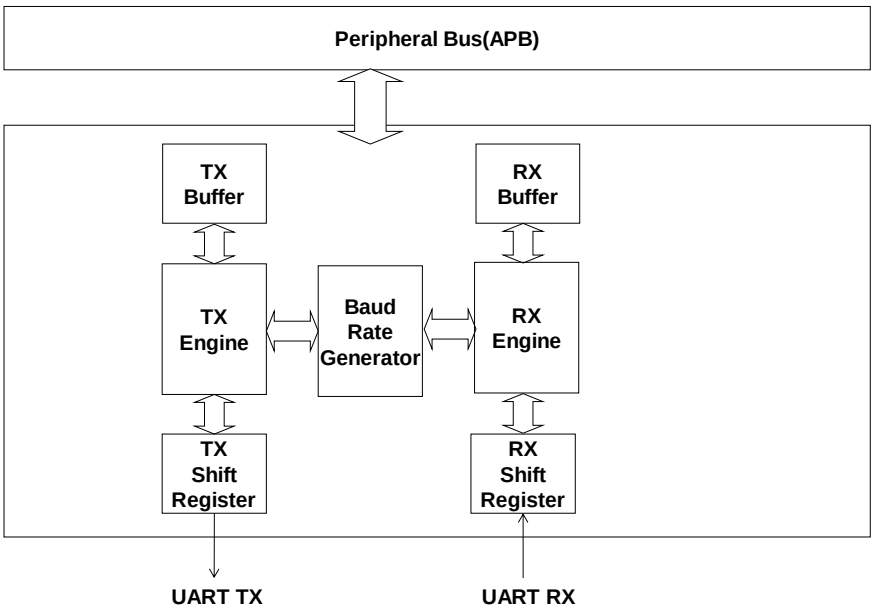
The UART controller is used to transmit/receive data via UART protocol. There are total 6 UART controller in V85XX, each UART controller can be program individually and has its own interrupt to CPU. The UART controller can support 8 bits transfer without parity or 9 bits transfer with even or odd parity. One data buffer and one shift register is used for transmit engine, and another set of data buffer and shift register are used for receive engine. The setting in UART controller will be reset after wake-up from sleep mode, programmer should restore the setting manually after wake-up from sleep state. The baud rate range of UART is 300~819200bps.

17.2 Feature

- Programmable baud rate generator
- 8 bits or 9 bits with odd/even parity transfer.
- Parity error detection.
- Transmit/ Receive interrupt flag.
- Transmit/ Receive overrun interrupt flag.

17.3 Block Diagram

Figure30. Functional Block Diagram of UART Controller



17.4 Register Location

Table246. UART Registers Map

Register Name	Offset	Type	Reset Value	Description
UART_DATA	0x0000	rw	0x0000_0000	UART data register
UART_STATE	0x0004	rc_w1	0x0000_0000	UART status register
UART_CTRL	0x0008	rw	0x0000_0000	UART control register
UART_INTSTS	0x000C	rc_w1	0x0000_0000	UART interrupt status register
UART_BAUDDIV	0x0010	rw	0x0000_0000	UART baud rate divide register
UART_CTRL2	0x0014	rw	0x0000_0000	UART control register 2

Table247. Register Location of MISC Controller for UART

Register Name	Offset	Type	Reset Value	Description
MISC_IREN	0x000C	rw	0x00	IR enable control register
MISC_DUTYL	0x0010	rw	0x0000	IR Duty low pulse control register
MISC_DUTYH	0x0014	rw	0x0000	IR Duty high pulse control register

17.5 Register Definition

17.5.1 UART_DATA Register

Table248. UART_DATA Register Description

Bit	Name	Type	Description
31:8	Rsvd	-	Reserved.
7:0	DATA	rw	Read: Receive data Write: Transmit data

17.5.2 UART_STATE Register

Table249. UART_STATE Register Description

Bit	Name	Type	Description
31:7	Rsvd	-	Reserved.
6	RXPSTS	r	Receive parity data flag. This flag shows the parity bit of last receive data.
5	TXDONE	rc_w1	Transmit done flag. This flag will be set when a single byte data is transmitted. The bit will be cleared when programmer write 1 to this bit or write 1 to TXDONEIF bit in UART_INTSTS register.
4	RXPE	rc_w1	Receive parity error flag.

			This flag will be set when receive data's parity does not meet expectation. The bit will be cleared when programmer write 1 to this bit or write 1 to RXPEIF bit in UART_INTSTS register.
3	RXOV	rc_w1	Receive buffer overrun flag. This flag will be set when RXFULL is 1 and another new data is received from RX engine. The bit will be cleared when programmer write 1 to this bit or write 1 to RXOVIF bit in UART_INTSTS register.
2	TXOV	rc_w1	Transmit buffer overrun flag. This flag will be set when TXFULL is 1 and another new data is written into UART_DATA register. The bit will be cleared when programmer write 1 to this bit or write 1 to TXOVIF bit in UART_INTSTS register.
1	RXFULL	r	Receive buffer full register. 0: Receive buffer is empty. 1: Receive buffer is full. This flag will be set when a data is received from the UART RX engine, and will be cleared to 0 when programmer read the data from UART_DATA register.
0	Rsvd	-	Reserved.

17.5.3 UART_CTRL Register

Table250. UART_CTRL Register Description

Bit	Name	Type	Description
31:9	Rsvd	-	Reserved.
8	TXDONEIE	rw	Transmit done interrupt enable register.
7	RXPEIE	rw	Receive parity error interrupt enable register.
5	RXOVIE	rw	Receive overrun interrupt enable register.
4	TXOVIE	rw	Transmit overrun interrupt enable register.
3	RXIE	rw	Receive interrupt enable register.
1	RXEN	rw	Receive engine enable register.
0	TXEN	rw	Transmit engine enable register.

17.5.4 UART_INTSTS Register

Table251. UART_INTSTS Register Description

Bit	Name	Type	Description
31:6	Rsvd	-	Reserved.
5	TXDONEIF	rc_w1	Transmit done flag. This flag will be set when a single byte is transmitted and

			TXDONEIE is 1. The bit will be cleared when programmer write 1 to this bit or write 1 to TXDONE bit in UART_STATE register.
4	RXPEIF	rc_w1	Receive parity error flag. This flag will be set when receive data's parity does not meet expectation and RXPEIEis1.The bit will be cleared when programmer write 1 to this bit or write 1 to RXPE bit in UART_STATE register.
3	RXOVIF	rc_w1	Receive buffer overrun flag. This flag will be set when RXOVIE is 1 and RXFULL is 1 and another new data is received from RX engine. The bit will be cleared when programmer write 1 to this bit or write 1 to RXOV bit in UART_STATE register.
2	TXOVIF	rc_w1	Transmit buffer overrun flag. This flag will be set when TXOVIE is 1 and TXFULL is 1 and another new data is written into UART_DATA register. The bit will be cleared when programmer write 1 to this bit or write 1 to TXOV bit in UART_STATE register.
1	RXIF	rc_w1	Receive interrupt flag. This bit will be set when a data is received before the EOF flag and put in UART_DATA register. This bit will be cleared when write 1 to this register.
0	Rsvd	-	Reserved.

17.5.5 UART_BAUDDIV Register

Table252. UART_BAUDDIV Register Description

Bit	Name	Type	Description
31:20	Rsvd	-	Reserved.
19:0	BAUDDIV	rw	Baud rate divider register, this register must be set before enable UART engine. BAUDDIV = APBCLK/Baud-rate. For example, when APBCLK = 6.5536MHz and baud-rate is 9600, fill 6553600/9600 = 682 in this register.

17.5.6 UART_CTRL2 Register

Table253. UART_CTRL2 Register Description

Bit	Name	Type	Description
31:4	Rsvd	-	Reserved.
3:2	PMODE	rw	Parity mode control register, this register is valid only when MODE is set to 1.

			0: Even parity. 1: Odd parity. 2: Always 0 at parity bit. 3: Always 1 at parity bit.
1	MODE	rw	UART mode control register. 0: 1+8+1 mode. 1: 1+8+1+1 mode, the parity bit is controlled by PMODE register.
0	MSB	rw	LSB/MSB transmit order control register. 0: LSB transmit first. 1: MSB transmit first.

17.5.7 MISC_IREN Register

Table254. Description of MISC_IREN Register

Bit	Name	Type	Description	Default
31:6	Rsvd	-	Reserved.	-
5:0	IREN	rw	IR enable control register. Each bit in this register corresponded to 1 UART TX channel. When IREN[x] is set to 1, it means UART TX[x] will be modulated with IR pulse to output.	0x00

17.5.8 MISC_DUTYL Register

Table255. Description of MISC_DUTYL Register

Bit	Name	Type	Description	Default
31:16	Rsvd	-	Reserved.	-
15:0	DUTYL	rw	IR low pulse width control register. The low pulse width will be (DUTYL + 1)*APBCLK period.	0x0000

17.5.9 MISC_DUTYH Register

Table256. Description of MISC_DUTYH Register

Bit	Name	Type	Description	Default
31:16	Rsvd	-	Reserved.	-
15:0	DUTYH	rw	IR high pulse width control register. The high pulse width will be (DUTYH + 1)*APBCLK period.	0x0000

18 UART 32K Controller

18.1 Introduction

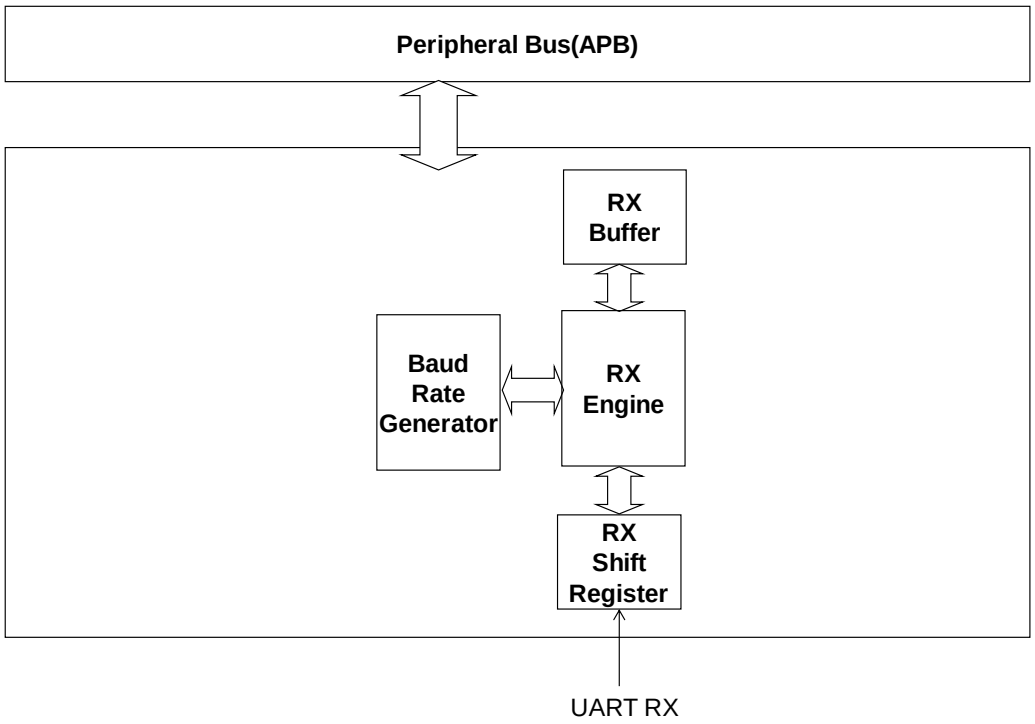
The UART 32K controller is used to receive data via UART protocol. There are two individual UART 32K controllers in V85XX, which can select input from UART rx0 ~ rx3. UART 32K controller is designed to operate at 32K crystal frequency, so it can work under sleep or mode. The typical baud rate is 9600. The UART 32K controller can support 8 bits transfer without parity or 9 bits transfer with even or odd parity. One data buffer and one shift register are used for receive engine. The baud rate range of UART 32K is 300~14400bps.

18.2 Feature

- Operated under sleep mode.
- Wake-up capability under sleep mode.
- Programmable Baud rate generator
- 8 bits or 9 bits with odd/even parity transfer.
- Parity error detection.
- Receive interrupt flag.
- Receive parity error flag.
- Receive overrun interrupt flag.

18.3 Block Diagram

Figure31. Functional Block Diagram of UART 32K Controller



18.4 Register Location

Table257. U32K Registers Map

Register Name	Offset	Type	Reset Value	Description
U32K_CTRL0	0x0000	rw	0x0000_0000	UART 32K control register 0
U32K_CTRL1	0x0004	rw	0x0000_0000	UART 32K control register 1
U32K_PHASE	0x0008	rw	0x0000_4B00	UART 32K baud rate control register
U32K_DATA	0x000C	r	0x0000_0000	UART 32K receive data buffer
U32K_STS	0x0010	rc_w1	0x0000_0000	UART 32K interrupt status register

18.5 Register Definition

18.5.1 U32K_CTRL0 Register

Table258. U32K_CTRL0 Register Description

Bit	Name	Type	Description
31:9	Rsvd	-	Reserved.
8	WKUMODE	rw	Wake-up mode control register. This register is valid when RXIE = 1. 0: Wake-up when a package is received no matter parity

			or stop bit is correct or not. 1: Wake-up only when parity bit and stop bit is correct.
7:6	DEBSEL	rw	De-bounce control register 0: No de-bounce. 1: 2 RTCCLK clocks de-bounce. 2: 3 RTCCLK clocks de-bounce. 3: 4 RTCCLK clocks de-bounce. This register is used when the UART bus is dirty, enable the de-bounce function can reduce the noise on the receive data. But a too large de-bounce cycles may result in loss of receive data.
5:4	PMODE	rw	Parity mode control register, this register is valid only when MODE is set to 1. 0: Even parity. 1: Odd parity. 2: Always 0 at parity bit. 3: Always 1 at parity bit.
3	MODE	rw	UART mode control register. 0: 1+8+1 mode. 1: 1+8+1+1 mode, the parity bit is controlled by PMODE register.
2	MSB	rw	UART receive order control register. 0: LSB receive first. 1: MSB receive first.
1	Rsvd	-	Reserved.
0	EN	rw	UART32K controller enable register. When this bit is set to 1, the UART32K controller will start to receive data after two 32768 Hz clock cycles. So use must set correct parameter and control register before set this register to 1. 0: Disable. 1: Enable.

18.5.2 U32K_CTRL1 Register

Table259. U32K_CTRL1 Register Description

Bit	Name	Type	Description
31:6	Rsvd	-	Reserved.
5:4	RXSEL	rw	Receive data select register. 0: From UART RX0 (IOA12). 1: From UART RX1 (IOA13). 2: From UART RX2 (IOA14). 3: From UART RX3 (IOA15).

2	RXOVIE	rw	Receive overrun interrupt/wake-up enable register.
1	RXPEIE	rw	Receive parity error interrupt/wake-up enable register.
0	RXIE	rw	Receive interrupt/wake-up enable register. When enabled, when WKUMODE is 0, it will wake up as long as it receives serial data; when WKUMODE is 1, it will wake up only when parity and stop bits are correct.

18.5.3 U32K_PHASE Register

Table260. U32K_PHASE Register Description

Bit	Name	Type	Description
31:16	Rsvd	-	Reserved.
15:0	PHASE	rw	Baud rate divider register, this register must be set before enable UART 32K engine. PHASE = 65536*Baud-rate/32768. For example, when baud-rate is 9600, fill 65536*9600/32768 = 19200 in this register. The maximum baud rate which UART 32K can support is 9600. When PSCA in RTC_PSCA register is not 0, the value in this register should be calculated by the divided RTCCLK frequency.

18.5.4 U32K_DATA Register

Table261. U32K_DATA Register Description

Bit	Name	Type	Description
31:8	Rsvd	-	Reserved.
7:0	DATA	r	Read: Receive data.

18.5.5 U32K_STS Register

Table262. U32K_STS Register Description

Bit	Name	Type	Description
31:3	Rsvd	-	Reserved.
2	RXOV	rc_w1	Receive buffer overrun flag This flag will be set when receive FIFO is full and another new data is received from RX engine. The bit will be

			cleared when programmer write 1 to this bit.
1	RXPE	rc_w1	Receive parity error flag This flag will be set when receive data's parity does not meet expectation. The bit will be cleared when programmer write 1 to this bit.
0	RXIF	rc_w1	Receive interrupt flag This bit will be set when a data is received and put in U32K_DATA register. This bit will be cleared when write 1 to this register.

19 ISO7816 Controller

19.1 Introduction

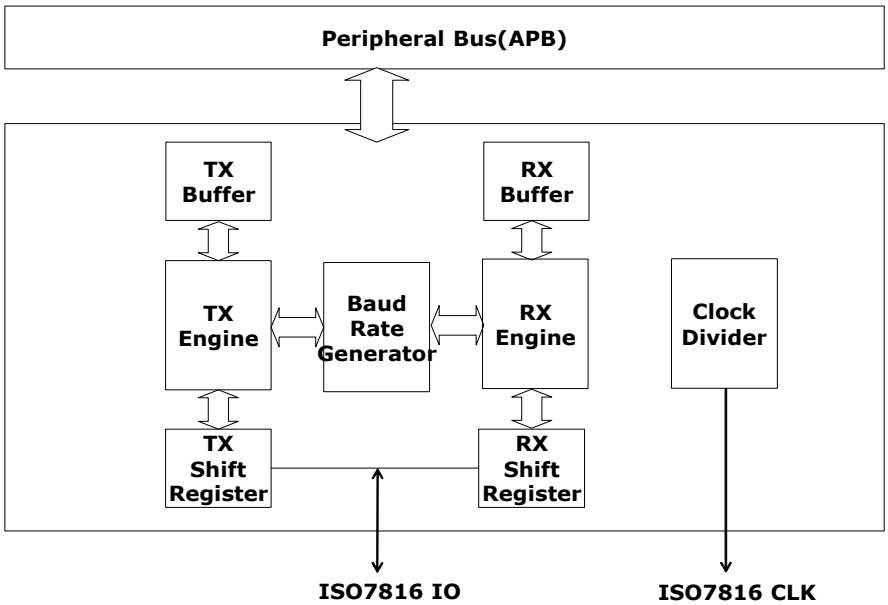
The ISO7816 controller is an enhanced UART protocol which supports half-duplex communication on the 2 wires bus. There are total 2 ISO7816 controllers in V85XX, each ISO7816 controller can be program individually and has its own interrupt to CPU. A clock divider is also included inside the IP which is capable to generate a 1~5MHz clock for ISO7816 device. The setting in ISO7816 controller will be reset after wake-up from sleep mode, programmer should restore the setting manually after wake-up from sleep state.

19.2 Feature

- Programmable Baud rate generator
- Support automatically retry
- Support half-duplex transmit/ receive
- Support clock divider

19.3 Block Diagram

Figure32. Functional Block Diagram of ISO7816 Controller



19.4 Register Location

Table263. ISO7816 Registers Map

Register Name	Offset	Type	Reset Value	Description
ISO7816_BAUDDIVL	0x0004	rw	0x0000_0000	ISO7816 baud-rate low byte register
ISO7816_BAUDDIVH	0x0008	rw	0x0000_0000	ISO7816 baud-rate high byte register
ISO7816_DATA	0x000C	rw	0x0000_0000	ISO7816 data register
ISO7816_INFO	0x0010	rc_w1	0x0000_0000	ISO7816 information register
ISO7816_CFG	0x0014	rw	0x0000_0000	ISO7816 control register
ISO7816_CLK	0x0018	rw	0x0000_0000	ISO7816 clock divider control register

19.5 Register Definition

19.5.1 ISO7816_BAUDDIVL Register

Table264. ISO7816_BAUDDIVL Register Description

Bit	Name	Type	Description
31:8	Rsvd	-	Reserved.
7:0	BAUDDIVL	rw	Low byte of baud-rate divider.

19.5.2 ISO7816_BAUDDIVH Register

Table265. ISO7816_BAUDDIVH Register Description

Bit	Name	Type	Description
31:8	Rsvd	-	Reserved.
7:0	BAUDDIVH	rw	High byte of baud-rate divider. The baud-rate counter is count from BAUDDIV to 0xFFFF, so the setting should be. BAUDDIV = 0x10000 – (APBCLK/Baud-rate). For example, when APBCLK is 6.5536MHz and baud-rate is 9600, then 0x10000-(6553600/9600) = 0xFD56 should be written into this register.

19.5.3 ISO7816_DATA Register

Table266. ISO7816_DATA Register Description

Bit	Name	Type	Description
31:8	Rsvd	-	Reserved.
7:0	DATA	rw	Data Read: Receive data

			When receive data is not read by programmer and another data has been received, the OVIF flag will be set. Write: Transmit data A write to this port will trigger a transmit event on the ISO7816 bus.

19.5.4 ISO7816_INFO Register

Table267. ISO7816_INFO Register Description

Bit	Name	Type	Description
31:8	Rsvd	-	Reserved.
7	OVIF	rc_w1	Receive overflow flag This bit will be set when a data is received by not been read by CPU but another receive data is coming in. This bit can be cleared by write 1 to this flag.
6	SDIF	rc_w1	Transmit interrupt flag This bit will set when a byte has been transmitted and ACK has been received. This bit will be set no matter the received ACK is 0 or 1. This bit can be cleared by write 1 to this flag.
5	RCIF	rc_w1	Receive interrupt flag This bit will set when a byte has been received and ACK has been transmitted. This bit can be cleared by write 1 to this flag.
4	LSB	rw	MSB/LSB transmit/receive order control register. 0: Transmit MSB first. 1: Transmit LSB first.
3	SDERR	rc_w1	When the received ACK is 0 during transmit mode, this bit will be set to 1. This bit can be clear by write 1 to this bit.
2	RCERR	rc_w1	When received data have check sum error, this bit will be set to 1. This bit can be clear by write 1 to this bit.
1	CHKSUM	rw	The transmitted or received data check sum bit. This bit can be read/write by CPU, by the original message will be lost.
0	RCACK	rw	The received ACK at the end of transmit. This bit can be read/write by CPU, by the original message will be lost.

19.5.5 ISO7816_CFG Register

Table268. ISO7816_CFG Register Description

Bit	Name	Type	Description

31:8	Rsvd	-	Reserved.
7	OVIE	rw	Receive overrun interrupt enable register.
6	SDIE	rw	Transmit interrupt enable register.
5	RCIE	rw	Receive interrupt enable register.
4	ACKLEN	rw	ACK low period when receive an error data. 0: 1 bit 1: 2 bits.
3	AUTOSD	rw	Automatic re-transmit when receive ACK is 0. 0: Disable automatic re-transmit mode. 1: Enable automatic re-transmit mode.
2	AUTORC	rw	Automatic response ACK as 0 when receive an error data to let transmitter re-send the data. 0: Disable automatic re-receive mode. 1: Enable automatic re-receive mode.
1	CHKP	rw	Parity mode control register. 0: Even parity 1: Odd parity.
0	EN	rw	ISO7816 enable register. 0: Disable ISO7816 function. 1: Enable ISO7816 function.

19.5.6 ISO7816_CLK Register

Table269. ISO7816_CLK Register Description

Bit	Name	Type	Description
31:8	Rsvd	-	Reserved.
7	CLKEN	rw	ISO7816 clock output enable. 0: Disable clock output. 1: Enable clock output.
6:0	CLKDIV	rw	The ISO7816 clock divider ratio. 0: APBCLK/1 1: APBCLK /2 2: APBCLK /3 … 127: APBCLK /128

In ISO7816's protocol, the re-transmit should be less or equal to 3 times, this part should be take care by software to disable the auto transmit or receive function after two times of failure retry.

The following table shows the ISO7816's package format.

Table270. Package format of ISO7816

bit	0	1~8	9	10	11	12	0	…

Transmit Direction	Transmitter→Receiver			Receiver→Transmitter	--	Transmitter→Receiver	
Definition	Start bit	Data	Parity bit	ACK(1)	Wait	Start bit	…
Value	0	MSB→LSB	P	ACK(1)	1	0	…
TX	0	MSB→LSB	P	1		0	…
RX	1	1	1	ACK(1)	1	1	…
Description	10 bits data			3 bits guarding time		Next Frame	

Note1: If ACK is 0, then the RX will be reset from 1 to 0 at the middle of 10th bit, and set to 1 at 11th or 12th bit, which is controlled by ACKLEN in ISO7816x_CFG.

The transmit package contains totally 10 bits including a start bit and 8 bits data and 1 parity bit. And then in a 3-bits guarding time, the receiver will check the parity correctness response 1 or 2 bits ACK to transmitter. At bit 12, both transmitter and receiver should be kept at high state before next package is ready to be transmitted.

20 Timer/PWM Controller

20.1 Introduction

There are in total 8 timers in V85XX. Four of them are general purpose 32 bits timer. Another 4 timers are 16 bits timers with PWM function. Each timer can generate interrupt to CM0. Each PWM can output 3 outputs with different output waveform. The setting in timer/PWM controller will be reset after wake-up from sleep mode, programmer should restore the setting manually after wake-up from these two states.

20.2 Feature

- 4 32 bits general purpose count timer
- 4 16 bits PWM timer.
- Each PWM timer can have at most 3 outputs.
- 8 output modes.

20.3 Block Diagram

Figure33. Functional Block Diagram of TIMER Controller

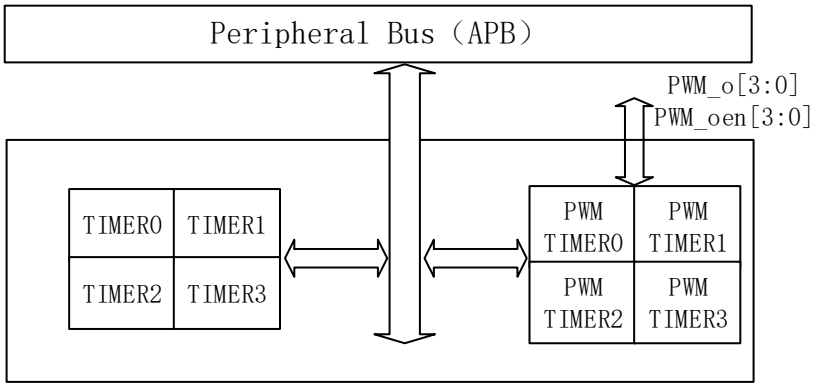
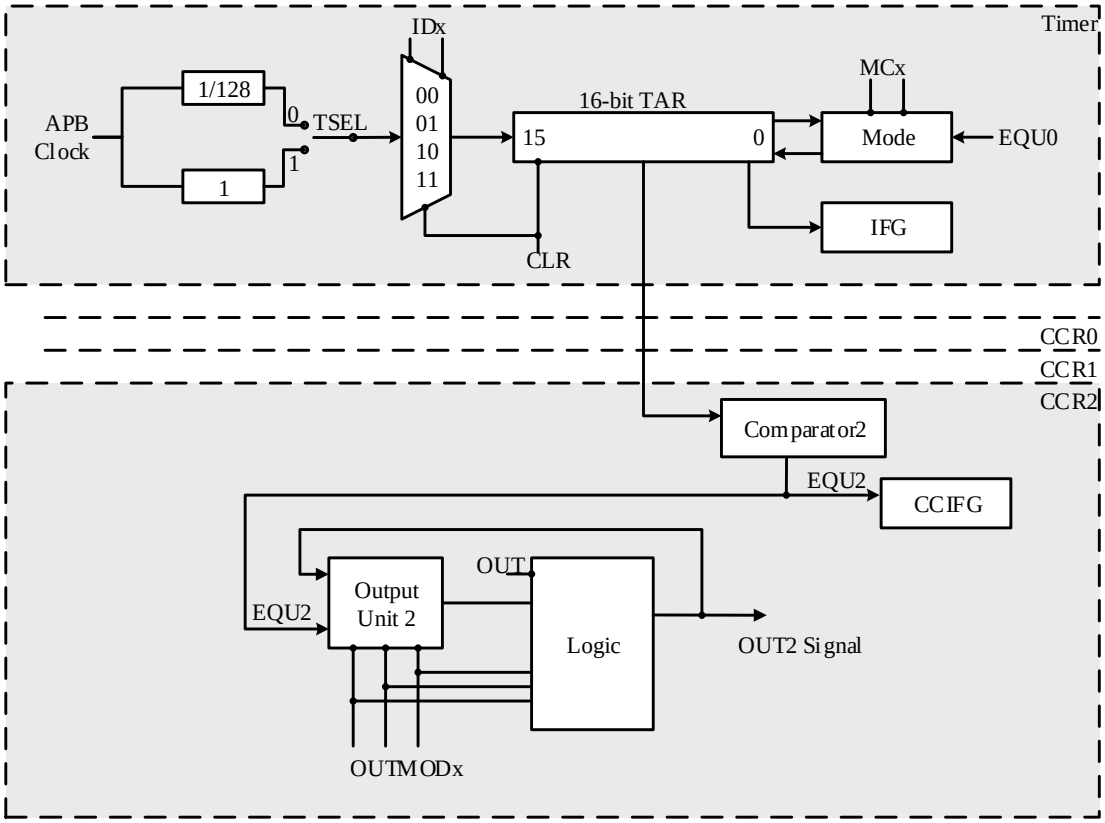


Figure34. Functional Block Diagram of PWM TIMER Controller



20.4 TMR Register Location

Table271. TMR Registers Map

Register Name	Offset	Type	Reset Value	Description
TMR_CTRL	0x0000	rw	0x0000_0000	TMR control register
TMR_VALUE	0x0004	rw	0x0000_0000	TMR current count register
TMR_RELOAD	0x0008	rw	0x0000_0000	TMR reload register
TMR_INT	0x000C	rc_w1	0x0000_0000	TMR interrupt status register

20.5 TMR Register Definition

20.5.1 TMR_CTRL Register

Table272. TMR_CTRL Register Description

Bit	Name	Type	Description
31:4	Rsvd	-	Reserved.
3	INTEN	rw	Timer interrupt enable register.

2	EXTCLK	rw	Select ext_clk (IOB15) as clock source. The ext_clk's rising edge will be used as internal down counter's enable signal. Every time when the ext_clk is rising, the internal counter will decrease by 1. Under this mode, the frequency of ext_clk should be lower than PLCK/6.
1	EXTEN	rw	When the ext_clk (IOB15) is logic 1, the internal down counter will be decreased by 1 with the speed of PCLK. A two clocks sync logic will be applied on the ext_clk to avoid the glitch on the ext_clk. When both the EXTCLK and EXTEN bits are enabled, the EXTCLK bit has higher priority.
0	EN	rw	Timer x enable control register.

20.5.2 TMR_VALUE Register

Table273. TMR_VALUE Register Description

Bit	Name	Type	Description
31:0	VALUE	rw	Timer current value register.

20.5.3 TMR_RELOAD Register

Table274. TMR_RELOAD Register Description

Bit	Name	Type	Description
31:0	RELOAD	rw	Timer x reload value register. A write to this register sets the current value. Every time when the timer down count to 0, the value in this register will be reloaded into the counter and start to down count again. At the same time, the INT bit will be set to 1. The RELOAD of the timer can be calculated by the following equation. RELOAD = Period * APBCLK - 1.

20.5.4 TMR_INT Register

Table275. TMR_INT Register Description

Bit	Name	Type	Description
31:1	Rsvd	-	Reserved.
0	INT	rc_w1	Timer x interrupt status register Write 1 to clear this bit. When the internal down counter timer reach 0, this bit will be set to 1.

20.6 PWM Register Location

Table276. PWM Registers Map

Register Name	Offset	Type	Reset Value	Description
PWM_CTL	0x0000	rw	0x0000_0000	PWM control register
PWM_TAR	0x0004	r	0x0000_0000	PWM current count register
PWM_CCTLx[0..2,0x4]	0x0008	rw	0x0000_0000	PWM compare control register x
PWM_CCRx[0..2,0x4]	0x0014	rw	0x0000_0000	PWM compare data register x

20.7 PWM Register Definition

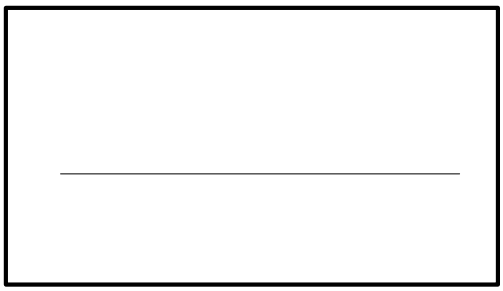
20.7.1 PWM_CTL Register

Table277. PWM_CTL Register Description

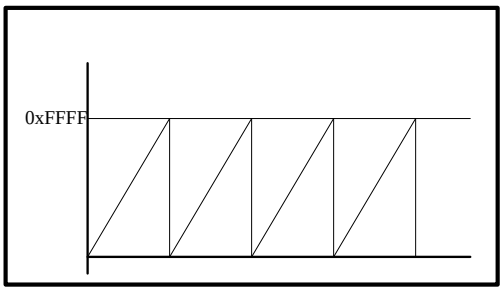
Bit	Name	Type	Description
31:8	Rsvd	-	Reserved.
7:6	ID	rw	PWM timer x Input clock divider control. 0: Input clock divide by 2 1: Input clock divide by 4 2: Input clock divide by 8 3: Input clock divide by 16
5:4	MC	rw	PWM Timer mode control 0: Timer stop. 1: Up-count mode: timer will count to CCR0 and restart from 0. 2: Continuous mode: timer will count to 0xFFFF and start from 0. 3: Up/Down mode: timer will count to CCR0 and then decrease to 0. Refer to Figure35 for each mode.
3	TSEL	rw	Clock source selection 0: APB Clock/128. 1: APB Clock.
2	CLR	rw	TAR clear register When this bit is set to 1, the TAR will be clear to 0. This bit will be cleared to 0 automatically after TAR is cleared.
1	IE	rw	PWM Timer x interrupt enable register.
0	IFG	rc_w1	PWM Timer x interrupt status flag Write 1 to clear this flag to 0. Up mode: Set when counter change from CCR0 to 0. Continuous mode: Set when counter change from

			0xFFFF to 0. Up-Down mode: Set when counter change from 0x0001 to 0.

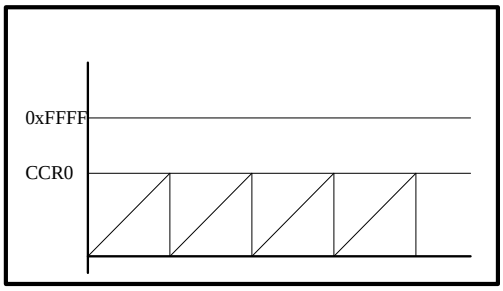
Figure35. Mode description of PWM TIMER Controller



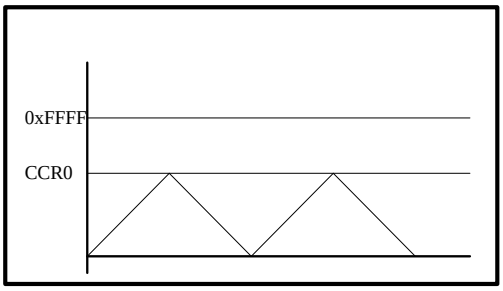
Stop Mode
Timer stop.



Continuous Mode
Timer will count to 0xFFFF, and restart from 0 and count to 0xFFFF.



Up Mode
Timer will count to CCR0, and restart from 0 to CCR0.



Up/Down Mode
Timer will count to CCR0, and then down count to 0x0, and then up_count to CCR0 again.

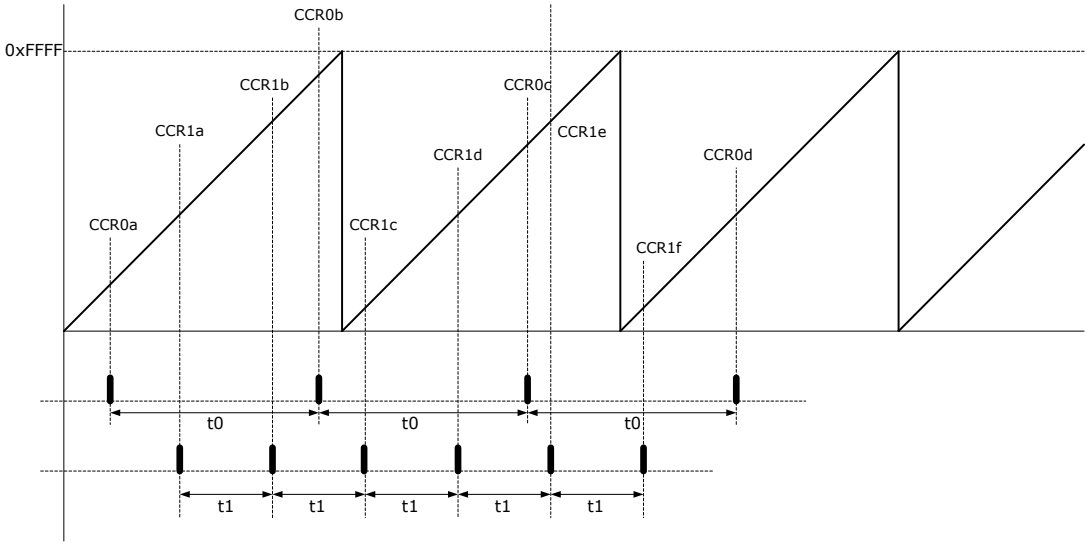
When MC is set to a non-zero value, the timer will start to work. Under up mode or up/down mode, if PWM_CCR0 is set to 0, then timer x will stop counting. The timer will start to count again if a non-zero value is written to PWM_CCR0.

Under up-mode, if the CCR0 is changed during the operation time and new CCR value is larger than current count value, then the timer will count to the new CCR0 then return to 0. And if the new CCR0 is smaller than current count value, the timer will count one tick and reset to 0 to start again.

Under up-down mode and the timer is under up-count process, if the CCR0 is changed during the operation time and new CCR value is larger than current count value, then the timer will count to the new CCR0 then down count to 0. And if the new CCR0 is smaller than current count value, the timer will count one tick and start to down count to 0. Under up-down mode and the timer is under down-count process, if the CCR0 is changed during the operation time, then the timer will continuously complete the down count process.

Under continuous mode, user can set the output frequency depends on the dynamic setting of CCR0~CCR2. The following diagram shows an example of this application.

Figure36. Example of Continuous Mode



In the above diagram, CCR0a or CCR1a is the CCR0 or CCR1 at Ta0 or Ta1, CCR0b or CCR1b is the CCR0 or CCR1 at Tb0 or Tb1. (Tb0=Ta0+t0, Tb1=Ta1+t1)

The above diagram shows that under continuous mode, user can use CCIFG (bit 0 of CCTLx) and CCIE (bit 4 of CCTLx) to generate a regulator interrupt by setting CCR0a and CCR1a to assert interrupt when TAR=CCR0a or TAR=CCR1a. And when TAR=CCR0b or TAR=CCR1b, it can generate another interrupt with different period. The t0 and t1 can be totally independent, so at most user can set 3 totally independent interrupt with one single PWM timer. Under this mode, the IFG flag will be set when the timer count from 0xFFFF to 0x0.

20.7.2 PWM_TAR Register

Table278. PWM_TAR Register Description

Bit	Name	Type	Description
31:0	TAR	rw	PWM Timer real time counting register

20.7.3 PWM_CCTLx Register

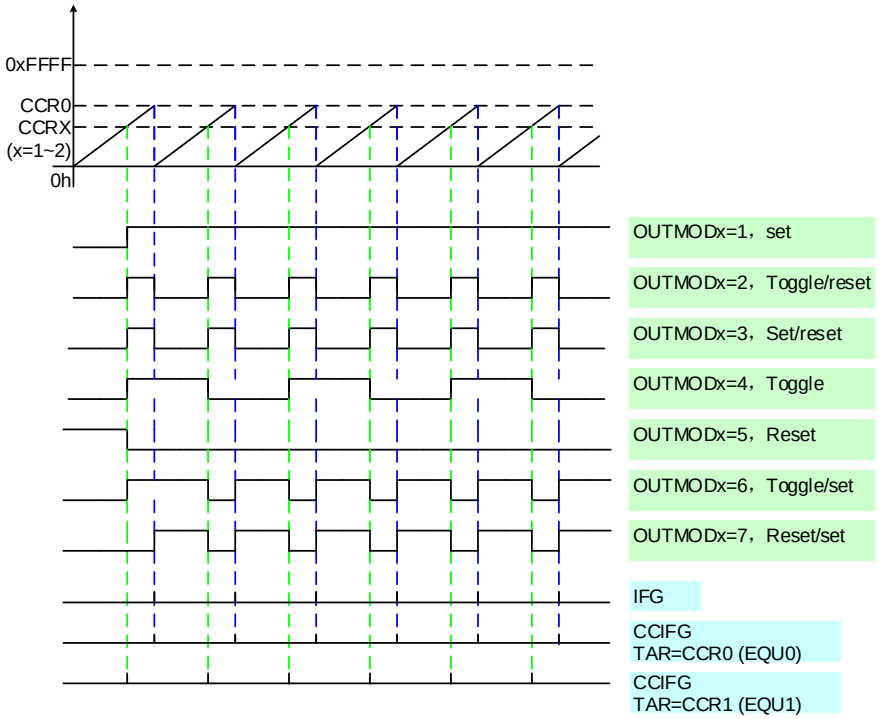
Table279. PWM_CCTLx Register Description

Bit	Name	Type	Description
31:10	Rsvd	-	Reserved.
9	OUTEN	rw	OUTx output enable control register. 0: OUTx output disable 1: OUTx output enable
7:5	OUTMOD	rw	Output mode selection. 0: Constant mode, OUTx output the value of OUT bit. 1: Set mode, OUTx will be set to 1 when TAR=CCRx (x=0~2). 2: Toggle/Reset mode, OUTx will be toggled when

			TAR=CCRx (x=1~2), and will be reset to 0 when TAR=CCR0. This mode can't be used on OUT0. 3: Set/Reset mode, OUTx will be set to 1 when TAR=CCRx (x=1~2), and will be reset to 0 when TAR=CCR0. This mode can't be used on OUT0. 4: Toggle mode, OUTx will be toggled when TAR=CCRx (x=0~2). 5: Reset mode, OUTx will be reset to 0 when TAR=CCRx (x=0~2). 6: Toggle/set mode, OUTx will be toggled when TAR=CCRx (x=1~2), and will be set to 1 when TAR=CCR0. This mode can't be used on OUT0. 7: Reset/set mode, OUTx will be reset to 0 when TAR=CCRx (x=1~2), and will be set to 1 when TAR=CCR0. This mode can't be used on OUT0.
4	CCIE	rw	Compare interrupt enable register.
2	OUT	rw	This bit is used to control the output value of OUTx when OUTMOD is set to 0.
0	CCIFG	rc_w1	Under compare mode, this bit will be set when TAR=CCRx. This bit can be cleared only when write 1 to this bit.

The following figure shows the PWM output under up-mode.

Figure37. PWM Output under Up-count Mode



The following figure shows the PWM output under continuous-mode.

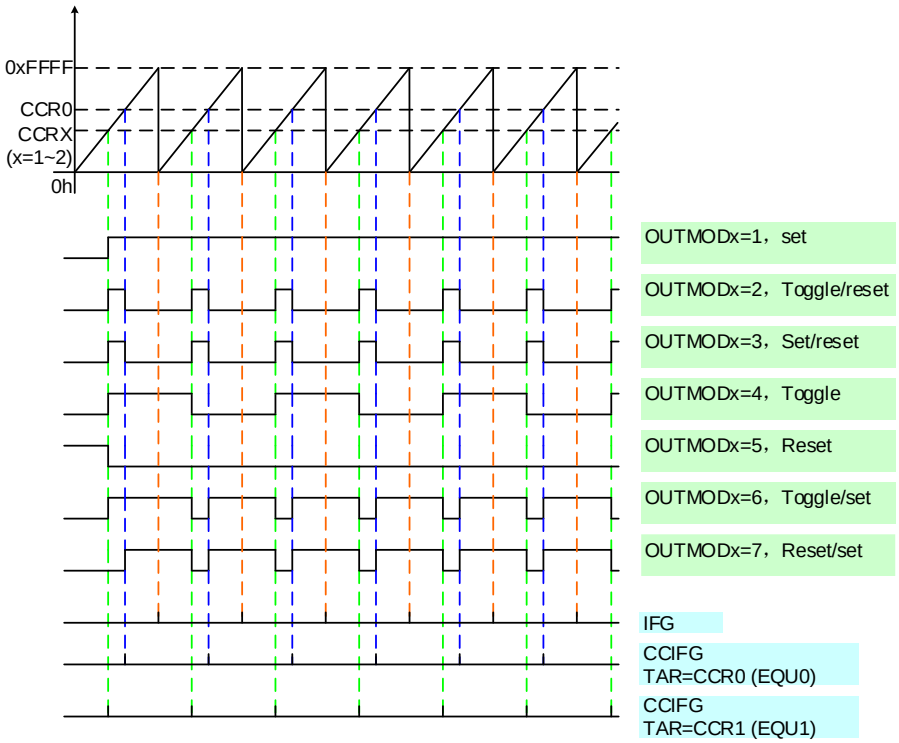
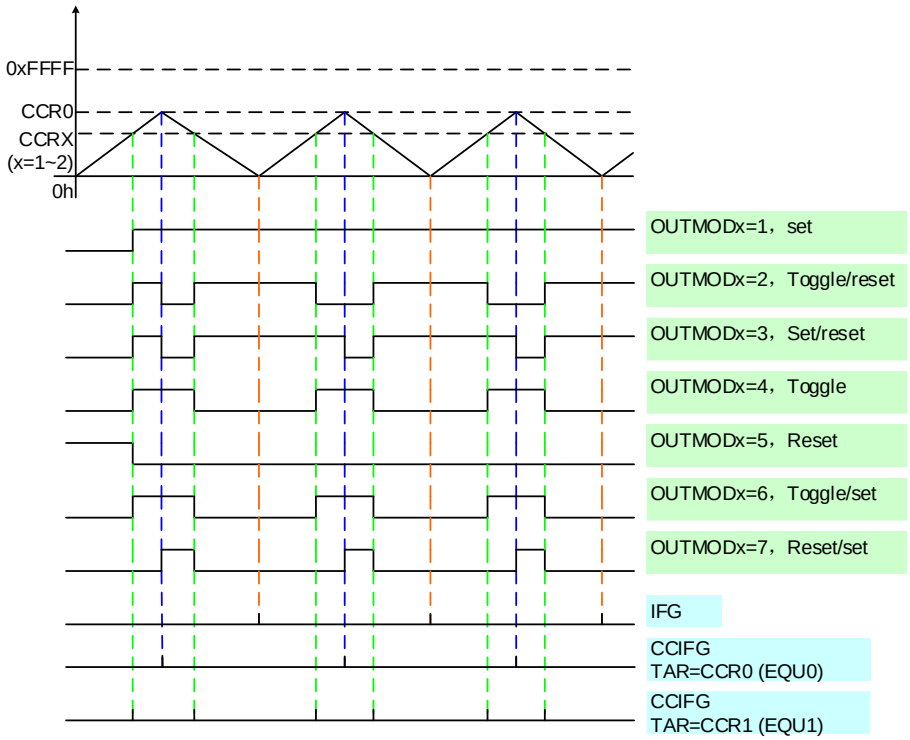


Figure38. PWM Output under Continuous Mode

The following figure shows the PWM output under up/down count mode.

Figure39. PWM Output under Up/down Count Mode



20.7.4 PWM_CCRx Register

Table280. PWM_CCRx Register Description

Bit	Name	Type	Description
31:16	Rsvd	-	Reserved.
15:0	CCRx	rw	Compare data register. This register is used to compare with TAR to generate PWM output.

20.8 PWMMUX Register Location

Table281. PWMMUX Registers Map

Register Name	Offset	Type	Reset Value	Description
PWMMUX_SEL	0x0000	rw	0x0000_DB51	PWM output selection register

20.9 PWMMUX Register Definition

20.9.1 PWMMUX_SEL Register

Table282. PWMMUX_SEL Register Description

Bit	Name	Type	Description

31:16	Rsvd	-	Reserved.
15:12	O_SEL3	rw	External output PWM3 output selection register. Same definition as O_SEL0
11:8	O_SEL2	rw	External output PWM2 output selection register. Same definition as O_SEL0
7:4	O_SEL1	rw	External output PWM1 output selection register. Same definition as O_SEL0
3:0	O_SEL0	rw	External output PWM0 output selection register. 0: From PWM0's OUT0 1: From PWM0's OUT1 2: From PWM0's OUT2 4: From PWM1's OUT0 5: From PWM1's OUT1 6: From PWM1's OUT2 8: From PWM2's OUT0 9: From PWM2's OUT1 10: From PWM2's OUT2 12: From PWM3's OUT0 13: From PWM3's OUT1 14: From PWM3's OUT2 Others: Reserved.

21 LCD Controller

21.1 Introduction

The LCD controller is used to display content on the LCD panel. The LCD controller supports 4 COMs or 6COMs and 8 COMs mode, and maximum 76 segments. There are two frame buffers inside the LCD controller, which support automatically switch function.

21.2 Feature

- Support 4, 6 or 8 COMs mode.
- Support maximum 4 COMs×76 SEGs, 6 COMs×74 SEGs or 8 COMs×72 SEGs.
- Support 1/3 Bias or 1/4 Bias modes
- Bias voltage generated by an individual 3.3V LDO, and can be adjusted from 3.6V-2.7V with resolution of 60mV/LSB
- An internal resistor ladder to generate the LCD waveform voltages--LCD scan frequency generated by the RTCCLK clock
- Two frame buffers which support automatically switch function.
- Adjustable frame rate.

21.3 Block Diagram

Figure40. Functional Block Diagram of LCD Controller

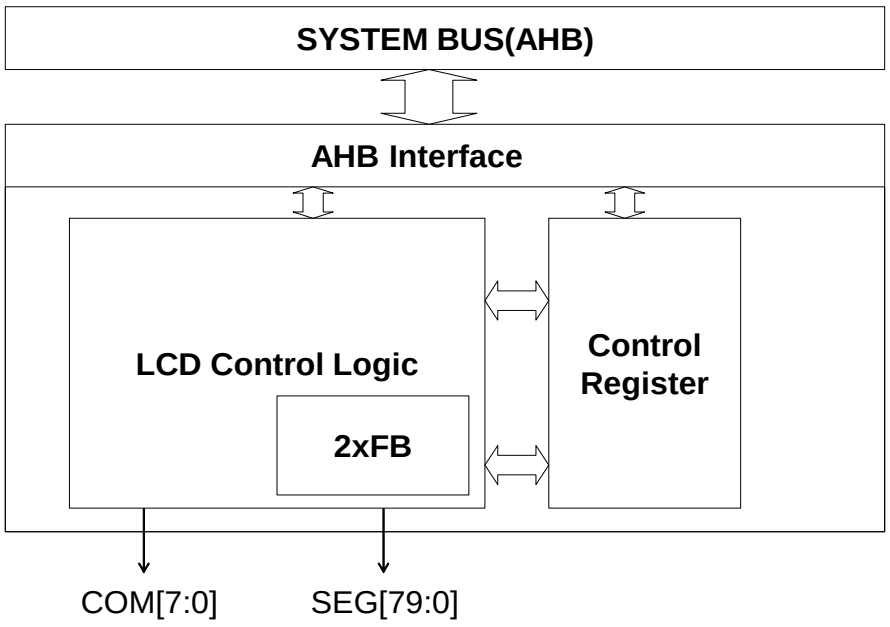
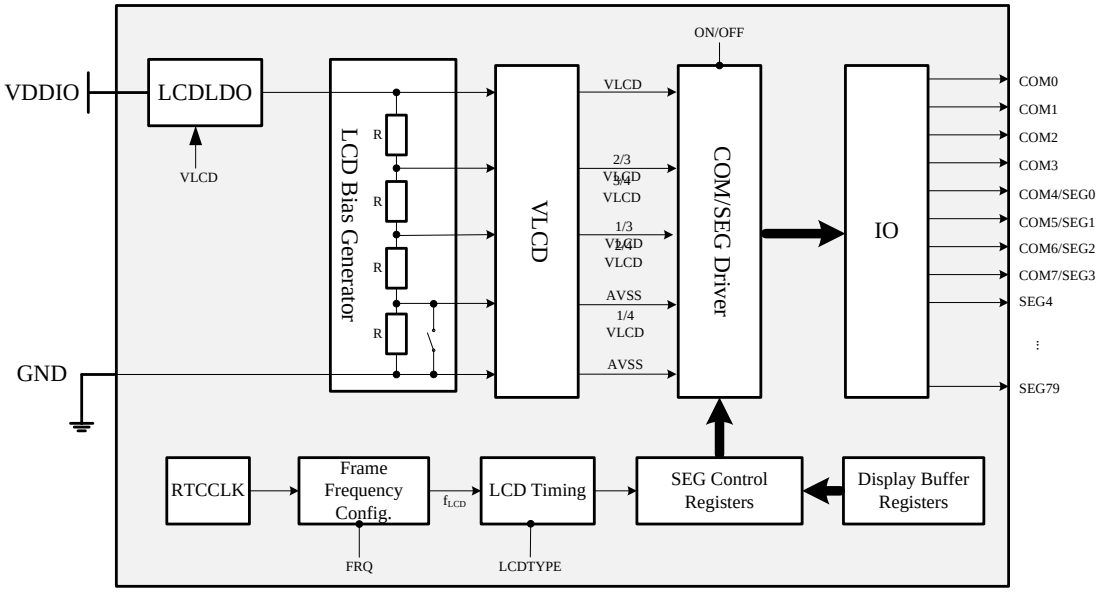


Figure41. LCD Controller Structure Diagram



21.4 LCD Timing

In the V85XX, the CLK, sourced by the 32.768kHz RTCCLK clock, provides the LCD driver with clock pulse for timing generation. Generally, the crystal oscillator keeps on running until it is powered off, so the LCD driver keeps on working even in Sleep state unless CLK is disabled. When the crystal stops running anomaly when power is still on, the internal RC clock will become the replacement of the XTAL clock to source the LCD driver until the crystal is stimulated to run again.

The CLK frequency is divided to generate frame frequency for the waveform. The MCU can configure bit[1:0] of LCD_CTRL to select the appropriate frame frequency. By default it is 64 Hz.

21.5 LCD Waveform Voltage

In the V85XX, the bias voltage of LCD driver is generated by an individual 3.3V LDO, and an internal resistor ladder is designed to generate LCD waveform voltage (VLCD). Users can adjust the waveform voltage via bits VLCD[3:0](bit[4:1] of ANA_REG6).

21.6 LCD Operating Current

Users can adjust the resistance value of each resistor in the resistor ladder of the bias voltage generation circuits via bits DRV[1:0] (bit[3:2] of LCD_CTRL) to adjust the current through the circuits to change the lightness of the display panel. By default, the resistance value is 300 kΩ.

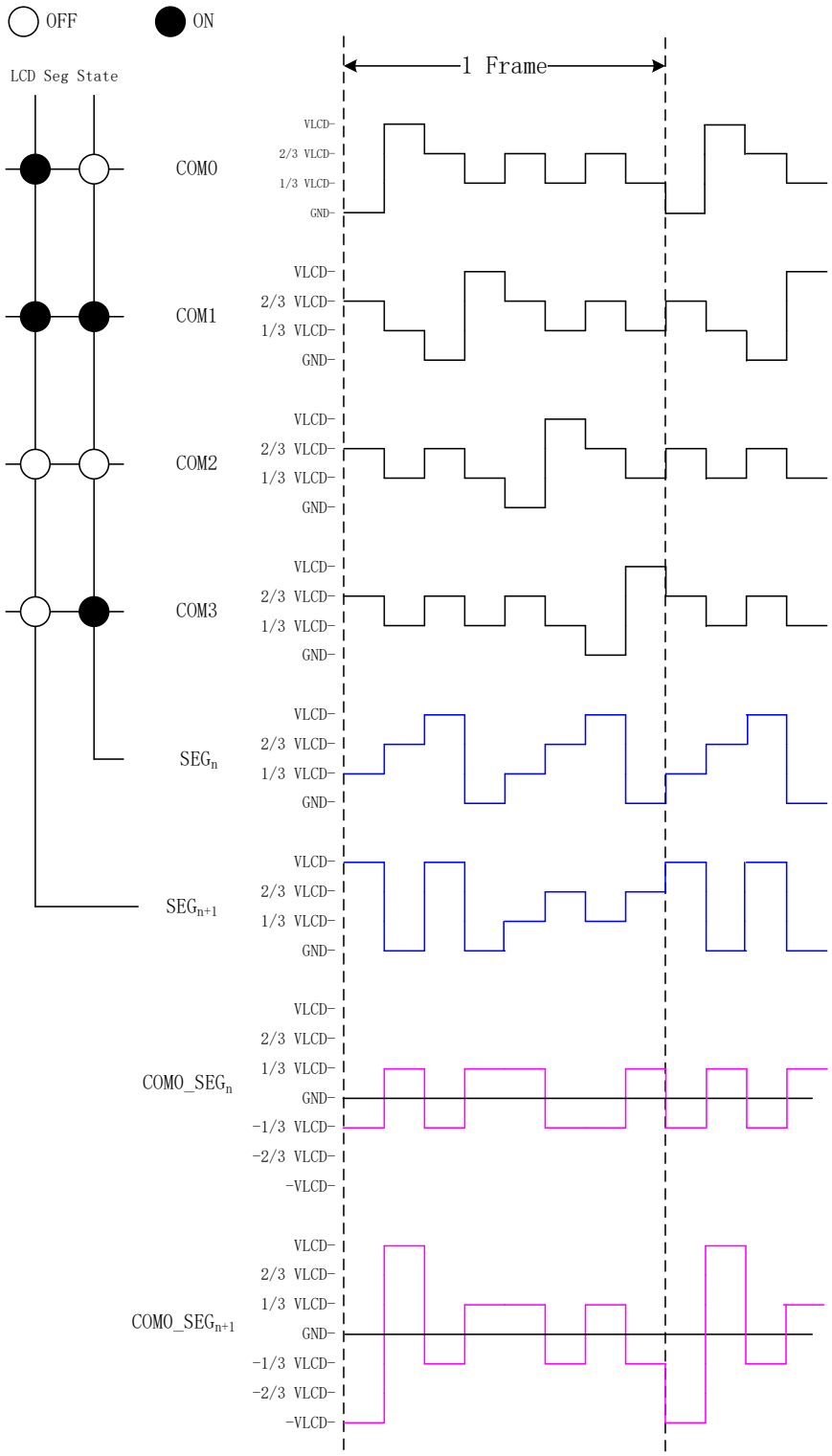
21.7 LCD Drive Waveform

There are 4 resistors in series in the bias voltage generation circuit, which can be configured to

work in 1/3 bias mode or 1/4 bias mode. Users can configure bit LCD_BMOD (bit0 of ANA_REG6) to disable or enable one resistor in the bias voltage generation circuit to enable the LCD driver to work in 1/3 bias mode or 1/4 bias mode.

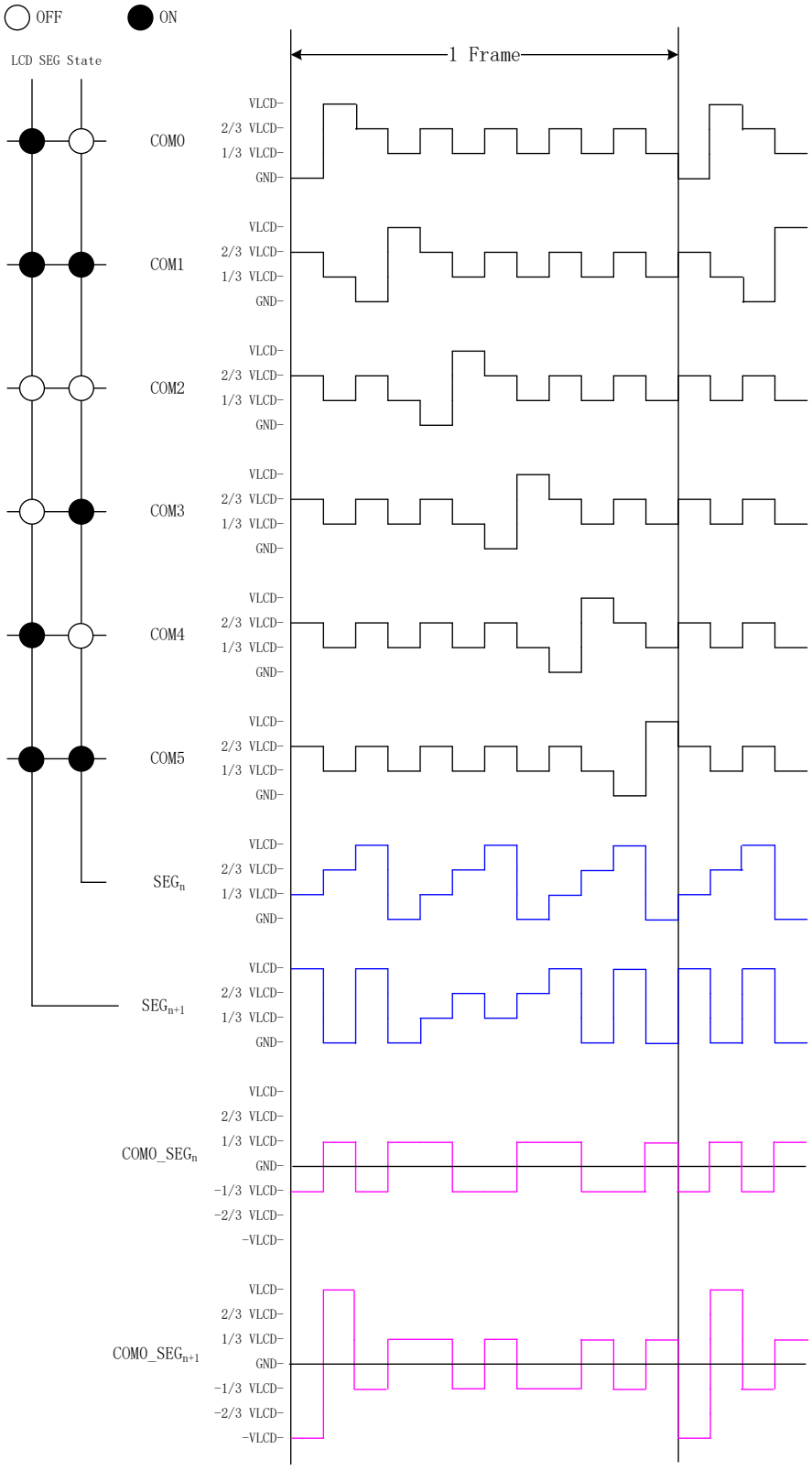
When an LCD panel of 1/4 duty 1/3 bias is applied, the LCD drive waveform is depicted in the following figure.

Figure42. LCD Drive Waveform of 1/4 Duty and 1/3 Bias



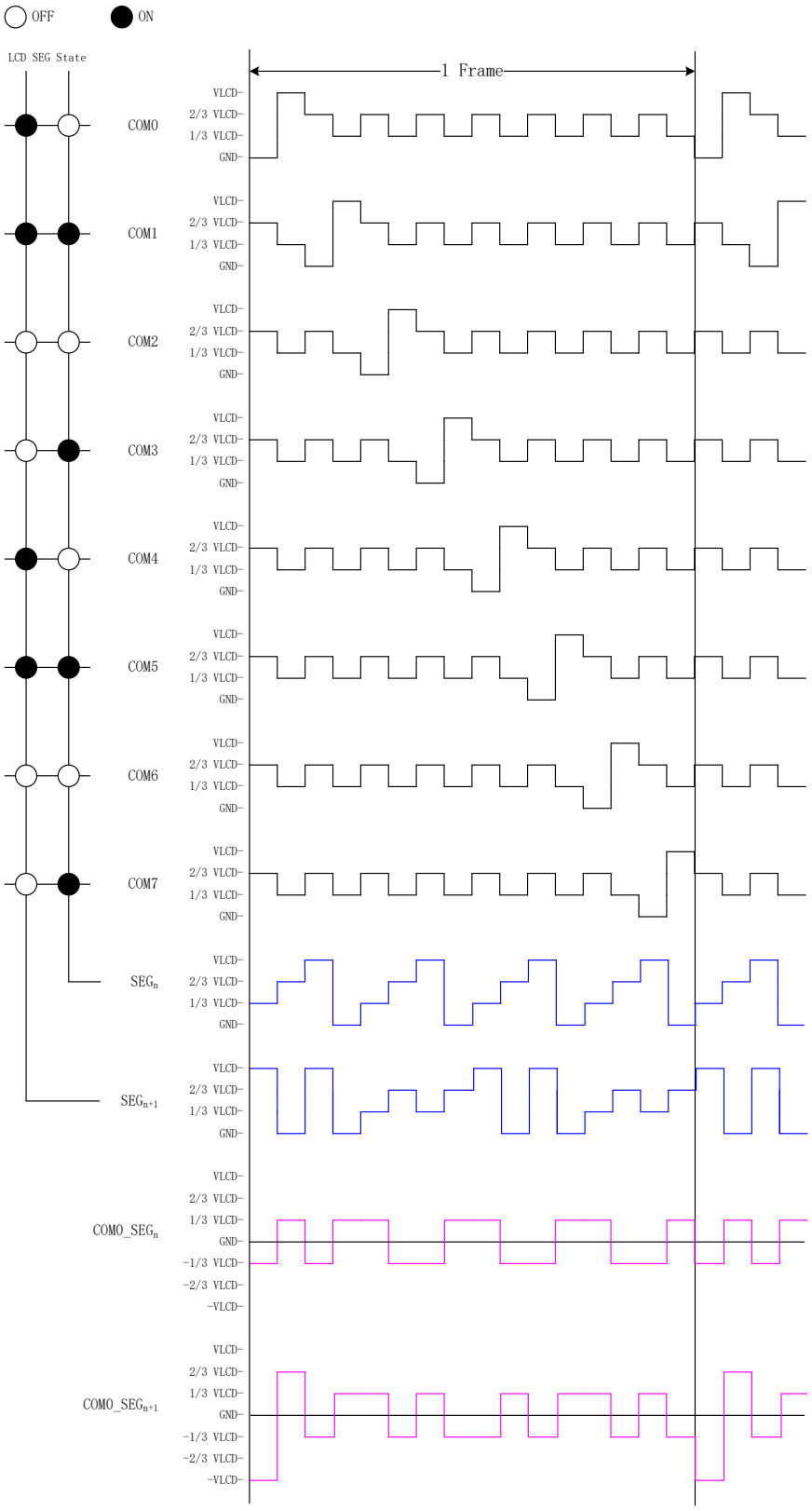
When LCD panel of 1/6 duty and 1/3 bias is applied, the LCD drive waveform is depicted in the following figure.

Figure43. LCD Drive Waveform of 1/6 Duty and 1/3 Bias



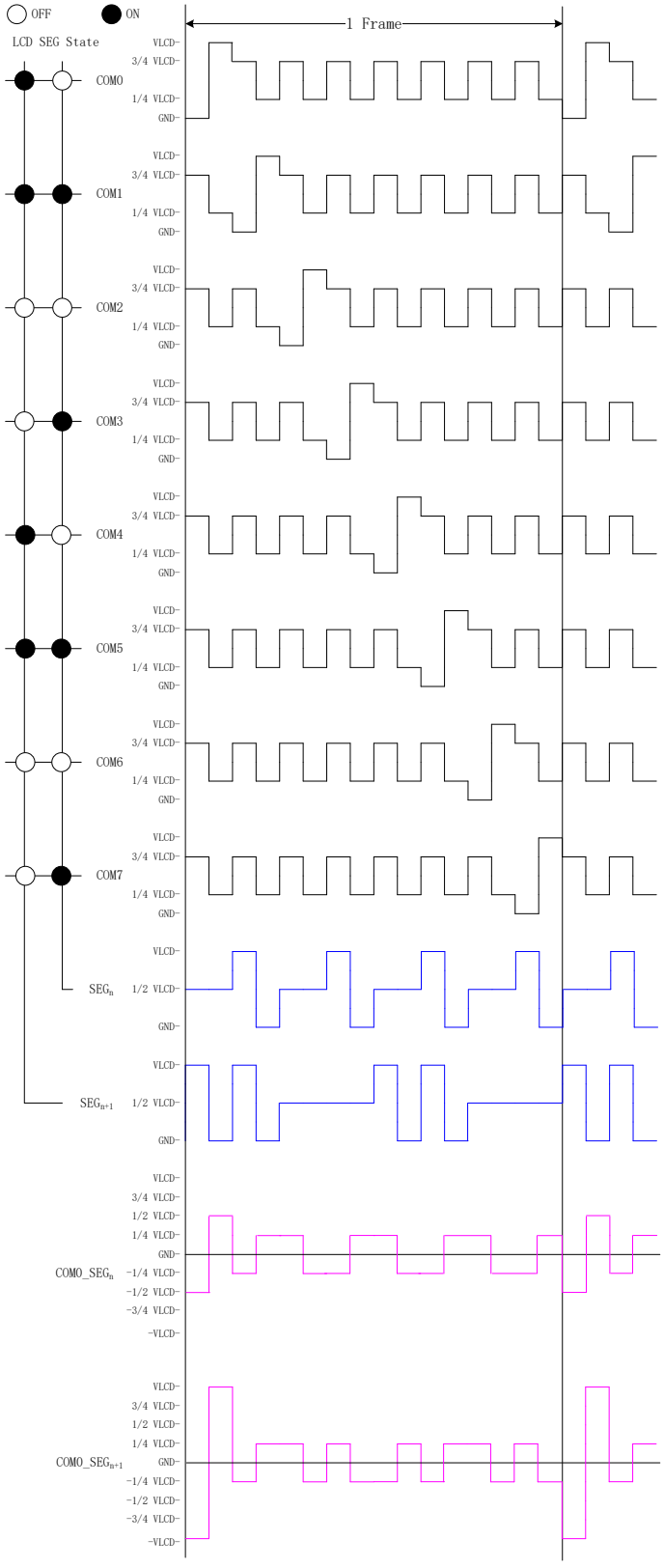
When an LCD panel of 1/8 duty and 1/3 bias is applied, the LCD drive waveform is depicted in the following figures.

Figure44. LCD Drive Waveform of 1/8 Duty and 1/3 Bias



When an LCD panel of 1/8 duty and 1/4 bias is applied, the LCD drive waveform is depicted in the following figures.

Figure45. LCD Drive Waveform of 1/8 Duty and 1/4 Bias



21.8 Register Location

Table283. Register Location of ANA Controller for LCD

Register Name	Offset	Type	Reset Value	Description
ANA_REG6	0x0018	rw	0x0000_0000	Analog control register 6

Table284. LCD Registers Map

Register Name	Offset	Type	Reset Value	Description
LCD_FBx[0..39,0x4]	0x0000	rw	0x0000_0000	LCD Frame buffer 0 register
LCD_CTRL	0x0100	rw	0x0000_0000	LCD control register
LCD_CTRL2	0x0104	rw	0x0000_0000	LCD control register 2
LCD_SEGCTRL0	0x0108	rw	0x0000_0000	LCD segment enable control register 0
LCD_SEGCTRL1	0x010C	rw	0x0000_0000	LCD segment enable control register 1
LCD_SEGCTRL2	0x0110	rw	0x0000_0000	LCD segment enable control register 2

21.9 Register Definition

21.9.1 LCD_FBx Register

Table285. LCD_FBx Register Description

Bit	Name	Type	Description
31:0	DATAx	rw	Each bit represents a data in the display array; see Table 3~6 for detail of data arrangement under different mode. These registers can do byte read or write, so programmer can use CPU or DMA to fill these registers.

The LCD_FB00~LCD_FB13 is frame buffer A.

The LCD_FB14~LCD_FB27 is frame buffer B.

The following tables show only for frame buffer A, if FBMODE is select to 1, the frame buffer B has the same data layout as frame buffer A.

Table286. Data arrangement of LCD_FBx

Register	Data bit			
	31:24	23:16	15:8	7:0
LCD_FB00	COM[7:0] of SEG3	COM[7:0] of SEG2	COM[7:0] of SEG1	COM[7:0] of SEG0

LCD_FB01	COM[7:0] of SEG7	COM[7:0] of SEG6	COM[7:0] of SEG5	COM[7:0] of SEG4
…..				
LCD_FB13	COM[7:0] of SEG79	COM[7:0] of SEG78	COM[7:0] of SEG77	COM[7:0] of SEG76

When 4 or 6 COMs mode is selected, the high bit of COM will be discarded, so the data format is the same as 8 COMs mode.

21.9.2 LCD_CTRL Register

Table287. LCD_CTRL Register Description

Bit	Name	Type	Description
31:8	Rsvd	-	Reserved.
7	EN	rw	LCD controller enable register. 0: Disable 1: Enable
5:4	TYPE	rw	LCD type control register. 0: 4 COM mode 1: 6 COM mode 2: 8 COM mode 3: Reserved.
3:2	DRV	rw	LCD driving resistance control register. 0: 300 kohm 1: 600 kohm 2: 150 kohm 3: 200 kohm
1:0	FRQ	rw	LCD scan frequency 0: 64Hz 1: 128 Hz 2: 256Hz 3: 512Hz The scan frequency here means the scan speed of each COM, so if total COM is 4, then the overall frame rate will be this value divided by 4.

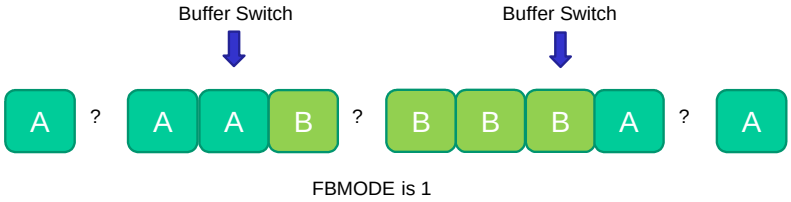
Note1: *If user want to switch COM type, user should disable LCD controller(bit7 of LCD_CTRL register) firstly, and then wait for a delay to ensure the current frame transmission is completed. The delay is calculated according to the current frame rate(bit7 and bit1:0 of LCD_CTRL register). For example, the current LCD scan frequency is 64Hz, and user want switch 4 COM to 6 COM, the delay is calculated as following:* T_{Delay}*=1/(64/4)=62.5ms*

21.9.3 LCD_CTRL2 Register

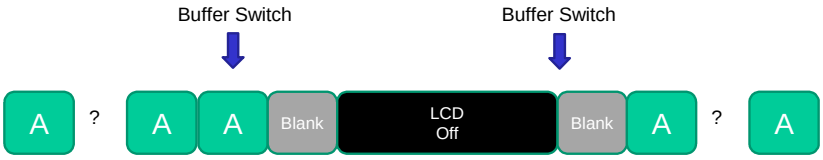
Table288. LCD_CTRL2 Register Description

Bit	Name	Type	Description
31:16	Rsvd	-	Reserved.
15:8	SWPR	rw	Frame buffer switch period. The switch period is calculated by the following equation. 0.5 sec * (SWPR + 1).
7:6	FBMODE	rw	LCD frame buffer switch mode control register. 0: Always show frame buffer A. 1: Switch between frame buffer A and frame buffer B. 2: Switch between frame buffer A and blank. 3: Reserved.
4	BKFILL	rw	Fill value at blank period. This register is used to control the filling value during blank period.

Figure46. Frame buffer operation mode under different FBMODE



FBMODE is 1



FBMODE is 2

21.9.4 LCD_SEGCTRL0 Register

Table289. LCD_SEGCTRL0 Register Description

Bit	Name	Type	Description
31:0	SEGCTRL	rw	Each bit control the SEG0~SEG31's LCD signal enable. Bit 0: SEG 0's enable control. Bit 1: SEG 1's enable control. …. Bit 31: SEG 31's enable control. 0: Disable SEG's output. 1: Enable SEG's output.

21.9.5 LCD_SEGCTRL1 Register

Table290. LCD_SEGCTRL1 Register Description

Bit	Name	Type	Description
31:0	SEGCTRL	rw	Each bit control the SEG32~SEG63's LCD signal enable. Bit 0: SEG 32's enable control. Bit 1: SEG 33's enable control. …. Bit 31: SEG 63's enable control. 0: Disable SEG's output. 1: Enable SEG's output.

21.9.6 LCD_SEGCTRL2 Register

Table291. LCD_SEGCTRL2 Register Description

Bit	Name	Type	Description
31:16	Rsvd	-	Reserved.
15:0	SEGCTRL	rw	Each bit control the SEG64~SEG79's LCD signal enable. Bit 0: SEG 64's enable control. Bit 1: SEG 65's enable control. …. Bit 15: SEG 79's enable control. 0: Disable SEG's output. 1: Enable SEG's output.

21.9.7 ANA_REG6 Register

Table292. Description of each bit in ANA_REG6

Bit	Name	Function	Notes
0	LCD_BMODE	LCD BIAS mode selection	0: 1/3 bias; 1: 1/4 bias.
4:1	VLCD	LCD driving voltage	When VLCD=0:default When VLCD=0~5: adjust range =+60mV*VLCD When VLCD=6~15: adjust range =-60mV* (VLCD-5)

For Each COM and SEG, before enable the corresponding pin's LCD function, programmer should disable corresponding IO input and output function manually, and disable all special function of the corresponding IO to ensure LCD function work correctly.

22 SPI Controller

22.1 Introduction

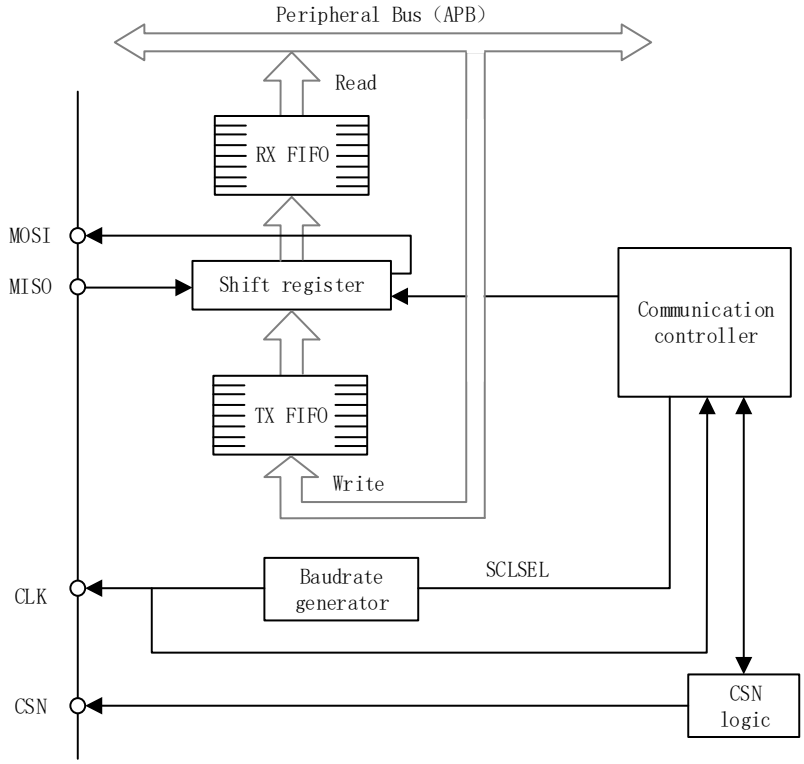
Four independent Serial Peripheral Interface (SPI) controllers are built in V85XX to facilitate communicating with other devices and components. The SPICLK range supported by SPI host mode is APBCLK /2/4/8/16/32/64/128. The maximum SPICLK clock supported by SPI slave mode is APBCLK /2.

22.2 Features

- Support both master and slave mode.
- Support single byte and consecutive bytes transferring.
- Support receiving overrun error indication
- Support transmitting / receiving interrupt request
- Programmable phase and polarity of master clock
- Selectable data sampling time (end or middle of clock period)
- Programmable master SCK clock frequency: APB Clock / 2, / 4, /8, /16, /32, /64, /128
- Built-in 8-depth 8-bits FIFO in both transmit and receive direction, the interrupt level of these two FIFOs is both programmable.

22.3 Block Diagram

Figure47. Functional Block Diagram of SPI Controller



Usually, the SPI is connected to the external device by 4 pins.

MOSI: The output pin in master mode/the input pin in slave mode. In general, MOSI is used to send data in master mode and receive data in slave mode.

MISO: The input pin in master mode/the output pin in slave mode. In general, MISO is used to receive data in master mode and send data in slave mode.

CLK: SPI serial clock pin, and controlled by master.

CSN: Slave chip select pin, According to the setting of SPI and CSN, CSN can be used as following:

- Select a slave to communication.
- Synchronous data frame.

Note1: The maximum SPICLK clock supported by SPI slave mode is 1/2 APBCLK.

22.4 Register Location

Table293. SPI Registers Map

Register Name	Offset	Type	Reset Value	Description
SPI_CTRL	0x0000	rw	0x0000_0000	SPI Control Register
SPI_TXSTS	0x0004	rw	0x0000_8200	SPI Transmit Status Register
SPI_TXDAT	0x0008	rw	0x0000_0000	SPI Transmit FIFO register
SPI_RXSTS	0x000C	rw	0x0000_0000	SPI Receive Status Register
SPI_RXDAT	0x0010	r	0x0000_0000	SPI Receive FIFO Register

SPI_MISC	0x0014	rw	0x0000_0003	SPI Misc. Control Register

22.5 Register Definition

22.6 SPI_CTRL Register

The SPI_CTRL register is used to control the SPI controller's behavior.

Table294. SPI_CTRL Register Description

Bit	Name	Type	Description
31:16	Rsvd	-	Reserved.
15	SPIEN	rw	SPI enable For SPI1 engine if this bit is set to "1", IOB[12:9] becomes SPI1 Interface. These pins cannot be used as GPIO. Therefore, any further corresponding setting on the selected GPIOs will be no effect. For SPI2 engine, if this bit is set to 1, IOC[3:0] becomes SPI2 interface. 0: Disabled 1: Enabled
11	SPIRST	w	SPI Soft Reset. If this bit is written by "1", the state machine of SPI controller and FIFO pointer will return to the original value. 0: No effect 1: Reset SPI Controller
10	CSGPIO	rw	SPI CS pin is controlled by GPIO or H/W. For Master mode. 0: SPI CS pin control by SPI H/W. 1: SPI CS pin control by GPIO setting. For Slave mode. 0: SPI CS pin is controlled by external master. 1: SPI CS pin is connected to logic 0.
9	SWAP	rw	SPI MISO/MOSI swap control register. 0: No swap MISO/MOSI 1: Swap MISO/MOSI.
8	MOD	rw	SPI Mode Selection register 0: Master mode 1: Slave mode
5	SCKPHA	rw	SPI clock phase, refer to timing scheme on following section.
4	SCKPOL	rw	SPI clock polarity, refer to timing scheme on following section.

2:0	SCKSEL	rw	Master mode clock selection 000: APBCLK / 2 001: APBCLK / 4 010: APBCLK / 8 011: APBCLK / 16 100: APBCLK / 32 101: APBCLK / 64 110: APBCLK / 128 111: Reserved.

22.6.1 SPI_TXSTS Register

The SPI_TXSTS register is used to control the SPI transmit FIFO and related interrupt.

Table295. SPI_TXSTS Register Description

Bit	Name	Type	Description
31:16	Rsvd	-	Reserved.
15	SPITXIF	rc_w1	SPI Transmit Interrupt flag. This bit is set to “1” by hardware when the transmit FIFO level is lower than the value set by the user. When SMART is set in SPI_MISC register, the bit will be cleared as long as the transmit FIFO level is high than interrupt level, else you should write “1” to this control bit to clear this flag. Read 0: Not Occurred Read 1: Occurred Write 0: No effect Write 1: Clear the flag
14	SPITXIEN	rw	SPI Transmit Interrupt Enable If this bit is set to “1”, and SPI interrupt (when 8-bit TX FIFO level in lower than interrupt level) occurs, hardware will issue an interrupt to CPU. If this bit is cleared to “0”, this interrupt will be masked. 0: Disabled 1: Enabled
9	TXEMPTY	r	Transmit FIFO empty register. This bit will be set by hardware when the transmit FIFO is empty. And will be clear by hardware when the transmit FIFO is not empty. 0: Not Empty 1: Empty
8	TXFUR	r	Transmit FIFO under run register This will be set when transmit FIFO is empty and more

			data is requested by external SPI master, this bit will be set only at SPI slave mode. This bit will be cleared when programmer write 1 to SPITXIF flag.
6:4	TXFLEV	rw	Transmit FIFO interrupt level register. This register is used to indicated how much bytes is stored in transmit FIFO when issued interrupt. The lower value is set, the lower interrupt penalty you have. Since you can write more data in one interrupt. FIFO Full Interrupt issue timing 000: data no. in FIFO <1, 8 write is allowed. 001: data no. in FIFO <2, 7 write is allowed. 010: data no. in FIFO <3, 6 write is allowed. 011: data no. in FIFO <4, 5 write is allowed. 100: data no. in FIFO <5, 4 write is allowed. 101: data no. in FIFO <6, 3 write is allowed. 110: data no. in FIFO <7, 2 write is allowed. 111: data no. in FIFO <8, 1 write is allowed.
2:0	TXFFLAG	r	Transmit FIFO Data Level. The register is used to indicate how much data is still in the FIFO. 0000: No data in FIFO or 8 bytes in FIFO. 0001: 1 byte in FIFO. 0010: 2 bytes in FIFO. 0011: 3 bytes in FIFO. 0100: 4 bytes in FIFO. 0101: 5 bytes in FIFO. 0110: 6 bytes in FIFO. 0111: 7 bytes in FIFO.

22.6.2 SPI_TXDAT Register

The SPI_TXDAT register is used to write data to transmit FIFO of SPI engine and shift out to external master or slave.

Table296. SPI_TXDAT Register Description

Bit	Name	Type	Description
31:8	Rsvd	-	Reserved.
7:0	SPITXD	w	Write data to SPI Transmit FIFO.

22.6.3 SPI_RXSTS Register

The SPI_RXSTS register is used to control the SPI receive FIFO and related interrupt. Table 18-5 shows the bit assignment of SPI_RXSTS register.

Table297. SPI_RXSTS Register Description

Bit	Name	Type	Description
31:16	Rsvd	-	Reserved.
15	SPIRXIF	rc_w1	SPI Receive Interrupt flag. This bit is set to “1” by hardware when the receive FIFO level is higher than the value set by the user. When SMART is set in SPI_MISC register, the bit will be cleared as long as the receive FIFO level is lower than interrupt level, else you should write “1” to this control bit to clear this flag. Read 0: Not Occurred Read 1: Occurred Write 0: No effect Write 1: Clear the flag
14	SPIRXIEN	rw	SPI Receive Interrupt Enable. If this bit is set to “1”, and SPI interrupt (when 8-bit RX FIFO level in higher than interrupt level) occurs, hardware will issue an interrupt to CPU. If this bit is cleared to “0”, this interrupt will be masked. 0: Disabled 1: Enabled
9	RXFULL	r	Receive FIFO full register. This bit will be set by hardware when the receive FIFO is full. And will be clear by hardware when the receive FIFO is not full. 0: Not Full 1: Full
8	RXFOV	r	Receive FIFO over run register. This will be set when receive FIFO is full and more data is receive on the SPI data bus. This bit will be cleared when write 1 to SPIRXIF.
6:4	RXFLEV	rw	Receive FIFO interrupt level register. This register is used to indicated how much bytes is stored in receive FIFO when issued interrupt. The larger value is set, the lower interrupt penalty you have. Since you can read more data in one interrupt. FIFO Full Interrupt issue timing. 000: data no. in FIFO >= 1, 1 read is allowed. 001: data no. in FIFO >= 2, 2 read is allowed. 010: data no. in FIFO >= 3, 3 read is allowed. 011: data no. in FIFO >= 4, 4 read is allowed. 100: data no. in FIFO >= 5, 5 read is allowed. 101: data no. in FIFO >= 6, 6 read is allowed.

			110: data no. in FIFO >= 7, 7 read is allowed. 111: data no. in FIFO >= 8, 8 read is allowed.
2:0	RXFFLAG	r	Receive FIFO Data Level The register is used to indicate how much data is still in the FIFO. 0000: No data in FIFO or 8 bytes in FIFO 0001: 1 byte in FIFO 0010: 2 bytes in FIFO 0011: 3 bytes in FIFO 0100: 4 bytes in FIFO 0101: 5 bytes in FIFO 0110: 6 bytes in FIFO 0111: 7 bytes in FIFO

22.6.4 SPI_RXDAT Register

The SPI_RXDAT register is used to read data from receive FIFO of SPI engine.

Table298. SPI_RXDAT Register Description

Bit	Name	Type	Description
31:8	Rsvd	-	Reserved.
7:0	SPIRXD	r	Read data from SPI Receive FIFO.

22.6.5 SPI_MISC Register

The SPI_MISC register is used to control misc. features of SPI engine.

Table299. SPI_MISC Register Description

Bit	Name	Type	Description
31:10	Rsvd	-	Reserved.
9	OVER	rw	SPI FIFO Over Write Mode This register is used to control the data will be overwrite or skipped when TX/RX FIFO is full. 0: The further write to the full FIFO will be skipped. 1: The further write to the full FIFO will overwrite the last written data in the FIFO.
8	SMART	rw	SPI FIFO SMART Mode Register When this bit is set to “1”, programmer don’t need to clear the transmit/receive interrupt flag when the FIFO status is reach, programmer only needs write-to/read-from transmit/receive FIFO and let the FIFO level lower/higher than the interrupt level, and the interrupt flag will clear

			automatically. When DMA mode is selected, this bit must be set to 1 to ensure the DMA operation correctly. 0: Normal Interrupt Clear 1: Smart Interrupt Clear
4	BSY	r	SPI Controller Busy Flag This bit is used to indicate if the SPI controller is busy or not. 0: Idle 1: Busy
3	RFF	r	Receive FIFO Full Flag This bit is used to indicate if the SPI controller is real full or not. If the receive FIFO is full, that means any data read from SPI bus can't be written into the FIFO, and the RFOV bit will be set in this situation. 0: Receive FIFO not full 1: Receive FIFO full.
2	RNE	r	Receive FIFO Not Empty Flag This bit is used to indicated if there is any data currently in the receive FIFO. 0: Receive FIFO is empty 1: Receive FIFO is not empty
1	TNF	r	Transmit FIFO Not Full Flag. This bit is used to indicated if there is any empty slots in the transmit FIFO. 0: Transmit FIFO is full, you can't write any more data into it. 1: Transmit FIFO is not full.
0	TFE	r	Transmit FIFO Empty Flag This bit is used to indicated if the transmit FIFO is empty or not. 0: Transmit FIFO is not empty. 1: Transmit FIFO is empty.

22.7 Application Note

22.7.1 Master Mode

When in master mode, the shifting clock (SPICLK) is generated by V85XX. There are two control bits to control the clock phase and polarity. The transmission starts immediately from a register writes to the SPI_TXDAT register. As long as there is data in the FIFO, the transmission will start automatically when one byte is transferred.

The SPI shifts the data from MSB to LSB through the SDO pin. The 8-bit data is shifted out after 8 SCK cycles. At the same time, the data is also shifted in through slave device SDI pin. When

the transmit FIFO level is lower than the interrupt trigger level, the SPITXIF flag bit will be set; besides, a SPI interrupt will be generated if the SPITXIEN bit is set. When the receive FIFO level is higher than the interrupt trigger level, the SPIRXIF flag bit will be set; besides, a SPI interrupt will be generated if the SPIRXIEN bit is set. Programmer can read SPI data from SPI_RXDAT register.

The following diagram depicts the timing scheme on SPI master mode for different operation types (polarity control bit equals “1” or “0”, phase control bit equals “1” or “0”, and sample strobe control bit equals “1” or “0”).

Figure48. Master Mode, SPO = 0, SPH=0

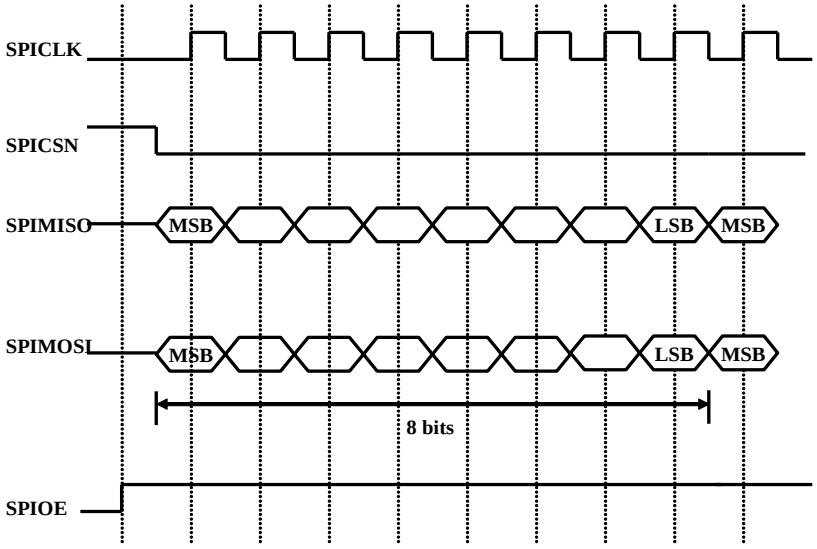


Figure49. Master Mode, SPO = 0, SPH=1

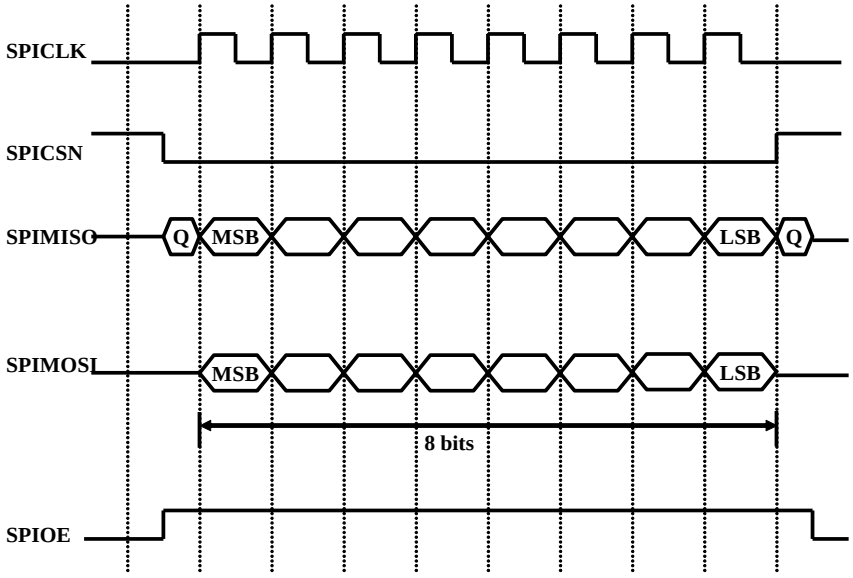


Figure50. Master Mode, SPO = 1, SPH=0

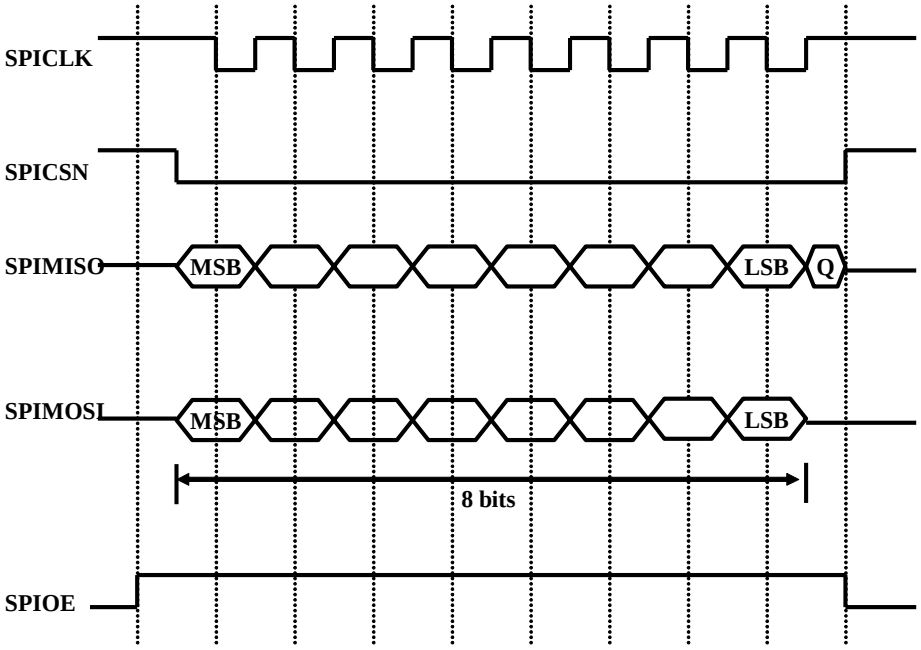
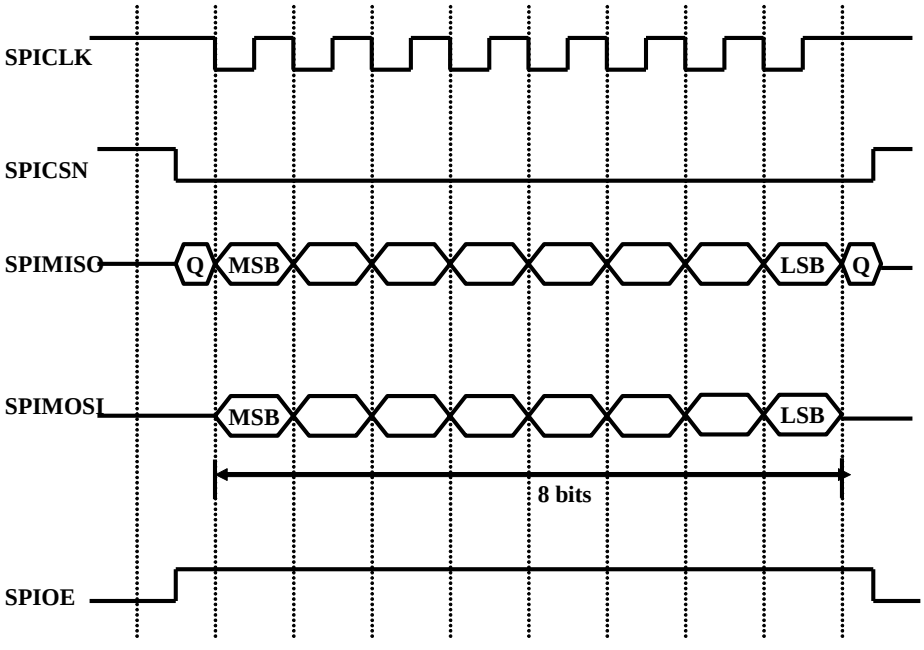


Figure51. Master Mode, SPO = 1, SPH=1



22.7.2 Salve Mode

During SPI salve mode, the SPICLK and SPICSN is generated by the external master. The SPI

slave mode is supported only for SPO=0 and SPH=0. The same SPI_TXDAT and SPI_RXDAT registers are used for data transmit and receive. The maximum allowed SPICLK during SPI slave mode is 1/2 APBCLK. And DMA transfer is recommended when the receive clock is fast.

22.7.3 Consecutive Bytes Transfer

Consecutive bytes transfer is available in master and slave modes. In transmission, software is able to send the data consecutively as long as the TNF bit is 1. In reception, software will check for overrun error to monitor if there is any missing data due to the polling rate is too low.

23 I2C Controller

23.1 Introduction

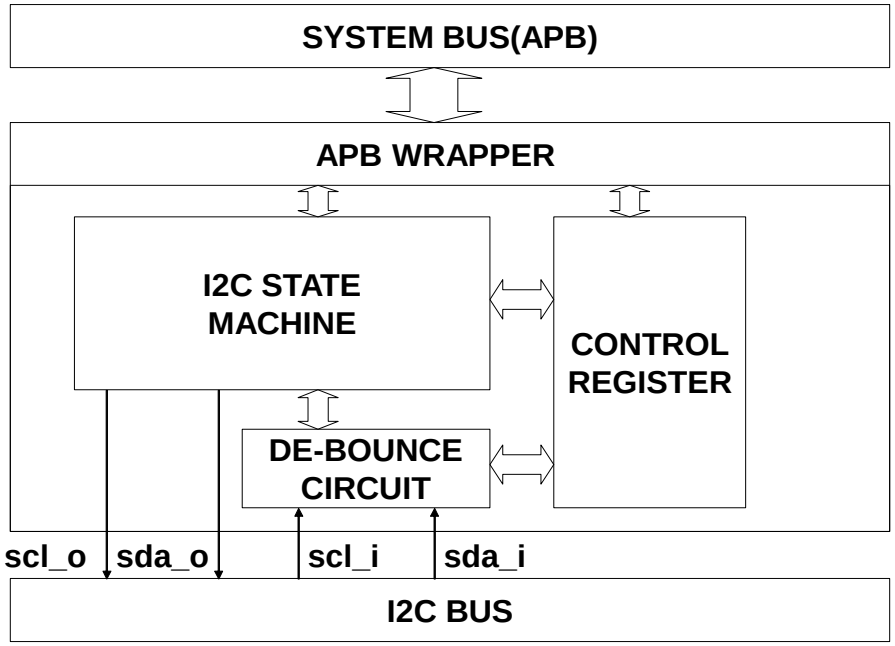
The I2C subcomponent is the I2C Bus Controller which provides an interface that meets the Philips I2C bus specification and supports all transfer modes from and to the I2C bus. The I2C bus uses two wires to transfer information between devices connected to the bus: “scl” (serial clock line) and “sda” (serial data line). The I2C logic handles bytes transfer autonomously. It also keeps track of serial transfers, and a status register reflects the status of the I2C Bus Controller and the I2C bus. The I2C Bus supports f_{SCL} = 1MHz (period: 1us) and can be realized by setting the overflow frequency of timer 3.

23.2 Feature

- Master transmit/receive mode supported.
- Slave transmit/receive mode supported.
- Detection of bus arbitration fail.
- Interrupt generation.
- Programmable ACK generation.
- Programmable clock speed in master mode.
- Input de-bounce circuit.

23.3 Block Diagram

Figure52. Functional Block Diagram of I2C Controller



23.4 Register Location

Table300. I2C Registers Map

Register Name	Offset	Type	Reset Value	Description
I2C_DATA	0x0000	rw	0x0000_0000	I2C data register
I2C_ADDR	0x0004	rw	0x0000_0000	I2C address register
I2C_CTRL	0x0008	rw	0x0000_0000	I2C control/status register
I2C_STS	0x000C	r	0x0000_00F8	I2C status register
I2C_CTRL2	0x0018	rw	0x0000_0000	I2C interrupt enable register

23.5 Register Definition

23.5.1 I2C_DATA Register

Table301. I2C_DATA Register Description

Bit	Name	Type	Description
31:8	Rsvd	-	Reserved.
7:0	DATA	rw	The I2C_DATA register contains a byte to be transmitted through I2C bus or a byte which has just been received through I2C bus. The CPU can read from and write to this 8-bit register while it is not in the process of byte shifting. The I2C_DATA register is not shadowed or double buffered so the user should only read I2C_DATA when an

			I2C interrupt occurs.

23.5.2 I2C_ADDR Register

Table302. I2C_ADDR Register Description

Bit	Name	Type	Description
31:8	Rsvd	-	Reserved.
7:1	SLA	rw	Own I2C slave address (7 bit)
0	GC	rw	General Call Address Acknowledge If this bit is set, the general call address is recognized; otherwise it is ignored.

23.5.3 I2C_CTRL Register

Table303. I2C_CTRL Register Description

Bit	Name	Type	Description
31:8	Rsvd	-	Reserved.
7	CR2	rw	Clock rate bit 2
6	EN	rw	I2C enable bit When EN='0' the "sdao" and "sclo" outputs are set to 1, that drives the output pads of the chip in high impedance, and "sdai" and "scli" input signals are ignored. When EN='1' I2C component is enabled and corresponded GPIO will be set to I2C function automatically.
5	STA	rw	START Flag When STA='1', the I2C component checks the I2C bus status and if the bus is free a START condition is generated.
4	STO	rw	STOP Flag When STO='1' and I2C interface is in master mode, a STOP condition is transmitted to the I2C bus.
3	SI	rc_w1	Serial Interrupt Flag The "SI" is set by hardware when one of 25 out of 26 possible I2C states is entered. The only state that does not set the "SI" is state F8h, which indicates that no relevant state information is available. The "SI" flag must be cleared by software. In order to clear the "SI" bit, '0' must be written to this bit. Writing a '1' to "SI" bit does not change value of the "SI". When an interrupt is occurred, clear SI means the trigger of next action, so all the necessary control register or data must be set before SI

			is cleared.
2	AA	rw	Assert Acknowledge Flag When AA='1', an "acknowledge" will be returned when: - the "own slave address" has been received - the general call address has been received while GC bit in i2caddr register was set - a data byte has been received while I2C was in master receiver mode - a data byte has been received while I2C was in slave receiver mode When AA='0', an "not acknowledge" will be returned when: - a data byte has been received while I2C was in master receiver mode - a data byte has been received while I2C was in slave receiver mode
1	CR1	rw	Clock rate bit 1
0	CR0	rw	Clock rate bit 0

Table304 shows the SCL clock frequency at master mode under different CR2~CR0 setting.

Table304. SCL clock speed setting

CR2	CR1	CR0	SCL Frequency (KHz)				Clock Divided by
			PCLK = 6.5536 MHz	PCLK = 13.1072 MHz	PCLK = 19.6608 MHz	PCLK = 26.2144 MHz	
0	0	0	25.6	51.2	76.8	102.4	256
0	0	1	29.2	58.4	87.6	116.8	224
0	1	0	34.1	68.2	102.3	136.4	192
0	1	1	40.9	81.9	122.9	163.8	160
1	0	0	6.8	13.7	20.5	27.3	960
1	0	1	54.6	109.2	163.8	218.4	120
1	1	0	109.2	218.4	327.7	436.9	60
1	1	1	TIMER3's overflow frequency divide by 8				

23.5.4 I2C_STS Register

Table305. I2C_STS Register Description

Bit	Name	Type	Description
31:8	Rsvd	-	Reserved.
7:3	STS	r	I2C Status Code.
2:0	Rsvd	-	Reserved.

Table306~Table310 shows the status code under different kind of I2C modes.

Table306. I2C Status in Master Transmitter Mode

STS	Status of I2C	Application Software Response					Next Action taken by I2C hardware
		Read/Write	To I2C_CTRL				
		I2C_DATA	STA	STO	SI	AA	
0x08	A START condition has been transmitted.	Write SLA+W*	X	0	0	X	SLA+W will be transmitted ACK will be received
0x10	A repeated START condition has been transmitted.	Write SLA+W	X	0	0	X	SLA+W will be transmitted ACK will be received
		Write SLA+R*	X	0	0	X	SLA+R will be transmitted I2C will be switched to master receive mode
0x18	SLA+W has been transmitted. ACK has been received.	Write data byte	0	0	0	X	Data byte will be transmitted. ACK will be received
		no action	1	0	0	X	Repeated START will be transmitted.
		no action	0	1	0	X	STOP condition will be transmitted. STO flag will be reset
		no action	1	1	0	X	STOP condition followed by a START condition will be transmitted. STO flag will be reset
0x20	SLA+W has been transmitted. NACK has been received.	Write data byte	0	0	0	X	Data byte will be transmitted. ACK will be received
		no action	1	0	0	X	Repeated START will be transmitted.
		no action	0	1	0	X	STOP condition will be transmitted. STO flag will be reset
		no action	1	1	0	X	STOP condition followed by a START condition will be transmitted. STO flag will be reset
0x28	Data byte in i2cdat has been	Write data byte	0	0	0	X	Data byte will be transmitted. ACK bit will

	transmitted. ACK has been received.						be received
		no action	1	0	0	X	Repeated START will be transmitted.
		no action	0	1	0	X	STOP condition will be transmitted. STO flag will be reset.
		no action	1	1	0	X	STOP condition followed by a START condition will be transmitted. STO flag will be reset.
0x30	Data byte in i2cdat has been transmitted. NACK has been received.	Write data byte	0	0	0	X	Data byte will be transmitted. ACK will be received.
		no action	1	0	0	X	Repeated START will be transmitted.
		no action	0	1	0	X	STOP condition will be transmitted. STO flag will be reset.
		no action	1	1	0	X	STOP condition followed by a START condition will be transmitted. STO flag will be reset.

Note1: SLA+W: Slave address [7:1] and write bit as bit 0, write bit is 0.

Note2: SLA+R: Slave address [7:1] and read bit as bit 0, read bit is 1.

Table307. I2C Status in Master Receiver Mode

STS	Status of I2C	Application Software Response					Next Action taken by I2C hardware
		Read/Write	To I2C_CTRL				
		I2C_DATA	STA	STO	SI	AA	
0x08	A START condition has been transmitted	Write SLA+R	X	0	0	X	SLA+R will be transmitted. ACK will be received
0x10	A repeated START condition has been transmitted.	Write SLA+R	X	0	0	X	SLA+R will be transmitted. ACK will be received
		Write SLA+W	X	0	0	X	SLA+W will be transmitted. I2C will be switched to master transmit mode
0x40	SLA+R has been transmitted. ACK has been received.	no action	0	0	0	0	Data byte will be received. not ACK will be returned

		no action	0	0	0	1	Data byte will be received. ACK will be returned
0x48	SLA+R has been transmitted. Not ACK has been received.	no action	1	0	0	X	Repeated START condition will be transmitted
		no action	0	1	0	X	STOP condition will be transmitted. STO flag will be reset
		no action	1	1	0	X	STOP condition followed by a START condition will be transmitted. STO flag will be reset
0x50	Data byte has been received. ACK has been returned.	Read data byte	0	0	0	0	Data byte will be received. not ACK will be returned
		Read data byte	0	0	0	1	Data byte will be received. ACK will be returned
0x58	Data byte has been received. Not ACK has been returned.	Read data byte	1	0	0	X	Repeated START condition will be transmitted
		Read data byte	0	1	0	X	STOP condition will be transmitted. STO flag will be reset
		Read data byte	1	1	0	X	STOP condition followed by a START condition will be transmitted. STO flag will be reset

Table308. I2C Status in Slave Receiver Mode

STS	Status of I2C	Application Software Response					Next Action taken by I2C hardware
		Read/Write	To I2C_CTRL				
		I2C_DATA	STA	STO	SI	AA	
0x60	Own SLA+W has been received. ACK has been returned.	no action	X	0	0	0	Data byte will be received and not ACK will be returned.
		no action	X	0	0	1	Data byte will be received and ACK will be returned.
0x68	Arbitration lost in SLA+R/W as master.	no action	X	0	0	0	Data byte will be received and not ACK

	Own SLA+W has been received, ACK returned.						will be returned.
		no action	X	0	0	1	Data byte will be received and ACK will be returned.
0x70	General call address (00H) has been received. ACK has been returned.	no action	X	0	0	0	Data byte will be received and not ACK will be returned.
		no action	X	0	0	1	Data byte will be received and ACK will be returned.
0x78	Arbitration lost in SLA+R/W as master. General call address has been received, ACK returned.	no action	X	0	0	0	Data byte will be received and not ACK will be returned.
		no action	X	0	0	1	Data byte will be received and ACK will be returned.
0x80	Previously addressed with own SLV address. DATA has been received. ACK returned.	Read data byte	X	0	0	0	Data byte will be received and not ACK will be returned.
		Read data byte	X	0	0	1	Data byte will be received and ACK will be returned.
0x88	Previously addressed with own SLA. DATA byte has been received. Not ACK returned.	Read data byte	0	0	0	0	Switched to not addressed SLV mode. No recognition of own SLA or general call address.
		Read data byte	0	0	0	1	Switched to not addressed SLV mode. Own SLA or general call address will be recognized.
		Read data byte	1	0	0	0	Switched to not addressed SLV mode. No recognition of own SLA or general call address. START condition will be transmitted when the bus becomes free.
		Read data byte	1	0	0	1	Switched to not addressed SLV mode. Own SLA or general call

							address will be recognized. START condition will be transmitted when the bus becomes free.
0x90	Previously addressed with general call address. DATA has been received. ACK returned.	Read data byte	X	0	0	0	Data byte will be received and not ACK will be returned.
		Read data byte	X	0	0	1	Data byte will be received and ACK will be returned.
0x98	Previously addressed with general call address. DATA has been received. Not ACK returned.	Read data byte	0	0	0	0	Switched to not addressed SLV mode. No recognition of own SLA or general call address
		Read data byte	0	0	0	1	Switched to not addressed SLV mode. Own SLA or general call address will be recognized.
		Read data byte	1	0	0	0	Switched to not addressed SLV mode; no recognition of own SLA or general call address. START condition will be transmitted when the bus becomes free.
		Read data byte	1	0	0	1	Switched to not addressed SLV mode. Own SLA or general call address will be recognized. START condition will be transmitted when the bus becomes free
0xA0	A STOP condition or repeated START condition has been received while still addressed as slave receive or slave transmit mode.	no action	0	0	0	0	Switched to not addressed SLV mode. No recognition of own SLA or general call address.
		no action	0	0	0	1	Switched to not addressed slave mode.

							Own SLA or general call address will be recognized.
		no action	1	0	0	0	Switched to not addressed SLV mode. No recognition of own SLA or general call address. START condition will be transmitted when the bus becomes free
		no action	1	0	0	1	Switched to not addressed SLV mode. Own SLA or general call address will be recognized. START condition will be transmitted when the bus becomes free.

Table309. I2C Status in Slave Transmitter Mode

STS	Status of I2C	Application Software Response					Next Action taken by I2C hardware
		Read/Write	To I2C_CTRL				
		I2C_DATA	STA	STO	SI	AA	
0xA8	Own SLA+R has been received. ACK has been returned.	Write data byte	X	0	0	0	Last data byte will be transmitted and ACK will be received.
		Write data byte	X	0	0	1	Data byte will be transmitted. ACK will be received.
0xB0	Arbitration lost in SLA+R/W as master. Own SLA+R has been received. ACK has been returned.	Write data byte	X	0	0	0	Last data byte will be transmitted and ACK will be received.
		Write data byte	X	0	0	1	Data byte will be transmitted. ACK will be received.
0xB8	Data byte has been transmitted. ACK has been received.	Write data byte	X	0	0	0	Last data byte will be transmitted and ACK will be received.
		Write data byte	X	0	0	1	Data byte will be transmitted; ACK will be received.

0xC0	Data byte has been transmitted. NACK has been received.	no action	0	0	0	0	Switched to not addressed SLV mode. No recognition of own SLA or general call address.
		no action	0	0	0	1	Switched to not addressed SLV mode. Own SLA or general call address will be recognized.
		no action	1	0	0	0	Switched to not addressed SLV mode. No recognition of own SLA or general call address. START condition will be transmitted when the bus becomes free.
		no action	1	0	0	1	Switched to not addressed SLV mode. Own SLA or general call address will be recognized. START condition will be transmitted when the bus becomes free.
0xC8	Last data byte has been transmitted. ACK has been received.	no action	0	0	0	0	Switched to not addressed SLV mode. No recognition of own SLA or general call address.
		no action	0	0	0	1	Switched to not addressed SLV mode. Own SLA or general call address will be recognized.
		no action	1	0	0	0	Switched to not addressed SLV mode. No recognition of own SLA or general call address. START condition will be transmitted when the bus becomes free.
		no action	1	0	0	1	Switched to not addressed SLV mode. Own SLA or general call address will be

							recognized. START condition will be transmitted when the bus becomes free.

Table310. I2C Misc. Status

STS	Status of I2C	Application Software Response					Next Action taken by I2C hardware
		Read/Write	To I2C_CTRL				
		I2C_DATA	STA	STO	SI	AA	
0x38	Arbitration lost	No action	0	0	0	X	I2C bus will be released; A start condition will be transmitted.
		No action	1	0	0	X	when the bus becomes free (enter to a master mode)
0xF8	No relevant state information available; si=0	No action	X	X	X	X	Wait or proceed current transfer
0x00	Bus error during MST or selected slave modes	No action	0	1	0	X	Only the internal hardware is affected in the MST or addressed SLV modes. In all cases, the bus is released and I2C is switched to the not addressed SLV mode. Sto flag is reset.

23.5.5 I2C_CTRL2 Register

Table311. I2C_CTRL2 Register Description

Bit	Name	Type	Description
31:1	Rsvd	-	Reserved.
0	INTEN	rw	Interrupt enable control of I2C controller. 0: Disable. 1: Enable.

23.6 Application Notes

23.6.1 I2C Bus Protocol: Start/Stop Generation

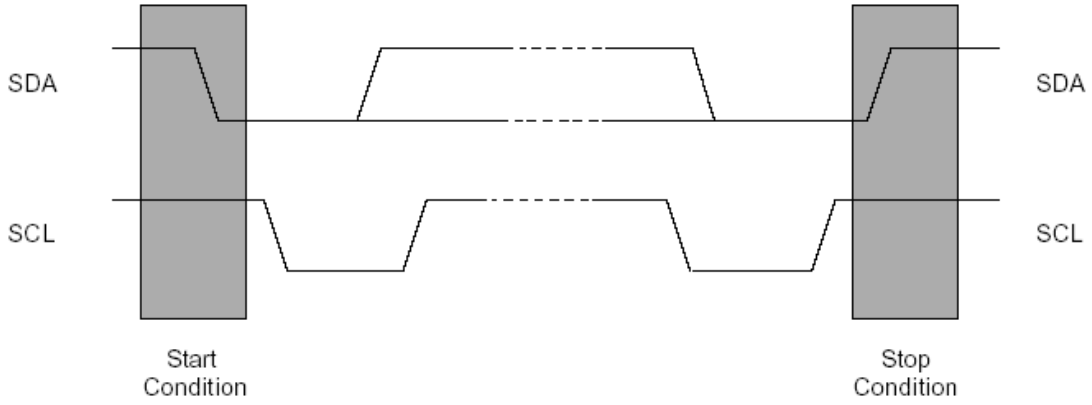
A Start condition can transfer a one-byte serial data over the SDA line, and a stop condition can terminate the data transfer. A stop condition is a Low-to-High transition of the SDA line while SCL

is high. Start and Stop conditions are always generated by the master. The I2C-bus is busy when a Start condition is generated. A few clocks after a Stop condition, the IIC-bus will be free, again.

When a master initiates a Start condition, it should send a slave address to notify the slave device. The one byte of address field consists of a 7-bit address and a 1-bit transfer direction indicator (that is, write or read). If bit 8 is 0, it indicates a write operation (transmit operation); if bit 8 is 1, it indicates a request for data read (receive operation).

The master will finish the transfer operation by transmitting a Stop condition. If the master wants to continue the data transmission to the bus, it should generate another Start condition as well as a slave address. In this way, the read/write operation can be performed in various formats.

Figure53. Start and Stop Conditions



23.6.2 Data Transfer Format

Every byte placed on the SDA line should be eight bits in length. The number of bytes which can be transmitted per transfer is unlimited. The first byte following a Start condition should have the address field. The address field can be transmitted by the master when the IIC-bus is operating in master mode. Each byte should be followed by an acknowledgement (ACK) bit. The MSB bit of the serial data and addresses are always sent first.

Figure54. Write Mode with 7-bits Address

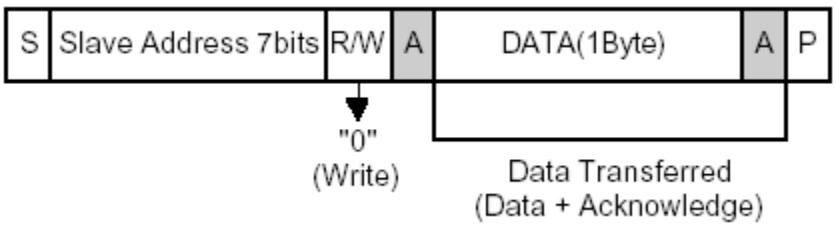


Figure55. Read Mode with 7-bits Address

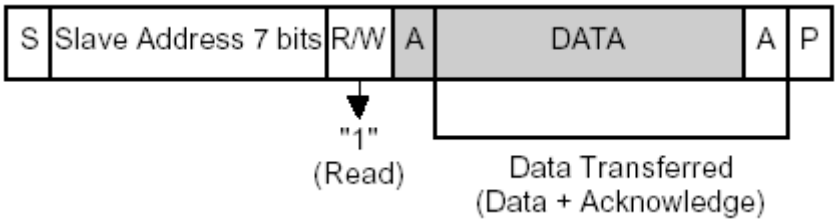
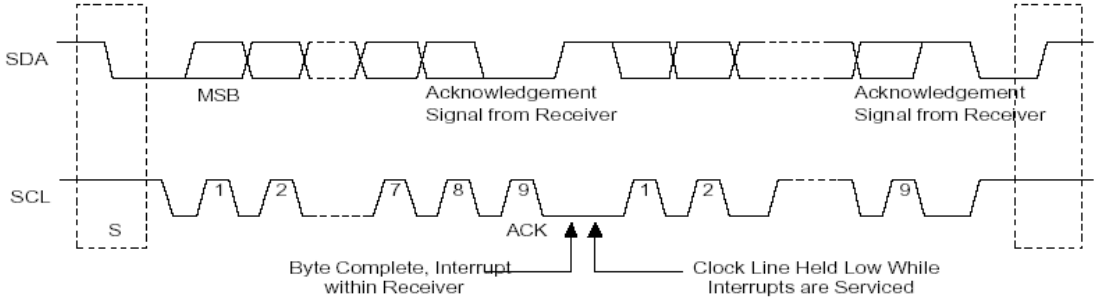


Figure56. Data Transfer on The I2C bus



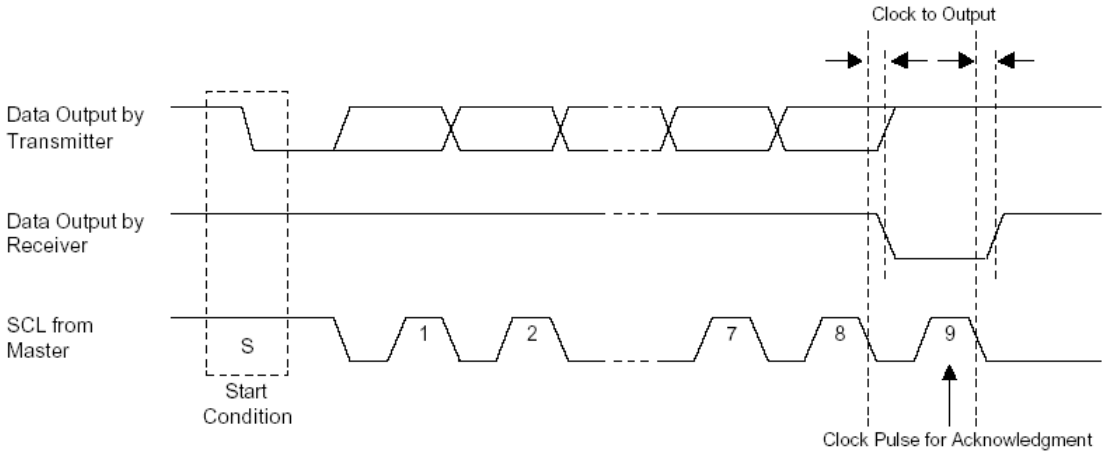
23.6.3 ACK Signal Transmission

To finish a one-byte transfer operation completely, the receiver should send an ACK bit to the transmitter. The ACK pulse should occur at the ninth clock of the SCL line. Eight clocks are required for the one-byte data transfer. The master should generate the clock pulse required to transmit the ACK bit.

The transmitter should release the SDA line by making the SDA line High when the ACK clock pulse is received. The receiver should also drive the SDA line Low during the ACK clock pulse so that the SDA is Low during the High period of the ninth SCL pulse.

The ACK bit transmit function can be enabled or disabled by software (AA). However, the ACK pulse on the ninth clock of SCL is required to complete a one-byte data transfer operation.

Figure57. Acknowledge on The I2C bus



23.6.4 Read-Write Operation

In the transmitter mode, after the data is transferred, the I2C-bus interface will wait until pending interrupt is cleared. Until the interrupt is cleared, the SCL line will be held low. After the interrupt is cleared, the SCL line will be released. After the CPU receives the interrupt request, it should write a new data into I2C_DATA before clear the pending interrupt.

In the receive mode, after a data is received, the I2C-bus interface will wait until pending interrupt is cleared. Until the pending interrupt is cleared, the SCL line will be held low. After the pending interrupt is cleared, the SCL line will be released. After the CPU receives the interrupt request, it should read the data from I2C_DATA before clear the pending interrupt.

Bus Arbitration Procedures

Arbitration takes place on the SDA line to prevent the contention on the bus between two masters. If a master with a SDA High level detects another master with a SDA active Low level, it will not initiate a data transfer because the current level on the bus does not correspond to its own. The arbitration procedure will be extended until the SDA line turns high.

However when the masters simultaneously lower the SDA line, each master should evaluate whether or not the mastership is allocated to itself. For the purpose of evaluation, each master should detect the address bits. While each master generates the slaver address, it should also detect the address bit on the SDA line because the

Lowering of SDA line is stronger than maintaining High on the line. For example, one master generates a Low as first address bit, while the other master is maintaining High. In this case, both masters will detect Low on the bus because Low is stronger than high even if first master is trying to maintain high on the line. When this happens, low (as the first bit of address) -generating master will get the mastership and high (as the first bit of address) - generating master should withdraw the mastership. If both masters generate Low as the first bit of address, there should be an arbitration for second address bit, again. This arbitration will continue to the end of last address bit.

Abort Condition

If a slave receiver can’t acknowledge the confirmation of the slave address, it should hold the

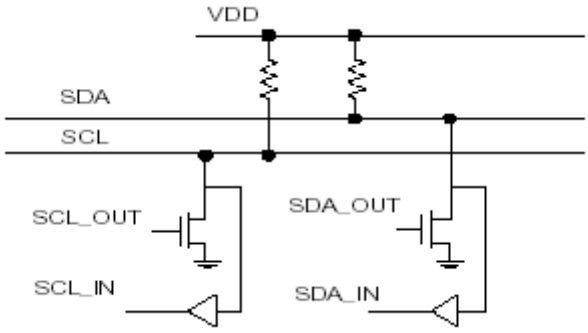
level of the SDA line High. In this case, the master should generate a Stop condition and abort the transfer.

If a master receiver is involved in the aborted transfer, it should signal the end of the slave transmit operation by canceling the generation of an ACK after the last data byte received from the slave. The slave transmitter should then release the SDA to allow a master to generate a Stop condition.

23.6.5 Interface Timing

The following diagram shows the interface connection of I2C bus.

Figure58. I2C Bus Connection Example



To control the frequency of the serial clock (SCL), programmer can use CR2~CR0 in the I2C_CTRL register.

The I2C Bus supports f_{SCL} = 1MHz (period: 1us).

- Rise Time of the SCL and SDA: f_{SCL}= 100kHz：1000ns；f_{SCL}= 400kHz：300ns
- Fall Time of the SCL and SDA: f_{SCL}= 100kHz：300ns；f_{SCL}= 400kHz：300ns

Figure59. Timing on the SCL and SDA

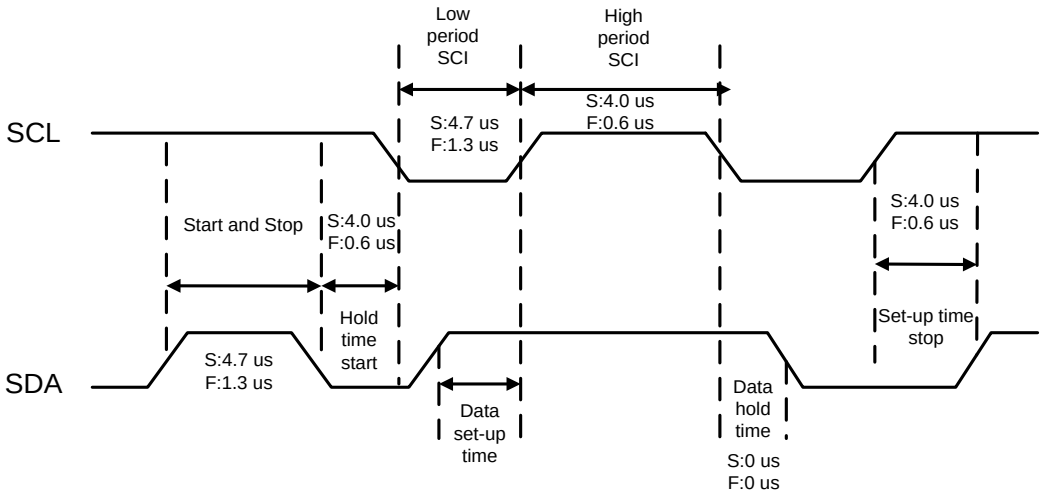


Table312. I2C AC Characteristics

Time	I2C – master mode (CR<7)		I2C – master mode (CR=7)	
$t_{HD:STA}$	scl/4	min(15 clk)	scl/4	(2 bclk)
t_{LOW}	scl/2	min(30 clk)	scl/2	(4 bclk)
t_{HIGH}	scl/2	min(30 clk)	scl/2	(4 bclk)
$t_{SU:STA}$	scl/4	min(15 clk)	scl/2 – if (scl/4<7 clk)	
			scl/4 – others	
$t_{HD:DAT}$	6*clk	(6 clk)	6*clk	(6 clk)
$t_{SU:DAT}$	1*clk (-for first bit)*	(1 clk)	1*clk (-for first bit)*	(1 clk)
	scl/2 - 6*clk	min(24 clk)	scl/2 - 6*clk	min(1clk)
$t_{SU:STO}$	scl/4 + 7*clk	min(22 clk)	min(bclk +9)	
t_{BUF}	(¾ scl)+9*clk	min(54 clk)	min (¾ scl)	

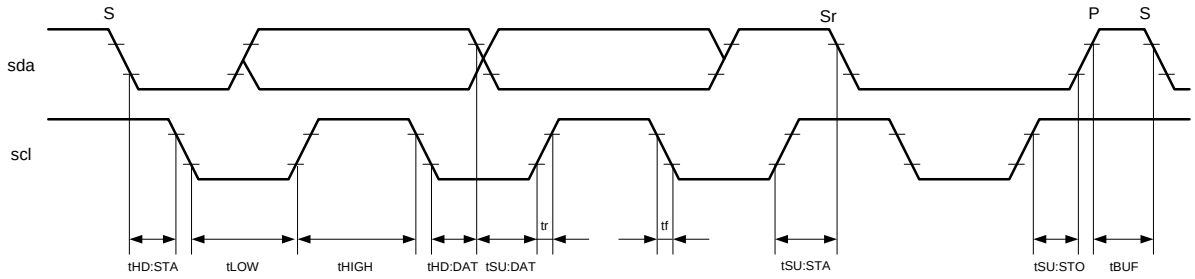
*- is a case when write to data register is close to the scl rising edge of the first bit data byte.

clk: APB clock period

bclk: Timer 3's overflow period

scl: I2C clock period

Figure60. AC Timing of I2C Controller



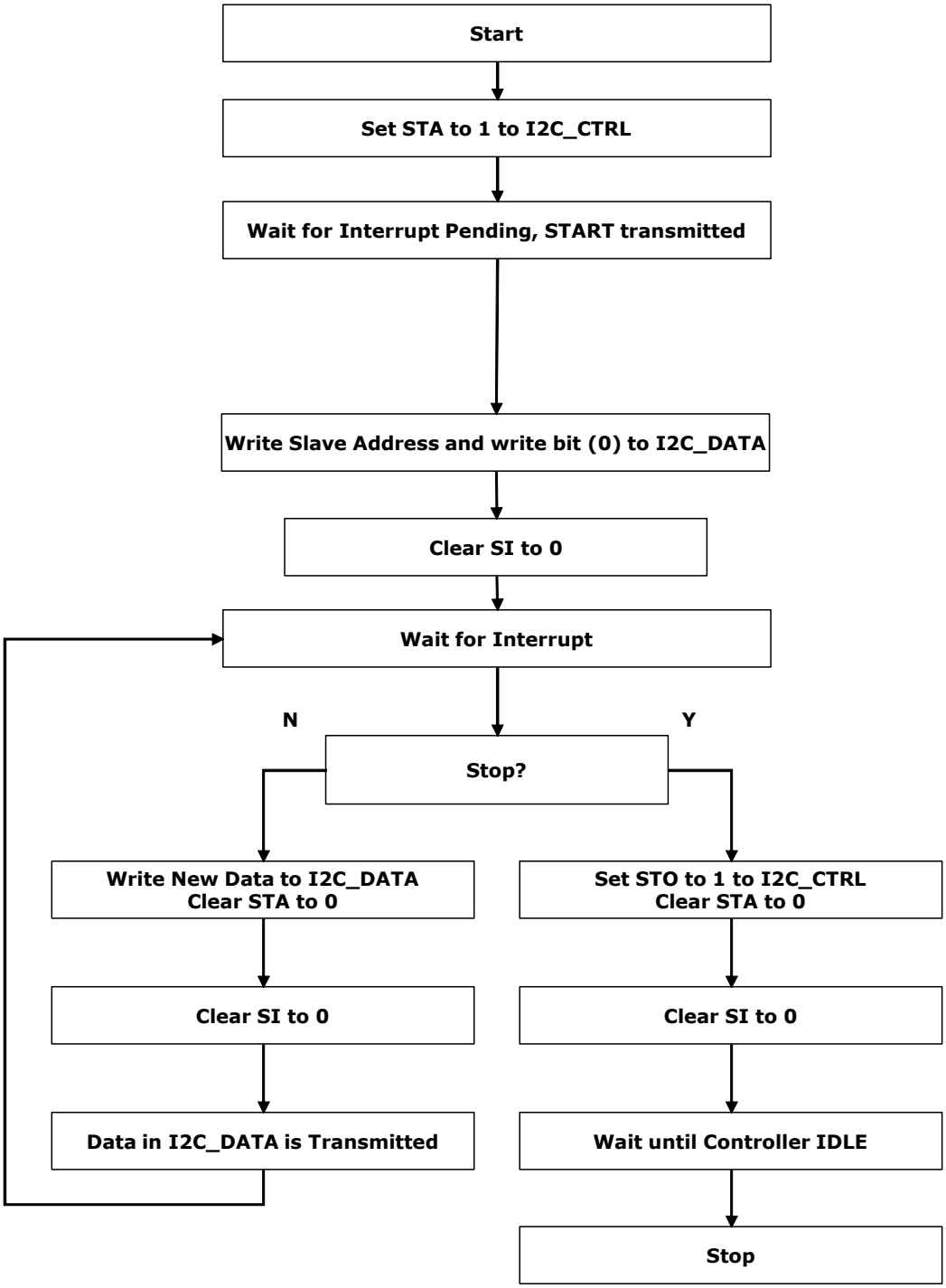
23.6.6 The Resolution for SDA Pin Lock-Status

In the process of I2C communication, when the chip is reset (software reset, WDT reset, external reset), it may cause the I2C data line (SDA is locked in low level) is stuck LOW, the master should send nine clock pulses. The device that held the bus LOW should release it within those nine clocks. If I2C is not stuck LOW in the current time, the nine clock pulses add by user will not affect I2C usage.

23.7 Firmware Flow

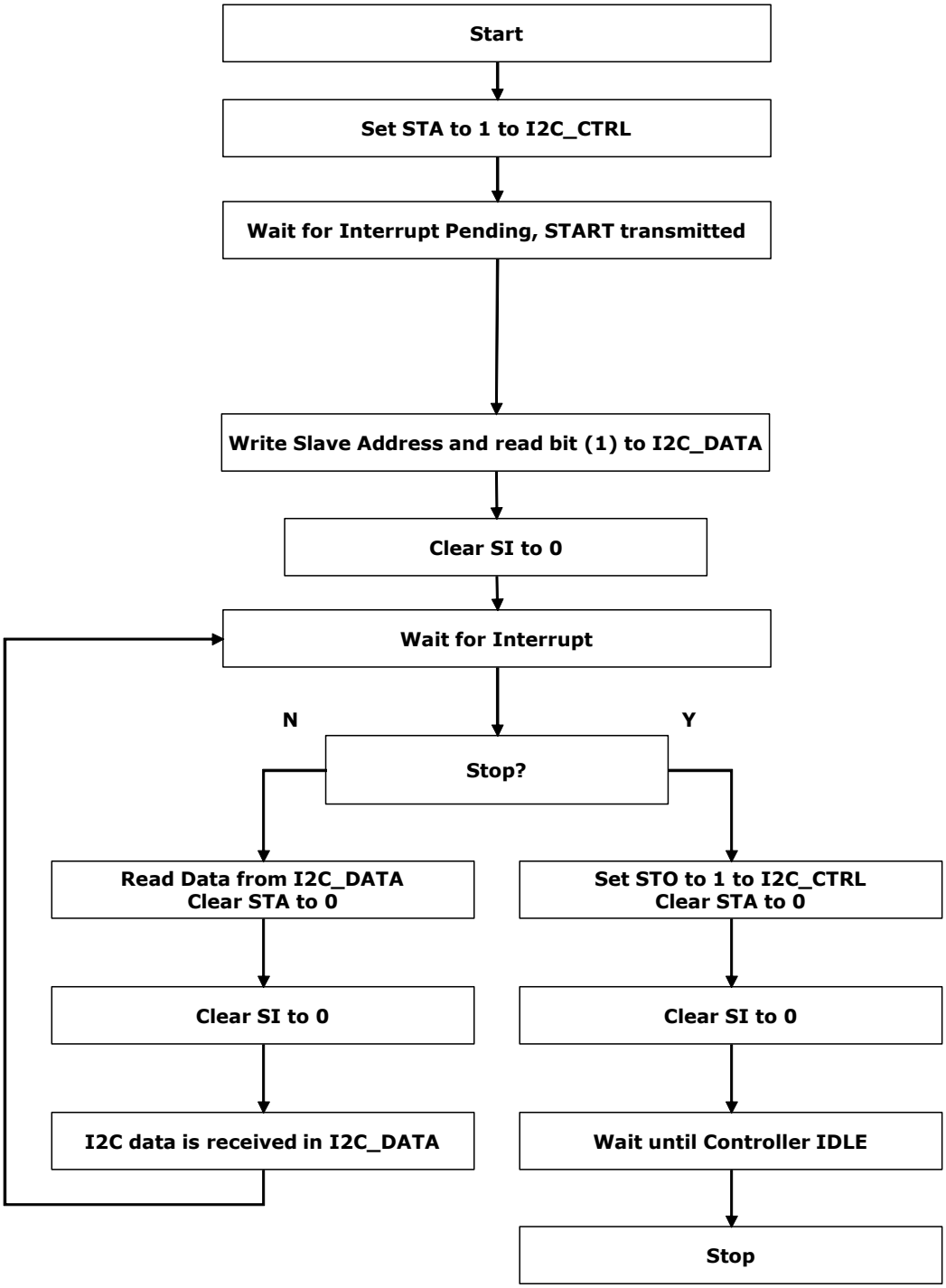
23.7.1 Master Transmit Mode

Figure61. Operations for Master Transmitter Mode



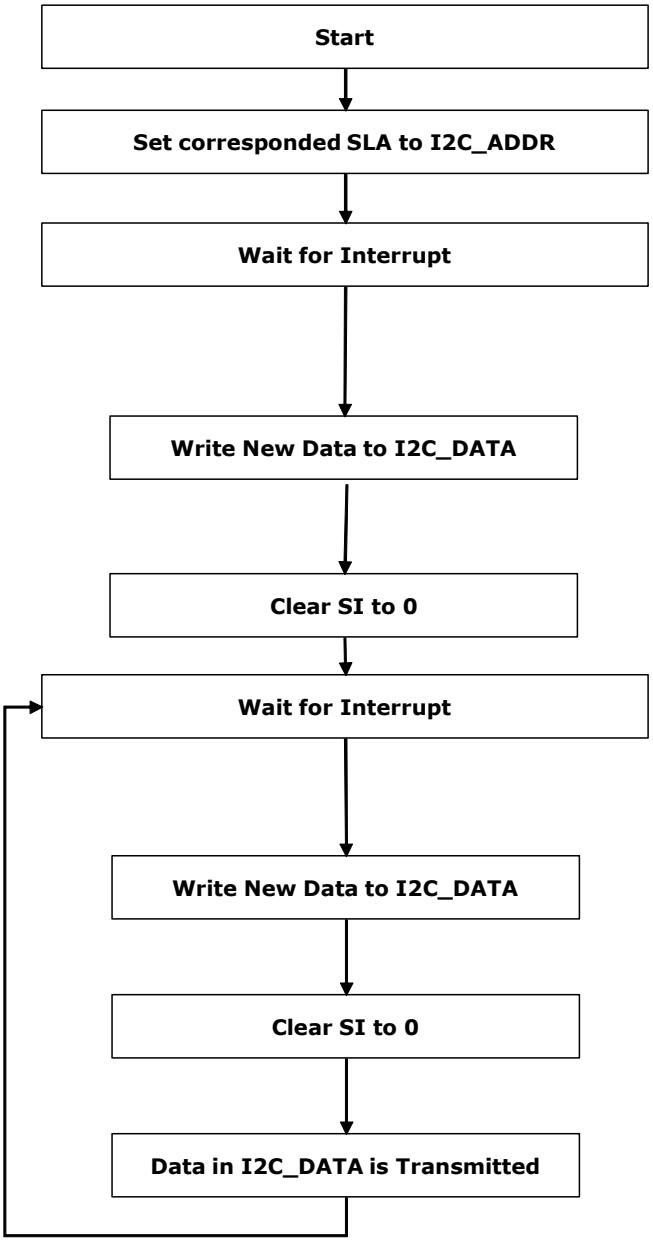
23.7.2 Master Receive Mode

Figure62. Operations for Master Receiver Mode



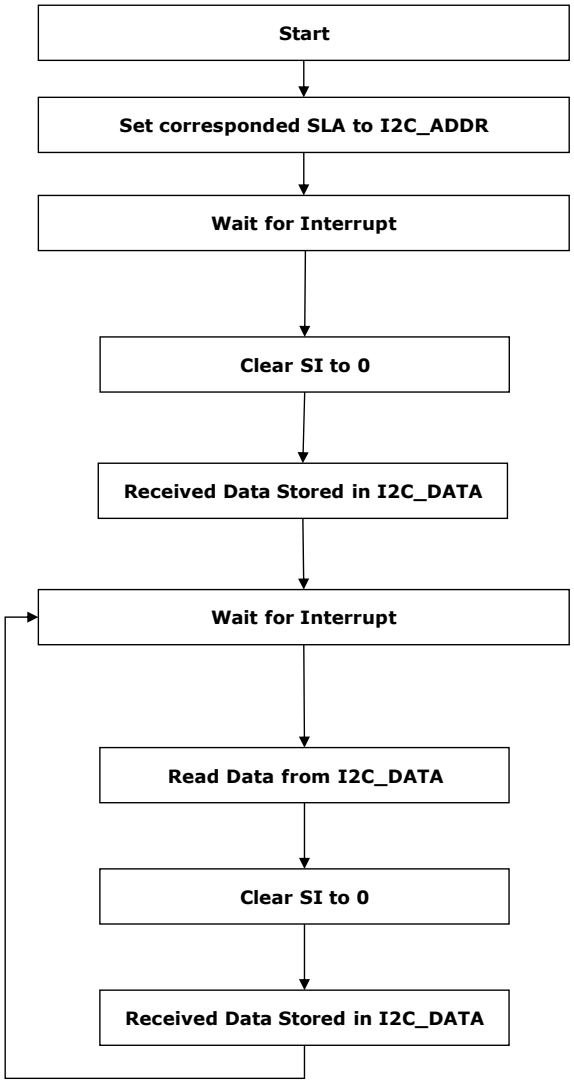
23.7.3 Slave Transmit Mode

Figure63. Operations for Slave Transmitter Mode



23.7.4 Slave Receive Mode

Figure64. Operations for Slave Receiver Mode



24 MISC Controller

24.1 Introduction

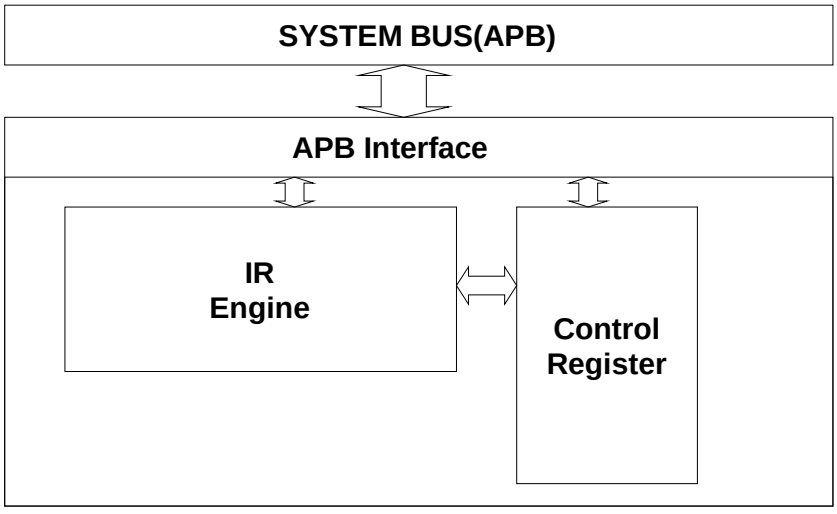
The MISC controller is used to control some special function of V85XX. There are two MISC controllers inside V85XX, one is in core domain (MISC controller) which will be power-off during sleep mode. The setting in MISC controller will be reset after wake-up from sleep mode, programmer should restore the setting manually after wake-up from sleep state. MISC2 will not be reset after being awakened from the sleep mode.

24.2 Feature

- Clock control of each sub-module
- Clock divider of AHBCLK and APBCLK.
- FLASH program tick control
- IR duty control.
- SRAM parity check interrupt control.

24.3 Block Diagram

Figure65. Functional Block Diagram of MISC Controller



24.4 MISC Register Location

Table313. MISC Registers Map

Register Name	Offset	Type	Reset Value	Description
MISC_SRAMINT	0x0000	rc_w1	0x0000_0000	SRAM Parity Error Interrupt.
MISC_SRAMINIT	0x0004	rw	0x0000_0001	SRAM initialize register
MISC_PARERR	0x0008	r	0x0000_0000	SRAM Parity Error address register
MISC_IREN	0x000C	rw	0x0000_0000	IR enable control register
MISC_DUTYL	0x0010	rw	0x0000_0000	IR Duty low pulse control register
MISC_DUTYH	0x0014	rw	0x0000_0000	IR Duty high pulse control register
MISC_IRQLAT	0x0018	rw	0x0000_0000	Cortex-M0 IRQ latency control register
MISC_HIADDR	0x0020	r	0x0000_0000	AHB invalid access address
MISC_PIADDR	0x0024	r	0x0000_0000	APB invalid access address

24.5 MISC Register Definition

24.5.1 MISC_SRAMINT Register

Table314. MISC_SRAMINT Register Description

Bit	Name	Type	Description
31:5	Rsvd	-	Reserved.
4	LOCKUP	rc_w1	This bit indicates the CM0 lockup has happened. Write 1 to clear this flag.
3	PIAC	rc_w1	This bit indicates that an invalid address access on APB bus is occurred. At the same time, the failure address is latched into MISC_PIADDR. The invalid APB address means not in the region of 0x40010000 ~ 0x40017FFF. If PIACIE is 1, then a NMI will be issued to CM0. Write 1 to clear this flag.
2	HIAC	rc_w1	This bit indicates that an invalid address access on AHB bus is occurred. At the same time, the failure address is latched into MISC_HIADDR. The invalid AHB address means not in the region of FLASH or SRAM or IO. If HIACIE is 1, then a NMI will be issued to CM0. Write 1 to clear this flag.
0	PERR	rc_w1	This bit indicates that a SRAM parity error is happened during the SRAM read process. If PERRIE is 1, then a NMI will be issued to CM0. Write 1 to clear this flag.

24.5.2 MISC_SRAMINIT Register

Table315. MISC_SRAMINIT Register Description

Bit	Name	Type	Description
31:8	Rsvd	-	Reserved.
7	LOCKIE	rw	CM0 lockup NMI enable register.
6	PIACIE	rw	APB invalid address access NMI enable register.
5	HIACIE	rw	AHB invalid address access NMI enable register.
4:2	Rsvd	-	Reserved.
1	PERRIE	rw	SRAM parity error NMI enable register.
0	Rsvd	-	Reserved.

24.5.3 MISC_PARERR Register

Table316. MISC_PARERR Register Description

Bit	Name	Type	Description
31:12	Rsvd	-	Reserved.
11:0	PEADDR	r	Parity error address. This register store the information of parity error address, when PE NMI is happened, programmer can check this register to know which SRAM address has defect bit. SRAM parity error address =0x20000000+4* PEADDR.

24.5.4 MISC_IREN Register

Table317. MISC_IREN Register Description

Bit	Name	Type	Description
31:6	Rsvd	-	Reserved.
5:0	IREN	rw	IR enable control register. Each bit in this register corresponded to 1 UART TX channel. When IREN[x] is set to 1, it means UART TX[x] will be modulated with IR pulse to output.

24.5.5 MISC_DUTYL Register

Table318. MISC_DUTYL Register Description

Bit	Name	Type	Description
31:16	Rsvd	-	Reserved.
15:0	DUTYL	rw	IR low pulse width control register. The low pulse width will be (DUTYL + 1)*APBCLK period.

24.5.6 MISC_DUTYH Register

Table319. MISC_DUTYH Register Description

Bit	Name	Type	Description
31:16	Rsvd	-	Reserved.
15:0	DUTYH	rw	IR high pulse width control register. The high pulse width will be (DUTYH + 1)*APBCLK period.

24.5.7 MISC_IRQLAT Register

Table320. MISC_IRQLAT Register Description

Bit	Name	Type	Description
31:10	Rsvd	-	Reserved.
9	NOHARDFAULT	rw	This register is used to disable the hard fault generation to CPU. 0: Enable hard fault generation when bus error is happened. 1: Disable hard fault generation when bus error is happened, the HIAL hard-fault is not able to be disabled by this bit. When CM0 detect hard fault is happened, it will jump to the hard fault service routine. After it complete the hard fault service, it will jump back to normal code and execute the same instruction again. So if the hard fault happens again, it will stop in this loop and never come out. This register is used for CPU to temporary disable the hard fault generation.
8	LOCKRESET	rw	This register is used to control if the lockup will issue a system reset. 0: Disable reset generation of CM0 lockup. 1: Enable reset generation of CM0 lockup.
7:0	IRQLAT	rw	This register is used to control the Cortex-M0 IRQ latency. The Cortex-M0 processor supports zero jitter interrupt latency for zero wait-state memory. IRQLAT specifies the minimum number of cycles between an interrupt that becomes pended in the NVIC, and the vector fetch for that interrupt being issued on the AHB-Lite interface. If this bus is set to 0, interrupts are taken as quickly as possible. For zero jitter in a zero wait state memory system, set this bus to at least a decimal value of 13. For non-zero wait state memory, zero jitter can be achieved with a higher value on IRQLAT.

24.5.8 MISC_HIADDR Register

Table321. MISC_HIADDR Register Description

Bit	Name	Type	Description
31:0	HIADDR	r	AHB bus error address. The register is stored the error address information for accessing AHB bus. When error happened, user can access the error address via the register located AHB bus. The error address = 0x40000000 + HIADDR

24.5.9 MISC_PIADDR Register

Table322. MISC_PIADDR Register Description

Bit	Name	Type	Description
31:0	PIADDR	r	APB bus error address. The register is stored the error address information for accessing APB bus. When error happened, user can access the error address via the register located APB bus. The error address= 0x40010000 + PIADDR

24.6 MISC2 Register Location

Table323. MISC2 Registers Map

Register Name	Offset	Type	Reset Value	Description
MISC2_FLASHWC	0x0000	rw	0x0000_2100	FLASH wait cycle register.
MISC2_CLKSEL	0x0004	rw	0x0000_0000	Clock selection register.
MISC2_CLKDIVH	0x0008	rw	0x0000_0000	AHB clock divider control register
MISC2_CLKDIVP	0x000C	rw	0x0000_0001	APB clock divider control register
MISC2_HCLKEN	0x0010	rw	0x0000_01FF	AHB clock enable control register
MISC2_PCLKEN	0x0014	rw	0xF83F_FFFF	APB clock enable control register
MISC2_EPUCLKCTRL	0x0020	rw	0x0000_0000	EPU clock control register
MISC2_RSTEPU	0x0024	rw	0x0000_0000	Reset EPU register

24.7 MISC2 Register Definition

24.7.1 MISC2_FLASHWC Register

Table324. MISC2_FLASHWC Register Description

Bit	Name	Type	Description
31:14	Rsvd	-	Reserved.

13:8	1USCYCLE	rw	This register is used for FLASH controller to calculate 1ustick from AHB clock 1ustick = (AHB clock period)*(1USCYCLE+1) This setting is related to the wake-up time of FLASH, and the programming time of FLASH. FLASH wake-up time =1ustick *10. It must meet 1ustick >=1 μs. For example, the clock frequency of AHB is 26.2144MHz. In order to ensure the minimum wake-up time, 1USCYCLE should be set to 26. So, the wake-up time of FLASH is 27 / 26214400 * 10, which is about 10 μs. For example, the clock frequency of AHB is 32.768KHz. In order to ensure the minimum wake-up time, 1USCYCLE should be set to 0. So, the wake-up time of FLASH is 1 / 32768 * 10, which is about 305 μs.
7:0	Rsvd	-	Reserved.

24.7.2 MISC2_CLKSEL Register

Table325. MISC2_CLKSEL Register Description

Bit	Name	Type	Description
31:3	Rsvd	-	Reserved.
2:0	CLKSEL	rw	This register is used to control AHB clock source. 0: RCH (6.5MHz RC) 1: XOH (6.5536MHz XTAH). 2: PLLH. 3: RTCCLK (controlled by RTCCLK_SEL in PMU_CONTROL register). 4: PLLL. Before clock select to one of the clock source, programmer should enable the corresponded module first by setting PMU_CONTROL register.

24.7.3 MISC2_CLKDIVH Register

Table326. MISC2_CLKDIVH Register Description

Bit	Name	Type	Description
31:8	Rsvd	-	Reserved.
7:0	CLKDIVH	rw	This register is used to control AHB clock divider. 0: Clock source divide by 1 1: Clock source divide by 2. 2: Clock source divide by 3. …. 255: Clock source divide by 256.

24.7.4 MISC2_CLKDIVP Register

Table327. MISC2_CLKDIVP Register Description

Bit	Name	Type	Description
31:8	Rsvd	-	Reserved.
7:0	CLKDIVP	rw	This register is used to control APB clock divider. 0: AHB clock divide by 1. 1: AHB clock divide by 2. 2: AHB clock divide by 3. …. 255: AHB clock divide by 256.

24.7.5 MISC2_HCLKEN Register

Table328. MISC2_HCLKEN Register Description

Bit	Name	Type	Description
31:9	Rsvd	-	Reserved.
8:0	HCLKEN	rw	This register is used to control clock enable of each AHB module. The corresponded module can be turned-off only when its function is not been used. Refer to Table329 for detail about each module. 0: Disable. 1: Enable.

Table329. HCLK Clock Enable of Each Module

Bit	Module	Note
0	--	
1	Arbiter & Bus Matrix	Shouldn’t off when CPU or DMA is active.
2	FLASH Controller	Shouldn’t off
3	SRAM Controller	Shouldn’t off
4	DMA Controller	
5	GPIO Controller	
6	LCD Controller	
7	--	
8	CRYPT Controller	

24.7.6 MISC2_PCLKEN Register

Table330. MISC2_PCLKEN Register Description

Bit	Name	Type	Description

31:0	PCLKEN	rw	This register is used to control clock enable of each APB module. The corresponded module can be turned-off only when its function is not been used. Refer to Table331 for detail about each module. 0: Disable. 1: Enable.

Table331. PCLK clock Enable of Each Module

Bit	Module	Note
0	AHB2APB Bridge	Shouldn't off when CPU or DMA is access APB peripheral.
1	DMA Controller	
2	I2C	
3	SPI1	
4	UART0	
5	UART1	
6	UART2	
7	UART3	
8	UART4	
9	UART5	
10	ISO78160	
11	ISO78161	
12	Timer	
13	MISC	
14	MISC2	
15	PMU	
16	RTC	
17	ANA	
18	U32K 0	
19	U32K 1	
20	Reserved	
21	SPI2	
22	EPU	
23	RNG	
24	SPI4	
25	Reserved	
26	SPI3	
31:27	Reserved	

24.7.7 MISC2_EPUCLKCTRL Register

Table332. MISC2_EPUCLKCTRL Register Description

Bit	Name	Type	Description
31:5	Rsvd	-	Reserved.
4	EPUCLKEN	rw	EPU function clock enable. 1: enable 0: disable
1:0	CLKDIVEPU	rw	EPU clock divider. (EPU clock source is same to HCLK clock source) 0: Clock source divide by 1. 1: Clock source divide by 2. 2: Clock source divide by 3. 3: Clock source divide by 4. Note: EPU work at 6.5536MHz clock.

24.7.8 MISC2_RSTEPU Register

Table333. MISC2_RSTEPU Register Description

Bit	Name	Type	Description
31:23	Rsvd	-	Reserved.
22	EPURST	rw	EPU reset control This bit is set and cleared by software. 1: reset EPU 0: does not reset EPU
21:0	Rsvd	-	Reserved.

25 CRYPT Controller

25.1 Introduction

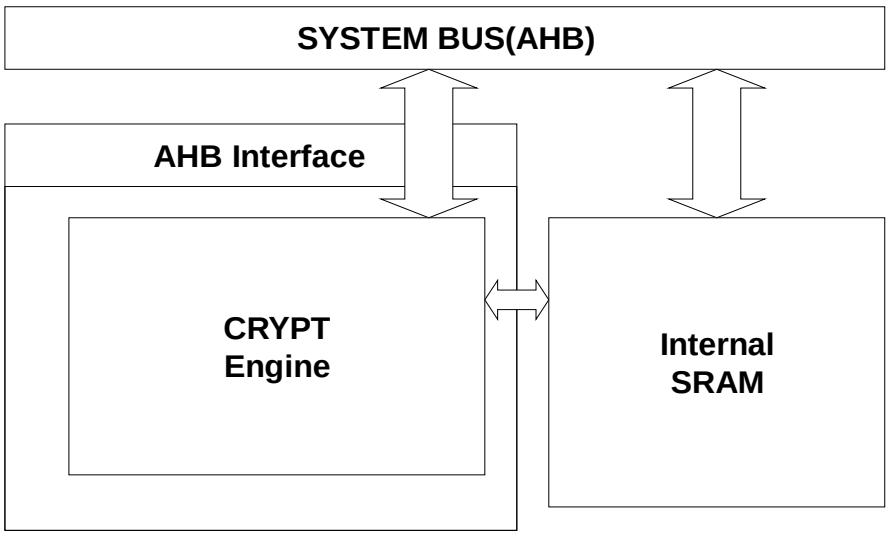
The CRYPT controller is used to accelerate the ECC's sign and verify process speed. The major feature of CRYPT controller is the VLI (variable length integer) multiply, add, sub, multiply modular, add modular, sub modular and shift. It can achieve overall about 12 times faster than pure software process. Every encryption algorithm use VLI can use this hardware to accelerate the process speed. The CRYPT controller can access internal SRAM directly without affect the M0's access, it can also generate the carry or borrow bit automatically.

25.2 Feature

- Support VLI from 32 bits to 512 bits.
- VLI multiplier.
- VLI add and carry bit generation.
- VLI substrate and borrow bit generation.
- VLI right shift 1 bit.
- Internal SRAM direct access.
- Support modular calculation of multiplier, add and substrate.
- Support 32bytes data move.

25.3 Block Diagram

Figure66. Functional Block Diagram of CRYPT Controller



25.4 Register Location

Table334. CRYPT Registers Map

Register Name	Offset	Type	Reset Value	Description
CRYPT_CTRL	0x0000	rw	0x0000_0000	CRYPT control register
CRYPT_PTRA	0x0004	rw	0x0000_0000	CRYPT pointer A
CRYPT_PTRB	0x0008	rw	0x0000_0000	CRYPT pointer B
CRYPT_PTRO	0x000C	rw	0x0000_0000	CRYPT pointer O
CRYPT_CARRY	0x0010	r	0x0000_0000	CRYPT carry/borrow bit register
CRYPT_PRIME0	0x0020	rw	0xFFFF_FFFF	The Prime number for modular calculation
CRYPT_PRIME1	0x0024	rw	0xFFFF_FFFF	The Prime number for modular calculation
CRYPT_PRIME2	0x0028	rw	0xFFFF_FFFF	The Prime number for modular calculation
CRYPT_PRIME3	0x002C	rw	0x0000_0000	The Prime number for modular calculation
CRYPT_PRIME4	0x0030	rw	0x0000_0000	The Prime number for modular calculation
CRYPT_PRIME5	0x0034	rw	0x0000_0000	The Prime number for modular calculation
CRYPT_PRIME6	0x0038	rw	0x0000_0001	The Prime number for modular calculation
CRYPT_PRIME7	0x003C	rw	0xFFFF_FFFF	The Prime number for modular calculation

25.5 Register Definition

25.5.1 CRYPT_CTRL Register

Table335. CRYPT_CTRL Register Description

Bit	Name	Type	Description
31:16	Rsvd	-	Reserved.
15	NOSTOP	rw	This register is used to control if the CPU will be stop by CRYPT engine when the CRYPT engine is busy and CPU read or write CRYPT engine register. 0: Stop CPU when CRYPT engine is busy. 1: No stop CPU when CRYPT engine is busy. This register only effect the behavior when CPU access the CRYPT register, if CPU didn't access the crypt register, this bit has no effect.

14:12	Rsvd	-	Reserved.
11:8	LENGTH	rw	This bit is used to control the VLI length of current operation. Programmer can set this register together with write 1 to ACT bit, but should not change this register when ACT is 1. 0: 32 bits VLI 1: 64 bits VLI 2: 96 bits VLI …… 15: 512 bits VLI
6:4	MODE	rw	This register controls the operation mode of crypt engine. Programmer can set this register together with write 1 to ACT bit, but should not change this register when ACT is 1. 0: Multiply mode, *PTRO = *PTRA x *PTRB 1: Add mode, *PTRO = *PTRA + *PTRB 2: Sub mode, *PTRO = *PTRA - *PTRB 3: RSHIFT1 mode, *PTRO = (*PTRA>>1) 4: Multiply modular mode, *PTRO = (*PTRA x *PTRB) mod Prime 5: Add modular mode, *PTRO = (*PTRA + *PTRB) mod Prime 6: Sub modular mode, *PTRO = (*PTRA - *PTRB) mod Prime 7: Data move. *PTRO=*PTRA
3:1	Rsvd	-	Reserved.
0	ACT	rw	Write 1 to this bit will start an operation specified in the MODE register. And this bit will be cleared automatically after the operation is done. Write 0 to this bit has no effect. Note: Before writing 1 to this bit, turn off all interrupts. After this bit is cleared to 0, the software needs to restore interrupts.

25.5.2 CRYPT_PTRA Register

Table336. CRYPT_PTRA Register Description

Bit	Name	Type	Description
31:15	Rsvd	-	Reserved.
14:0	PTRA	rw	This is the PTRA register of CRYPT controller. The value here defines an address in the SRAM (byte unit). The data in this address will be read out to do the CRYPT calculation. Since the CRYPT control only support 32 bits

			process, the PTRA[1:0] should be 0 for all the time.

25.5.3 CRYPT_PTRB Register

Table337. CRYPT_PTRB Register Description

Bit	Name	Type	Description
31:15	Rsvd	-	Reserved.
14:0	PTRB	rw	This is the PTRB register of CRYPT controller. The value here defines an address in the SRAM (byte unit). The data in this address will be read out to do the CRYPT calculation. Since the CRYPT control only support 32 bits process, the PTRB[1:0] should be 0 for all the time.

25.5.4 CRYPT_PTRO Register

Table338. CRYPT_PTRO Register Description

Bit	Name	Type	Description
31:15	Rsvd	-	Reserved.
14:0	PTRO	rw	This is the PTRO register of CRYPT controller. The value here defines an address in the SRAM (byte unit). The CRYPT engine will write calculation result into this address. Since the CRYPT control only support 32 bits process, the PTRO[1:0] should be 0 for all the time.

25.5.5 CRYPT_CARRY Register

Table339. CRYPT_CARRY Register Description

Bit	Name	Type	Description
31:1	Rsvd	-	Reserved.
0	CARRY	r	This bit represent the carry bit after add operation is done. The bit represent borrow bit after sub operation is done. Programmer can read this register immediately after the ACT bit is clear to 0.

25.5.6 CRYPT_PRIME0 Register

Table340. CRYPT_PRIME0 Register Description

Bit	Name	Type	Description
31:0	NUM	rw	The prime 0 for modular calculation.

Example:

P = 0xFFFFFFFF00000001000000000000000000000000FFFFFFFFFFFFFFFFFFFFFFFF

Table341. The prime register configuration

Name	Offset	Description
PRIME0	0x20	0xFFFFFFFF
PRIME1	0x24	0xFFFFFFFF
PRIME2	0x28	0xFFFFFFFF
PRIME3	0x2c	0x00000000
PRIME4	0x30	0x00000000
PRIME5	0x34	0x00000000
PRIME6	0x38	0x00000001
PRIME7	0x3c	0xFFFFFFFF

25.5.7 CRYPT_PRIME1 Register

Table342. CRYPT_PRIME1 Register Description

Bit	Name	Type	Description
31:0	NUM	rw	The prime 1 for modular calculation.

25.5.8 CRYPT_PRIME2 Register

Table343. CRYPT_PRIME2 Register Description

Bit	Name	Type	Description
31:0	NUM	rw	The prime 2 for modular calculation.

25.5.9 CRYPT_PRIME3 Register

Table344. CRYPT_PRIME3 Register Description

Bit	Name	Type	Description
31:0	NUM	rw	The prime 3 for modular calculation.

25.5.10 CRYPT_PRIME4 Register

Table345. CRYPT_PRIME4 Register Description

Bit	Name	Type	Description
31:0	NUM	rw	The prime 4 for modular calculation.

25.5.11 CRYPT_PRIME5 Register

Table346. CRYPT_PRIME5 Register Description

Bit	Name	Type	Description
31:0	NUM	rw	The prime 5 for modular calculation.

25.5.12 CRYPT_PRIME6 Register

Table347. CRYPT_PRIME6 Register Description

Bit	Name	Type	Description
31:0	NUM	rw	The prime 6 for modular calculation.

25.5.13 CRYPT_PRIME7 Register

Table348. CRYPT_PRIME7 Register Description

Bit	Name	Type	Description
31:0	NUM	rw	The prime 7 for modular calculation.

25.6 Application Note

25.6.1 Data Format

The VLI is a positive integer with 32~512 bits. So all the operations here are unsigned processes.

Table349. the data sequence in the SRAM.

Address	Data
PTR + 0	VLI[31:0]
PTR + 4	VLI[63:32]
PTR + 8	VLI[95:64]
PTR + 12	VLI[127:96]
……	……
PTR + 60	VLI[511:480]

When different kind of LENGTH mode is selected, only the selected range of VLI will be used as input data.

Table350. The valid VLI bits under different LENGTH setting

LENGTH	Data
0	VLI[31:0]
1	VLI[63:0]
2	VLI[95:0]

3	VLI[127:0]
……	……
15	VLI[511:0]

25.6.2 Operation Detail

For each operation, they will have different behavior on many ways, like the process cycles and the output width.

Table351. Detail of each mode.

	MULT	ADD	SUB	RSHIFT1
Operation	*PTRO = *PTRA x *PTRB	*PTRO = *PTRA + *PTRB	*PTRO = *PTRA - *PTRB	*PTRO = (*PTRA>>1)
Output length	2*input length	input length	input length	input length
CARRY bit	X	0: Output not overflow. 1: Output overflow	0: *PTRA > *PTRB 1: *PTRA < *PTRB	X
LENGTH	Operation Cycles			
0	8	6	6	6
1	17	8	8	8
2	32	12	12	10
3	53	14	14	12
4	80	18	18	14
5	113	20	20	16
6	152	24	24	18
7	197	26	26	20
8	248	30	30	22
9	305	32	32	24
10	368	36	36	26
11	437	38	38	28
12	512	42	42	30
13	593	44	44	32
14	680	48	48	34
15	773	50	50	36

By default, during the operation cycle, if the CPU accesses any of the register of CRYPT engine, the CPU will be halted until the operation is done. This is to prevent the configuration change during the operation. So if there is any high priority task in the system, it may block until the CPU is released by CRYPT engine. Set NOSTOP bit in the CRYPT_CTRL register to prevent this kind of situation. Under this condition, programmer should take care not to change the CRYPT configuration during the operation busy time.

Since the CRYPT only supports operations in the SRAM, when one of the input is not in the

SRAM (ex. In FLASH or ROM), it is necessary to copy it into SRAM before do any operation.

26 RNG Controller

26.1 Introduction

The RNG enables generation and collection of truly random bit stream from digital logics. The typical usage of RNG is key generation with seeding approved deterministic random numbers.

26.2 Features

- Includes an internal entropy source that is based on a chain of digital inverters.
- Built-in hardware tests for auto correlation and continuous random number generation testing.

26.3 Register Location

Table352. RNG Registers Map

Register Name	Offset	Type	Reset Value	Description
RNG_IMR	0x0100	rw	0x0000_0000	RNG interrupt mask register
RNG_ISR	0x0104	rw	0x0000_0000	RNG interrupt status register
RNG_ICR	0x0108	rw	0x0000_0000	RNG interrupt clear register
RNG_CFG	0x010C	rw	0x0000_0000	RNG configure register
RNG_DATA0	0x0114	rw	0x0000_0000	RNG data register 0
RNG_DATA1	0x0118	rw	0x0000_0000	RNG data register 1
RNG_DATA2	0x011C	rw	0x0000_0000	RNG data register 2
RNG_DATA3	0x0120	rw	0x0000_0000	RNG data register 3
RNG_DATA4	0x0124	rw	0x0000_0000	RNG data register 4
RNG_DATA5	0x0128	rw	0x0000_0000	RNG data register 5
RNG_CMD	0x012C	rw	0x0000_0000	RNG source enable register
RNG_CNT	0x0130	rw	0x0000_0000	RNG sample counter register
RNG_BYPASS	0x0138	rw	0x0000_0000	RNG testing bypass register

26.4 Register Definition

26.4.1 RNG_IMR Register

Table353. RNG_IMR Register Description

Bit	Name	Type	Description
31:4	Rsvd	-	Reserved.
3	VN_ERR_MASK	rw	This bit masks the VN_ERR interrupt signal from

			RNG_ISR register. 0: VN_ERR interrupt is unmasked. 1: VN_ERR interrupt is masked.
2	CRNGT_ERR_MASK	rw	This bit masks the CRNGT_ERR interrupt signal from RNG_ISR register. 0: CRNGT_ERR interrupt is unmasked. 1: CRNGT_ERR interrupt is masked.
1	AUTOCORR_ERR_MASK	rw	This bit masks the AUTOCORR_ERR interrupt signal from RNG_ISR register. 0: AUTOCORR_ERR interrupt is unmasked. 1: AUTOCORR_ERR interrupt is masked.
0	DATA_VALID_MASK	rw	This bit masks the DATA_VALID interrupt signal from RNG_ISR register. 0: DATA_VALID interrupt is unmasked. 1: DATA_VALID interrupt is masked.

26.4.2 RNG_ISR Register

Table354. RNG_ISR Register Description

Bit	Name	Type	Description
31:4	Rsvd	-	Reserved.
3	VN_ERR	r	A Von Neumann error occurs if 32 consecutive collected bits are identical, that is, 32 zeros or 32 ones. 1: A Von Neumann error occurs. 0: No Von Neumann error occurs.
2	CRNGT_ERR	r	When set to 1, it indicates a Continuous Random Number Generation Testing (CRNGT) error in the RNG test failed. Failure occurs when two consecutive blocks of 16 collected bits are equal. 1: A Continuous Random Number Generation Testing error occurs. 0: No Continuous Random Number Generation Testing error occurs.
1	AUTOCORR_ERR	r	When set to 1, it indicates that the Autocorrelation test failed four times in a row. When set, the RNG stops functioning until the next reset. 1: A Autocorrelation error occurs. 0: No Autocorrelation error occurs.
0	DATA_VALID	r	Set to 1 when 192 bits have been collected in the RNG, and the DATA0~5 registers are ready to be read. 1: Data in DATA0~5 registers are ready. 0: Data in DATA0~5 registers are not ready.

26.4.3 RNG_ICR Register

Table355. RNG_ICR Register Description

Bit	Name	Type	Description
31:4	Rsvd	-	Reserved.
3	VN_ERR	w	Write 1 to clear a Von Neumann error.
2	CRNGT_ERR	w	Write 1 to clear a Continuous Random Number Generation Testing (CRNGT) error.
1	Rsvd	-	Reserved.
0	DATA_VALID	w	Write 1 after DATA0~5 registers have been read to clear DATA_VALID status.

26.4.4 RNG_CFG Register

Table356. RNG_CFG Register Description

Bit	Name	Type	Description
31:2	Rsvd	-	Reserved.
1:0	CHAIN_SEL	rw	Selects the length of inverters in the ring oscillator. 0b00: Selects the shortest inverter chain length. 0b01: Selects the short inverter chain length. 0b10: Selects the long inverter chain length. 0b11: Selects the longest inverter chain length.

26.4.5 RNG_DATA0 Register

Table357. RNG_DATA0 Register Description

Bit	Name	Type	Description
31:0	DATA	r	Returns bits[31:0] of entropy holding register.

26.4.6 RNG_DATA1 Register

Table358. RNG_DATA1 Register Description

Bit	Name	Type	Description
31:0	DATA	r	Returns bits[63:32] of entropy holding register.

26.4.7 RNG_DATA2 Register

Table359. RNG_DATA2 Register Description

Bit	Name	Type	Description
31:0	DATA	r	Returns bits[95:64] of entropy holding register.

26.4.8 RNG_DATA3 Register

Table360. RNG_DATA3 Register Description

Bit	Name	Type	Description
31:0	DATA	r	Returns bits[127:96] of entropy holding register.

26.4.9 RNG_DATA4 Register

Table361. RNG_DATA4 Register Description

Bit	Name	Type	Description
31:0	DATA	r	Returns bits[159:128] of entropy holding register.

26.4.10 RNG_DATA5 Register

Table362. RNG_DATA5 Register Description

Bit	Name	Type	Description
31:0	DATA	r	Returns bits[191:160] of entropy holding register.

26.4.11 RNG_CMD Register

Table363. RNG_CMD Register Description

Bit	Name	Type	Description
31:1	Rsvd	-	Reserved.
0	EN	rw	1: The entropy source is enabled. 0: The entropy source is disabled.

26.4.12 RNG_CNT Register

Table364. RNG_CNT Register Description

Bit	Name	Type	Description
31:0	CNT	rw	Sets the number of clock cycles between two consecutive ring oscillator samples.

26.4.13 RNG_BYPASS Register

Table365. RNG_BYPASS Register Description

Bit	Name	Type	Description
31:4	Rsvd	-	Reserved.
3	AUTOCORR_BYPASS	rw	When set to 1, the autocorrelation test in the RNG module is bypassed.

2	CRNGT_BYPASS	rw	When set to 1, the CRNGT test in the RNG module is bypassed.
1	VN_BYPASS	rw	When set to 1, the Von Neumann balancer in the RNG module is bypassed (including the 32 consecutive bits test).
0	Rsvd	-	Reserved.

26.5 Internal Random Source

The RNG module includes an internal ring oscillator circuit, implemented as an inverter chain with 4 length options, serving as the entropy source and responsible for generating a single random bit. The four inverter chain options must be implemented, because each single ring oscillator tends to have large variance between chip lots and environmental conditions (temperature, voltage, system clock oscillator, and device age). At runtime, the RNG module can select each of the chain length optionally and identify which inverter chain produces the best results.

27 EPU Controller

27.1 Introduction

There are total 8 energy accumulators, including two high-speed energy accumulators and six low-speed energy accumulators. The low-speed energy accumulators accumulate data every 50 Hz and work at 6.5536 MHz. The high-speed energy accumulators accumulate data every 204.8 KHz or 32.768 KHz, and work at 6.5536 MHz or 32.768 KHz. The high-speed energy accumulators' data comes from constant, low-speed energy accumulators' data comes from constant.

27.2 Feature

Energy accumulators feature:

- Configurable threshold.
- Support anti-creep.
- The High-speed energy accumulator work in sleep mode.
- High-speed energy accumulator supports CF output.
- Counter can be cleared.

27.3 Block Diagram

Figure67. Functional Block Diagram of EPU Controller

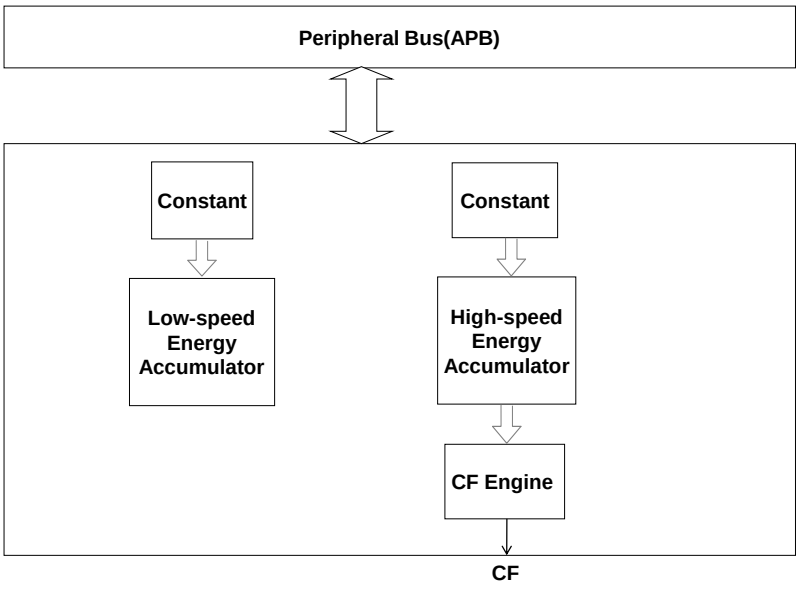


Figure68. Functional Block Diagram of high-speed energy accumulator

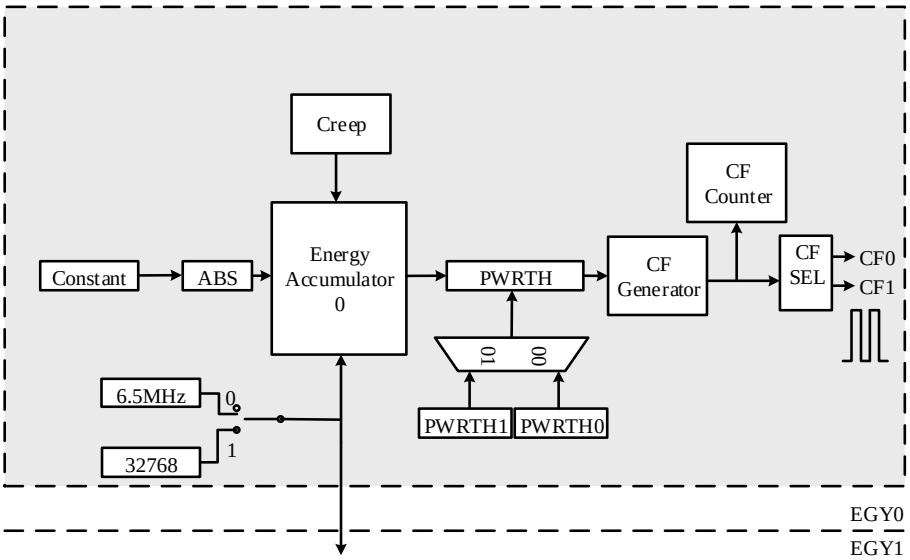
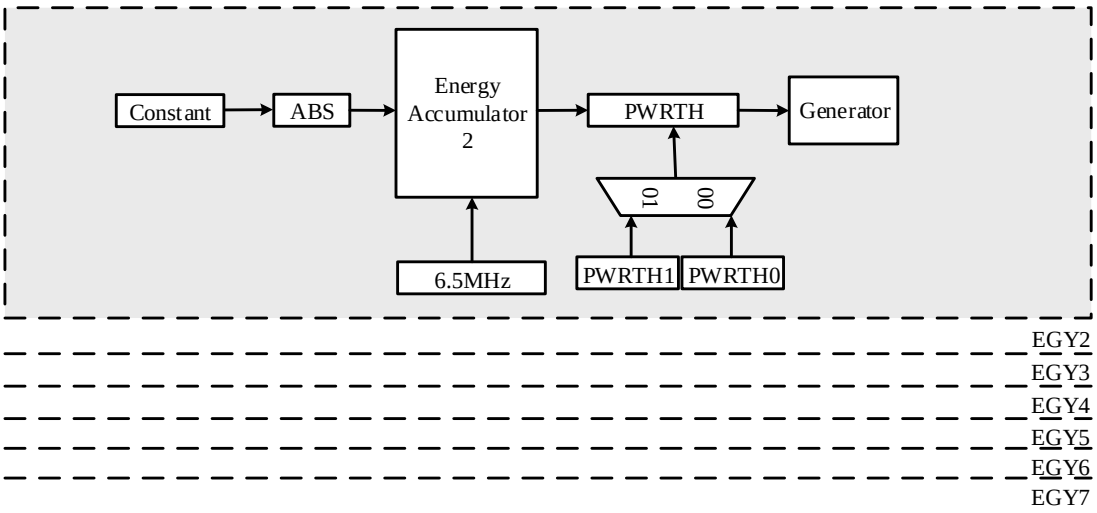


Figure69. Functional Block Diagram of low-speed energy accumulator



27.4 EPU Register Location

Table366. EPU Registers Map

Register Name	Offset	Type	Reset Value	Description
EPU_CFCTRL	0x0008	rw	0x0000_0000	CF output control register
EPU_HSCTRL	0x000C	rw	0x0000_0606	High-speed energy accumulators control register
EPU_LSCTRL	0x0010	rw	0x0000_6666	Low-speed energy accumulators control register
EPU_CLR	0x0014	rw	0x0000_0000	Energy accumulators clear register
EPU_CRPTH	0x0018	rw	0x0000_0000	Anti-creep threshold for energy

				accumulator register
EPU_PWRTH0	0x001C	rw	0x0000_0000	Accumulation threshold for energy accumulator register 0
EPU_PWRTH1	0x0020	rw	0x0000_0000	Accumulation threshold for energy accumulator register 1
EPU_INTEN	0x0024	rw	0x0000_0000	EPU interrupt enable register
EPU_INTSTS	0x0028	rc_w1	0x0000_0000	EPU interrupt status register
EPU_STS	0x002C	r	0x0000_0000	EPU status register
EPU_CONST0	0x0034	rw	0x0000_0000	Energy accumulator 0 accumulating constant register
EPU_OUTL0	0x0038	r	0x0000_0000	Energy accumulator 0 accumulating low bit register
EPU_OUTH0	0x003C	r	0x0000_0000	Energy accumulator 0 accumulating high bit register
EPU_CFCNT0	0x0040	r	0x0000_0000	Energy accumulator 0 pulse counter register
EPU_CONST1	0x0048	rw	0x0000_0000	Energy accumulator 1 accumulating constant register
EPU_OUTL1	0x004C	r	0x0000_0000	Energy accumulator 1 accumulating low bit register
EPU_OUTH1	0x0050	r	0x0000_0000	Energy accumulator 1 accumulating high bit register
EPU_CFCNT1	0x0054	r	0x0000_0000	Energy accumulator 1 pulse counter register
EPU_CONSTx[2..7,0xC]	0x0070	rw	0x0000_0000	Energy accumulator x accumulating constant register
EPU_OUTx[2..7,0xC]	0x0074	r	0x0000_0000	Energy accumulator x accumulating register
EPU_CFCNTx[2..7,0xC]	0x0078	r	0x0000_0000	Energy accumulator x pulse counter register

27.5 Register Definition

27.5.1 EPU_CFCTRL Register

Table367. EPU_CFCTRL Register Description

Bit	Name	Type	Description
31:11	Rsvd	-	Reserved.
10	CF1INV	rw	CF1 polarity selection 0: Original polarity. 1: Reverse polarity.
9	CF1EN	rw	CF1 enable

			0: Disable. 1: Enable.
8	CF1SEL	rw	CF1 data source selection. 0: High-speed energy accumulator 0. 1: High-speed energy accumulator 1.
7	Rsvd	-	Reserved.
6	CF0INV	rw	CF0 polarity selection 0: Original polarity. 1: Reverse polarity.
5	CF0EN	rw	CF0 enable 0: Disable. 1: Enable.
4	CF0SEL	rw	CF0 data source selection. 0: High-speed energy accumulator 0. 1: High-speed energy accumulator 1.
3:2	CFPLUSE	rw	CF pulse width selection. 0: 80 ms 1: 40 ms 2: 20 ms 3: 10 ms
1:0	CFFASTEN	rw	CF pulse speed up output. 0: Normal mode 1: 4x faster 2: 8x faster 3: 16x faster

27.5.2 EPU_HSCTRL Register

Table368. EPU_HSCTRL Register Description

Bit	Name	Type	Description
31:18	Rsvd	-	Reserved.
17	CRPEN	rw	High-speed energy accumulators creep enable. 0: Creep disable. 1: Creep enable.
16	CLKSEL	rw	High-speed energy accumulators clock source selection. 0: 6.5MHz 1: 32768Hz Switch clock flow is: Disable EGYEN->Waiting for CF output to complete ->Switch clock->Enable EGYEN
12	EGY1DATASEL	rw	EGY1 data source enable. 0: Disable. 1: Enable.
11	EGY1PWRTHSEL	rw	EGY1 threshold value selection.

			0: EGY_PWRTH0. 1: EGY_PWRTH1.
10:9	Rsvd	-	Reserved, must be set to 0x03.
8	EGY1EN	rw	EGY1 enable. 0: Disable EGY1. 1: Enable EGY1.
7:5	Rsvd	-	Reserved.
4	EGY0DATASEL	rw	EGY0 data source enable. 0: Disable. 1: Enable.
3	EGY0PWRTHSEL	rw	EGY0 threshold value selection. 0: EGY_PWRTH0. 1: EGY_PWRTH1.
2:1	Rsvd	-	Reserved, must be set to 0x03.
0	EGY0EN	rw	EGY0 enable. 0: Disable EGY0. 1: Enable EGY0.

27.5.3 EPU_LSCTRL Register

Table369. EPU_LSCTRL Register Description

Bit	Name	Type	Description
31:24	Rsvd	-	Reserved.
23	EGY7PWRTHSEL	rw	EGY7 threshold value selection. 0: EGY_PWRTH0. 1: EGY_PWRTH1.
22:21	Rsvd	-	Reserved, must be set to 0x03.
20	EGY7EN	rw	EGY7 enable. 0: Disable EGY7. 1: Enable EGY7.
19	EGY6PWRTHSEL	rw	EGY6 threshold value selection. 0: EGY_PWRTH0. 1: EGY_PWRTH1.
18:17	Rsvd	-	Reserved, must be set to 0x03.
16	EGY6EN	rw	EGY6 enable. 0: Disable EGY6. 1: Enable EGY6.
15	EGY5PWRTHSEL	rw	EGY5 threshold value selection. 0: EGY_PWRTH0. 1: EGY_PWRTH1.
14:13	Rsvd	-	Reserved, must be set to 0x03.
12	EGY5EN	rw	EGY5 enable. 0: Disable EGY5.

			1: Enable EGY5.
11	EGY4PWRTHSEL	rw	EGY4 threshold value selection. 0: EGY_PWRTH0. 1: EGY_PWRTH1.
10:9	Rsvd	-	Reserved, must be set to 0x03.
8	EGY4EN	rw	EGY4 enable. 0: Disable EGY4. 1: Enable EGY4.
7	EGY3PWRTHSEL	rw	EGY3 threshold value selection. 0: EGY_PWRTH0. 1: EGY_PWRTH1.
6:5	Rsvd	-	Reserved, must be set to 0x03.
4	EGY3EN	rw	EGY3 enable. 0: Disable EGY3. 1: Enable EGY3.
3	EGY2PWRTHSEL	rw	EGY2 threshold value selection. 0: EGY_PWRTH0. 1: EGY_PWRTH1.
2:1	Rsvd	-	Reserved, must be set to 0x03.
0	EGY2EN	rw	EGY2 enable. 0: Disable EGY2. 1: Enable EGY2.

27.5.4 EPU_CLR Register

Table370. EPU_CLR Register Description

Bit	Name	Type	Description
31:16	Rsvd	-	Reserved.
15	EGY7OUTCLR	rc_w1	Write 1 clear EPU_OUT7.
14	EGY6OUTCLR	rc_w1	Write 1 clear EPU_OUT6.
13	EGY5OUTCLR	rc_w1	Write 1 clear EPU_OUT5.
12	EGY4OUTCLR	rc_w1	Write 1 clear EPU_OUT4.
11	EGY3OUTCLR	rc_w1	Write 1 clear EPU_OUT3.
10	EGY2OUTCLR	rc_w1	Write 1 clear EPU_OUT2.
9	EGY1OUTCLR	rc_w1	Write 1 clear EPU_OUTH1 and EPU_OUTL1.
8	EGY0OUTCLR	rc_w1	Write 1 clear EPU_OUTH0 and EPU_OUTL0.
7	EGY7CFCNTCLR	rc_w1	Write 1 clear EPU_CNT7.
6	EGY6CFCNTCLR	rc_w1	Write 1 clear EPU_CNT6.
5	EGY5CFCNTCLR	rc_w1	Write 1 clear EPU_CNT5.
4	EGY4CFCNTCLR	rc_w1	Write 1 clear EPU_CNT4.
3	EGY3CFCNTCLR	rc_w1	Write 1 clear EPU_CNT3.
2	EGY2CFCNTCLR	rc_w1	Write 1 clear EPU_CNT2.

1	EGY1CFCNTCLR	rc_w1	Write 1 clear EPU_CNT1.
0	EGY0CFCNTCLR	rc_w1	Write 1 clear EPU_CNT0.

27.5.5 EPU_CRPTH Register

Table371. EPU_CRPTH Register Description

Bit	Name	Type	Description
31:0	CRPTH	rw	Anti-creep threshold for high-speed energy accumulator. When the accumulated value of the anti-creep energy accumulator over this threshold and the accumulated value of the high-speed energy accumulator under this threshold, the accumulated value of the high-speed energy accumulator will be cleared.

27.5.6 EPU_PWRTH0 Register

Table372. EPU_PWRTH0 Register Description

Bit	Name	Type	Description
31:0	PWRTH	rw	Accumulation threshold for energy accumulator. Due to the energy accumulator was 44bit, the accumulated value of the high-speed energy accumulator equals to this value*4096; the accumulated value of the low-speed energy accumulator equals to this value*1.

27.5.7 EPU_PWRTH1 Register

Table373. EPU_PWRTH1 Register Description

Bit	Name	Type	Description
31:0	PWRTH	rw	Accumulation threshold for energy accumulator. Due to the energy accumulator was 44bit, the accumulated value of the high-speed energy accumulator equals to this value*4096; the accumulated value of the low-speed energy accumulator equals to this value*1.

27.5.8 EPU_INTEN Register

Table374. EPU_INTEN Register Description

Bit	Name	Type	Description
31:8	Rsvd	-	Reserved.
7	EGY7OVIE	rw	EGY7 overflow interrupt enable.
6	EGY6OVIE	rw	EGY6 overflow interrupt enable.

5	EGY5OVIE	rw	EGY5 overflow interrupt enable.
4	EGY4OVIE	rw	EGY4 overflow interrupt enable.
3	EGY3OVIE	rw	EGY3 overflow interrupt enable.
2	EGY2OVIE	rw	EGY2 overflow interrupt enable.
1	EGY1OVIE	rw	EGY1 overflow interrupt enable.
0	EGY0OVIE	rw	EGY0 overflow interrupt enable.

27.5.9 EPU_INTSTS Register

Table375. EPU_INTSTS Register Description

Bit	Name	Type	Description
31:8	Rsvd	-	Reserved.
7	EGY7OVIF	rc_w1	EGY7 overflow interrupt flag, write 1 to clear this flag.
6	EGY6OVIF	rc_w1	EGY6 overflow interrupt flag, write 1 to clear this flag.
5	EGY5OVIF	rc_w1	EGY5 overflow interrupt flag, write 1 to clear this flag.
4	EGY4OVIF	rc_w1	EGY4 overflow interrupt flag, write 1 to clear this flag.
3	EGY3OVIF	rc_w1	EGY3 overflow interrupt flag, write 1 to clear this flag.
2	EGY2OVIF	rc_w1	EGY2 overflow interrupt flag, write 1 to clear this flag.
1	EGY1OVIF	rc_w1	EGY1 overflow interrupt flag, write 1 to clear this flag.
0	EGY0OVIF	rc_w1	EGY0 overflow interrupt flag, write 1 to clear this flag.

27.5.10 EPU_STS Register

Table376. EPU_STS Register Description

Bit	Name	Type	Description
31:2	Rsvd	-	Reserved.
1	EGY1CRP	r	EGY1 creep status 0: EGY1 is in a starting state. 1: EGY1 is in a creeping state.
0	EGY0CRP	r	EGY0 creep status 0: EGY0 is in a starting state. 1: EGY0 is in a creeping state.

27.5.11 EPU_CONST0 Register

Table377. EPU_CONST0 Register Description

Bit	Name	Type	Description
31:0	CONST0	rw	Energy accumulator 0 accumulating constant.

27.5.12 EPU_OUTL0 Register

Table378. EPU_OUTL0 Register Description

Bit	Name	Type	Description
31:0	OUTL0	r	Energy accumulator 0 accumulating low bit.

27.5.13 EPU_OUTH0 Register

Table379. EPU_OUTH0 Register Description

Bit	Name	Type	Description
31:0	OUTH0	r	Energy accumulator 0 accumulating high bit. Low 13 bit effective.

27.5.14 EPU_CFCNT0 Register

Table380. EPU_CFCNT0 Register Description

Bit	Name	Type	Description
31:0	CFCNT0	r	Energy accumulator 0 overflow counter.

27.5.15 EPU_CONST1 Register

Table381. EPU_CONST1 Register Description

Bit	Name	Type	Description
31:0	CONST1	rw	Energy accumulator 1 accumulating constant.

27.5.16 EPU_OUTL1 Register

Table382. EPU_OUTL1 Register Description

Bit	Name	Type	Description
31:0	OUTL1	r	Energy accumulator 1 accumulating low bit.

27.5.17 EPU_OUTH1 Register

Table383. EPU_OUTH1 Register Description

Bit	Name	Type	Description
31:0	OUTH1	r	Energy accumulator 1 accumulating high bit. Low 13 bit effective.

27.5.18 EPU_CFCNT1 Register

Table384. EPU_CFCNT1 Register Description

Bit	Name	Type	Description
31:0	CFCNT1	r	Energy accumulator 1 overflow counter.

27.5.19 EPU_CONSTx (x=2-7) Register

Table385. EPU_CONSTx Register Description

Bit	Name	Type	Description
31:0	CONSTx	rw	Energy accumulator x accumulating constant.

27.5.20 EPU_OUTx (x=2-7) Register

Table386. EPU_OUTx Register Description

Bit	Name	Type	Description
31:0	OUTx	r	Energy accumulator x accumulating value.

27.5.21 EPU_CFCNTx (x=2-7) Register

Table387. EPU_CFCNTx Register Description

Bit	Name	Type	Description
31:0	CFCNTx	r	Energy accumulator x overflow counter.

28 Debug Features

V85XX uses the Cortex-M0 core, which contains the hardware debug module.

28.1 Feature

The Cortex-M0 processor supports a number of useful debug features:

- Halting, resuming, and single stepping of program execution
- Access to processor core registers and special registers
- Hardware breakpoints (up to four comparators)
- Software breakpoints (BKPT instruction)
- Data watch points (up to two comparators)
- On-the-fly memory access (system memory can be accessed without stopping the processor)
- PC sampling for basic profiling
- Support of serial wire debug (SWD) protocol

28.2 SWD Port

Table388. Special Function of SW Port

MODE	Function 1	Function 2
Debug (PIN MODE is L)	SWCLK	SWDIO
Normal (PIN MODE is H)	SEG54/IOA0	SEG53/IOA1

29 Cortex-M0 Core Brief Description

The ARM Cortex-M0 processor is designed to meet the needs of modern ultra-low-power microcontroller units (MCUs) and mixed-signal devices. The ARM Cortex-M0 processor is as small as an 8-bit or 16-bit processor, but it is a full 32-bit processor that incorporates advanced technologies with many compelling benefits over 8-bit or 16-bit devices. The ARM Cortex-M0 processor can achieve high Energy Efficiency and Code Density.

29.1 CMSIS Function Specification

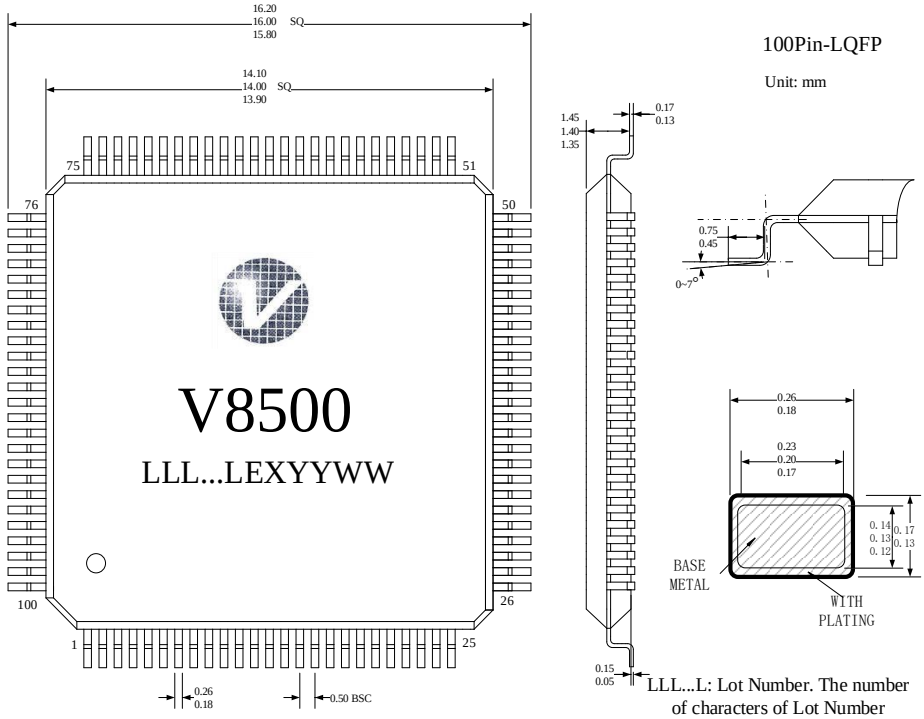
Table389. CMSIS Function

Function	Specification
void NVIC_EnableIRQ(IRQn_Type IRQn);	Enable an interrupt. This function does not apply to system exceptions.
void NVIC_DisableIRQ(IRQn_Type IRQn);	Disable an interrupt. This function does not apply to system exceptions.
void VIC_SetPendingIRQ(IRQn_Type IRQn);	Set the pending status of an interrupt. This function does not apply to system exceptions.
void NVIC_ClearPendingIRQ(IRQn_Type IRQn);	Clear the pending status of an interrupt. This function does not apply to system exceptions.
uint32_t NVIC_GetPendingIRQ(IRQn_Type IRQn);	Obtain the interrupt pending status of an interrupt. This function does not apply to system exceptions.
void NVIC_SetPriority(IRQn_Type IRQn,uint32_t priority);	Set up the priority level of an interrupt or system exception. The priority level value is automatically shifted to the implemented bits in the priority level register.
uint32_t NVIC_GetPriority(IRQn_TypeIRQn);	Obtain the priority level of an interrupt or system exception. The priority level is automatically shifted to remove unimplemented bits in the priority level values.
void __enable_irq(void);	Clear PRIMASK. Enable interrupts and system exceptions.
void __disable_irq(void);	Set PRIMASK. Disable all interrupts including system exceptions (apart from hard fault and NMI).
uint32_t SysTick_Config(uint32_t ticks);	Initialize and start the SysTick counter

	and its interrupt; this function programs the SysTick to generate SysTick except ionfor every “ticks” number of core clock cycles.
void NVIC_SystemReset(void);	M0-soft reset.
SCB->SCR |= SCB_SCR_SLEEPDEEP_Msk; void __WFI(void);	Wait for interrupt (enter sleep mode).
SCB->SCR &= (uint32_t)~((uint32_t)SCB_SCR_SLEEPDEEP_Msk); void __WFI(void);	Wait for interrupt (enter idle mode).

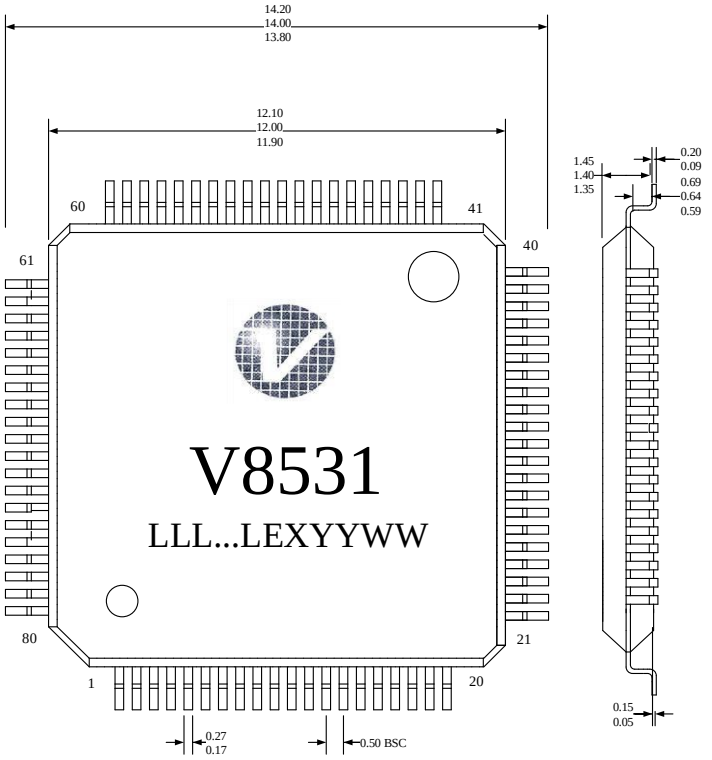
30 Outline Dimensions

30.1 Outline Dimensions_V8500



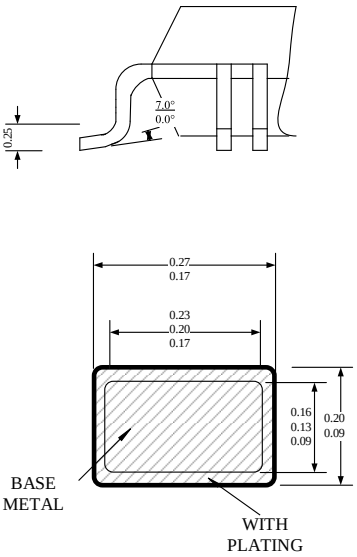
LLL...L: Lot Number. The number of characters of Lot Number varies between 8 to 11.
EX: E0,E1,...
YY: Year
WW: Week

30.2 Outline Dimensions_V8531



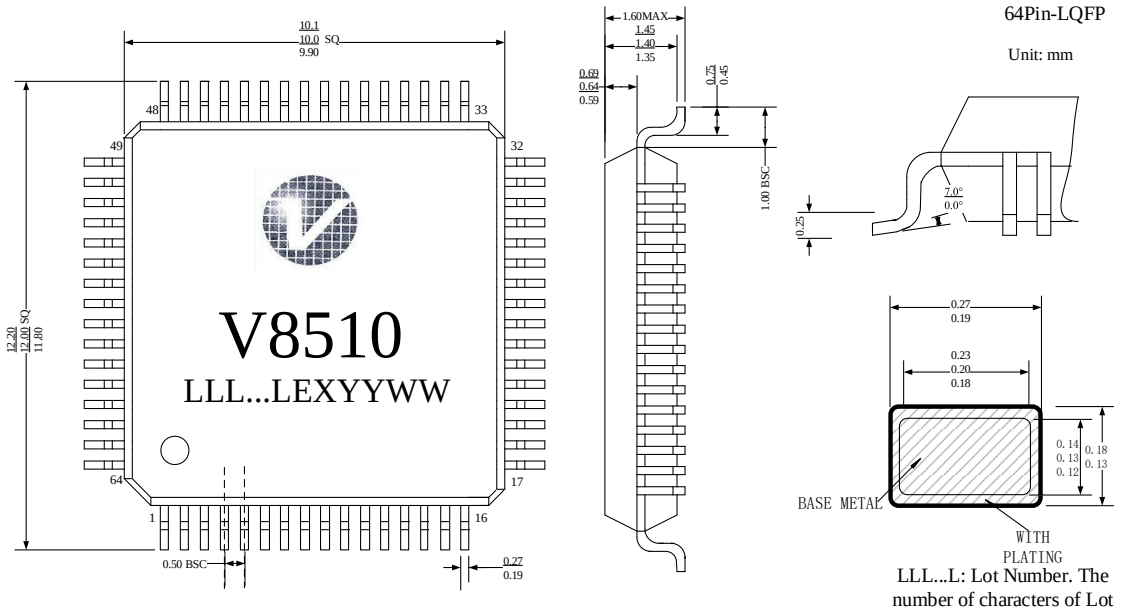
80Pin-LQFP

Unit: mm



LLL...L: Lot Number. The number of characters of Lot Number varies between 8 to 11.
EX: E0,E1,...
YY: Year
WW: Week

30.3 Outline Dimensions_V8510



LLL...L: Lot Number. The number of characters of Lot Number varies between 8 to 11. EX: E0,E1,...
YY: Year
WW: Week

Innovates for the Internet of Energy

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