VANGO TECHNOLOGIES, INC.

V9160 Datasheet

The V9160 is a three - phase metering chip. It supports full-wave and fundamental-wave energy metering in various modes, and can monitor a variety of power grid events. At the same time, the sampled data can be transmitted out via DMA according to the SPI protocol.

Function

- Power Supply: 3.3V power supply, voltage input range 3.0 - 3.6V
- Reference Voltage: 1.2V (typical temperature coefficient 10 ppm/°C)
- Power Consumption:

  Typical power consumption of the chip during normal operation at room temperature:
  - 8.5 mA (when the system clock is 26.2144 MHz)
- Measurement Features:
  - 6 independent oversampling ∑/Δ ADCs: 3 voltage channels and 3 current channels
  - Supports arbitrary mapping of voltage/ current channels, adjustable through configuration registers
  - Measurement accuracy:

    Meets the requirements of IEC 62053-21:2020/ IEC 62053-22:2020 and IEC 62053-23:2020

    Within a 10000:1 dynamic range, the error of full-wave / fundamental active energy measurement is less than 0.1%

    Within a 10000:1 dynamic range, the error of full-wave/ fundamental reactive energy measurement is less than 0.1%

    Within a 2000:1 dynamic range, the error of full-wave/ fundamental voltage / current RMS value is less than 0.2%
  - Measurement data:

    Instantaneous and average values of full-wave/ fundamental current/ voltage RMS

    Instantaneous and average values of full-wave/ fundamental active / reactive power

    Instantaneous and average values of full-wave apparent power

    Active/ reactive/ apparent power/ current RMS/ constant values

    Three-phase line voltage value

    Vector sum value of three-phase current

    Frequency and phase
  - Supports software calibration
  - Supports small signal accelerated calibration
- Supports Detection of: Overcurrent, overvoltage, undercurrent, undervoltage, voltage swell, and voltage dip
- Supports sampled data DMA Transmission, up to 512 points per cycle.

- Current sampled: Supports CT and Rogowski coil
- Supports UART Interface
- Operating Temperature: -40 ~ +105°C
- Storage Temperature: -55 ~ +150°C
- Package: SOP16

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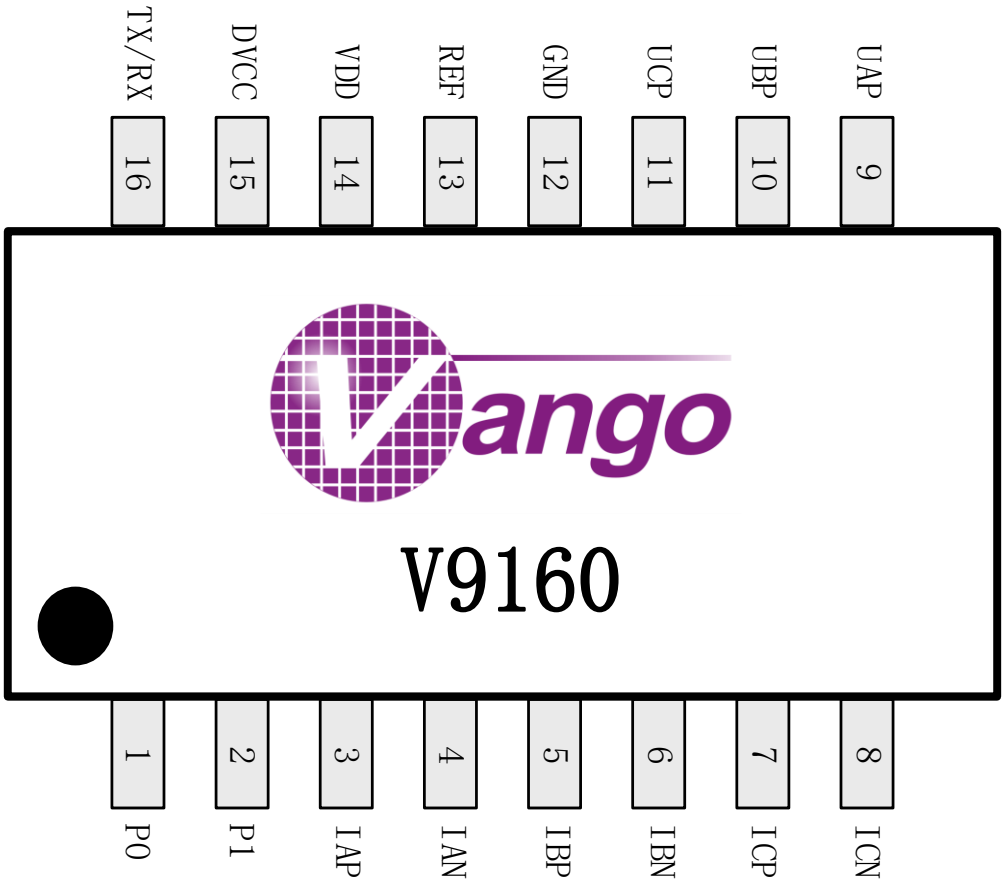
Revision History

Table1. Document Version History

Date	Revision	Description
2024.11.18	V1.0	Initial Version;
2025.01.21	V1.1	Delete the POR function;
2025.04.09	V1.2	Modify the RCH performance parameter values;

1 Pin Configuration



2 Pin Description

Table2. Pin Description

Pin Number	Pin Name	Input / Output	Function
1	P0	O	Configurable output
2	P1	O	Configurable output
3	IAP	I	Current A channel P-terminal input
4	IAN	I	Current A channel N-terminal input
5	IBP	I	Current B channel P-terminal input
6	IBN	I	Current B channel N-terminal input
7	ICP	I	Current C channel P-terminal input
8	ICN	I	Current C channel N-terminal input
9	UAP	I	Voltage A channel P-terminal input
10	UBP	I	Voltage B channel P-terminal input
11	UCP	I	Voltage C channel P-terminal input
12	GND	P	Ground
13	REF	O	Reference voltage
14	VDD	P	Main power supply
15	DVCC	O	Digital power output
16	TX/ RX	I / O	UART communication

3 Parameters

Table3. Parameters

Parameter		Min.	Typ.	Max.	Unit	Remark
Analog Input						
Maximum Signal Level	Voltage channel	-200		200	mV	Peak value
	Current channel	-400		400		
Bandwidth (-3dB)			2		kHz	
On-chip Reference						
Temperature Coefficient			10		ppm/°C	
Output Voltage		1.1	1.2	1.3	V	
VDD Power-on rate		3.3V/s		1V/ms		
PVD						
Detection Threshold for Power-Down		2.7	2.8	2.9	V	
Hysteresis			30		mV	
Clock Frequency						
RCH			6.5		MHz	
Phase Error Between Channels						
Total Active Energy Metering Error			0.1		%	Dynamic Range 10000:1 @ 25°C
Total Active Energy Metering Bandwidth			2		kHz	
Total Reactive Energy Metering Error			0.1		%	Dynamic Range 10000:1 @ 25°C
Total Reactive Energy Metering Bandwidth			2		kHz	
Fundamental Active Energy Metering Error			0.1		%	Dynamic Range 10000:1 @ 25°C
Fundamental Active Energy Metering Bandwidth			65		Hz	
Fundamental Reactive Energy Metering Error			0.1		%	Dynamic Range 10000:1 @ 25°C
Fundamental Reactive Energy Metering Bandwidth			65		Hz	
Total Apparent Energy Metering Error			0.2		%	Dynamic Range 2000:1 @ 25°C
Fundamental Apparent Energy Metering Error			0.2		%	Dynamic Range 2000:1 @ 25°C
VRMS Metering Error			0.2		%	Dynamic Range 2000:1 @ 25°C
VRMS Metering Bandwidth			2		kHz	
IRMS Metering Error			0.2		%	Dynamic Range 2000:1 @ 25°C
IRMS Metering Bandwidth			2		kHz	
digital I/O						
Driving capability			4		mA	

Output High Voltage, V_{OH}	2.4			V	
Output Low Voltage, V_{OL}			0.4	V	
Input High Voltage, V_{INH}	2.0		3.6	V	
Input Low Voltage, V_{INL}	-0.3		0.8	V	
Power Input					
AVDD	3.0	3.3	3.6	V	
Digital Power Output (DVCC)					
Voltage		1.2		V	
Input voltage of current sampling channel	-0.4		AVDD+0.3	V	relative to ground
Input voltage of voltage sampling channel	-0.2		AVDD+0.3	V	relative to ground
Operating temperature	-40		+105	˚C	
Storage temperature	-55		+150	˚C	

Table4. Power Consumption

Working Mode/Circuit Module		**Power Consumption**	**Unit**	**Explanation**
Full-Speed Operation	Normal Working Mode	8.5	mA	The data of the chip's current consumption when the system clock frequency is 26.2144 MHz, the ADC clock frequency is 6.5536 MHz, and the ADCs of A/B/C three-phase voltage/current channels are enabled.

4 Power System

The power system of V9160 has the following characteristics:

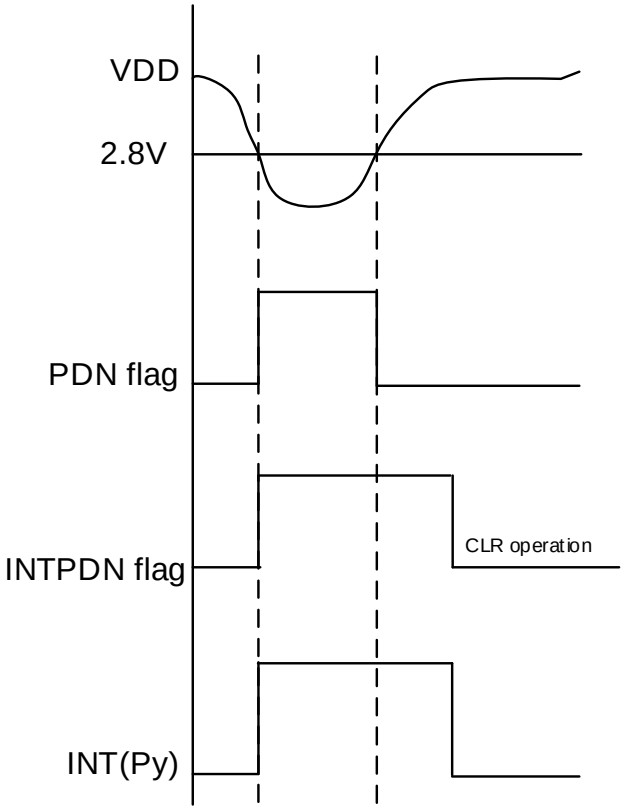
- 3.3V single power supply, voltage input range: 2.8 - 3.6V;
- Supports power-down monitoring;

4.1 Power-down Monitoring Circuit

The V9160 has a built-in power-down monitoring circuit that can monitor the input signal of the VDD pin in real-time. When the level on the VDD pin is lower than 2.8V, the system generates a power-down interrupt. At this time, the metering accuracy cannot be guaranteed, but normal communication is still possible.

The power-down monitoring circuit is always active.

Figure1. Power-down Monitoring



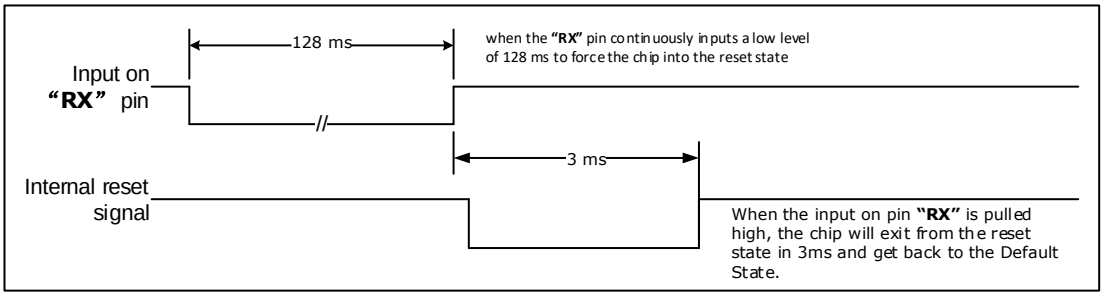
5 Reset

5.1 RX Reset

When the "RX" pin is continuously low for 128 ms, the chip generates an internal reset. After that, when the "RX" pin is high, the chip reset is completed after 3 ms.

Attention: A RX reset operation needs to be performed after the chip is powered on.

Figure2. RX Reset Timing Diagram during UART Communication



In the reset state, the external cannot access the RAM. After the system exits the reset state, the RAM performs a self-check that lasts approximately 0.35ms. After the self-check passes, the RAM can be freely accessed.

After the system exits the reset state and the RAM initialization is completed, the UART immediately starts working.

5.2 Software Reset

Executing the soft reset function can cause an internal reset of the chip, and the reset will be completed after 1ms.

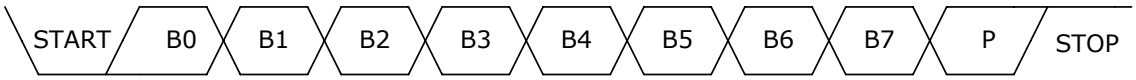
Ensure that the system communication is normal before executing the software reset function.

6 Universal Asynchronous Receiver Transmitter (UART)

6.1 Overview

The V9160 supports UART communication. After a POR reset, RX reset, or soft reset, the V9160 defaults to using UART communication. The V9160 UART is a standard 8-bit UART with odd parity. The UART uses low-byte-first and low-bit-first transmission. The following figure shows the standard format of a UART byte.

Figure3. 11-Bit Byte Data Format (LSB to MSB)



The UART protocol is a half-duplex protocol. After the MCU finishes sending a command, the V9160 uploads data after 1ms (depending on the accuracy of the system clock). The V9160 UART supports adaptive baud rate and recommends using a baud rate of 1200bps - 19200bps. The V9160 automatically adapts to the communication baud rate by receiving the first frame header. This baud rate is also fine-tuned during subsequent communications. If the communication baud rate changes significantly, the baud rate adaptation needs to be performed again.

The V9160 supports a continuous write communication command, which can save parameter configuration time.

Under the following conditions, the UART reception of the V9160 stops.

Table5. UART Communication Errors

Number	Conditions	UART_ERR Set to 1
1	Frame header error in UART reception.	No
2	UART reception timeout, the time interval between two consecutive bytes is greater than 20ms (related to the accuracy of the system clock).	Yes
3	Odd parity bit error in UART reception.	Yes
4	Checksum byte error in UART reception.	Yes

6.2 Communication Protocol

In read, write or block read communication, the master MCU needs a command frame that is composed of 8 data bytes to operate a 32-bit data in the V9160.

Figure4. Command Frame for Read/Write/Broadcast Operation

Head Byte	Control Byte	Address Byte	Data Byte 0	Data Byte 1	Data Byte 2	Data Byte 3	Check Byte

In read or write operation, when the V9160 receives the command frame from the master MCU, it will reply to the master MCU with a respond frame of different structures. In broadcast communication, the V9160 will not reply to the master MCU to avoid communication conflict.

The following figure depicts the timing of UART communication.

Figure5. Timing of UART Communication

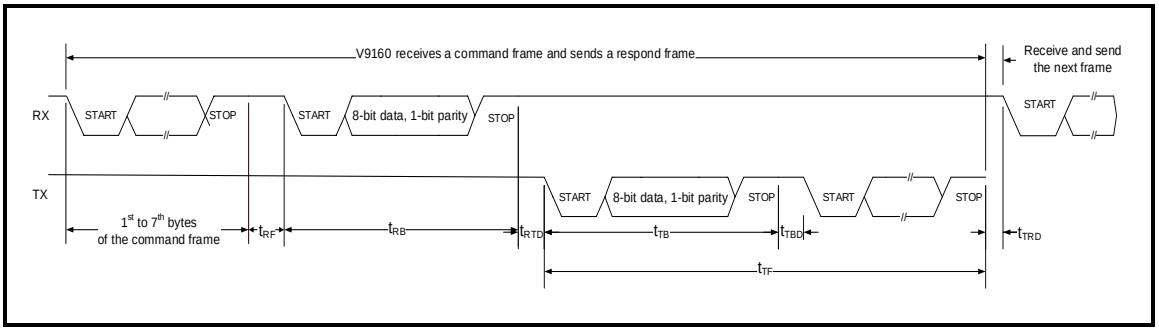


Table6. UART Communication Timing Parameters

Parameter	Description
t_{RB}	Time to receive a data byte on pin RX. $t_{RB}=\frac{11}{baudrate}$ Where, *baudrate* is the actual baud rate.
t_{RF}	The maximum time between two bytes when receiving a command frame on pin **"RX"** t_{RF}=20ms After a timeout event, the UART interface is idle and waits for the next command frame.
t_{RTD}	The delay between command frame reception on pin RX and respond frame transmission on pin TX. 1ms≤t_{RTD}≤20ms Please note no respond frame will be transmitted in broadcast communication, and at least 1ms delay is recommended between two continuous command frames for broadcast communications.
t_{TF}	Time to transmit a respond frame in read or write operation, depending on the structure of the frame.
t_{TB}	Time to transmit a data byte. $t_{TB}=\frac{11}{baudrate}$ Where *baudrate* is the actual baud rate.
t_{TBD}	Delay between two continuous data bytes in a respond frame. 0ms≤t_{TBD}≤20ms
t_{TRD}	The delay between respond frame transmission on pin TX and the next command frame reception on pin RX. More than 1ms is recommended.

6.3 Read Operation

- Supports reading 1 ~ 16 consecutive registers.
- The V9160 will respond.

Figure6. Read Operation Communication Protocol

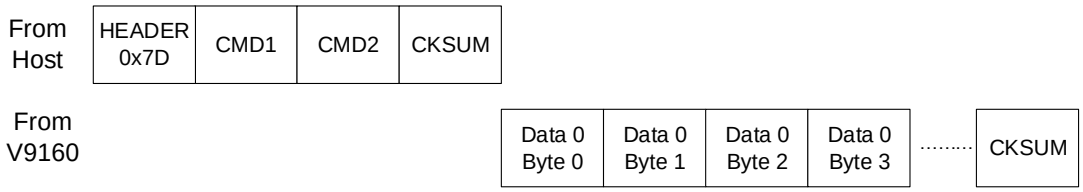


Table7. Command Frame Structure Sent by the MCU to V9160 for Read Operation (Only Listing the Data Bits B7:B0 of Each Byte)

Sequence	Byte	B7	B6	B5	B4	B3	B2	B1	B0
1	HEADER	0	1	1	1	1	1	0	1
2	CMD1	Read operation length selection (N) 0: Read 1 32-Bits data. 1: Read 2 32-Bits data. … 15: Read 16 32-Bits data				0	0	0	1
3	CMD2	Read operation starting address (D0)							
4	CKSUM	Checksum. Calculation method: Add CMD1 and CMD2 byte by byte, take the inverse of the sum, and then add 0x33. The formula is as follows: CKSUM = 0x33 + ~(CMD1 + CMD2)							

Table8. Response Frame Structure Sent by V9160 to MCU for Read Operation (Only Listing the Data Bits B7:B0 of Each Byte)

Sequence	Byte	B7	B6	B5	B4	B3	B2	B1	B0
1	Data 0 Byte 0	Bit[7:0] of the target data read from the register (address D0)							
2	Data 0 Byte 1	Bit[15:8] of the target data read from the register (address D0)							
3	Data 0 Byte 2	Bit[23:16] of the target data read from the register (address D0)							
4	Data 0 Byte 3	Bit[31:24] of the target data read from the register (address D0)							
…	…	…							
4xN+1	Data N Byte 0	Bit[7:0] of the target data read from the register (address DN = D0 + N)							
4xN+2	Data N Byte 1	Bit[15:8] of the target data read from the register (address DN = D0 + N)							
4xN+3	Data N Byte 2	Bit[23:16] of the target data read from the register (address DN = D0 + N)							
4xN+4	Data N Byte 3	Bit[31:24] of the target data read from the register (address DN = D0 + N)							

4xN+5	CKSUM	Checksum. Calculation method: Add the 4×(N + 1) target data bytes (Data 0 - N Byte 0 - 3, from V9160) and CMD1 and CMD2 (from MCU) byte by byte, take the inverse of the sum, and then add 0x33. The formula is as follows: CKSUM = 0x33 + ~(CMD1 + CMD2 + Data 0 Byte 0 + Data 0 Byte 1 + Data 0 Byte 2 + Data 0 Byte 3 + … + Data N Byte 0 + Data N Byte 1 + Data N Byte 2 + Data N Byte 3)
When the read operation length N is equal to 0, the V9160 will only send a 5 - byte response frame to the MCU.		

6.4 Write Operation

- Supports writing 1 ~ 16 consecutive registers.
- The V9160 will respond.

Figure7. Write Operation Communication Protocol

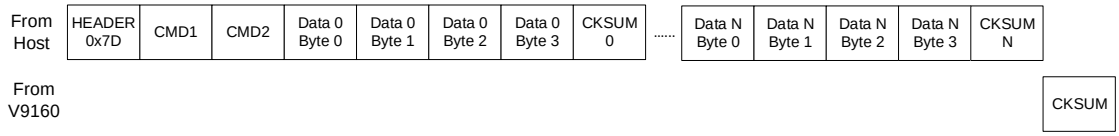


Table9. Command Frame Structure Sent by the MCU to V9160 for Write Operation (Only Listing the Data Bits B7:B0 of Each Byte)

Sequence	Byte	B7	B6	B5	B4	B3	B2	B1	B0
1	HEADER	0	1	1	1	1	1	0	1
2	CMD1	Write length selection (N): 0: Write 1 32-bit data. 1: Write 2 32-bit data. ... 15: Write 16 32-bit data.				0	0	1	0
3	CMD2	Write operation starting address (D0).							
4	Data 0 Byte 0	Bit[7:0] of the target data written to the register (address D0).							
5	Data 0 Byte 1	Bit[15:8] of the target data written to the register (address D0).							
6	Data 0 Byte 2	Bit[23:16] of the target data written to the register (address D0).							
7	Data 0 Byte 3	Bit[31:24] of the target data written to the register (address D0).							
8	CKSUM 0	Checksum 0. Calculation method: Add the above 4 target data bytes (Data 0 Byte 0 - 3) and CMD1 and CMD2 byte by byte, take the inverse of the sum, and then add 0x33. The formula is as follows: CKSUM 0 = 0x33 + ~(CMD1 + CMD2 + Data 0 Byte 0 + Data 0 Byte 1 + Data 0 Byte 2 + Data 0 Byte 3).							
…	…	…							
5xN+4	Data N Byte 0	Bit[7:0] of the target data written to the register (address DN = D0 + N).							

5xN+5	Data N Byte 1	Bit[15:8] of the target data written to the register (address DN = D0 + N).
5xN+6	Data N Byte 2	Bit[23:16] of the target data written to the register (address DN = D0 + N).
5xN+7	Data N Byte 3	Bit[31:24] of the target data written to the register (address DN = D0 + N).
5xN+8	CKSUM N	Checksum N (from MCU). Calculation method: Add the 4×(N + 1) target data bytes (Data 0 - N Byte 0 - 3) and CMD1 and CMD2 byte by byte, take the inverse of the sum, and then add 0x33. The formula is as follows: CKSUM N = 0x33 + ~(CMD1 + CMD2 + Data 0 Byte 0 + Data 0 Byte 1 + Data 0 Byte 2 + Data 0 Byte 3 + … + Data N Byte 0 + Data N Byte 1 + Data N Byte 2 + Data N Byte 3).
When the write operation length N is equal to 0, the MCU only needs to send the first 8 bytes of the command frame to the V9160.		

Table10. Response frame structure sent by V9160 to MCU for write operation (only listing the data bits B7:B0 of each byte).

Sequence	Byte	B7	B6	B5	B4	B3	B2	B1	B0
1	CKSUM	Checksum (from V9160). Used to check whether the write operation is successful. If CKSUM is equal to CKSUM N (from MCU), then this write operation is successful. If CKSUM is not equal to CKSUM N (from MCU), then this write operation fails.							

6.5 Block Read Operation

To facilitate users to read the required data at once and improve communication efficiency, the V9160 provides a fixed continuous read function.

Features are as follows:

- Support block read operations on registers with fixed addresses that are not continuous.
- When the current phase measurement mode is single-phase measurement mode, after the UART block read is completed, a single-phase measurement is automatically triggered.
- V9160 will respond.
- The fixed return data order of block read registers is shown in the following table.

Table11. Block Read Data Sequence

Number	Data Item
0	Average active power value of phase A full wave
1	Average active power value of phase B full wave
2	Average active power value of phase C full wave
3	Average reactive power value of phase A full wave
4	Average reactive power value of phase B full wave
5	Average reactive power value of phase C full wave
6	Average apparent power value of phase A full wave
7	Average apparent power value of phase B full wave

8	Average apparent power value of phase C full wave
9	Average RMS voltage value of phase A full wave
10	Average RMS voltage value of phase B full wave
11	Average RMS voltage value of phase C full wave
12	Average RMS current value of phase A full wave
13	Average RMS current value of phase B full wave
14	Average RMS current value of phase C full wave
15	Average frequency value of phase A full wave
16	Average frequency value of phase B full wave
17	Average frequency value of phase C full wave
18	Phase angle of phase B voltage
19	Phase angle of phase C voltage
20	Phase angle of phase A current
21	Phase angle of phase B current
22	Phase angle of phase C current
23	Chip status register STS1
24	Baud rate measurement value DAT_BAUDCNT8

Figure8. Block Read Operation Communication Protocol

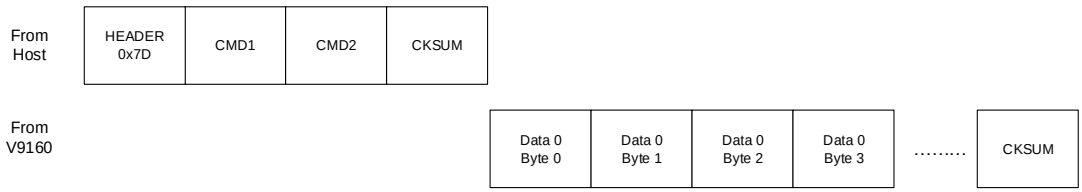


Table12. Command frame structure sent by MCU to V9160 for block read operation (only listing the data bits B7:B0 of each byte).

Sequence	Byte	B7	B6	B5	B4	B3	B2	B1	B0
1	HEADER	0	1	1	1	1	1	0	1
2	CMD1	0	0	0	0	0	0	1	1
3	CMD2	0	0	0	Starting sequence number selection for block read operation (M). For example: If M = 3, the first returned data is the average reactive power value of phase A full wave. If M = 0, the first returned data is the average active power value of phase A full wave.				
4	CKSUM	Checksum. Calculation method: Add CMD1 and CMD2 byte by byte, take the inverse of the sum, and then add 0x33. The formula is as follows: CKSUM = 0x33 + ~(CMD1 + CMD2).							

Table13. Response frame structure sent by V9160 to MCU for block read operation (only listing the data bits B7:B0 of each byte).

Sequence	Byte	B7	B6	B5	B4	B3	B2	B1	B0
1	Data 0 Byte 0	Bit[7:0] of the target data read from the block read register sequence number M.							

Sequence	Byte	B7	B6	B5	B4	B3	B2	B1	B0
2	Data 0 Byte 1	Bit[15:8] of the target data read from the block read register sequence number M.							
3	Data 0 Byte 2	Bit[23:16] of the target data read from the block read register sequence number M.							
4	Data 0 Byte 3	Bit[31:24] of the target data read from the block read register sequence number M.							
…	…	…							
4xN+1	Data N Byte 0	Bit[7:0] of the target data read from the block read register sequence number (M + N).							
4xN+2	Data N Byte 1	Bit[15:8] of the target data read from the block read register sequence number (M + N).							
4xN+3	Data N Byte 2	Bit[23:16] of the target data read from the block read register sequence number (M + N).							
4xN+4	Data N Byte 3	Bit[31:24] of the target data read from the block read register sequence number (M + N).							
4xN+5	CKSUM	Checksum. Calculation method: Add the 4×(N + 1) target data bytes (Data 0 - N Byte 0 - 3, from V9160) and CMD1 and CMD2 (from MCU) byte by byte, take the inverse of the sum, and then add 0x33. The formula is as follows: CKSUM = 0x33 + ~(CMD1 + CMD2 + Data 0 Byte 0 + Data 0 Byte 1 + Data 0 Byte 2 + Data 0 Byte 3 +... + Data N Byte 0 + Data N Byte 1 + Data N Byte 2 + Data N Byte 3).							
When the read operation sequence number is greater than or equal to 24, the V9160 will only send a 5-byte response frame to the MCU.									

8. Measurement Data Processing Unit

7 Measurement Data Processing Unit

7.1 Overview

The MDPU is mainly used to calculate the full-wave and fundamental active power, full-wave and fundamental reactive power, full-wave and fundamental apparent power, full-wave and fundamental RMS values, full-wave and fundamental combined phase power, line voltages, and provides grid event monitoring functions. It also provides original waveform data, which can be output through DMA.

7.2 Features

- Supports simultaneous metering of 3 voltage channels and 3 current channels.
- Provides various measurement data:
  - 6 channels voltage/ current signal original waveforms (22-bit), output in DMA mode
  - DC components of 6 channels voltage / current signals, full-wave/ fundamental RMS values and active/ reactive/ apparent power of each phase
  - 3 channels line voltages
  - Frequency/ phase/ power factor
  - Line voltage measurement data between each phase
- Selectable full-wave bandwidth.
- Supports software calibration:
  - Supports waveform pre-calibration
  - Supports ratio error correction and secondary compensation (offset correction) for full-/ fundamental active power, reactive power, and fundamental active power
- Selectable refresh time for average power value or average RMS value.
- Provides 10-cycle or 12-cycle average RMS values for voltage flicker detection.
- Supports judgment of voltage swell/ dip, overvoltage/ undervoltage, and overcurrent/ undercurrent.

7.3 Calibration

7.3.1 Phase Calibration

$$N = Round(C \times E)$$

Where:

C: the constant coefficient for angle difference calibration;

N: the value written into the register related to angle difference calibration, with a sign. It is represented in two's complement.

E: the error displayed on the test bench.

Table14. Phase Calibration Description

MODE	calibration accuracy(degree)	Calibration range(degree)
0x00	0.00274658203125	±1.93084716796875

For MODE = 0x00, the offset is within the range of 0 to 7, the fine adjustment precision is 0.00274658203125°, and the fine adjustment range is ±0.17303466796875°. For medium adjustment, the offset is within the range of 0 - 3, the medium adjustment precision is 0.3515625°, and the medium adjustment range is ±1.0546875°. For coarse adjustment, the offset is within the range of 0 - 1, the coarse adjustment precision is 0.703125°, and the coarse adjustment range is ±0.703125°.

Phase correction of IA phc_ia = Angle to be corrected /calibration_acuracy

Phase correction of IB phc_ib = Angle to be corrected /calibration_acuracy

IA and IB error correction values are combined in complement form and written into the error correction register.

7.3.2 Ratio Difference Calibration

$$S = 2^{31}\left(\frac{1}{1+e} - 1\right) + S1\left(\frac{1}{1+e}\right)$$

Where:

S: the value written into the register for effective value / power ratio difference calibration, in two's complement;

$S1$: the original ratio difference value, that is, the original value displayed on the uncalibrated effective power ratio difference calibration register, in two's complement;

e: the error. When performing power ratio difference calibration, e is the error value (E) displayed on the test bench.

7.3.3 Power Small Signal Calibration

$$C = -E \times P \times a\%$$

Where:

E: when the power factor is 1.0, the error displayed on the test bench when a%Ib is passed through the test bench;

P: the value of the power register.

7.3.4 Frequency Measurement

Frequency measurement involves zero-crossing detection and counting of the fundamental wave signal. Whenever a positive zero-crossing event occurs, the current count value is latched as the instantaneous frequency measurement value (the number of points in one cycle), and it is determined according to the configuration whether to reset the counter to 1 to start counting again. If it is directly reset, it is the instantaneous frequency measurement value; otherwise, it is the average frequency measurement value.

The average frequency of any required number of cycles can be obtained by accumulating the instantaneous frequency measurement values through the configuration register counter.

$$f = \text{result\_freq} \times (\text{cfg\_frq\_unit\_sel} + 1)/\text{f\_clk}$$

where,

f_clk: System clock frequency.

result_freq: Output frequency counting result.

cfg_frq_unit_sel: Selection of the average period for measuring frequency.

8 Sampled data Upload

8.1 Overview

The V9160 supports the DMA mode data transmission method and sends a maximum of 6 channels of original sampled data to the external MCU in the SPI protocol master mode. The data upload rate varies depending on the number of sampling points. Before enabling the sampled data active upload function, it is necessary to turn on the sampled data upload switches of the corresponding channels. The switches between each channel are independent. Configure the sampled data upload IO ports P0/ P1 through the IO configuration function.

Table15. Relationship Between Sampling Points and Transmission Rate

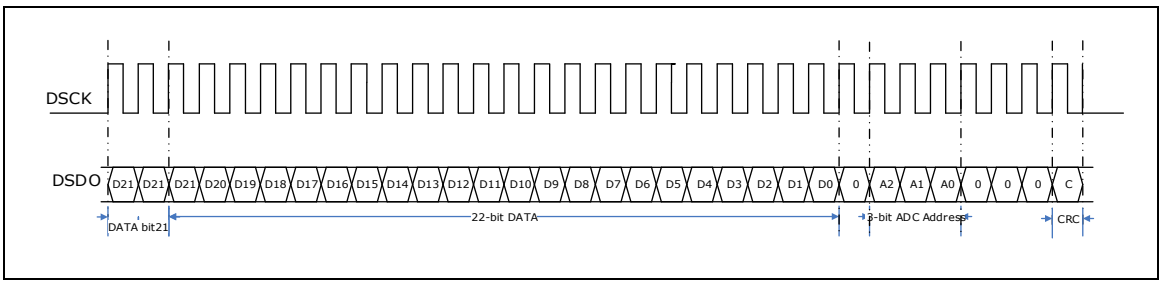
Sampling Points	Transmission Rate
512 points/cycle	Half-frequency division
256 points/cycle	Quarter-frequency division
128 points/cycle	Eighth-frequency division
64 points/cycle	Sixteenth-frequency division

The triggering methods for uploading sampled data of V9160 support command-triggered and event-triggered. The event-triggered cases include all the following situations: swell and dip events of UA/ UB/ UC, overvoltage and undervoltage events of UA/ UB/ UC, and overcurrent and undercurrent events of IA/ IB/IC.

8.2 Timing and Format

The V9160 can transmit the original sampled data of the signal to the peripheral device through the DMA SPI interface. The SPI polarity and phase can be configured. When the polarity is 0 and the phase is 0, the transmission timing is as follows:

Figure9. DMA SPI Transmission Timing



Transmission method: Complete the transmission of 32-bit data at a time. The format of each transmitted data frame is shown in the following table:

Table16. Active Waveform Upload Data Format

Bit	Content
31	The same value as Bit 29
30	The same value as Bit 29
29:8	Original sampled data of each channel ADC signal, 22-bit
7	0
6	Indicates whether the current sampled data comes from the UA channel 0: No 1: Yes
5	Indicates whether the current sampled data comes from the IA channel 0: No 1: Yes
4	Indicates whether the current sampled data comes from the UB channel 0: No 1: Yes
3	Indicates whether the current sampled data comes from the IB channel 0: No 1: Yes
2	Indicates whether the current sampled data comes from the UC channel 0: No 1: Yes
1	Indicates whether the current sampled data comes from the IC channel 0: No 1: Yes
0	Parity bit, the parity check range is the first 31 bits

9 Power Quality Processing Unit

9.1 Overview

Power quality processing unit mainly includes the detection of overvoltage, overcurrent, undervoltage, and undercurrent of voltage/current, as well as the detection of swell/dip of the voltage channel.

9.2 Features

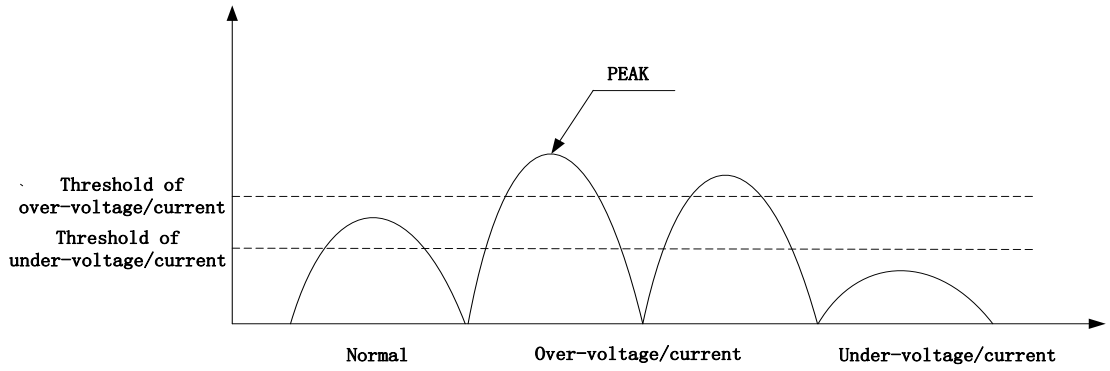
- DIP/SWELL
  - Detect the swell and dip of the instantaneous effective values of the three-phase voltages A, B, and C.
  - Generate the flag bits and interrupts for the swell and dip of the voltage effective value, and the end flag bits and interrupts for the swell and dip.
  - Record the maximum swell and dip time.
  - Record the values at the maximum swell and dip.
- Overvoltage/ Undervoltage/ Overcurrent/ Under-current
  - Realize the instantaneous overcurrent and undercurrent detection of the current and the overvoltage and undervoltage detection of the instantaneous voltage.
  - Realize the flag bits and interrupts for overvoltage, undervoltage, overcurrent, and undercurrent.

9.3 Voltage Swell/ Dip

The V9160 can be programmed to indicate the swell and dip of the three-phase voltage channels.

9.4 Overvoltage, Undervoltage, Overcurrent, and Undercurrent

Figure10. Schematic Diagram of Electrical Signal Detection



The number of sampling points above the upper threshold: For example, if the set value is 4, it means that if more than 4 points in a half-cycle sampling point exceed the threshold, the waveform of that half-cycle is considered to be over the limit.

The number of half-cycles above the upper threshold: For example, if it is set to 2, it means that if two consecutive half-cycles are both over the limit, an overvoltage or overcurrent event is considered to occur.

The number of sampling points below the lower threshold: For example, if it is set to 4, if it is found that less than or equal to 4 points in a half-cycle sampling point are higher than the lower threshold, the half-cycle is considered to be below the lower limit.

The number of half-cycles below the lower limit: For example, if it is set to 2, it means that if two consecutive half-cycles are both below the lower limit, an undervoltage or undercurrent event is considered to occur.

9.5 Zero-Crossing Detection

The V9160 supports zero-crossing detection for 3 voltage channels and 3 current channels. The zero-crossing direction can be selected. When a zero-crossing event occurs in the voltage/ current channel signal, the voltage zero-crossing flag bit and the current zero-crossing flag bit in the system interrupt status register will be set to 1. The user needs to write 1 to clear them.

When enabling the voltage/ current zero-crossing interrupt output, configure the voltage/current zero-crossing interrupt output through the IO configuration function. The output level of the pin Px automatically flips according to the voltage zero-crossing flag bit and the current zero-crossing flag bit.

The zero-crossing detection accuracy is related to the choice of sampling points. If there are 256 points in one cycle, the accuracy is 360/256.

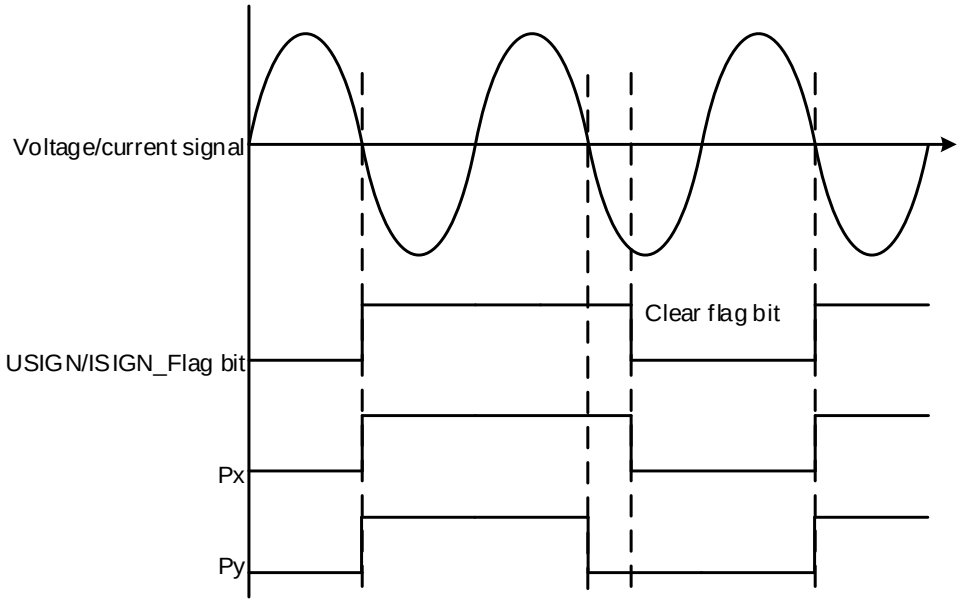
Configure the voltage/current zero-crossing output square wave through the IO configuration function. The output level of the pin Py automatically flips in real-time according to the voltage/current zero-crossing state. Every time a zero-crossing event occurs, the IO port flips

once. Since the zero-crossing square wave passes through a band-pass filter, there will be a phase lag between the output and the input, and the delay time is about 8ms (related to the fundamental frequency).

When performing voltage/current zero-crossing detection, the system will also provide a voltage/current threshold detection function. The system will automatically compare whether the instantaneous effective value of the voltage/current exceeds the threshold. If it does not exceed the threshold, it will be judged as an invalid input, and the voltage/current zero-crossing interrupt output and zero-crossing output will be masked until the instantaneous effective value of the voltage/current exceeds the threshold.

The following figure shows the configuration for enabling the zero-crossing interrupt output and the waveforms of the voltage/current zero-crossing flag bits, zero-crossing interrupt output, and zero-crossing output square wave when the zero-crossing detection method is selected as negative zero-crossing.

Figure11. Voltage/Current Zero-Crossing Output Diagram



10 Signal Output Port

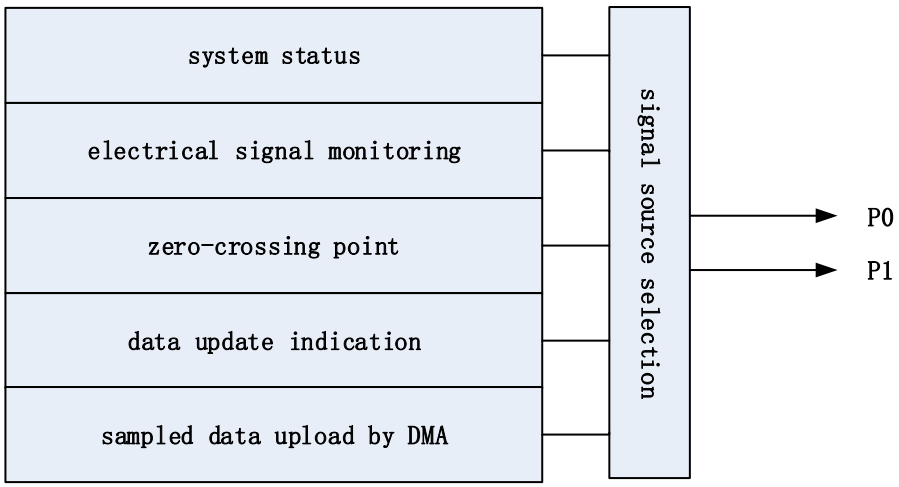
10.1 Overview

The V9160 provides at most 2 output signals (P0/P1) for mapping internal output signal sources.

10.2 Functional Description

The 2 signal output ports can be configured as the DMA channel interface for sampled data active upload, zero-crossing square wave, and four types of interrupt outputs. The signal output port can be set to output a single signal or several types of interrupt signals.

Figure12. Functional Block Diagram of Signal Output Port



Note1: When used as an interrupt event output port, the output port defaults to a low-level output. If an event occurs, it outputs a high level until the user clears the event flag bit, and the output state returns to the default level.

Note2: When used as a zero-crossing square wave output, the output port defaults to a low-level output. If configured as a positive zero-crossing, the IO port flips when the signal transitions from a negative signal to a positive signal.

Note3: When used as a DMA output port, the SPI protocol is used, and the user needs to select the SPCK and SPDO ports.

Note4: The IO output configuration has 8 bits, and the output interrupt type is determined according to the following table:

Table17. IO output configuration

Bit6 - Bit3	Bit2 - Bit0	Function

0	0	High impedance state
0	1	High impedance state
0	2	High impedance state
0	3	High impedance state
0	4	High impedance state
0	5	High impedance state
0	6	UA voltage dip interrupt
0	7	UA voltage swell interrupt
1	0	UB voltage dip interrupt
1	1	UB voltage swell interrupt
1	2	UC voltage dip interrupt
1	3	UC voltage swell interrupt
1	4	UA voltage dip end interrupt
1	5	UA voltage swell end interrupt
1	6	UB voltage dip end interrupt
1	7	UB voltage swell end interrupt
2	0	UC voltage dip end interrupt
2	1	UC voltage swell end interrupt
2	2	UA overvoltage interrupt
2	3	UA undervoltage interrupt
2	4	UB overvoltage interrupt
2	5	UB undervoltage interrupt
2	6	UC overvoltage interrupt
2	7	UC undervoltage interrupt
3	0	IA overcurrent interrupt
3	1	IA undercurrent interrupt
3	2	IB overcurrent interrupt
3	3	IB undercurrent interrupt
3	4	IC overcurrent interrupt
3	5	IC undercurrent interrupt
3	7	UART error interrupt
4	0	Sampled data active upload completion interrupt
4	1	Checksum error interrupt
4	3	Reference error interrupt
4	4	Bist error interrupt
4	5	UA zero-crossing interrupt
4	6	UB zero-crossing interrupt
4	7	UC zero-crossing interrupt
5	0	IA zero-crossing interrupt
5	1	IB zero-crossing interrupt
5	2	IC zero-crossing interrupt
5	6	Sampled data update interrupt
5	7	Instantaneous effective value update interrupt
6	0	Average effective value update interrupt
6	1	Instantaneous power update interrupt
6	2	Average power update interrupt
6	3	Power-down interrupt
6	4	High impedance state
6	7	Phase sequence detection error interrupt
7	1	Sampled data active upload SPI clock SPIMAS_SPCK
7	2	Sampled data active upload SPI data SPIMAS_SPDO
7	3	UA phase loss interrupt
7	4	UB phase loss interrupt
7	5	UC phase loss interrupt
7	6	Type 1 interrupt
7	7	Type 2 interrupt

8	0	Type 3 interrupt
8	1	Type 4 interrupt
8	2	Type 1 and Type 2 interrupts
8	3	Type 1 and Type 3 interrupts
8	4	Type 1 and Type 4 interrupts
8	5	Type 2 and Type 3 interrupts
8	6	Type 2 and Type 4 interrupts
8	7	Type 3 and Type 4 interrupts
9	0	Type 1, Type 2, and Type 3 interrupts
9	1	Type 1, Type 2, and Type 4 interrupts
9	2	Type 2, Type 3, and Type 4 interrupts
9	3	Type 1, Type 2, Type 3, and Type 4 interrupts
10	1	UA zero-crossing loss interrupt
10	2	UB zero-crossing loss interrupt
10	3	UC zero-crossing loss interrupt
10	4	IA zero-crossing loss interrupt
10	5	IB zero-crossing loss interrupt
10	6	IC zero-crossing loss interrupt
Others	Others	High impedance

Among them, when the IO port is not configured (i.e., all 0s or other undefined configurations), it outputs high impedance.

Type 1 interrupts: Current zero-crossing interrupt, voltage zero-crossing interrupt.

Type 2 interrupts: Sampled data refresh interrupt, instantaneous effective value refresh interrupt, average effective value refresh interrupt, instantaneous power value refresh interrupt, average power value refresh interrupt, sampled data active upload completion interrupt.

Type 3 interrupts: Current channel undercurrent interrupt, current channel overcurrent interrupt, voltage channel undervoltage interrupt, voltage channel overvoltage interrupt, voltage dip interrupt, voltage swell interrupt, voltage dip end interrupt, voltage swell end interrupt, UA phase loss interrupt, UB phase loss interrupt, UC phase loss interrupt, UA/ UB/ UC/ IA/ IB/ IC zero-crossing loss interrupt.

Type 4 interrupts: UART communication error interrupt, parameter self-check error interrupt, power-down interrupt, Reference error interrupt, RAM self-check error interrupt, phase sequence detection error interrupt.

11 Rogowski Coil Processing

When the external sampling circuit uses a Rogowski coil, the input current signal needs to be integrated to truly restore the sampled current signal.

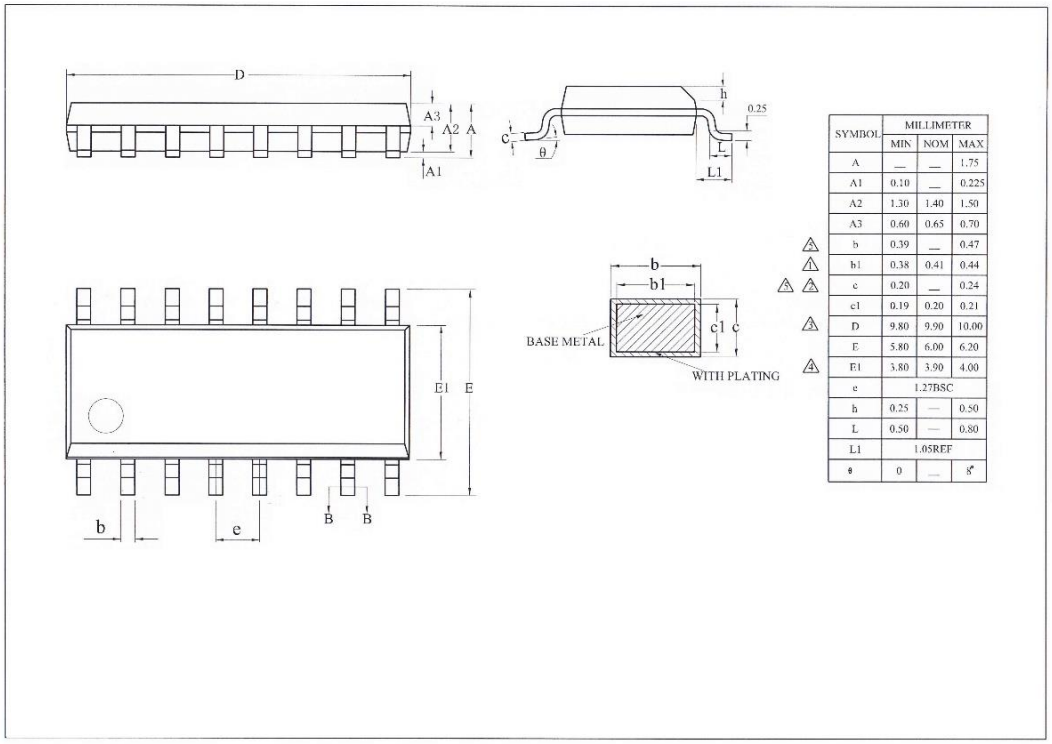
The relationship between the induced voltage of the Rogowski coil and the measured current is as follows:

$$U_{out} = M \frac{di}{dt}$$

M represents that the differential of the current with respect to time is proportional to the measured voltage. By adjusting the value of M (such as the number of turns and type of the coil), Uout can be controlled within a reasonable range (1% - 100% of the ADC range), and a more accurate result can be obtained. Integrating the output voltage again can obtain the current to be measured. At the same time, the output voltage of the Rogowski coil should have a 90° phase relationship with the voltage channel (the coil voltage output by the Rogowski coil lags the voltage channel by 90°).

12 Outline Dimensions

Figure13. Outline dimension for V9160



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.10	—	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
2 b	0.39	—	0.47
1 b1	0.38	0.41	0.44
2 5 c	0.20	—	0.24
c1	0.19	0.20	0.21
3 D	9.80	9.90	10.00
E	5.80	6.00	6.20
4 E1	3.80	3.90	4.00
e	1.27BSC		
h	0.25	—	0.50
L	0.50	—	0.80
L1	1.05REF		
θ	0	—	8°

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VANGO TECHNOLOGIES, INC.

Add:368 Liuhe Rd, North Bldg, Hi-Tech Park, Binjiang, Hangzhou, China

Tel:+86-571-88157065

Fax:+86-571-88157067

Email:service@vangotech.com

https://www.vangotech.com/en