VANGO TECHNOLOGIES, INC.

V9240

Datasheet

V9240 is a multifunction, ultralow power, single-phase power measurement IC with automatic baud rate adaption UART serial interface.

Function

- 3.3V power supply: 2.6V to 3.6V.
- Reference: 1.21V (typical drift 10ppm/°C).
- The typical power consumption of the chip during normal operation is approximately 1.7 mA (when the system clock is 6.5536 MHz).
- Supporting one current channel for active and reactive energy metering simultaneously
- Highly metering accurate:
  - Supporting the requirements of IEC 62053-21:2020/ IEC 62053-22:2020/ IEC 62053-23:2020 and IEC 62053-24:2020;
  - Less than 0.1% error for active/reactive energy metering over a dynamic range of 5000:1;
- Various measurements:
  - DC components of voltage and current signals;
  - Full-wave voltage/current average root mean square value
  - Full-wave active/reactive power average value
  - Fundamental wave reactive power average value
  - Line frequency;
  - Phase
- Supports waveform buffer
- Automatic baud rate adaption UART interface, supporting baud rate: 1200bps~19200bps
- No input crystal required.
- Current input: Shunt resistor or CT
- Operating temperature: -40~+105°C
- Storage temperature: -55~+150°C
- Package: SOP8

Contents

List of Tables

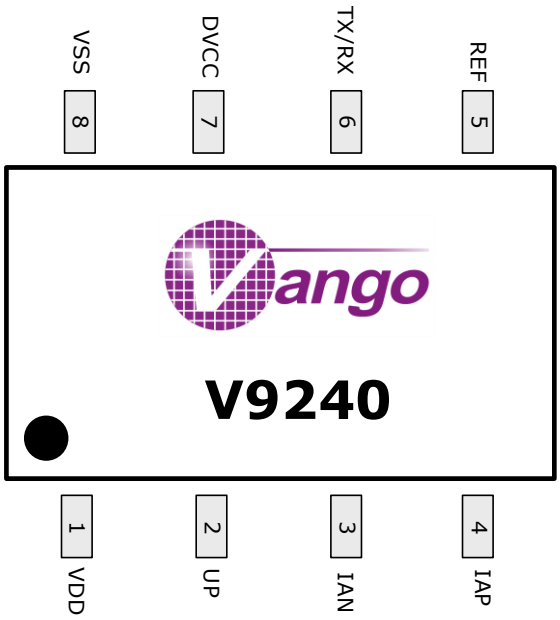
List of Figure

Revision History

Table1. Document Version History

Date	Revision	Description
2025.03.07	V1.0	Initial Version;
2025.05.06	V1.1	Supports waveform buffer;
2025.08.13	V1.2	Add instantaneous value; Add current phase measurement;
2025.12.09	V1.3	Add UART block reading operation;
2026.01.14	V1.4	Delete analog mode frequency measurement
2026.03.09	V1.5	Update electrical parameters and add VDD power-up rate.

1 Pin Description



1.1 Pin Description

Table2. Pin description

Pin No.	Name	Type	Description
1	VDD	Power	3.3 V power supply. This pin must be decoupled to a ≥0.1 μF capacitor.
2	UP	Input	Positive input pin for Voltage Channel Sampling.
3	IAN	Input	Negative input pin for current channel A sampling.
4	IAP	Input	Positive input pin for current channel A sampling.
5	VREF	Input/Output	On-chip reference voltage. This pin must be connected to a 1 μF capacitor, and then grounded.
6	TX/RX	Input/Output	UART TX/RX pin There is a pull-up resistor inside the chip, which is about 50 Kohm.
7	DVCC	Power	Digital power output. This pin must be decoupled to a 0.1 μF capacitor.
8	VSS	Ground	Ground

2 Parameters

Unless otherwise specified, the data are based on the test results of TA = 25 ℃, VDD = 3.3 V.

Parameter	Min.	Typ.	Max.	Unit	Remark
Phase Error Between Channels					
PF=0.8 Capacitive		±0.05		Degree	
PF=0.5 Inductive		±0.05		Degree	
Active Energy Metering Error		0.1		%	Dynamic Range 5000:1 @ 25°C Fundamental frequency deviation within ± 25%
Active Energy Metering Bandwidth		3.2		kHz	
Reactive Energy Metering Error		0.1		%	Dynamic Range 5000:1 @ 25°C Fundamental frequency deviation within ± 25%
Reactive Energy Metering Bandwidth		1.6		kHz	
VRMS Metering Error		1		%	Dynamic Range 2000:1 @ 25°C Fundamental frequency deviation within ± 25%
VRMS Metering Bandwidth		3.2		kHz	
IRMS Metering Error		1		%	Dynamic Range 5000:1 @ 25°C Fundamental frequency deviation within ± 25%
IRMS Metering Bandwidth		3.2		kHz	
Instantaneous value refresh time (t_{ivr})		10/20		ms	Effective value
		20/40		ms	Power value
Stabilization time of instantaneous value		3* t_{ivr}		ms	

Parameter	Min.	Typ.	Max.	Unit	Remark
Frequency Measurement					
Range	40		70	Hz	
Error		0.01		Hz	
Analog Input					
Maximum Signal Level			±200	mV	Peak value
ADC					
DC Offset			10	mV	
Resolution		23		Bit	Sign bit is included.
On-chip Reference					
Reference Error	-20		20	mV	@ 25˚C
Power Supply Rejection Ratio		92		dB	
Temperature Coefficient		10	30	ppm/ °C	
Output Voltage		1.208		V	
Power Supply					
VDD33	2.6	3.3	3.6	V	
Power-Down Detection Threshold	2.6	2.8	3.05	V	
Digital Power Supply (DVCC)					
Voltage		1.5		V	
CTI					
Internal high-frequency RC oscillator		6.5536		MHz	The deviation is within ±20%.
The frequency of the external input high-frequency clock		6.5536		MHz	
Logic Output TX					
Output High Voltage, V_{OH}	2.4		V_{DD}	V	
Output Low Voltage, V_{OL}	0		0.4	V	
Logic Input RX					
Input High Voltage, V_{INH}	2.0		V_{DD}+0.3	V	
Input Low Voltage, V_{INL}	-0.3		0.8	V	
Input Current, I_{IN}			1	μA	
Input Capacitance, C_{IN}			10	pF	

Parameter	Min.	Typ.	Max.	Unit	Remark
UART Baud Rate	1200		19200	bps	Automatic baud rate adaption

3 Absolute Maximum Ratings

Table3. Absolute maximum ratings

Parameter	Min.	Max.	Unit	Description
Analog Power Supply	-0.3	4	V	To ground.
Digital Power Supply	-0.3	+1.98	V	To ground.
Analog Input Voltage	-0.3	3.3	V	To ground.
Analog Input Voltage	-0.3	3.3	V	To ground.
VDD setup speed	3.3V/s	1V/μs		
Operating Temperature	-40	+105	˚C	
Storage Temperature	-55	+150	˚C	

4 Reset

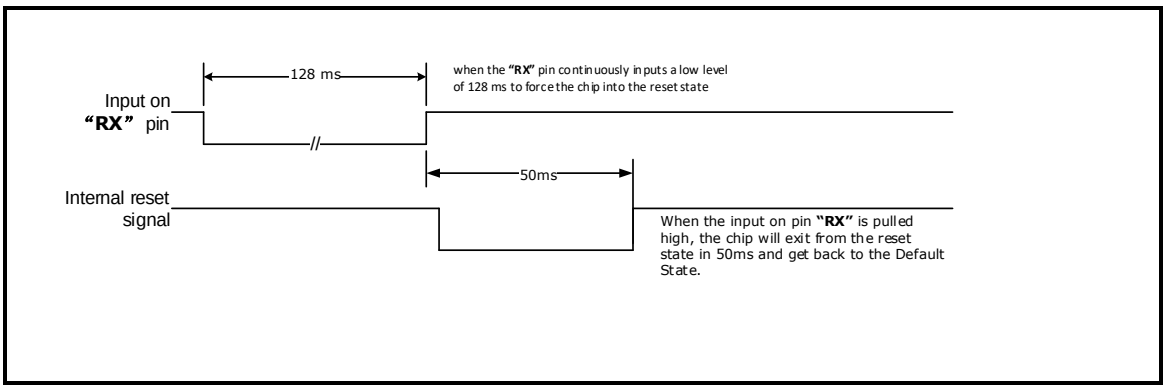
In the V9240, the chip will be reset to Default State when RX reset or software reset occurs.

4.1 RX Reset

When the "RX" pin is continuously input low for more than 128 ms, a reset occurs inside the chip. After that, the "RX" pin input high is greater than 50ms to complete the chip reset.

Note1: A RX reset operation needs to be performed after the chip is powered on.

Figure1. Timing for RX Reset of UART



4.2 Software Reset

Running the soft reset function can cause a reset inside the chip, and the reset is completed after 20 ms.

Ensure that the system communication is normal before executing the software reset function.

5 Main Power Supply

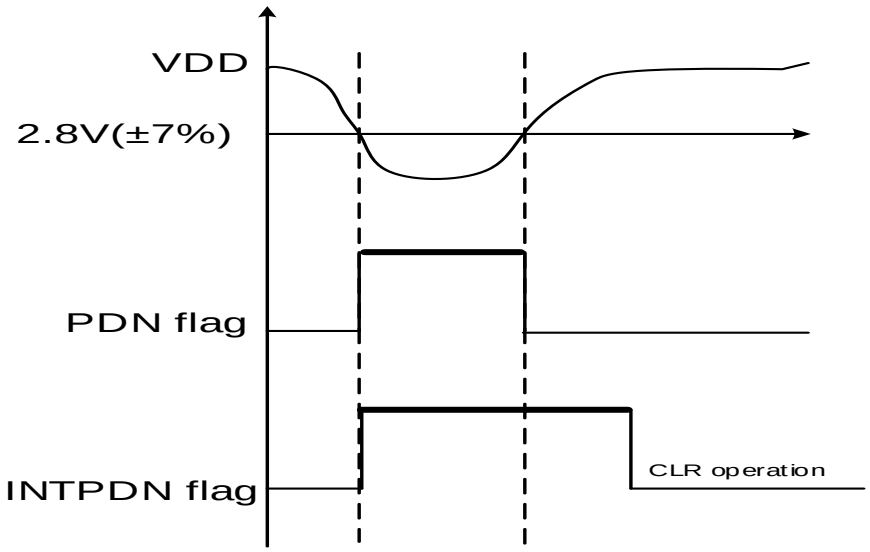
Features of V9240 main power system as below:

- 3.3V single main power supply, the voltage input range: 2.6~3.6V
- Supporting power down detection

5.1 Power Supply Monitoring Circuit

V9240 integrates an internal power-down detection circuit to supervise the voltage on pin “VDD” all the time. When the voltage on the pin “VDD” is lower than 2.8V (±7%), the power-down interrupt would be generated. The power supply monitoring circuit is always on work.

Figure2. Power-down monitoring



5.2 Digital Power Supply Circuit

The V9240 integrates an internal LDO (Digital Power Supply Circuit DVCCLDO). This circuit can stably supply power to the digital circuit even when the input power supply varies. This LDO is always operational.

The digital power supply circuit has a driving capacity of 35 mA. That is, when the load current on the digital circuit is less than 35 mA, the circuit can maintain a stable voltage output. When the load current is greater than 35 mA, the output voltage of the circuit will significantly drop as the load current increases.

6 Voltage Reference Circuit (Bandgap)

The voltage reference circuit (Bandgap) outputs a reference voltage of approximately 1.21V with a relatively small variation with temperature (a typical temperature drift of 10 ppm/˚C), providing a reference voltage for the chip. The Bandgap circuit is turned on by default.

7 UART

7.1 Overview

The V9240 supports communication with the master MCU as a slave via UART serial interface. The UART serial interface has features:

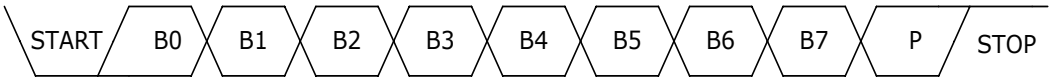
- Asynchronous, half-duplex communication;
- A 11-bit data byte, composed of 1-bit Start bit, 8-bit Data bits, 1-bit Parity bit (odd), and 1-bit Stop bit;
- Least significant bit (LSB) shifted in or out firstly when the chip receives or transmits a byte;
- Automatic baud rate adaption: support 1200bps~19200bps, and typical baud rates are 1200bps, 2400bps, 4800bps, 9600bps, and 19200bps.

When a reset event, such as RX reset or global software reset, occurs, the UART serial interface is reset.

7.2 Data Byte

The data byte received and transmitted via the UART serial interface of the V9240 is composed of 11 bits, including 1-bit Start bit (logic low), 8-bit Data bits, 1-bit odd Parity bit and 1-bit Stop bit (logic high), as shown in the following figure. When the V9240 receives or sends a data byte, the least significant bit always is shifted in or out firstly.

Figure3. Structure of an 11-Bit data byte (from LSB to MSB)



7.3 Communication Protocol

In read, write or broadcast communication, the master MCU needs a command frame that is composed of 8 data bytes to operate a 32-bit data in the V924X.

Figure4. Command Frame for Read/Write/Broadcast Operation

Head Byte	Control Byte	Address Byte	Data Byte 0	Data Byte 1	Data Byte 2	Data Byte 3	Check Byte

7.4 Communication Protocol

In read or write operation, when the V9240 receives the command frame from the master MCU, it will reply to the master MCU with a respond frame of different structures. In broadcast communication, the V9240 will not reply to the master MCU to avoid communication conflict.

The following figure depicts the timing of UART communication.

Figure5. Timing of UART Communication

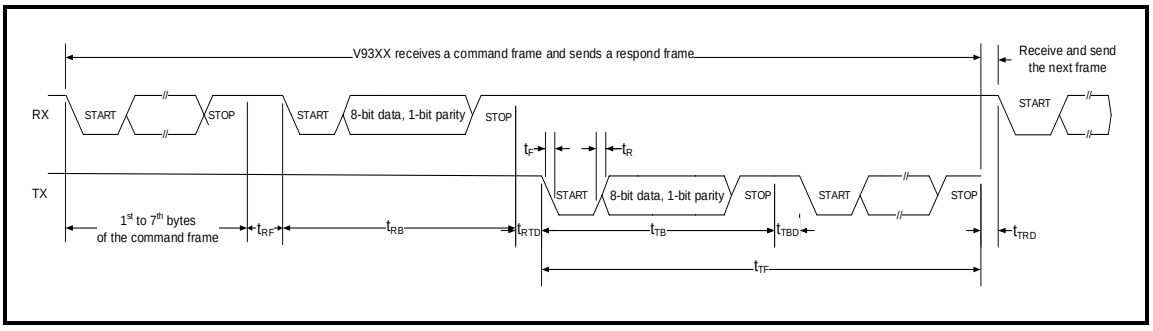


Table4. UART Communication Timing Parameters

Parameter	Description
t_{RB}	Time to receive a data byte on pin RX. $t_{RB}=\frac{11}{baudrate}$ where, *baudrate* is the actual baud rate.
t_{RF}	The maximum time between two bytes when receiving a command frame on pin **"RX"** $t_{RF}=\frac{16}{baudrate}$ Where, *baudrate* is the actual baud rate. *Baudrate=4800bps*， t_{RF}=3.33ms. After a timeout event, the UART serial interface is idle and waits for the next command frame.
t_{RTD}	The delay between command frame reception on pin RX and respond frame transmission on pin TX. 2 ms≤t_{RTD}≤20 ms Please note no respond frame will be transmitted in broadcast communication, and at least 2ms delay is recommended between two continuous command frames for broadcast communications.
t_{TF}	Time to transmit a respond frame in read or write operation, depending on the structure of the frame.

Parameter	Description
t_{TB}	Time to transmit a data byte. $t_{TB}=\frac{11}{baudrate}$ where *baudrate* is the actual baud rate.
T_{TBD}	Delay between two continuous data bytes in a respond frame. $0ms \le t_{TBD} \le 20ms$
t_{TRD}	The delay between respond frame transmission on pin TX and the next command frame reception on pin RX. More than 2ms is recommended.
t_R	Rise time of RX and TX, about 300ns.
t_F	Fall time of RX and TX, about 300ns.

7.5 Broadcast Communication

- Supports writing to consecutive registers of 1 address
- V9240 no response

Batch writes to register for multiple V9240 devices via broadcast writing by master MCU. This mode can save the parameter configurable time. The figure below is the command frame for broadcast writing operation.

Figure6. command frame for broadcast writing operation

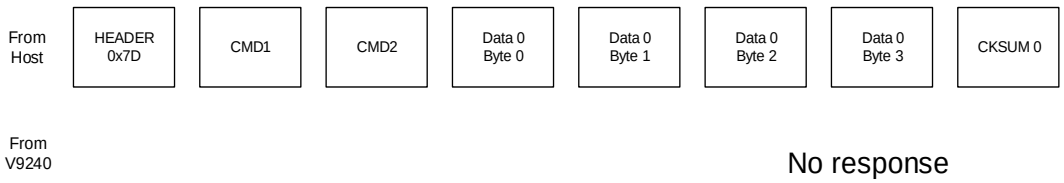


Table5. Structure of Data Byte (B7:B0) From Master MCU to V9240 on Broadcast Operation

Order	Byte	B7	B6	B5	B4	B3	B2	B1	B0
1	HEADER	0	1	1	1	1	1	0	1
2	CMD1	To select the data length on broadcast writing (N) 0: write 1 data of 32 bits 1: write 2 data of 32 bits … 15: write 16 data of 32 bits				X*	X*	0	0
3	CMD2	Start address for broadcast writing operation (D_0)							
4	Data 0	**"Bit[7:0]"** of the target data write into register (address D_0)							

Order	Byte	B7	B6	B5	B4	B3	B2	B1	B0
	Byte 0								
5	Data 0 Byte 1	**"Bit[15:8]"** of the target data write into register (address D_0)							
6	Data 0 Byte 2	**"Bit[23:16]"** of the target data write into register (address D_0)							
7	Data 0 Byte 3	**"Bit[31:24]"** of the target data write into register (address D_0)							
8	CKSUM 0	Checksum 0. Add the above 4 target data bytes (Data 0 Byte 0~3), CMD1, and CMD2, invert the sum, and then add it to **"0x33"** to obtain the checksum. The equation is as below: CKSUM 0 = 0x33 + ~(CMD1 + CMD2 + Data 0 Byte 0 + Data 0 Byte 1 + Data 0 Byte 2 + Data 0 Byte 3)							

7.6 Read Operation

- Supports writing to consecutive registers of 1 address
- V9240 would be responded

Figure7. Communication protocol for read operation

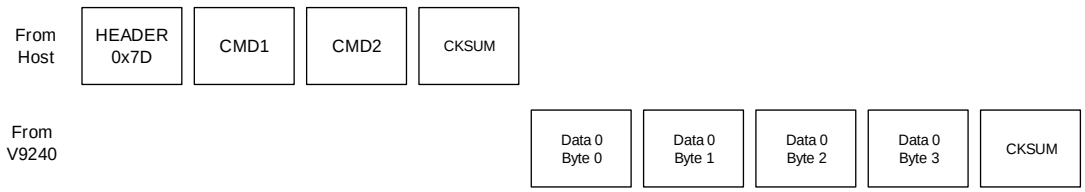


Table6. Structure of Data Byte (B7:B0) From Master MCU to V9240 on Read Operation

Order	Byte	B7	B6	B5	B4	B3	B2	B1	B0
1	HEADER	0	1	1	1	1	1	0	1
2	CMD1	To select the data length on read operation 0: write 1 data of 32 bits 1: write 2 data of 32 bits … 15: write 16 data of 32 bits				0	0	0	1
3	CMD2	Start address for read operation (D_0)							
4	CKSUM	Checksum. Add the above CMD1 and CMD2, invert the sum, and then							

Order	Byte	B7	B6	B5	B4	B3	B2	B1	B0
		add it to **"0x33"** to obtain the checksum. The equation is as below: CKSUM = 0x33 + ~(CMD1 + CMD2)							

Table7. Structure of Data Byte (B7:B0) From V9240 to Master MCU on read Operation

Order	Byte	B7	B6	B5	B4	B3	B2	B1	B0
1	Data 0 Byte 0	**"Bit[7:0]"** of the target data read from register (address D_0)							
2	Data 0 Byte 1	**"Bit[15:8]"** of the target data read from register (address D_0)							
3	Data 0 Byte 2	**"Bit[23:16]"** of the target data read from register (address D_0)							
4	Data 0 Byte 3	**"Bit[31:24]"** of the target data read from register (address D_0)							
5	CKSUM	Checksum. Add the above 4 target data bytes (Data 0~N Byte 0~3, comes from V9240), CMD1, and CMD2(comes from MCU), invert the sum, and then add it to **"0x33"** to obtain the checksum. The equation is as below: CKSUM = 0x33 + ~(CMD1 + CMD2 + Data 0 Byte 0 + Data 0 Byte 1 + Data 0 Byte 2 + Data 0 Byte 3)							
If the length N equals to 0 on read operation, V9240 only sends 5 bytes of response frame to master MCU.									

7.7 Write Operation

- Supports writing to consecutive registers of 1 address
- V9240 would be responded

Figure8. Communication protocol for write operation

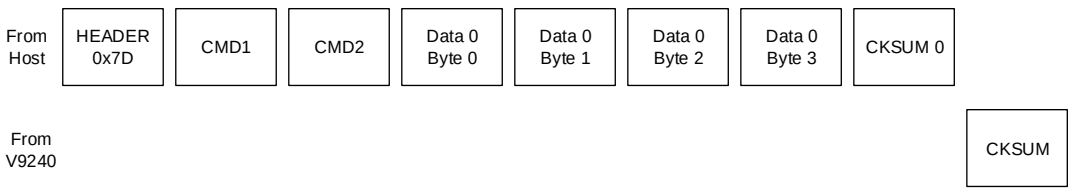


Table8. Structure of Data Byte (B7:B0) From Master MCU to V9240 on Write Operation

Order	Byte	B7	B6	B5	B4	B3	B2	B1	B0
1	HEADER	0	1	1	1	1	1	0	1

Order	Byte	B7	B6	B5	B4	B3	B2	B1	B0
2	CMD1	To select the data length on write operation 0: write 1 data of 32 bits 1: write 2 data of 32 bits … 15: write 16 data of 32 bits				0	0	1	0
3	CMD2	Start address for write operation (D_0)							
4	Data 0 Byte 0	**"Bit[7:0]"** of the target data write into register (address D_0)							
5	Data 0 Byte 1	**"Bit[15:8]"** of the target data write into register (address D_0)							
6	Data 0 Byte 2	**"Bit[23:16]"** of the target data write into register (address D_0)							
7	Data 0 Byte 3	**"Bit[31:24]"** of the target data write into register (address D_0)							
8	CKSUM 0	Checksum 0. Add the above 4 target data bytes (Data 0 Byte 0~3), CMD1, and CMD2, invert the sum, and then add it to **"0x33"** to obtain the checksum. The equation is as below: CKSUM 0 = 0x33 + ~(CMD1 + CMD2 + Data 0 Byte 0 + Data 0 Byte 1 + Data 0 Byte 2 + Data 0 Byte 3)							

Table9. Structure of Data Byte (B7:B0) From V9240 to Master MCU on Write Operation

Order	Byte	B7	B6	B5	B4	B3	B2	B1	B0
1	CKSUM	Checksum (comes from V9240). Used to verify that the write operation was successful. If CKSUM and CKSUM N (comes from master MCU) was equal, this time write operation was succeeded. If CKSUM and CKSUM N (comes from master MCU) was not equal, this time write operation was failed.							

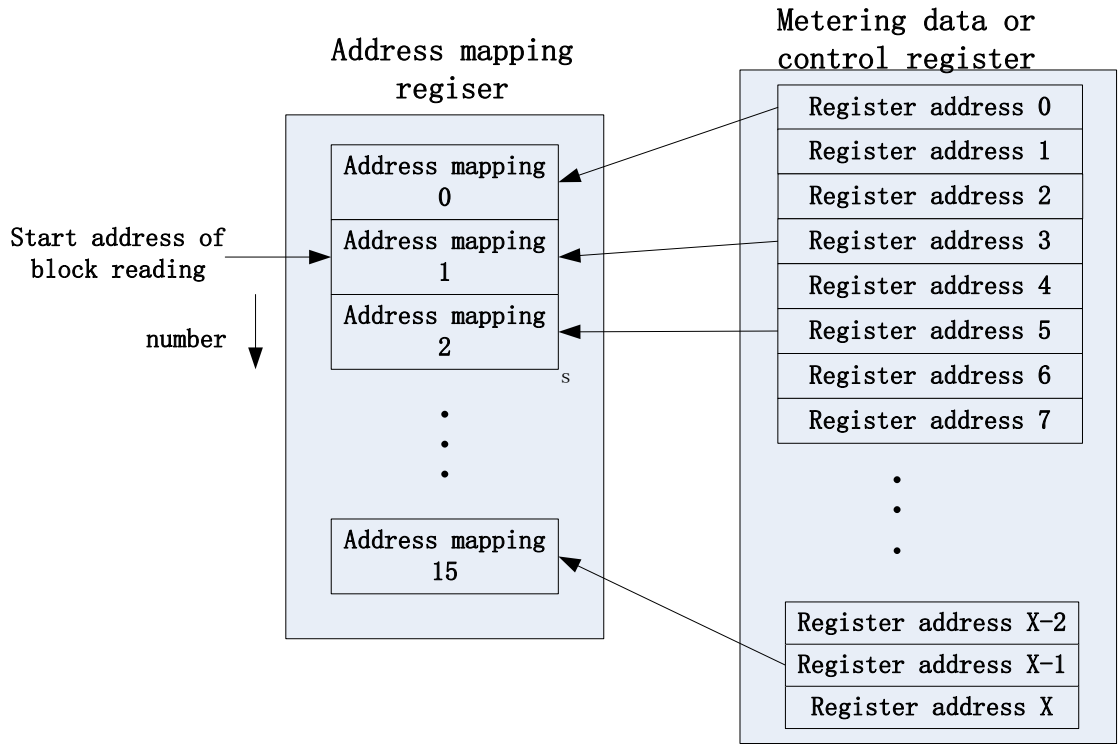
7.8 Block Reading Operation

In order to facilitate the user to read the required data at one time and improve communication efficiency, V9240 provides address mapping function: The user maps the address of the data item that needs to be continuously operated to the address register, so that the user can perform the block read operation on the data in different places by operating the address register.

Up to 16 data register addresses can be mapped.

The block reading operation can start from any position in the mapped address register. If the address plus the number of reads exceeds the buffer size, the read is started from the beginning. For example, 10 data are read from the 13th mapping address, and after the 16th address, the data of 6 addresses is continuously read from the first one.

Figure9. address mapping for block reading



Feature:

- Support block reading operation by address mapping from 1~16 addresses that are not consecutive.
- V9240 would be responded.

Figure10. Communication protocol for block reading operation

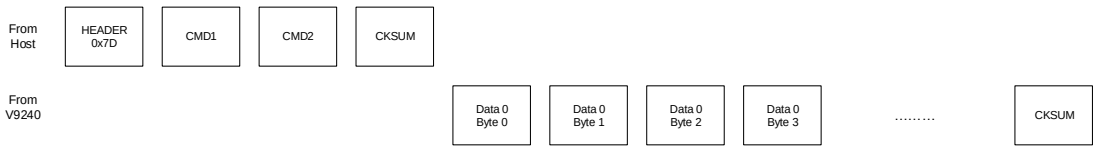


Table10. Structure of Data Byte (B7:B0) From Master MCU to V93XX on block reading Operation

Order	Byte	B7	B6	B5	B4	B3	B2	B1	B0
1	HEADER	0	1	1	1	1	1	0	1
2	CMD1	To select the data length on				0	0	1	1

Order	Byte	B7	B6	B5	B4	B3	B2	B1	B0
		block reading operation 0: write 1 data of 32 bits 1: write 2 data of 32 bits … 15: write 16 data of 32 bits							
3	CMD2	X*	X*	X*	X*	To select the start address on block reading operation 16 block reading addresses are set by 4 registers of SYS_BLKX_ADDR For example: if N=4 (length is 5) and M=4(setting start address), it would start to read address from the bit7~0 of SYS_BLK1_ADDR register in the ADDR4. The 5 register addresses for block reading operation as below: 1: stored address ADDR4 in the Bit7~0 of the SYS_BLK1_ADD 2: stored address ADDR5 in the Bit15~8 of the SYS_BLK1_ADD 3: stored address ADDR6 in the Bit23~16 of the SYS_BLK1_ADD 4: stored address ADDR7 in the Bit31~24 of the SYS_BLK1_ADD 5: stored address ADDR8 in the Bit7~0 of the SYS_BLK2_ADD			
4	CKSUM	Checksum. Add the above CMD1 and CMD2, invert the sum, and then add it to **"0x33"** to obtain the checksum. The equation is as below: CKSUM = 0x33 + ~ (CMD1 + CMD2)							

Table11. Structure of Data Byte (B7:B0) From V9240 to Master MCU on block reading Operation

Order	Byte	B7	B6	B5	B4	B3	B2	B1	B0
1	Data 0 Byte 0	**"Bit[7:0]"** of the target data read from register (address $ADDR_M$)							
2	Data 0 Byte 1	**"Bit[15:8]"** of the target data read from register (address $ADDR_M$)							
3	Data 0 Byte 2	**"Bit[23:16]"** of the target data read from register (address $ADDR_M$)							
4	Data 0	**"Bit[31:24]"** of the target data read from register (address $ADDR_M$)							

Order	Byte	B7	B6	B5	B4	B3	B2	B1	B0
	Byte 3								
…	…	…							
4xN+1	Data N Byte 0	**"Bit[7:0]"** of the target data read from register (address $ADDR_{M+N}$)							
4xN+2	Data N Byte 1	**"Bit[15:8]"** of the target data read from register (address $ADDR_{M+N}$)							
4xN+3	Data N Byte 2	**"Bit[23:16]"** of the target data read from register (address $ADDR_{M+N}$)							
4xN+4	Data N Byte 3	**"Bit[31:24]"** of the target data read from register (address $ADDR_{M+N}$)							
4xN+5	CKSUM	Checksum. Add the above 4×(N+1) target data bytes (Data 0~N Byte 0~3, comes from V9240), CMD1, and CMD2(comes from MCU), invert the sum, and then add it to **"0x33"** to obtain the checksum. The equation is as below: CKSUM = 0x33 + ~ (CMD1 + CMD2 + Data 0 Byte 0 + Data 0 Byte 1 + Data 0 Byte 2 + Data 0 Byte 3 + ….. + Data N Byte 0 + Data N Byte 1 + Data N Byte 2 + Data N Byte 3)							
If the length N equals to 0 on read operation, V9240 only sends 5 bytes of response frame to master MCU.									

8 Measurement Data Processing Unit

8.1 Overview

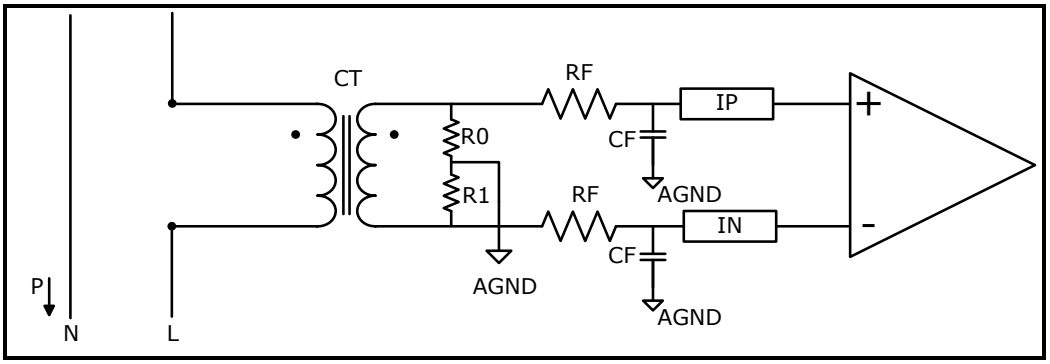
The measurement data processing unit is mainly used to calculate the full-wave active power, either the full-wave or fundamental wave reactive power (select one of the two), full-wave apparent power, and full-wave effective value, also provides waveform storage functions.

8.2 Analog Inputs

The V9240 supports 1 analog input of current channel.

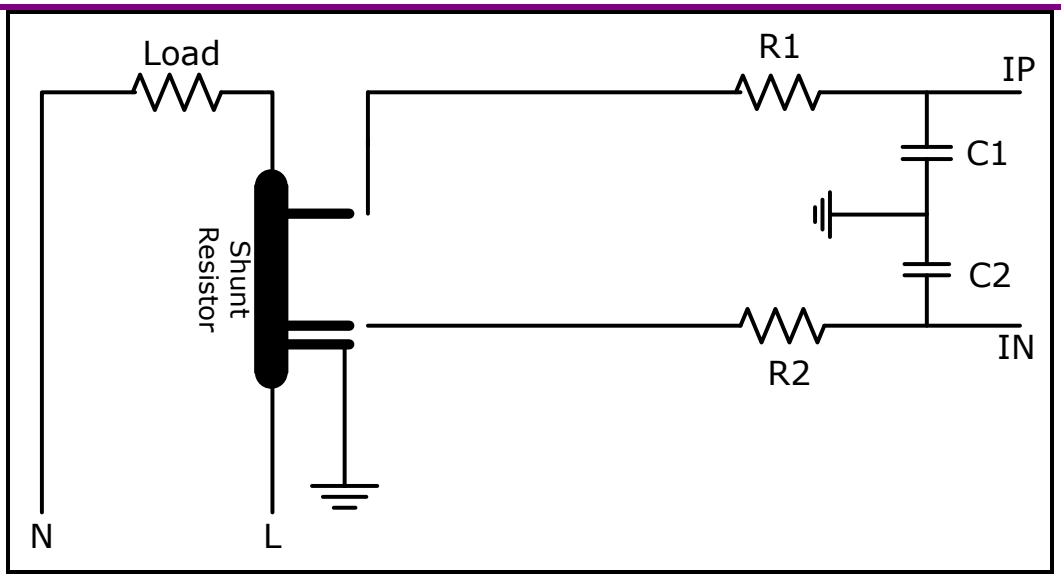
For the current channel, a current transformer (CT) or shunt resistor can be used for analog inputs. The double-ended full differential input is adopted. The wiring is shown as below. The shunt resistor can also be used for the current input with AGND grounded.

Figure11. CT for Current Analog Input



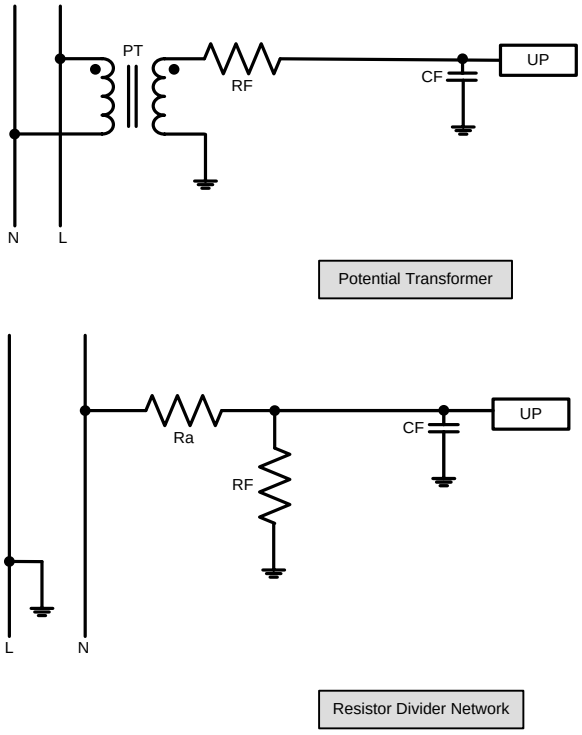
Manganese copper resistance can also be used to shunt the network input current, and AGND can be used for grounding.

Figure12. Shunt Resistor Network for Current Analog Input



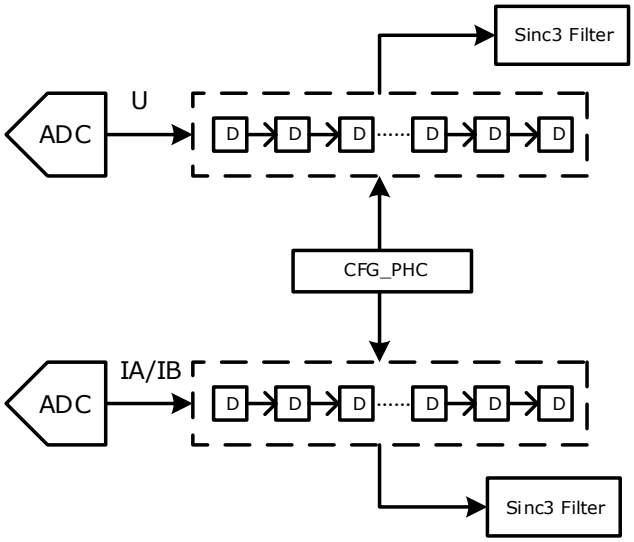
The V9240 supports the input of voltage signals in the form of a voltage transformer or resistive voltage division. It adopts the pseudo-differential input mode, with UN (internally grounded in the chip) as the negative terminal and UP as the positive terminal.

Figure13. Analog Input of Voltage



8.3 Phase Compensation

Figure14. Phase Compensation Schematics



The principle of angular error correction is to introduce a delay chain of fixed length in the voltage and current channels. According to the phase lead or lag relationship between the voltage and the current, either the voltage or the current is selected to be delayed. Therefore, the minimum resolution of the angular error correction is the phase difference between two adjacent units on the delay chain, and the total angular error correction angle is the product of the minimum resolution and the length of the delay chain.

The angular error correction function is turned off by default. Users can enable the angular error correction function through configuration.

In the V9240, when the sampling frequency (f_{smpl}) of the angular error correction circuit is 6.5536 MHz, the resolution of the angular error correction is 0.0055°/lsb, and the total correction amount is ±4.21875°. The angular error resolution and correction range under different f_{smpl} values

Table12. *f_{smpl}* Determines Phase Compensation Resolution and Correction Range

DSP_MODE	f_{smpl}	calibration_accuracy (degree)	Calibration_range (degree)
0x00	6.5536MHz	0.005493164	±4.21875

The angular error correction value of IA, phc_ia = the angle to be corrected / calibration_accuracy.

The angular error correction value of IB, phc_ib = the angle to be corrected / calibration_accuracy.

The angular error correction value of IA and the angular error correction value of IB are combined in the form of two's complement and then written into the angular error correction register.

8.4 RMS Calculation and Calibration

Users can set the ratio difference correction value of the effective value of the voltage/current in the effective value ratio difference register. The effective value data after the ratio difference correction is stored in the voltage/current effective value register. This data will be averaged, and the averaged value is stored in the voltage/current effective value average register. The average effective values of 10 cycles or 12 cycles are provided for voltage flicker detection. All the above-mentioned registers store 32-bit two's complement data.

8.5 Active Power Calculation and Calibration

The original waveform signals of the current and the voltage are multiplied. The product is passed through a low-pass filter to filter out the ripples caused by harmonics and noise, obtaining 32-bit active power data. After this data undergoes offset correction, it is then subjected to ratio difference correction.

The active power data after ratio difference correction will be averaged and stored in the power average value register.

8.6 Reactive Power and Calibration

The original current waveform signal is filtered by a Hilbert filter to adjust its phase by 90°, and then multiplied by the original voltage waveform signal. The product is passed through a low - pass filter to filter out the ripples caused by harmonics and noise, resulting in 32 - bit reactive power data.

The reactive power data can be sourced from either full - wave data or fundamental - wave data (choose one of the two).

The reactive power data after ratio difference correction will be averaged and stored in the power average value register.

8.7 Apparent Power Calculation

The V9240 supports apparent power calculation. There are two calculation methods for apparent power: calculation by RMS value and calculation by power value.

In the V9240, the instantaneous current and voltage RMS are multiplied to acquire the apparent power, as described in the following equation:

$$S = Irms \times Urms \qquad \text{Equation 1}$$

Where, *S* represents apparent power;

Irms and *Urms* are the average current and voltage RMS.

In the V93XX, the apparent power is obtained by square root of the sum of the square of the instantaneous active power and the square of the instantaneous reactive power, as described in the following equation:

$$S = \sqrt{P^2 + Q^2}$$ Equation 2

Where, S is the apparent power;

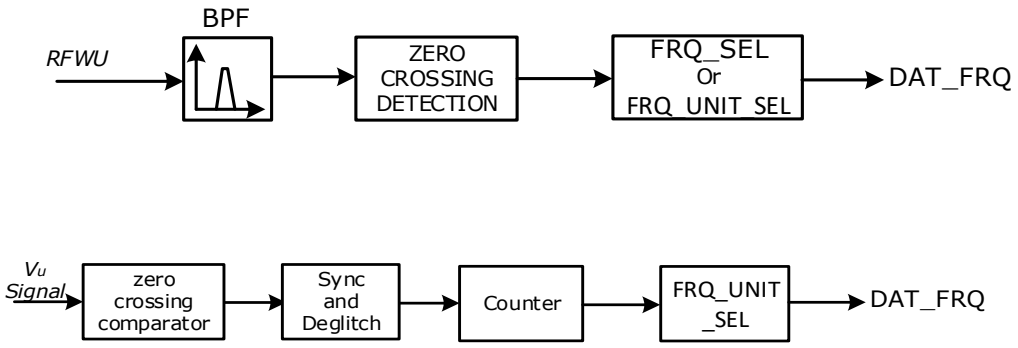
P is the instantaneous active power value;

Q is the instantaneous reactive power value.

The content of the apparent power registers are in the form of 32-bit 2'-complement. When RX reset, global software reset occurs, these registers are reset to their default states.

8.8 Frequency measurement

Figure15. Frequency measurement



The V9240 supports line voltage frequency measurement with a range of 35Hz to 75Hz, and it supports frequency measurement in digital mode.

The principle of frequency measurement in digital mode involves filtering the original fundamental voltage waveform through a band-pass filter with a center frequency of 50Hz (which provides 25dB attenuation at 150Hz). The output signal is then subjected to zero-crossing detection, and the frequency measurement result is output after averaging over 16 signal periods.

Based on the line voltage frequency, the user can directly calculate the signal frequency:

$$f = wave\_cnt * freq\_const / DSP\_DAT\_FRQ$$

Where,

f: Signal frequency, Hz;

wave_cnt: number of cycles;

freq_const: frequency constant, Hz;

8.9 Phase measurement

V9240 supports voltage phase and current phase measurement. The operation principle is, write 1 to start phase measurement. It starts counting at a certain frequency, until zero-crossing events happened, it stops counting. This counting value will write into the voltage phase register or current phase register. It also records two sampling values before and after the zero-crossing. User can obtain better accurate phase value by interpolation method.

8.10 Waveform Buffer

After the waveform buffer function is enabled, the waveform data is stored in the RAM, supporting both the single-channel waveform data storage mode and the dual-channel waveform data simultaneous storage mode. Configure the relevant settings for waveform buffer, as well as select the enable and end conditions. The number of points in the waveform cache can be configured as 32 points, 64 points, or 128 points. After the waveform buffer configuration is completed, users can check whether the waveform buffer is finished through the system interrupt register. Once completed, users can obtain the waveform cached data by repeatedly reading the waveform data register, and can read up to 309 data items each time.

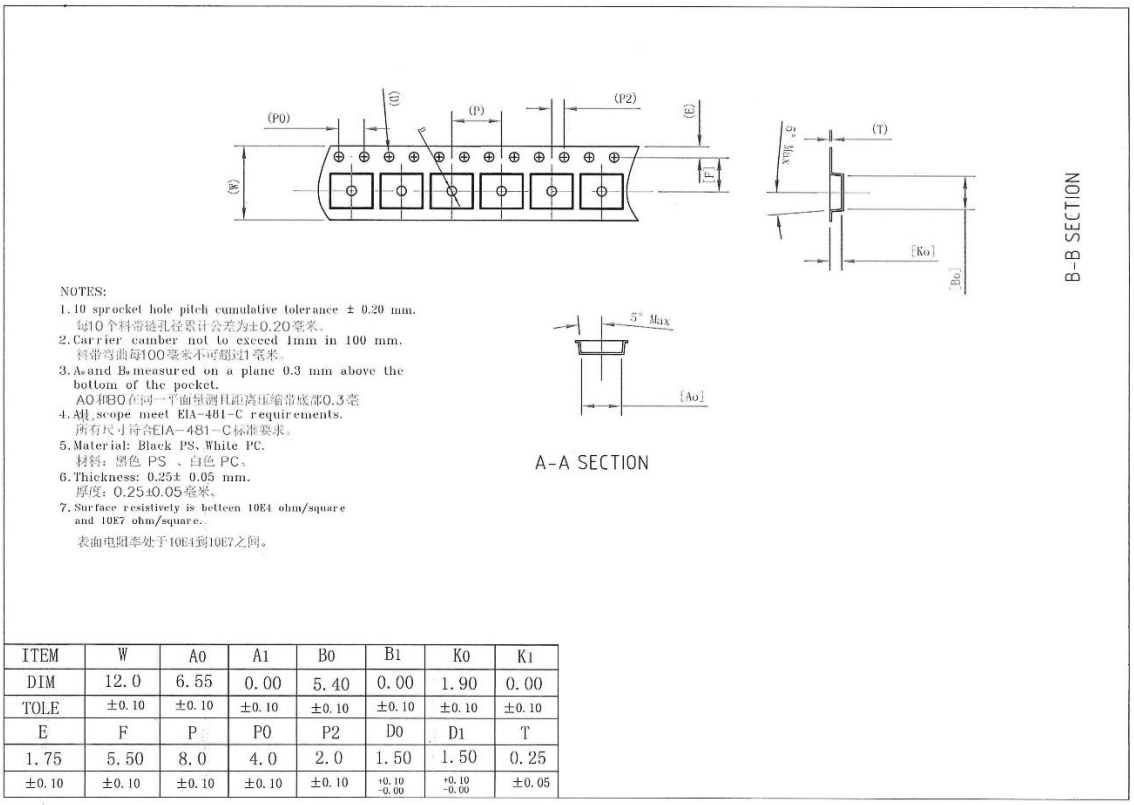
Table13. waveform buffer data format

channel	High 16Bit	Low 16Bit
IA	$IADATA_{2n+1}$	$IADATA_{2n}$
U	$UDATA_{2n+1}$	$UDATA_{2n}$
IA+U	$IADATA_{n}$	$UDATA_{n}$

Where the range of n is 0~308

9 Packaging Information

Figure16. Taping Information of V9240



NOTES:
1. 10 sprocket hole pitch cumulative tolerance ± 0.20 mm.
   每10个料带链孔径累计公差为±0.20毫米。
2. Carrier camber not to exceed 1mm in 100 mm.
   料带弯曲每100毫米不可超过1毫米。
3. A_0 and B_0 measured on a plane 0.3 mm above the bottom of the pocket.
   A0和B0在同一平面量测且距离压缩带底部0.3毫
4. All scope meet EIA-481-C requirements.
   所有尺寸符合EIA-481-C标准要求。
5. Material: Black PS, White PC.
   材料：黑色 PS 、白色 PC。
6. Thickness: 0.25± 0.05 mm.
   厚度：0.25±0.05毫米。
7. Surface resistivety is betteen 10E4 ohm/square and 10E7 ohm/square.
   表面电阻率处于10E4到10E7之间。

ITEM	W	A0	A1	B0	B1	K0	K1
DIM	12.0	6.55	0.00	5.40	0.00	1.90	0.00
TOLE	±0.10	±0.10	±0.10	±0.10	±0.10	±0.10	±0.10
E	F	P	P0	P2	D0	D1	T
1.75	5.50	8.0	4.0	2.0	1.50	1.50	0.25
±0.10	±0.10	±0.10	±0.10	±0.10	+0.10 -0.00	+0.10 -0.00	±0.05

10 Reflow soldering process

All Wango chips provided to customers are lead-free RoHS compliant products.

The reflow soldering process recommended in this article is a lead-free reflow soldering process, which is suitable for the pure lead-free process of lead-free solder paste. If customers need to use lead solder paste, please contact the smart chip FAE connect.

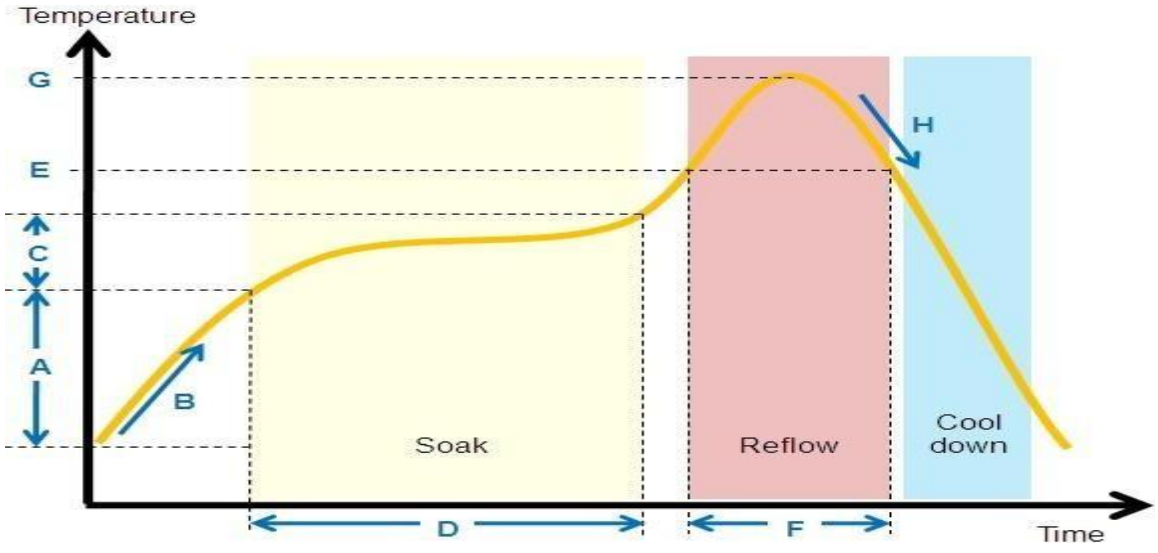
See Table14 for lead-free reflow profile conditions. This table is for reference only.

Table14. Reflow profile conditions

	QTI typical SMT reflow profile conditions(for reference only)	
	Step	**Reflow condition**
Environment	N2 purge reflow usage (yes/no)	Yes, N2 purge used
	If yes, O2 ppm level	O2 < 1500 ppm
A	Preheat ramp up temperature range	25°C -> 150°C
B	Preheat ramp up rate	1.5~2.5 °C /sec
C	Soak temperature range	150°C -> 190°C
D	Soak time	80~110 sec
E	Liquidus temperature	217°C
F	Time above liquidus	3-6 sec
G	Peak temperature	255-265°C
H	Cool down temperature rate	≤4°C /sec

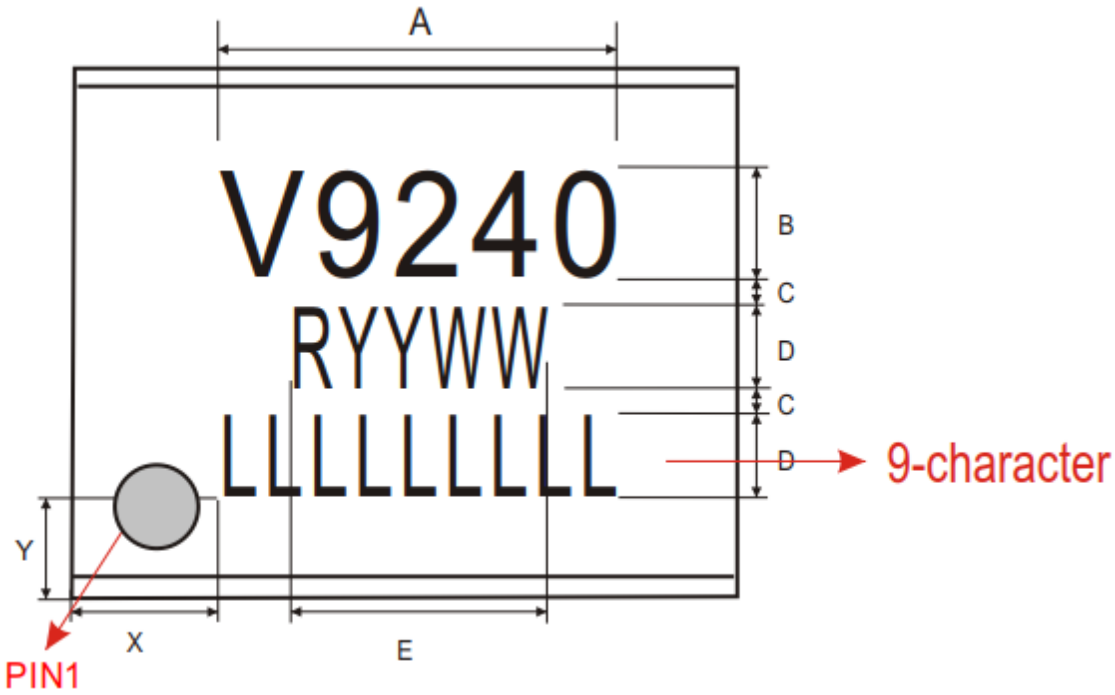
The figure below shows a typical lead-free reflow mode.

Figure17. A typical lead-free reflow mode



11 Part Marking

Figure18. V9240 marking



Among them:

"V9240" is the chip model;

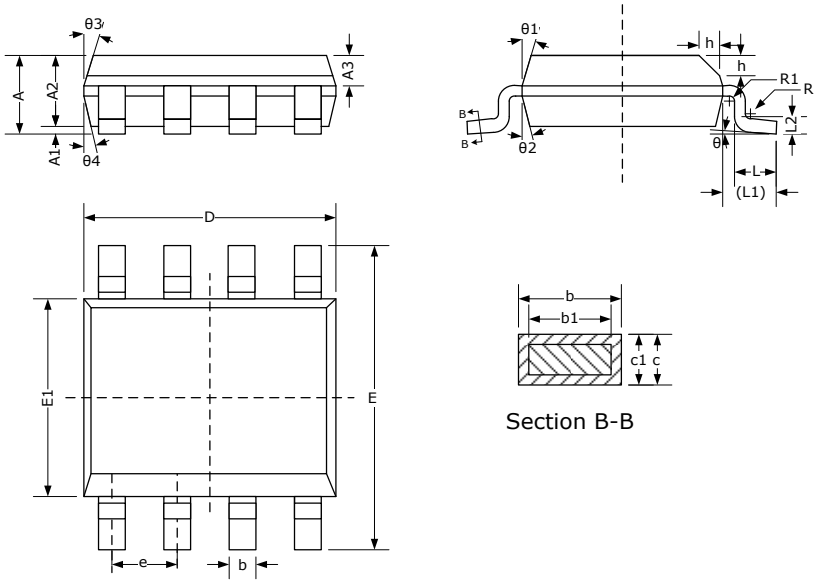
"R" is the version number;

"YYWW" represents the actual year-week number; the year-week number is the same for the same work order;

"LLLLLLLLL" represents the printing batch number, which is specified in the customer order;

12 Outline Dimensions

Figure19. Outline dimension for V9240



Dimensions (Unit: mm)

Symbol	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.05	0.15	0.25
A2	1.25	1.40	1.65
A3	0.50	0.60	0.70
b	0.38	-	0.51
b1	0.37	0.42	0.47
c	0.17	-	0.25
c1	0.17	0.20	0.23
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
L	0.45	0.60	0.80
L1	1.04REF		
L2	0.25BSC		
R	0.07	-	-
R1	0.07	-	-
h	0.30	0.40	0.50
θ	0°	-	8°
θ1	15°	17°	19°
θ2	11°	13°	15°
θ3	15°	17°	19°
θ4	11°	13°	15°

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