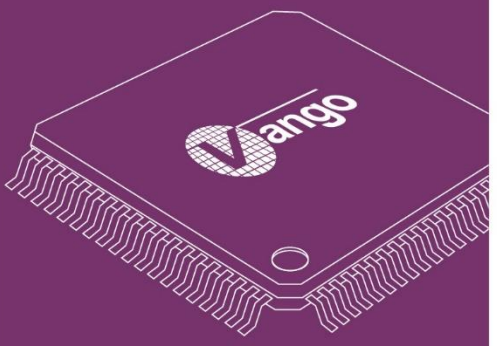
VANGO TECHNOLOGIES, INC.

V32G410x

Datasheet



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Revision History

Table1. Document Version History

Date	Revision	Description
2022.08.19	V1.0	Initial Version
2023.01.09	V1.4	Modify package
2023.02.17	V1.5	Add V32G410RGT7
2023.04.21	V1.6	Delete GPIO open drain output and input pull-up mode I2C delete slave mode I2S delete slave mode and data extension Mode Remove LSE stable signal
2023.05.08	V1.7	CAN delete CLKOUT function
2023.09.12	V1.8	Modify stop mode wakeup timings
2023.11.10	V1.9	Correct electrical parameters
2024.01.30	V1.10	Modify accuracy of the HSI oscillator Delete V32G410RGT7
2024.06.19	V1.11	Modify the external reset capacitor to 1uF
2024.08.21	V1.12	Modify the maximum working temperature is 85 °C.
2025.01.07	V1.13	Add V32G410DUU6
2025.05.20	V1.14	Correct the data of QFN48 package

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(C) Environmental applications;
(D) Weapons or other military equipment systems, as well as nuclear facility control system applications;
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ARM®-based 32-bit Cortex®-M4F MCU + FPU, with 4096 Kbyte Internal Flash Memory, 17 Timers, 2 ADCs, 16 Communication Interfaces

Feature

- Core: ARM®32-bit Cortex®-M4F CPU with FPU
  - 200 MHz maximum frequency, with a Memory Protection Unit (MPU), single cycle multiplication and hardware division
  - Floating Point Unit (FPU), DSP instructions
- Memory
  - Up to 4096 Kbytes of Flash instruction/data memory
  - SPIM interface: Extra interfacing up to 16 Mbytes of external SPI Flash
  - Up to 1536 Kbytes of SRAM
- Clock, Reset, and Power Management
  - 2.6 V ~ 3.6 V application supply and I/Os
  - POR/ PDR, and programmable voltage detector (PVD)
  - 4 to 25 MHz crystal oscillator
  - Internal 48 MHz factory-trimmed RC
  - Internal 40 KHz RC oscillator
  - 32 KHz oscillator with calibration
- Low Power Consumption
  - Sleep and Stop modes
- 2 12-bit A/D converters, 0.5 μs converting time (Up to 16 channels)
  - Conversion range: 0 V to 3.6 V
  - Triple sample and hold capability
  - Temparature sensor
- DMA: 14 channel DMA controller
  - Peripherals supported: timers, ADC, I2S, SPI, I2C, and USART
- Debug Mode
  - Serial Wire Debug (SWD) and JTAG interface
- Up to 86 Fast I/O Interfaces
  - 86 multifunctional and bidirectional I/Os, up to 79 GPIOs mappable to 16 external interrupt vectors and almost 5 V-tolerant
  - All fast I/Os, control registers accessable with f_{AHB} speed
- Up to 17 Timers
  - Up to 8 x 16-bit timers + 2 x 32-bit timers; each with 4 input capture/ output comparison/PWM or pulse counter and quadrature (incremental) encoder input.
  - Up to 2 x 16-bit motor control PWM advanced timers with dead-time generator and emergency stop

  - 2 x Watchdog timers (independent and window)
  - SysTick timer: 24-bit downcounter
  - 2 x 16-bit basic timers
- Up to 16 Communication Interfaces
  - Up to 3 x I2C interfaces (SMBus/ PMBus)
  - Up to 8 x USARTs (ISO7816 interface, LIN, IrDA capability, and modem control)
  - Up to 4 x SPIs (36 Mbit/s), all with I2S interface multiplexed
  - CAN interface (2.0A and 2.0B)
- CRC Calculation Unit
- Packaging
  - QFN48 7x7 mm (V32G410CGU7)
  - QFN60 6x6 mm (V32G410DUU6)
  - LQFP100 14x14 mm (V32G410VUT7)
  - LQFP100 14x14 mm (V32G410VGT7)

1 Introduction

This article gives the function information of the V32G410x series products.

The introduction of the V32G410x series must be read together with the V32G410x series product manual and the V32G410x series reference manual. About internal flash storage Information about programming, erasing and protection of the device can also be obtained in the V32G410x series reference manual. For information about the Cortex®-M4 core, please refer to The Cortex-M4 technical reference manual can be downloaded from the ARM website: http://infocenter.arm.com

2 Description

The V32G410x incorporates the high-performance ARM® Cortex®-M4F 32-bit RISC core operating at 200MHZ. The Cortex®-M4F core features a Floating point unit (FPU) single precision which supports all ARM single-precision data processing instructions and data type. It also implements a full set of DSP instructions and a memory protection unit (MPU) which enhances application security.

The V32G410x incorporates high-speed embedded memories (up to 4096 Kbytes of Flash memory, up to 1536 Kbytes of SRAM), the extensive external SPI Flash (up to 16 Mbytes addressing capability), and enhanced I/Os and peripherals connected to two APB buses.

The V32G410x offers two 12-bit ADCs, eight general-purpose 16-bit timers plus two general- purpose 32-bit timers, and up to two PWM timers for motor control, as well as standard and advanced communication interfaces, up to three I2Cs, four SPIs (all multiplexed as I2S), eight USART/UART and a CAN.

The V32G410x operates in the -40 to +85°C temperature range, from a 2.6 to 3.6 V power supply. A comprehensive set of power-saving mode allows the design of low-power application.

2.1 Device overview

The V32G410x offers devices in four different package types: from 48 pins, 60 pin and 100 pins. The description below gives an overview of the complete range of peripherals proposed in different devices.

Table2. V32G410x series device function and configuration

Part Number		V32G410VGT7	V32G410CGU7	V32G410VUT7	V32G410DUU6
CPU frequency (MHz)		200			
Flash (Kbytes)		1024	1024	4096	4096
SRAM (Kbytes)(1)		1536	1536	1536	1536
SPIM		0	0	0	0
Timers	Advanced-control	2			
	32-bit general-purpose	2			
	16-bit general-purpose	8			
	Basic	2			
	SysTick	1			
	IWDG	1			
	WWDG	1			
	RTC	1			

Comm.	I2C	3	1	3	3
	SPI_I2S	4	3	4	4
	USART+UART	4+4	2+3	4+4	4+4
	CAN	1	1	1	1
Analog	12-bit ADC numbers/channels	2			
		16	10	16	16
GPIOs		80	41	80	53
Operating temperatures		-40 to + 85°C			
Packages		LQFP100 14 x 14 mm	QFN48 7 x 7 mm	LQFP100 14 x 14 mm	QFN60 6 x 6 mm

Note1: *In 1536KB mode, the flash memory capacity with zero wait state is disabled;*
In 1408KB mode, the flash memory capacity with zero wait state is limited to 128K bytes;
In 1152KB mode, the flash memory capacity with zero wait state is limited to 384K bytes;
In 1024KB mode, the flash memory capacity with zero wait state is limited to 512K bytes;
In 896KB mode, the flash memory capacity with zero wait state is limited to 640K bytes.

2.2 Overview

The ARM Cortex®-M4F with FPU processor is the latest generation of ARM processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

2.2.1 ARM® Cortex®-M4F with FPU core and DSP instruction set

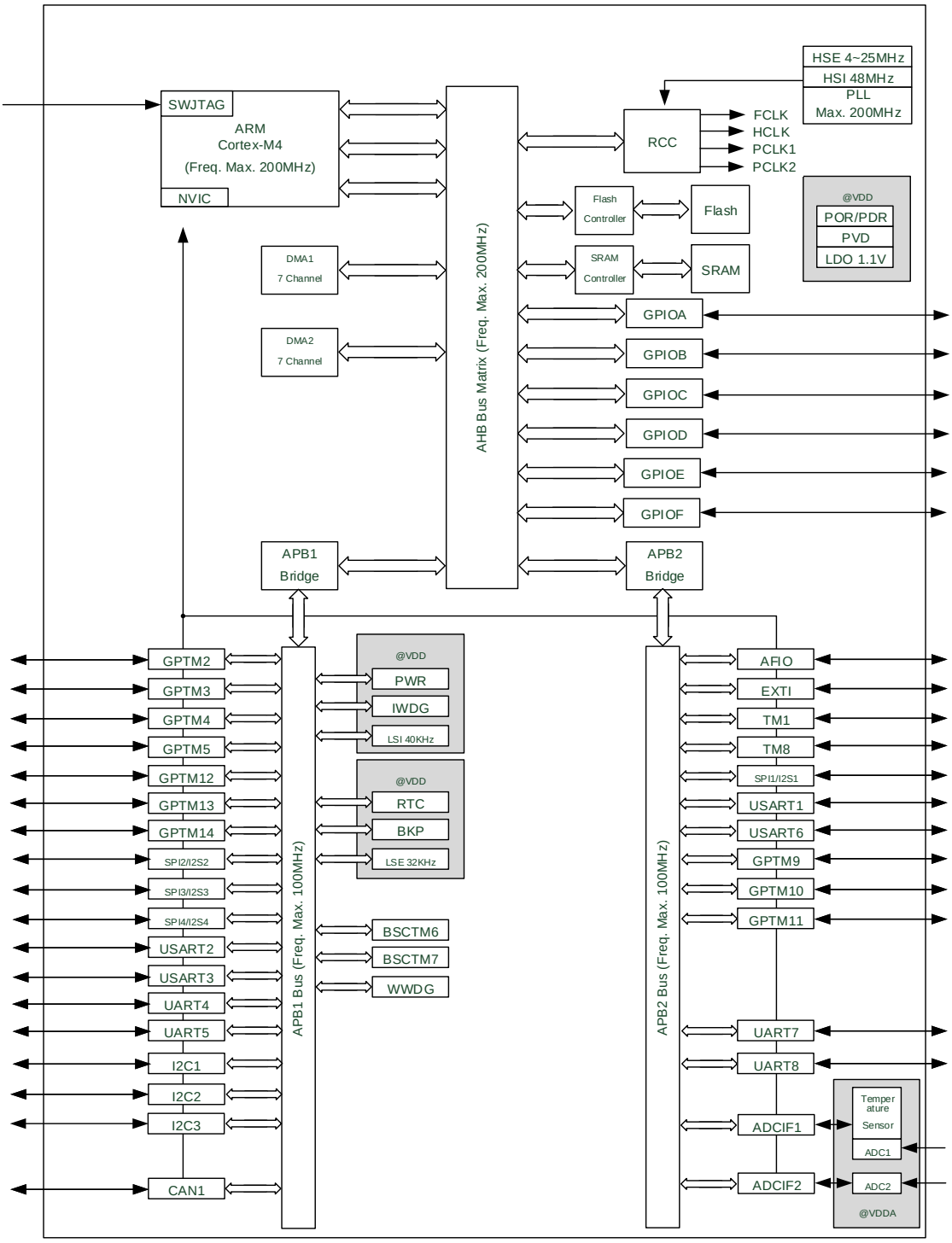
The ARM Cortex®-M4F with FPU 32-bit RISC processor features exceptional code efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices. The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution. Its single precision FPU (floating point unit) speeds up software development by using meta language development tools, while avoiding saturation.

With its embedded ARM core, the V32G410x is compatible with all ARM tools and software.

Figure 1 shows the general block diagram of the V32G410x.

Note1: *Cortex®-M4F with FPU is binary compatible with Cortex®-M3.*

Figure1. V32G410x block diagram



2.2.2 Memory protection unit (MPU)

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area is organized into up to 8 protected areas that can in turn be divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

2.2.3 Flash memory

Up to 4096 Kbytes of embedded Flash is available for storing programs and data.

The V32G410x provides extra interface called SPIM (SPI memory), which interfaces the external SPI Flash memory storing programs and data. With maximum 16 Mbytes addressing capability, SPIM can be used as an extensive Flash memory Bank 2.

2.2.4 Cyclic redundancy check (CRC) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link time and stored at a given memory location.

2.2.5 Embedded SRAM

Up to 1536 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states.

2.2.6 Nested vectored interrupt controller (NVIC)

The V32G410x embed a nested vectored interrupt controller able to manage 16 priority levels and handle up to 79 maskable interrupt channels plus the 16 interrupt lines of the Cortex®-M4 with FPU.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail-chaining

- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

2.2.7 External interrupt/event controller (EXTI)

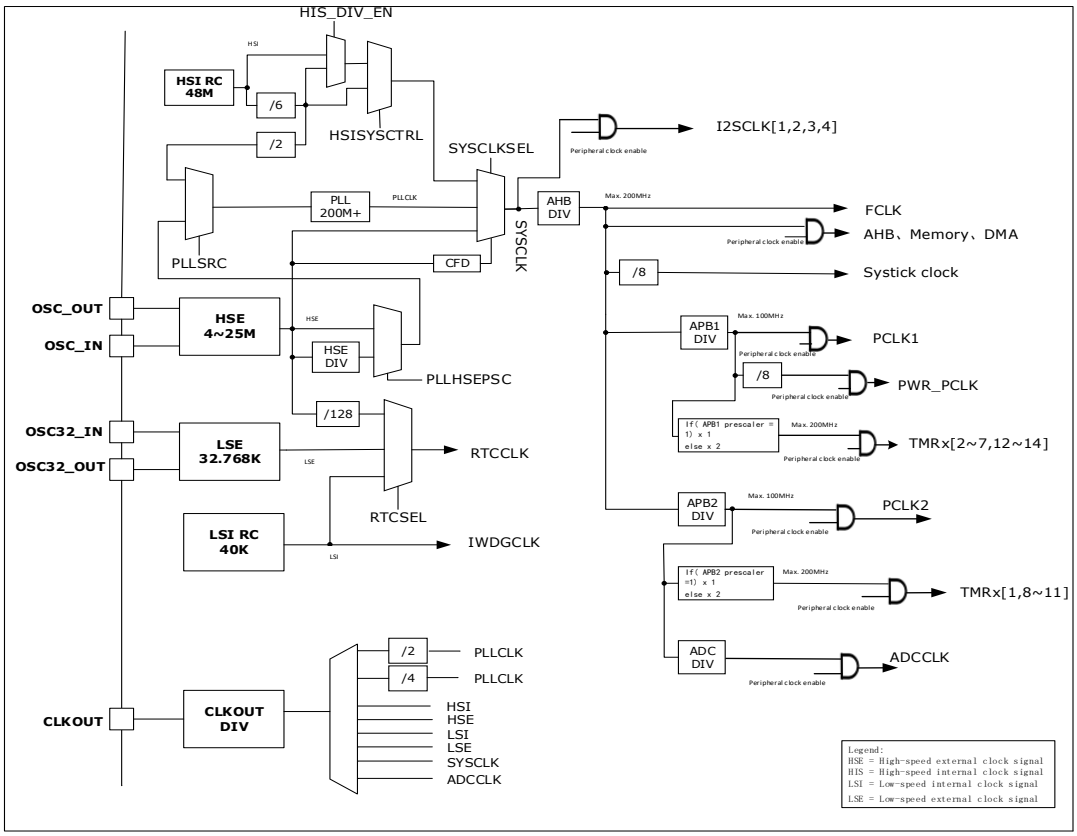
The external interrupt/event controller consists of 18 edge detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 86 GPIOs can be connected to the 16 external interrupt lines.

2.2.8 Clocks and startup

System clock selection is performed on startup, however the internal RC 48 MHz oscillator (HSI) through a divided-by-6 divider (8 MHz) is selected as default CPU clock on reset. An external 4 to 25 MHz clock (HSE) can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example with failure of an indirectly used external oscillator).

Multiple prescalers allow the configuration of the AHB and the APB (APB1 and APB2) frequency. The maximum frequency of the AHB domain is 200MHZ. The maximum allowed frequency of the APB domains are 100 MHz See Figure 2 for details on the clock tree.

Figure2. Clock tree



2.2.9 Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from user Flash. By default, boot from Flash memory bank 1 is selected. User can choose to boot from Flash memory bank 2 by setting a bit in the option bytes.
- Boot from system memory
- Boot from embedded SRAM

The bootloader is stored in system memory. The flash memory can be reprogrammed via USART1 or USART2. Table3 provides the the bootloader pin configurations.

Table3. The bootloader pin configurations

Interface	Pin
USART1	PA9: USART1_TX PA10: USART1_RX
USART2	PA2: USART2_TX (remapped) PA3: USART2_RX (remapped)

2.2.10 Power supply schemes

- V_{DD} = 2.6～3.6 V: external power supply for I/Os, RCL, XOL and the internal regulator provided externally through V_{DD} pins.
- V_{DDA} = 2.6～3.6 V: external analog power supplies for ADC\RCH\Tempersensor. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively.

For more detail on how to connect power pins, refer to Figure9.

2.2.11 Power supply supervisor

The device has an integrated power-on reset (POR)/power-down reset (PDR) circuitry. It is always active, and ensures proper operation starting from/down to 2.6 V. The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$, without the need for an external reset circuit.

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when V_{DD} drops below the V_{PVD} threshold and/or when V_{DD} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software. Refer to Table 13 for the characteristic values of $V_{POR/PDR}$ and V_{PVD}.

2.2.12 Low-power modes

The V32G410x supports two low-power modes to achieve the best compromise between low-power consumption, short startup time and available wakeup sources:

Sleep mode

In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

Stop mode

Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the 1.1 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator is put in normal mode.

The device can be woken up from Stop mode by any of the EXTI line. The EXTI line source can be one of the 16 external lines, the PVD output or the RTC alarm.

2.2.13 Direct Memory Access Controller (DMA)

The flexible 14-channel general-purpose DMAs (7 channels for DMA1 and 7 channels for DMA2) are able to manage memory-to-memory, peripheral-to-memory, and

memory-to-peripheral transfers. The two DMA controllers support circular buffer management, removing the need for user code intervention when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, I2C, USART, general-purpose, basic, and advanced-control timers TMRx, I2S, and ADC.

2.2.14 Real-time clock (RTC) and backup registers

The RTC and the backup registers are supplied with VDD. The backup registers are sixty- four 16-bit registers used to store 128 bytes of user application data. They are not reset by a system or power reset.

The real-time clock provides a set of continuously running counters which can be used with suitable software to provide a clock calendar function, and provides an alarm interrupt and a periodic interrupt. It is clocked by a 32.768 kHz external crystal, resonator or oscillator, the internal low- power RC oscillator, or the high-speed external clock divided by 128. The internal low-speed RC has a typical frequency of 40 kHz. The RTC can be calibrated using a divied-by-64 output of TAMPER pin to compensate for any natural quartz deviation. The RTC features a 32-bit programmable counter for long term measurement using the Compare register to generate an alarm. A 20-bit prescaler is used for the time base clock and is by default configured to generate a time base of 1 second from a clock at 32.768 kHz.

2.2.15 Timers and watchdogs (TMR/WDG)

The V32G410x devices include up to 2 advanced-control timers, up to 10 general-purpose timers, 2 basic timers, 2 watchdog timers, and a SysTick timer.

The table below compares the features of the advanced-control, general-purpose, and basic timers.

Table4. Timer feature comparison

Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Complement ary outputs
TMR1, TMR8	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	Yes
TMR2,	32-bit	Up, down,	Any integer between	Yes	4	No

TMR5		up/down	1 and 65536			
TMR3, TMR4	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
TMR9, TMR12	16-bit	Up	Any integer between 1 and 65536	No	2	No
TMR10, TMR11, TMR13, TMR14	16-bit	Up	Any integer between 1 and 65536	No	1	No
TMR6, TMR7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No

Advanced-control timers (TMR1 and TMR8)

The two advanced-control timers (TMR1 and TMR8) can each be seen a three-phase

PWM multiplexed on 6 channels. They have complementary PWM outputs with programmable inserted dead-times. They can also be seen as a complete general-purpose timer. The 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes)
- One-pulse mode output

If configured as a standard 16-bit timer, it has the same features as the TMRx timer. If configured as the 16-bit PWM generator, it has full modulation capability (0-100%).

In debug mode, the advanced-control timer counter can be frozen and the PWM outputs disabled to turn off any power switch driven by these outputs.

Many features are shared with those of the general-purpose TMR timers which have the same architecture. The advanced-control timer can therefore work together with the TMR timers via the link feature for synchronization or event chaining.

General-purpose timers (TMRx)

There are 10 synchronizable general-purpose timers embedded in the V32G410x.

- TMR2, TMR3, TMR4, and TMR5

The V32G410x has 4 full- featured general-purpose timers: TMR2, TMR3, TMR4, and TMR5. The TMR2 and TMR5 timers are based on a 32-bit auto-reload up/down counter and a 16-bit prescaler. The TMR3 and TMR4 timers are based on a 16-bit auto-reload up/down counter and a 16-bit prescaler. They all feature four independent channels for input capture/output compare, PWM or one-pulse mode output. This gives up to 16 input capture/output compare/PWMs.

The TMR2, TMR3, TMR4, and TMR5 general-purpose timers can work together, or

with the other general-purpose timers and the advanced-control timers via the link feature for synchronization or event chaining. In debug mode, their counter can be frozen. Any of these general-purpose timers can be used to generate PWM outputs.

The TMR2, TMR3, TMR4, and TMR5 are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

- TMR9 and TMR12

TMR9 and TMR12 are based on a 16-bit auto-reload up-counter, a 16-bit prescaler, and two independent channels for input capture/output compare, PWM, or one-pulse mode output. They can be synchronized with the TMR2, TMR3, TMR4, and TMR5 full-featured general-purpose timers. They can also be used as simple time bases.

- TMR10, TMR11, TMR13, and TMR14

These timers are based on a 16-bit auto-reload up-counter, a 16-bit prescaler, and one independent channels for input capture/output compare, PWM, or one-pulse mode output.

They can be synchronized with the TMR2, TMR3, TMR4, and TMR5 full-featured general-purpose timers. They can also be used as simple time bases.

Basic timers (TMR6 and TMR7)

These two timers can be used as a generic 16-bit time base.

Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit down-counter and 8-bit prescaler. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stop modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

Window watchdog (WWDG)

The window watchdog is based on a 7-bit down-counter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Auto-reload capability
- Mask-able system interrupt generation when the counter reaches 0

- Programmable clock source

2.2.16 Inter-integrated-circuit interface (I2C)

Up to 3 I2C bus interfaces can operate master mode. They can support standard and fast modes.

They support 7/10-bit addressing. A hardware CRC generation/verification is included.

They can be served by DMA and they support SMBus 2.0/PMBus.

2.2.17 Universal synchronous/asynchronous receiver transmitters (USART)

The V32G410x embeds 4 universal synchronous/asynchronous receiver transmitters (USART1, USART2, USART3, and USART6) and 4 universal asynchronous receiver transmitters (UART4, UART5, UART7, and UART8).

These eight interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode, and have LIN Master/Slave capability.

These eight interfaces are able to communicate at speeds of up to 5.625 Mbit/s.

USART1, USART2, and USART3 provide hardware management of the CTS and RTS signals. USART1, USART2, USART3, and USART6 also provide Smart Card mode (ISO7816 compliant) and SPI-like communication capability. All interfaces can be served by the DMA controller.

Table5. USART/UART feature comparison

USART/UART name	USART1	USART2	USART3	UART4	UART5	USART6	UART7	UART8
Hardware flow control for modem	Yes	Yes	Yes	-	-	-	-	-
Continuous communication using DMA	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Multiprocessor communication	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Synchronous mode	Yes	Yes	Yes	-	-	Yes	-	-

Smartcard mode	Yes	Yes	Yes	-	-	Yes	-	-
Single-wire half-duplex communication	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
IrDA SIR ENDEC block	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
LIN mode	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

2.2.18 Serial peripheral interface (SPI)

Up to four SPIs are able to communicate up to 50 Mbits/s in slave and master modes in full- duplex and simplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC/SDHC modes.

All SPIs can be served by the DMA controller.

2.2.19 Inter-integrated sound interface (I2S)

Four standard I2S interfaces (multiplexed with SPI) are available, that can be operated in master mode in half-duplex mode. These interfaces can be configured to operate with 16/32 bit resolution, as input or output channels. Audio sampling frequencies from 8 kHz up to 192 kHz are supported. The master clock can be output to the external CODEC at 256 times the sampling frequency.

2.2.20 Controller area network (CAN)

Two CANs are compliant with specifications 2.0A and B with a bit rate up to 1 Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. It has three transmit mailboxes, two receive FIFOs with 3 stages and 14 scalable filter banks.

2.2.21 General-purpose inputs/outputs (GPIO)

Each of the GPIO pins can be configured by software as output (push-pull), as input (with pull-down or without pull-up or pull-down), or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high current-capable.

The I/Os alternate function configuration can be locked, if needed, in order to avoid spurious writing to the I/Os registers by following a specific sequence.

2.2.22 Remap capability

This feature allows the use of a maximum number of peripherals in a given application. Indeed, alternate functions are available not only on the default pins but also on other specific pins onto which they are remappable. This has the advantage of making board design and port usage much more flexible.

For details refer to Table 6; it shows the list of remappable alternate functions and the pins onto which they can be remapped. See the V32G410x reference manual for software considerations.

2.2.23 Analog to digital converter (ADC)

Two 12-bit analog-to-digital converters are embedded into V32G410x devices and they share up to 16 external channels, performing conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the general-purpose timers and the advanced-control timers can be internally connected to the ADC start trigger and injection trigger, respectively, to allow the application to synchronize A/D conversion and timers.

2.2.24 Temperature sensor

The temperature sensor has to generate a voltage that varies linearly with temperature. The conversion range is between 2.6 V ≤ VDDA ≤ 3.6 V. The temperature sensor is internally connected to the ADC1_IN16 input channel which is used to convert the sensor output voltage into a digital value.

2.2.25 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP Interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target. The JTAG TMS and TCK pins are shared respectively with SWDIO and SWCLK and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

3 Pinouts and pin descriptions

Figure3. V32G410CGU7 QFN48 pinout

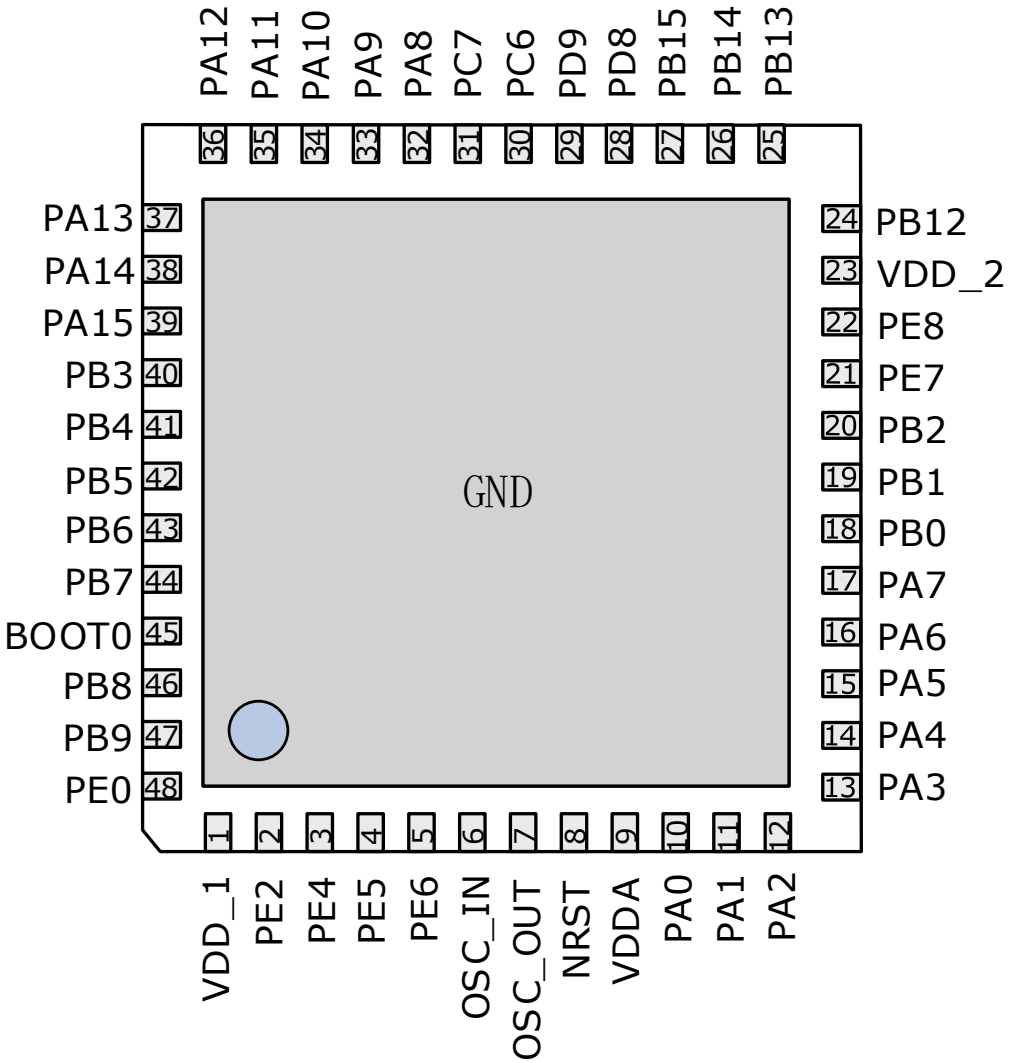


Figure4. V32G410DUU6 QFN60 pinout

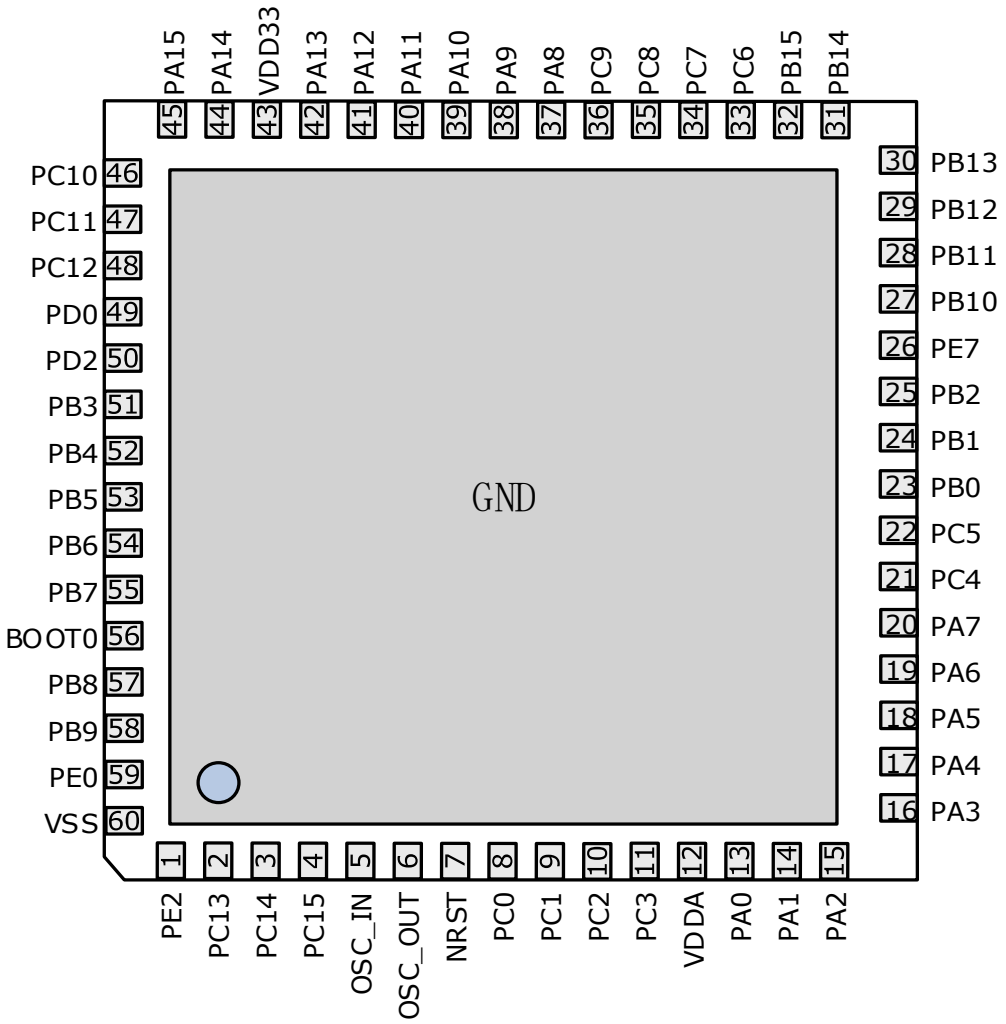
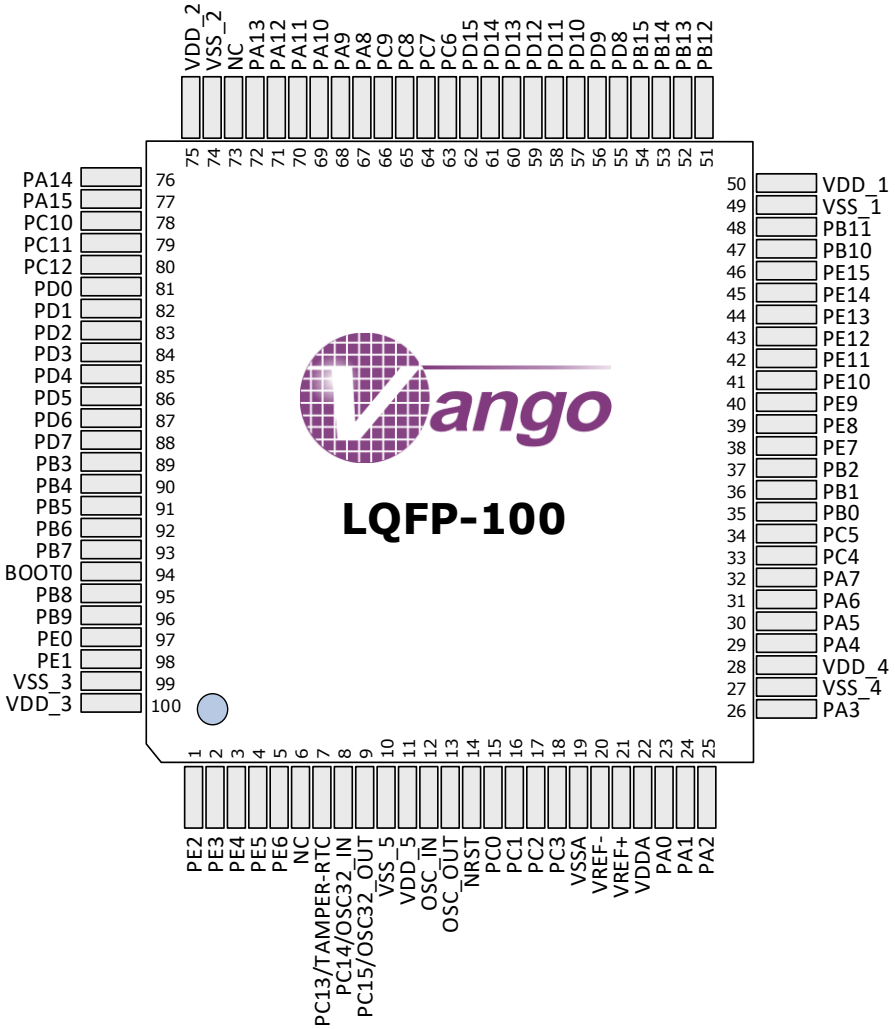


Figure5. V32G410VUT7/ V32G410VGT7 LQFP100 pinout



The following table is the pin definition of V32G410x series. The multiplexing functions are arranged in order of priority. The basic principle is that the analog signal is higher than the digital signal, and the output digital signal is higher than the input digital signal.

Table6. V32G410x series pin definitions

Pin number				Pin name	Type (1)	IO lever (2)	Main function	Alternate functions(3)	
V32G410x	V32G410VUT7 V32G410VGT7	V32G410CGU7	V32G410DUU6					Default Remap	Default Remap
1	-	-		NC	not connected				
2	1	2	1	PE2	I/O	NT	PE2	SPI4_SCK(5)/ I2S4_CK(5)	-
3	2	-		PE3	I/O	FT	PE3	-	-
4	3	3		PE4	I/O	FT	PE4	SPI4_NSS(5)/ I2S4_WS(5)	-
5	4	4		PE5	I/O	FT	PE5	SPI4_MISO(5)	TMR9_CH1
6	5	5		PE6	I/O	FT	PE6	SPI4_MOSI(5)/ I2S4_SD(5)	TMR9_CH2
7	-	-		NC	not connected				
8	6	-		NC	not connected				
9	7	-	2	TAMPER-RTC/PC13 (5)	I/O	FT	PC13(4)	TAMPER-RTC	-
10	8	-	3	OSC32_IN/ PC14(5)	I/O	NT	PC14(4)	OSC32_IN	-
11	9	-	4	OSC32_OUT/	I/O	NT	PC15	OSC32_OUT	-

Pin number				Pin name	Type（1）	IO lever（2）	Main function	Alternate functions(3)	
V32G410x	V32G410VUT7 V32G410VGT7	V32G410CGU7	V32G410DUU6					Default Remap	Default Remap
				PC15(5)					
12	-	-		NC	not connected				
13	10	-		VSS_5	S	-	VSS_5	-	-
14	11	-		VDD_5	S	-	VDD_5	-	-
15	12	6	5	OSC_IN	I/O	NT	OSC_IN	-	-
16	13	7	6	OSC_OUT	I/O	NT	OSC_OUT	-	-
17	14	8	7	NRST	I/O	-	NRST	-	-
18	-	-		NC	not connected				
19	15	-	8	PC0	I/O	NT	PC0	ADC1/2_IN10	-
20	16	-	9	PC1	I/O	NT	PC1	ADC1/2_IN11	-
21	-	-		NC	not connected				
22	17	-	10	PC2	I/O	NT	PC2	ADC1/2_IN12	UART8_TX
23	18	-	11	PC3	I/O	NT	PC3	ADC1/2_IN13	UART8_RX
24	19	-		VSSA	S	-	VSSA	-	-
25	-	-		NC	not connected				
26	20	-		VREF-	S	-	VREF-	-	-
27	21	-		VREF+	S	-	VREF+	-	-
28	22	9	12	VDDA	S	-	VDDA	-	-
29	23	10	13	PA0	I/O	NT	PA0	ADC1/2_IN0/	UART4_TX

Pin number				Pin name	Type（1）	IO lever（2）	Main function	Alternate functions(3)	
V32G410x	V32G410VUT7 V32G410VGT7	V32G410CGU7	V32G410DUU6					Default Remap	Default Remap
								USART2_CTS(5)/ TMR2_CH1(5) / TMR2_ETR(5)/ TMR5_CH1/ TMR8_ETR	
30	24	11	14	PA1	I/O	NT	PA1	ADC1/2_IN1/ USART2_RTS(5)/ TMR2_CH2(5)/ TMR5_CH2	UART4_RX
31	25	12	15	PA2	I/O	NT	PA2	ADC1/2_IN2/ USART2_TX(5)/ TMR2_CH3(5)/ TMR5_CH3/ TMR9_CH1(5)	-
32	-			NC	not connected				
33	-			SPIM_IO0	I/O	FT	SPIM_IO0	PF2	-
34	26	13	16	PA3	I/O	NT	PA3	ADC1/2_IN3/ USART2_RX(5)/ TMR2_CH4(5)/ TMR5_CH4/	I2S2_MCK

Pin number				Pin name	Type（1）	IO lever（2）	Main function	Alternate functions(3)	
V32G410x	V32G410VUT7 V32G410VGT7	V32G410CGU7	V32G410DUU6					Default Remap	Default Remap
								TMR9_CH2(5)	
35	27			VSS_4	S	-	VSS_4	-	-
36	28			VDD_4	S	-	VDD_4	-	-
37	-			SPIM_SCK	O	FT	SPIM_SCK	PF4	-
38	29	14	17	PA4	I/O	NT	PA4	ADC1/2_IN4/ USART2_CK(5)/ SPI1_NSS(5)/ I2S1_WS(5)	USART6_TX/ SPI3_NSS/ I2S3_WS
39	30	15	18	PA5	I/O	NT	PA5	ADC1/2_IN5/ SPI1_SCK(5)/ I2S1_CK(5)	USART6_RX
40	31	16	19	PA6	I/O	NT	PA6	ADC1/2_IN6/ SPI1_MISO(5)/ TMR3_CH1(5)/ TMR8_BKIN/ TMR13_CH1	I2S2_MCK/ TMR1_BKIN
41	-			SPIM_IO3	I/O	FT	SPIM_IO3	PF0	-
42	32	17	20	PA7	I/O	NT	PA7	ADC1/2_IN7/ SPI1_MOSI(5)/ I2S1_SD(5)/	TMR1_CH1N

Pin number				Pin name	Type（1）	IO lever（2）	Main function	Alternate functions(3)	
V32G410x	V32G410VUT7 V32G410VGT7	V32G410CGU7	V32G410DUU6					Default Remap	Default Remap
								TMR3_CH2(5)/ TMR8_CH1N/ TMR14_CH1	
43	33		21	PC4	I/O	NT	PC4	ADC1/2_IN14	-
44	34		22	PC5	I/O	NT	PC5	ADC1/2_IN15	
45	35	18	23	PB0	I/O	NT	PB0	ADC1/2_IN8/ I2S1_MCK(5)/ TMR3_CH3(5)/ TMR8_CH2N	TMR1_CH2N
46	-			NC	not connected				
47	36	19	24	PB1	I/O	NT	PB1	ADC1/2_IN9/ TMR3_CH4(5)/ TMR8_CH3N	TMR1_CH3N
48	37	20	25	PB2	I/O	FT	PB2 / BOOT1	-	-
49	38	21	26	PE7	I/O	FT	PE7	UART7_RX(5)	TMR1_ETR
50	39	22		PE8	I/O	FT	PE8	UART7_TX(5)	TMR1_CH1N
51	40			PE9	I/O	FT	PE9		TMR1_CH1
52	-			NC	not connected				
53	41			PE10	I/O	FT	PE10		TMR1_CH2N
54	42			PE11	I/O	FT	PE11		SPI4_SCK/

Pin number				Pin name	Type（1）	IO lever（2）	Main function	Alternate functions(3)	
V32G410x	V32G410VUT7 V32G410VGT7	V32G410CGU7	V32G410DUU6					Default Remap	Default Remap
									I2S4_CK/ TMR1_CH2
55	43			PE12	I/O	FT	PE12		SPI4_NSS/ I2S4_WS/ TMR1_CH3N
56	-			NC	not connected				
57	44			PE13	I/O	FT	PE13		SPI4_MISO/ TMR1_CH3
58	45			PE14	I/O	FT	PE14		SPI4_MOSI/ I2S4_SD/ TMR1_CH4
59	46			PE15	I/O	FT	PE15		TMR1_BKIN
60	47		27	PB10	I/O	FT	PB10	USART3_TX(5)/ I2C2_SCL	I2S3_MCK/ TMR2_CH3
61	48		28	PB11	I/O	FT	PB11	USART3_RX(5) / I2C2_SDA	TMR2_CH4
62	49			VSS_1	S	-	VSS_1	-	-
63	50	1		VDD_1	S	-	VDD_1	-	-
64	-			NC	not connected				
65	-			NC	not connected				

Pin number				Pin name	Type（1）	IO lever（2）	Main function	Alternate functions(3)	
V32G410x	V32G410VUT7 V32G410VGT7	V32G410CGU7	V32G410DUU6					Default Remap	Default Remap
66	51	24	29	PB12	I/O	FT	PB12	USART3_CK(5)/ I2C2_SMBA/ SPI2_NSS / I2S2_WS/ TMR1_BKIN(5)	-
67	52	25	30	PB13	I/O	FT	PB13	USART3_CTS(5)/ SPI2_SCK/ I2S2_CK/ TMR1_CH1N(5)	-
68	53	26	31	PB14	I/O	FT	PB14	USART3_RTS(5)/ SPI2_MISO/ TMR1_CH2N(5)/ TMR12_CH1	-
69	-			NC	not connected				
70	54	27	32	PB15	I/O	FT	PB15	SPI2_MOSI/ I2S2_SD/ TMR1_CH3N(5)/ TMR12_CH2	-
71	55	28		PD8	I/O	FT	PD8	-	USART3_TX
72	56	29		PD9	I/O	FT	PD9	-	USART3_RX

Pin number				Pin name	Type（1）	IO lever（2）	Main function	Alternate functions(3)	
V32G410x	V32G410VUT7 V32G410VGT7	V32G410CGU7	V32G410DUU6					Default Remap	Default Remap
73	-			NC	not connected				
74	57			PD10	I/O	FT	PD10	-	USART3_CK
75	58			PD11	I/O	FT	PD11	-	USART3_CTS
76	59			PD12	I/O	FT	PD12	-	USART3_RTS/ TMR4_CH1
77	60			PD13	I/O	FT	PD13	-	TMR4_CH2
78	-			NC	not connected				
79	61			PD14	I/O	FT	PD14	-	TMR4_CH3
80	62			PD15	I/O	FT	PD15	-	TMR4_CH4
81	63	30	33	PC6	I/O	FT	PC6	USART6_TX(5)/ I2S2_MCK(5)/ TMR8_CH1	TMR3_CH1
82	64	31	34	PC7	I/O	FT	PC7	USART6_RX(5)/ I2S3_MCK(5)/ TMR8_CH2	TMR3_CH2
83	65		35	PC8	I/O	FT	PC8	USART6_CK/ I2S4_MCK(5)/ TMR8_CH3	TMR3_CH3
84	-			NC	not connected				
85	66		36	PC9	I/O	FT	PC9	I2C3_SDA(5)/	TMR3_CH4

Pin number				Pin name	Type（1）	IO lever（2）	Main function	Alternate functions(3)	
V32G410x	V32G410VUT7 V32G410VGT7	V32G410CGU7	V32G410DUU6					Default Remap	Default Remap
								TMR8_CH4	
86	67	32	37	PA8	I/O	NT	PA8	CLKOUT/ USART1_CK/ I2C3_SCL/ TMR1_CH1(5)	-
87	68	33	38	PA9	I/O	FT	PA9	USART1_TX(5)/ I2C3_SMBA/ TMR1_CH2(5)	-
88	-			NC	not connected				
89	69	34	39	PA10	I/O	FT	PA10	USART1_RX(5) / TMR1_CH3(5)	I2S4_MCK
90	70	35	40	PA11	I/O	FT	PA11	USART1_CTS/ CAN1_RX(5)/ TMR1_CH4(5)	-
91	71	36	41	PA12	I/O	FT	PA12	USART1_RTS/ CAN1_TX(5)/ TMR1_ETR(5)	-
92	72	37	42	PA13	I/O	FT	JTMS-SWDIO	-	PA13
93	73			NC	not connected				
94	74			VSS_2	S	-	VSS_2	-	-

Pin number				Pin name	Type（1）	IO lever（2）	Main function	Alternate functions(3)	
V32G410x	V32G410VUT7 V32G410VGT7	V32G410CGU7	V32G410DUU6					Default Remap	Default Remap
95	75	23	43	VDD_2	S	-	VDD_2	-	-
96	-			NC	not connected				
97	-			NC	not connected				
98	76	38	44	PA14	I/O	FT	JTCK-SWCLK	-	PA14
99	77	39	45	PA15	I/O	FT	JTDI	SPI3_NSS(5)/ I2S3_WS(5)	PA15/ SPI1_NSS/ I2S1_WS/ TMR2_CH1/ TMR2_ETR
100	78		46	PC10	I/O	FT	PC10	UART4_TX(5)	USART3_TX/ SPI3_SCK/ I2S3_CK
101	79		47	PC11	I/O	FT	PC11	UART4_RX(5)	USART3_RX/ SPI3_MISO
102	-			NC	not connected				
103	80		48	PC12	I/O	FT	PC12	UART5_TX(5)	USART3_CK/ SPI3_MOSI/ I2S3_SD
104	81		49	PD0	I/O	FT	PD0		CAN1_RX
105	82			PD1	I/O	FT	PD1		CAN1_TX

Pin number				Pin name	Type（1）	IO lever（2）	Main function	Alternate functions(3)	
V32G410x	V32G410VUT7 V32G410VGT7	V32G410CGU7	V32G410DUU6					Default Remap	Default Remap
106	83		50	PD2	I/O	FT	PD2	UART5_RX(5)/ TMR3_ETR	
107	-			NC	not connected				
108	84			PD3	I/O	FT	PD3	-	USART2_CTS
109	85			PD4	I/O	FT	PD4	-	USART2_RTS
110	86			PD5	I/O	FT	PD5	-	USART2_TX
111	-			NC	not connected				
112	87			PD6	I/O	FT	PD6	-	USART2_RX
113	88			PD7	I/O	FT	PD7	-	USART2_CK
114	89	40	51	PB3	I/O	FT	JTDO	SPI3_SCK(5)/ I2S3_CK(5)	PB3/ UART7_RX/ SPI1_SCK/ I2S1_CK/ TMR2_CH2
115	90	41	52	PB4	I/O	FT	NJTRST	SPI3_MISO(5)	PB4/ SPI1_MISO/ I2C3_SDA/ UART7_TX/ TMR3_CH1
116	-			SPIM_NSS	O	FT	SPIM_NSS	PF5	-

Pin number				Pin name	Type（1）	IO lever（2）	Main function	Alternate functions(3)	
V32G410x	V32G410VUT7 V32G410VGT7	V32G410CGU7	V32G410DUU6					Default Remap	Default Remap
117	91	42	53	PB5	I/O	FT	PB5	SPI3_MOSI(5)/ I2S3_SD(5)/ I2C1_SMBA(5)	SPI1_MOSI/ I2S1_SD/ TMR3_CH2
118	92	43	54	PB6	I/O	FT	PB6	I2C1_SCL(5)/ TMR4_CH1(5)	USART1_TX/ I2S1_MCK/ SPI4_NSS/ I2S4_WS
119	93	44	55	PB7	I/O	FT	PB7	I2C1_SDA(5)/ TMR4_CH2(5)	USART1_RX/ SPI4_SCK/ I2S4_CK
120	-			SPIM_IO1	I/O	FT	SPIM_IO1	PF1	-
121	94	45	56	BOOT0	I	-	BOOT0	-	-
122	95	46	57	PB8	I/O	FT	PB8	TMR4_CH3(5)/ TMR10_CH1	UART5_RX/ SPI4_MISO/ I2C1_SCL/ CAN1_RX
123	96	47	58	PB9	I/O	FT	PB9	TMR4_CH4(5)/ TMR11_CH1	UART5_TX/ SPI4_MOSI/ I2S4_SD/ I2C1_SDA/

Pin number				Pin name	Type（1）	IO lever（2）	Main function	Alternate functions(3)	
V32G410x	V32G410VUT7 V32G410VGT7	V32G410CGU7	V32G410DUU6					Default Remap	Default Remap
									CAN1_TX
124	-			SPIM_IO2	I/O	FT	SPIM_IO2	PF3	-
125	97	48	59	PE0	I/O	FT	PE0	UART8_RX(5)/ TMR4_ETR	-
126	98			PE1	I/O	FT	PE1	UART8_TX(5)	-
127	99		60	VSS_3	S	-	VSS_3	-	-
128	100			VDD_3	S	-	VDD_3	-	-

Note1: *I = input, O = output, S = supply.*

Note2: *FT = general 5 V-tolerant I/O, NT = Not support general 5 V-tolerant I/O.*

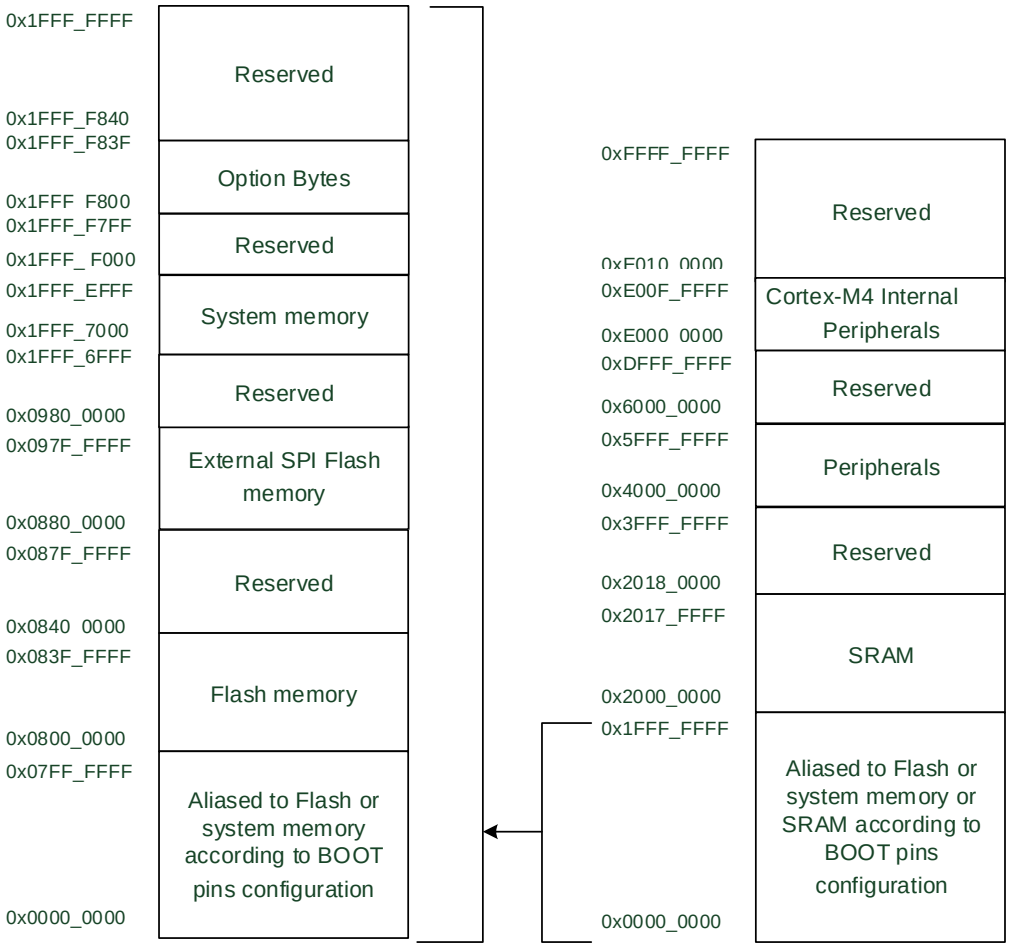
Note3: *If several peripherals share the same I/O pin, to avoid conflict between these alternate functions only one peripheral should be enabled at a time through the peripheral clock enable bit (in the corresponding RCC peripheral clock enable register).*

Note4: *Main function after the first backup domain power-up. Later on, it depends on the contents of the Backup registers even after reset (because these registers are not reset by the main reset). For details on how to manage these IOs, refer to the backup domain and BKP register description sections in the V32G410x reference manual.*

Note5: *This alternate function can be remapped by software to some other port pins (if available on the used package). For more details, refer to the Alternate function I/O and debug configuration section in the V32G410x reference manual.*

4 Memory mapping

Figure6. Memory map



5 Electrical characteristics

5.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to VSS.

5.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production with an ambient temperature at TA = 25 °C and TA = TA max.

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production.

5.1.2 Typical values

Unless otherwise specified, typical data are based on TA = 25 °C, VDD = 3.3 V. They are given only as design guidelines and are not tested.

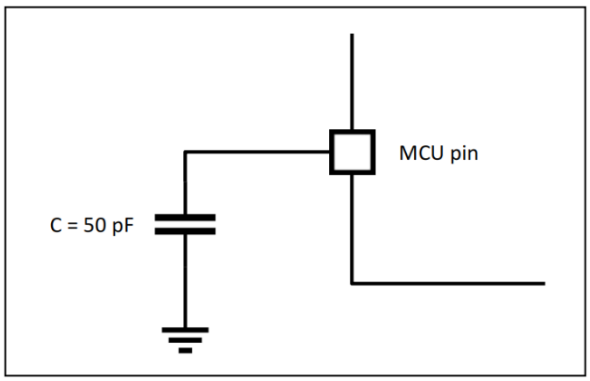
5.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

5.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in Figure7.

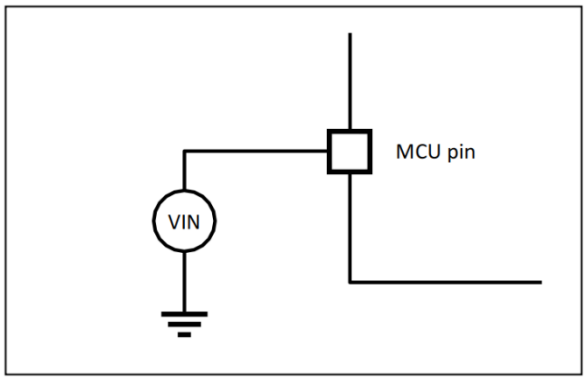
Figure7. Pin loading conditions



5.1.5 Pin input voltage

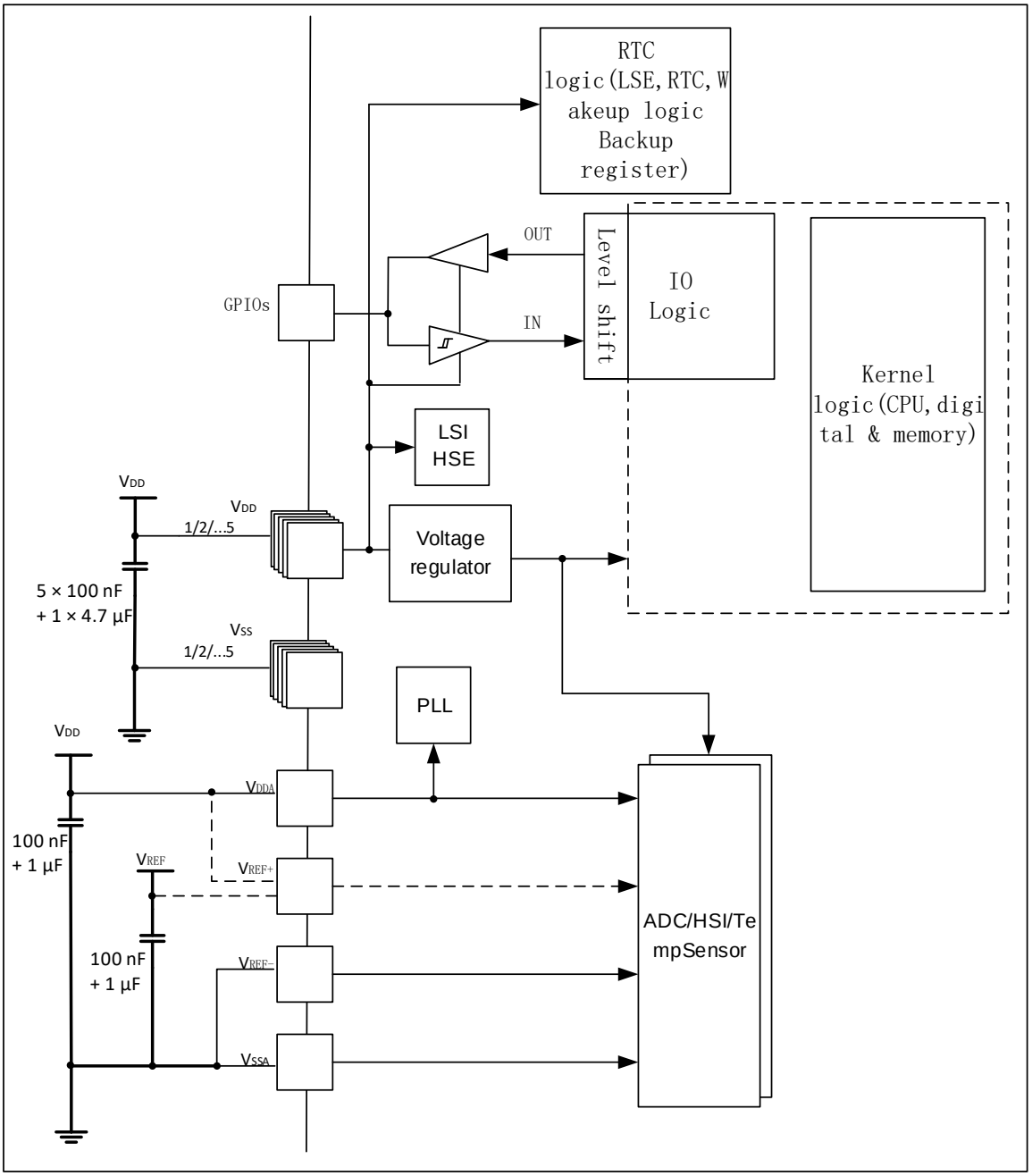
The input voltage measurement on a pin of the device is described in Figure8.

Figure8. Pin input voltage



5.1.6 Power supply scheme

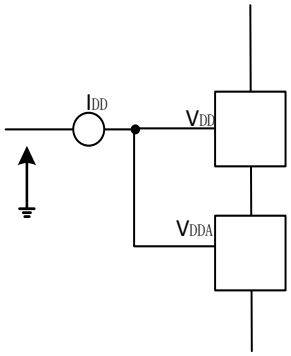
Figure9. Power supply scheme



Note1: *In this figure, the 4.7 µF capacitor must be connected to VDD3.*

5.1.7 Current consumption measurement

Figure10. Current consumption measurement scheme



5.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in Table 8, Table 9, and Table 10 may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table7. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DD}-V_{SS}	External main supply voltage (including VDDA and VDD)(1)	-0.3	4.0	V
V_{IN}	Input voltage on FT I/O	VSS-0.3	6.0	
	Input voltage on NT I/O	VSS-0.3	4.0	
$\|\Delta V_{DDx}\|$	Variations between different VDD power pins	-	50	mV
$\|V_{SSx}-V_{SS}\|$	Variations between all the different ground pins (2)	-	50	

Note1: *All main power (VDD, VDDA) and ground (VSS, VSSA) pins must always be connected to the external power supply, in the permitted range.*

Note2: *VREF- included.*

Table8. Current characteristics

Symbol	Ratings	Max	Unit
IVDD	Total current into VDD/VDDA power lines (source)(1)	150	mA
IVSS	Total current out of VSS ground lines (sink)(1)	150	
IIO	Output current sunk by any I/O and control pin	25	
	Output current source by any I/Os and control pin	-25	

Note1: *All main power (VDD, VDDA) and ground (VSS, VSSA) pins must always be connected to the external power supply, in the permitted range.*

Table9. Thermal characteristics

Symbol	Ratings	Value	Unit
TSTG	Storage temperature range	-60 ~ +150	°C
TJ	Maximum junction temperature	105	

5.3 Operating conditions

5.3.1 General operating conditions

Table10. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency		0	200	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	0	100	MHz
f_{PCLK2}	Internal APB2 clock frequency	-	0	100	MHz
VDD	Standard operating voltage	-	2.6	3.6	V
VDDA(1)	Analog operating voltage	Must be the same potential as VDD(1)	2.6	3.6	V
VDD	Backup operating voltage	-	2.6	3.6	V
PD	Power dissipation: TA = 85 °C	-	-	373	mW
TA	Ambient temperature	-	-40	105	°C

Note1: *It is recommended to power VDD and VDDA from the same source. A maximum difference of 300 mV between VDD and VDDA can be tolerated during power-up and operation.*

5.3.2 Operating conditions at power-up/ power-down

The parameters given in the table below are derived from tests performed under the ambient temperature condition summarized in Table10.

Table11. Operating conditions at power-up / power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	VDD rise time rate	-	0	∞(1)	ms/V
	VDD fall time rate		20	∞	μs/V

Note1: *If VDD rising time rate is slower than 120 ms/V, the code should access the backup registers after VDD higher than VPOR + 0.1V.*

5.3.3 Embedded reset and power control block characteristics

The parameters given in the table below are derived from tests performed under ambient temperature and VDD supply voltage conditions summarized in Table10.

Table12. Embedded reset and power control block characteristics

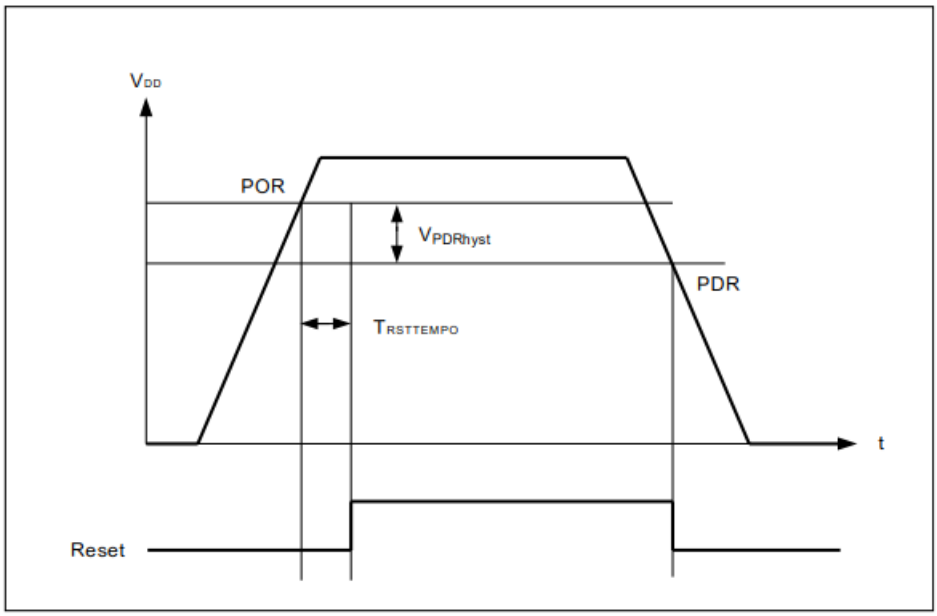
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD}	Programmable voltage detector level selection	PVDS[2:0] = 001 (rising edge)(1)		2.4		V
		PVDS[2:0] = 001 (falling edge)(1)		2.3		V
		PVDS[2:0] = 010 (rising edge)		2.5		V
		PVDS[2:0] = 010 (falling edge)		2.4		V
		PVDS[2:0] = 011 (rising edge)		2.6		V
		PVDS[2:0] = 011 (falling edge)		2.5		V
		PVDS[2:0] = 100 (rising edge)		2.7		V
		PVDS[2:0] = 100 (falling edge)		2.6		V
		PVDS[2:0] = 101 (rising edge)		2.8		V
		PVDS[2:0] = 101 (falling edge)		2.7		V
		PVDS[2:0] = 110 (rising edge)		2.9		V
		PVDS[2:0] = 110 (falling edge)		2.8		V
		PVDS[2:0] = 111 (rising edge)		3.0		V
		PVDS[2:0] = 111 (falling edge)		2.9		V
$V_{PVDhyst}$(2)	PVD hysteresis	-	-	100	-	mV
$V_{POR/PDR}$	Power on/power down reset threshold	Falling edge		2.15		V
		Rising edge		2.31		V
$V_{PDRhyst}$(2)	PDR hysteresis	-	-	160	-	mV
$T_{RSTTEMPO}$(2)	Reset temporization: CPU starts execution after VDD keeps higher than VPOR for TRSTTEMPO	EOPB0 = 0/1/2/3	-	0.7	-	ms
		EOPB0 = 4	-	70	-	
		EOPB0 = 5	-	200	-	
		EOPB0 = 6	-	270	-	
		EOPB0 = 7	-	330	-	

Note1: *PVDS[2:0] = 001 may be not available for its voltage detector level may be lower than*

VPOR/PDR.

Note2: *Guaranteed by design, not tested in production.*

Figure11. Power on reset/power down reset waveform



5.3.4 Supply current characteristics

Current consumption is a comprehensive index of many parameters and factors, including operating voltage, ambient temperature, I/O pin load, product software configuration, operating frequency, I/O pin flip rate, and executed code.

Typical current consumption

The microcontroller is under the following conditions:

- All I/O pins are on analog inputs.

All peripherals are turned off unless otherwise specified.

Instruction prefetch function is turned on (hint: this parameter must be set before setting clock and bus frequency division).

- Ambient temperature and VDD supply voltage conform to electrical characteristic parameters
- When the peripheral is turned on:
  - If f_{HCLK} > 100 MHz, $f_{PCLK1} = f_{HCLK}/2$, $f_{PCLK2} = f_{HCLK}/2$, $f_{ADCCLK} = f_{PCLK2}/4$;
  - If $f_{HCLK} \leq$ 100 MHz, $f_{PCLK1} = f_{HCLK}$, $f_{PCLK2} = f_{HCLK}$, $f_{ADCCLK} = f_{PCLK2}/4$.

Table13. Typical Current Consumption in Operating Modes

Symbol	Parameter	Condition	FHCLK	Typical (1)		Unit
				Enable all	Close all	

				peripherals	peripherals	
IDD	Supply current in operation mode	External clock (2)	200 MHz	57.1	39.4	mA
			192 MHz	55.7	38.4	
			180 MHz	53.4	37.1	
			100 MHz	38.7	27.1	
			48 MHz	25.4	19.5	
			24 MHz	19.4	16.0	
			8 MHz	13.6	12.5	
			4 MHz	12.2	11.7	
			2 MHz	11.7	11.4	
			1 MHz	11.5	11.3	
			500 KHz	11.3	11.2	
			125 KHz	11.2	11.1	
		Operating on high-speed internal RC oscillator (HSI)	200 MHz	48.1	33.2	mA
			192 MHz	46.7	32.3	
			180 MHz	44.8	31.2	
			100 MHz	32.7	23.0	
			48 MHz	21.6	16.7	
			24 MHz	16.6	13.8	
			8 MHz	11.8	10.9	
			4 MHz	10.6	10.2	
			2 MHz	10.2	10.0	
			1 MHz	10.0	9.8	
			500 KHz	9.9	9.8	
			125 KHz	9.8	9.7	

Note1: *Typical values are measured at TA = 25 °C and VDD = 3.3 V.*

Note2: *The external clock is 8 MHz and PLL is enabled when fHCLK > 8 MHz.*

Table14. Typical Current Consumption in Sleep Mode

Symbol	Parameter	Condition	FHCLK	Typical (1)		Unit
				Enable all	Close all	

				peripherals	**peripherals**	
IDD	Supply current in sleep mode	External clock (2)	200 MHz	36.4	20.7	mA
			192 MHz	35.2	18.0	
			180 MHz	33.7	17.6	
			100 MHz	24.3	12.9	
			48 MHz	15.0	9.1	
			24 MHz	10.9	7.6	
			8 MHz	6.4	5.4	
			4 MHz	5.4	5.0	
			2 MHz	5.1	4.8	
			1 MHz	4.9	4.7	
			500 KHz	4.8	4.7	
			125 KHz	4.8	4.7	
		Operating on high-speed internal RC oscillator (HSI)	200 MHz	29.6	18.0	mA
			192 MHz	28.6	14.3	
			180 MHz	27.4	14.0	
			100 MHz	19.5	10.0	
			48 MHz	11.9	7.0	
			24 MHz	8.4	5.7	
			8 MHz	4.8	3.9	
			4 MHz	3.9	3.5	
			2 MHz	3.6	3.4	
			1 MHz	3.5	3.4	
			500 KHz	3.4	3.4	
			125 KHz	3.4	3.3	

Note1: *Typical values are measured at TA = 25 °C and VDD = 3.3 V.*

Note2: *The external clock is 8 MHz and PLL is enabled when fHCLK > 8 MHz.*

Maximum current consumption

The microcontroller is under the following conditions:

- All I/O pins are on analog inputs.
- All peripherals are turned off unless otherwise specified.
- Instruction prefetch function is turned on (hint: this parameter must be set before setting clock and bus frequency division).
- When the peripheral is turned on:
  - If f_{HCLK} > 100 MHz, $f_{PCLK1} = f_{HCLK}/2$, $f_{PCLK2} = f_{HCLK}/2$;
  - If $f_{HCLK} \leq$ 100 MHz, $f_{PCLK1} = f_{HCLK}$, $f_{PCLK2} = f_{HCLK}$.

Table15. Maximum Current Consumption in Operating Mode

Symbol	Parameter	Condition	FHCLK	Maximum (1) TA = 85 °C	Unit
IDD	Supply current in operation mode	External clock (2) enables all peripherals	200 MHz	93.1	mA
			192 MHz	90.5	
			180 MHz	88.0	
			100 MHz	71.8	
			48 MHz	58.5	
			24 MHz	53.0	
			8 MHz	47.1	
		The external clock (2) turns off all peripherals	200 MHz	72.8	mA
			192 MHz	71.9	
			180 MHz	70.7	
			100 MHz	59.9	
			48 MHz	52.5	
			24 MHz	49.7	
			8 MHz	46.1	

Note1: *It is obtained from comprehensive evaluation and is not tested in production.*

Note2: *The external clock is 8 MHz and PLL is enabled when fHCLK > 8 MHz.*

Table16. Maximum Current Consumption in Sleep Mode

Symbol	Parameter	Condition	FHCLK	Maximum (1) TA = 85 ° C	Unit
IDD	Supply current in sleep mode	External clock (2) enables all peripherals	200 MHz	45.5	mA
			192 MHz	44.2	
			180 MHz	42.6	
			100 MHz	32.0	
			48 MHz	22.6	
			24 MHz	19.0	
			8 MHz	14.4	
		The external clock (2) turns	200 MHz	27.2	mA
			192 MHz	26.7	

		off all peripherals	180 MHz	26.2	
			100 MHz	20.9	
			48 MHz	17.3	
			24 MHz	15.9	
			8 MHz	13.6	

Note1: *It is obtained from comprehensive evaluation and is not tested in production.*

Note2: *The external clock is 8 MHz and PLL is enabled when fHCLK > 8 MHz.*

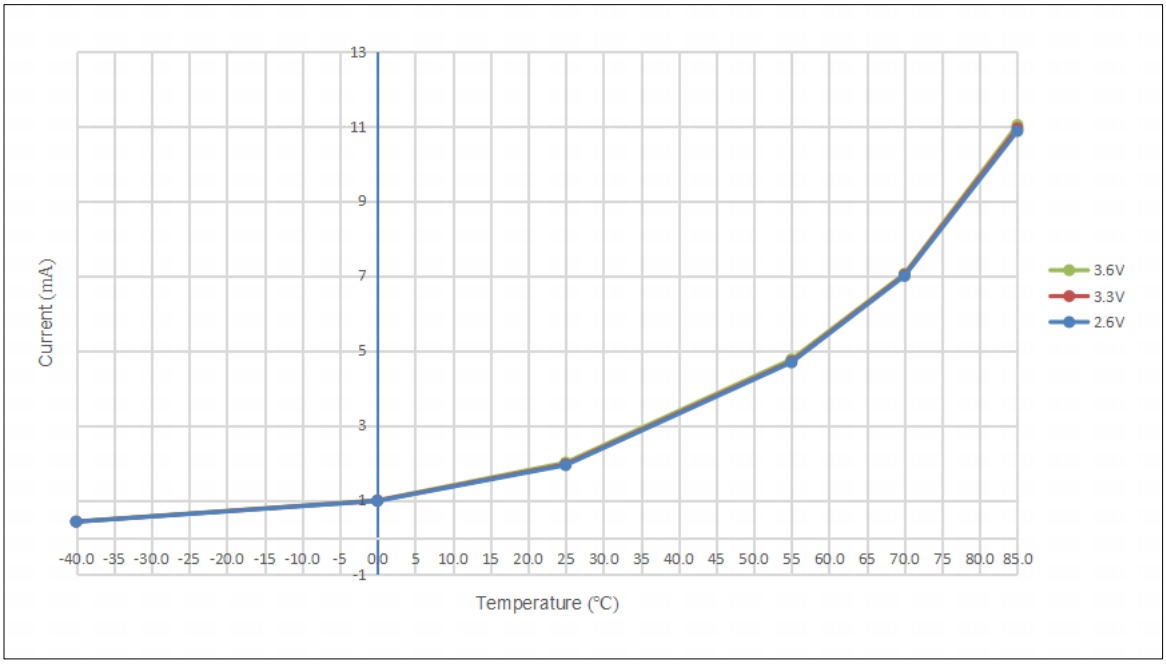
Table17. Typical and Maximum Current Consumption in Shutdown Modes

Symbol	Parameter	Condition	Typical (1)		Max (2)	Unit
			VDD = 2.6 V	VDD = 3.3 V	TA = 85 °C	
IDD	Supply current in shutdown mode	High-speed internal RC oscillator and high-speed external oscillator are off (no independent watchdog)	1.5	1.9	10.9	mA

Note1: *Typical values are measured at TA = 25 ℃.*

Note2: *It is obtained by comprehensive evaluation and is not tested in production.*

Figure12. Typical Current Consumption in Shutdown Mode vs. Temperature at Different VDD



Internal peripheral current consumption

The current consumption of the built-in peripherals is listed in Table 18, and the operating conditions of the microcontroller are as follows:

- All I/O pins are on analog inputs.

All peripherals are turned off unless otherwise specified.

- The values given are calculated by measuring current consumption
  - Turn off all peripheral clocks
  - Turn on the clock of only one peripheral

Ambient temperature and VDD supply voltage conditions conform to electrical characteristics.

Table18. Current Consumption of Built-in Peripherals

Built-in peripheral		Typical value	Unit
AHB (up to 200 MHz)	DMA1	3.0	μA/MHz
	DMA2	4.6	
	CRC	1.0	
APB1 (up to 100 MHz)	TMR2	9.2	μA/MHz
	TMR3	7.7	
	TMR4	9.2	
	TMR5	11.5	
	TMR6	6.2	
	TMR7	3.8	
	TMR12	7.6	
	TMR13	6.5	
	TMR14	7.1	
	SPI2/I2S2	6.6	
	SPI3/I2S3	5.1	
	SPI4/I2S4	7.8	
	USART2	6.5	
	USART3	5.2	
	UART4	2.6	
	UART5	7.0	
	I2C1	7.1	
	I2C2	7.8	
	CAN	15.2	
	WWDG	5.5	
	PWR	6.2	
	BKP	6.2	
	I2C3	7.5	
APB2 (up to 100 MHz)	AFIO	7.2	μA/MHz

	GPIOA	7.2	
	GPIOB	5.7	
	GPIOC	3.6	
	GPIOD	4.0	
	GPIOE	5.3	
	SPI1/I2S1	8.4	
	USART1	7.2	
	USART6	6.1	
	UART7	4.7	
	UART8	3.8	
	TMR1	11.7	
	TMR8	13.3	
	TMR9	8.4	
	TMR10	9.9	
	TMR11	9	
	ADC1+ADC2	5.2	

5.3.5 External clock source characteristics

High-speed external user clock generated from an external source

The characteristics given in the table below result from tests performed using a high-speed external clock source, and under ambient temperature and supply voltage conditions summarized in Table10.

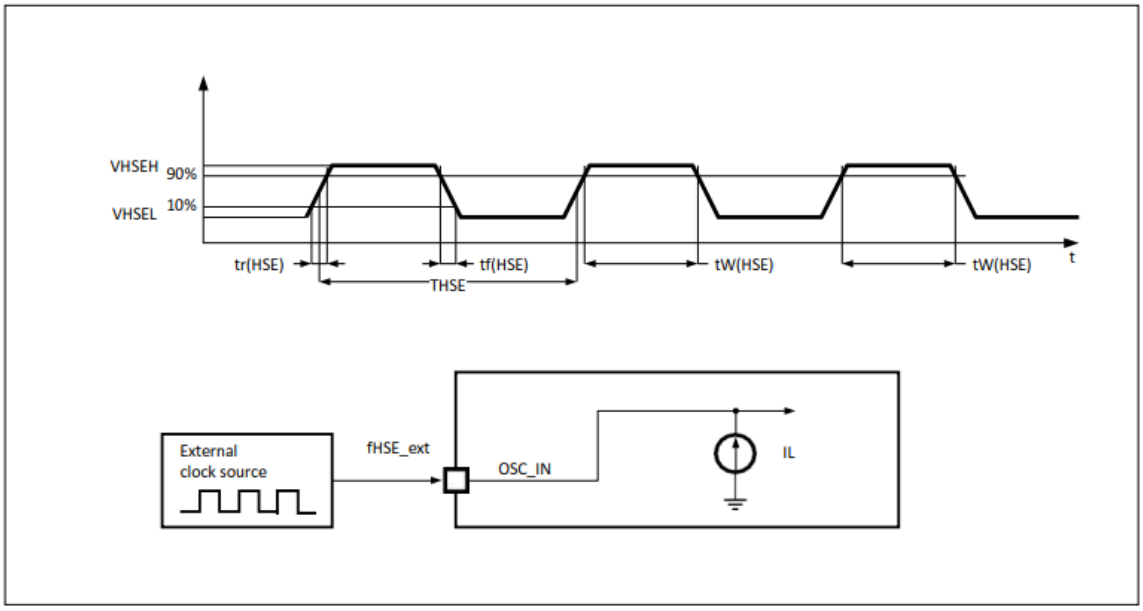
Table19. High-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSCIN}	Crystal frequency	2.6V≤VDD≤3.6V	2	8	30	MHz
V_{HSEH}	OSC_IN input pin high level voltage		0.7*V_{DD}	-	V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage		V_{SS}	-	0.3*V_{DD}	
$t_{w(HSE)}$ $t_{w(HSE)}$	OSC_IN high or low time(1)		5	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time(1)		-	-	20	
Cin(HSE)	OSC_IN input capacitance	-		3		pF
$DuCy_{(HSE)}$	Duty cycle	-	30	50	70	%

I	HSE driving current	VDD=3.3V,VIN=VSS With 20pF load		3		mA
I_L	OSC_IN input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$			± 1	uA

Note1: *Guaranteed by design, not tested in production.*

Figure13. High-speed external clock source AC timing diagram



Low-speed external user clock generated from an external source

The characteristics given in the table below result from tests performed using a low-speed external clock source, and under ambient temperature and supply voltage conditions summarized in Table10.

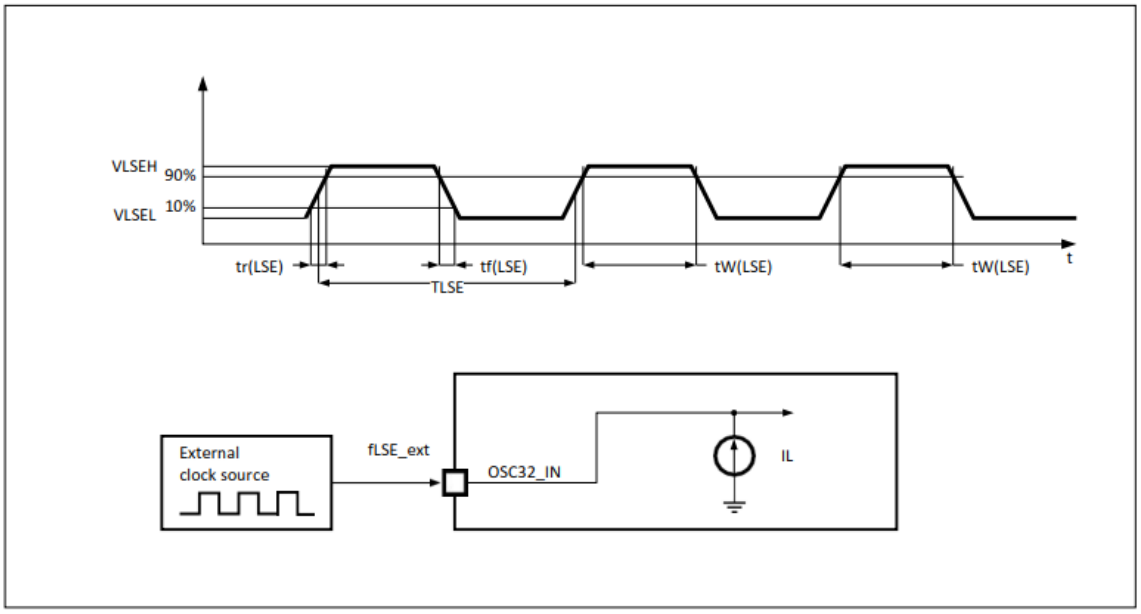
Table20. Low-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User External clock source frequency(1)	-	-	32.768	1000	KHz
V_{LSEH}	OSC32_IN input pin high level voltage		0.7*V_{DD}	-	V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage		V_{SS}	-	0.3*V_{DD}	
$t_{w(LSE)}$	OSC32_IN high		450	-	-	

$t_{w(LSE)}$	or low time(1)					ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time(1)		-	-	50	
$C_{in(LSE)}$	OSC32_IN input capacitance(1)	-	-	3	-	pF
$DuCy_{(LSE)}$	Duty cycle	-	30	-	70	%
I_L	OSC32_IN input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$	-	-	±1	μA

Note2: *Guaranteed by design, not tested in production.*

Figure14. Low-speed external clock source AC timing diagram



High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 25 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in the table below. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table21. HSE 4-25 MHz oscillator characteristics(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-	4	8	25	MHz
$t_{SU(HSE)}$(3)	Startup time	V_{DD} is stabilized	-	30	-	ms

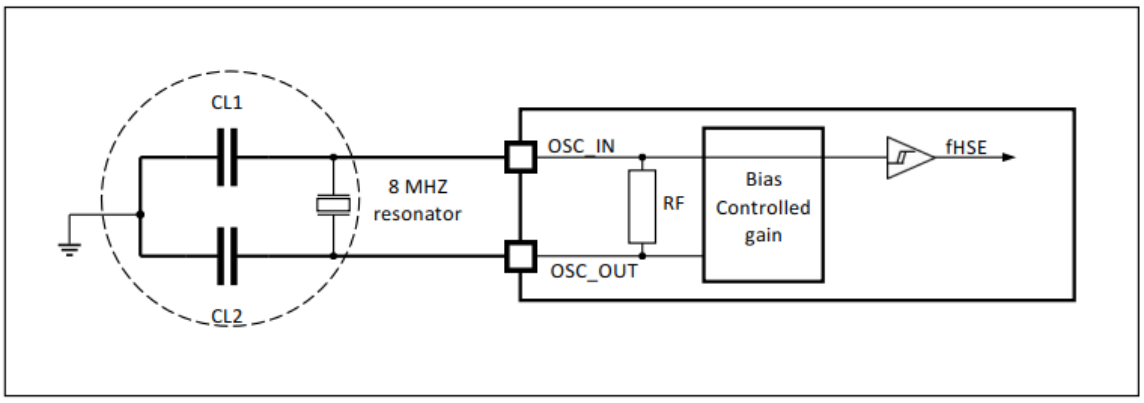
Note1: *Resonator characteristics given by the crystal/ceramic resonator manufacturer.*

Note2: *Guaranteed by characterization results, not tested in production.*

Note3: *$t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer*

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator. C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.

Figure15. Typical application with an 8 MHz crystal



Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in the table below. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table22. LSE oscillator characteristics (f_{LSE} = 32.768 kHz)(1)

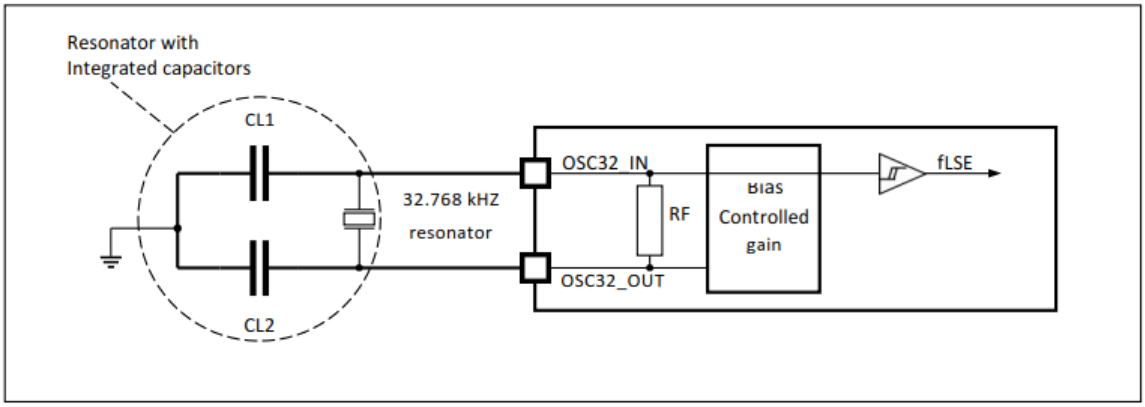
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{SU(LSE)}$	Startup time	V_{DD} is stabilized	-	150	-	ms

Note1: *Guaranteed by characterization results, not tested in production.*

For C_{L1} and C_{L2}, it is recommended to use high-quality ceramic capacitors in the 5 pF to 15 pF range selected to match the requirements of the crystal or resonator. C_{L1} and C_{L2}, are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}.

Load capacitance CL has the following formula: $C_L = C_{L1} \times C_{L2} / (C_{L1} + C_{L2}) + C_{stray}$ where Cstray is the pin capacitance and board or trace PCB-related capacitance. Typically, it is between 2 pF and 7 pF.

Figure16. Typical application with a 32.768 KHz crystal



5.3.6 Internal clock source characteristics

The parameters given in the table below are derived from tests performed under ambient temperature and VDD supply voltage conditions summarized in Table10.

High-speed internal (HSI) RC oscillator

Table23. HSI oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency	-	-	48	-	MHz
$DuCy_{(HSI)}$	Duty cycle	-	45	-	55	%
ACCHSI	Accuracy of the HSI oscillator	User-trimmed with the RCC_CTRL register	-	-	1(2)	%
		TA = -40 ~ 85 °C	-5	-	5	
		TA = 25 °C	-2	-	2	
$t_{SU(HSI)}$(3)	HSI oscillator startup time	-	-	12		μs
$I_{DD(HSI)}$(3)	HSI oscillator power consumption	-	-		250	μA

Note1: *VDD = 3.3 V, TA = -40~85 °C, unless otherwise specified.*

Note2: *Guaranteed by design, not tested in production.*

Note3: *Guaranteed by characterization results, not tested in production.*

Low-speed internal (LSI) RC oscillator

Table24. LSI oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}(2)	Frequency	-	30	40	60	kHz

Note1: *VDD = 3.3 V, TA = -40 to 85 °C, unless otherwise specified.*

Note2: *Guaranteed by characterization results, not tested in production.*

5.3.7 Wakeup time from low-power mode

The wakeup times given in the table below is measured on a wakeup phase with the HSI RC oscillator. The clock source used to wake up the device depends from the current operating mode:

- Stop mode: the clock source is the HSI RC oscillator
- Sleep mode: the clock source is the clock that was set before entering Sleep mode

All timings are derived from tests performed under ambient temperature and VDD supply voltage conditions summarized in Table10.

Table25. Low-power mode wakeup timings

Symbol	Parameter	Typ	Unit
$t_{WUSLEEP}$(1)	Wakeup from Sleep mode	3.3	μs
t_{WUSTOP}(1)	Wakeup from Stop mode (regulator in run mode)	490	μs

Note1: *wakeup times are measured from the wakeup event to the point in which the user application code reads the first instruction.*

5.3.8 PLL characteristics

The parameters given in the table below are derived from tests performed under ambient temperature and VDD supply voltage conditions summarized in Table10.

Table26. PLL characteristics

Symbol	Parameter	MIN	TYP	MAX	Unit
f_{DIV}	Divided reference frequency range	30		375000	KHz
f_{OUT}	Total output frequency range	1.88		375	MHz
P_P	Period jitter (P-P) (max)			+/-2.5% output cycle	ps
I_{PD}	Power dissipation (nom)		20@ 30MHz (/1 output)		uA
t_{RST}	Reset pulse width	5			μs

	(min)				
t_{LOCK}	Lock time (min allowed)	500 div. reference cycles			us

5.3.9 Memory characteristics

The characteristics in Table 30 are given at TA = 25 °C and VDD = 3.3 V.

Table27. Internal Flash memory characteristics

Symbol	Parameter	Conditions	Typ					Unit
			Bank Size					
			1	2	4	8	16	MB
T_{PROG}	Programming time	-	20					μs
t_{ERASE}	Page (4 KB) erase time	-	60	60	50	35		ms
t_{ME}	Mass erase time	-	7	10	15	30	60	s
I_{DD}	Supply current	Programming mode	9.3					mA
		Erase mode	2.2					

Table28. Internal Flash memory endurance and data retention

Symbol	Parameter	Conditions	Min(1)	Typ	Max	Unit
NEND	Endurance	TA = -40 ~ 85 °C	100	-	-	kcycles
t_{RET}	Data retention	TA = 105 °C	20	-	-	years

Note1: *Guaranteed by design, not tested in production.*

5.3.10 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the conditions summarized in Table10. All I/Os are CMOS.

Table29. I/O static characteristics

Symb	Parameter	Min	Typ	Max	Unit
V_{T+}	FT I/O pin input high-level voltage	0.7*VDD		VDD+0.3	V
	NT I/O pin input high-level voltage			5.5	
V_{T-}	I/O pin input low-level voltage	-0.3		0.3*VDD	V
V_{hys}	I/O Schmidt trigger voltage		0.6		V

	hysteresis				
I_I	Input Leakage Current@VI=3.3V or 0V@125℃		2n	51n	A
	Input Leakage Current@VI=3.3V or 0V@85℃		2n	19n	A
I_{OZ}	Tri-state Output Leakage Current @Vo=3.3V or 0V		2n	51n	A
R_{PU}	Pull-up Resistor	25K	40k	60K	Ω
R_{PD}	Pull-down Resistor	25k	40K	75K	Ω
V_{OL}	Output Low Voltage			0.4	V
V_{OH}	Output High Voltage	2.4			V
I_{OL}	Low Level Output Current @VOL(max)	9.21	14.1	18.96	mA
I_{OH}	High Level Output Current @VOH(min)	22.17	31.45	40.44	mA

Note1: *The following IOs: IOA0, IOA1, IOC0, IOC4, IOC13, IOC14, IOC15, IOF0, IOF1, IOF2, IOF3, IOF4, IOF5 do not support the input of Schmitt hysteresis.*

5.3.11 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, RPU (see the table below).

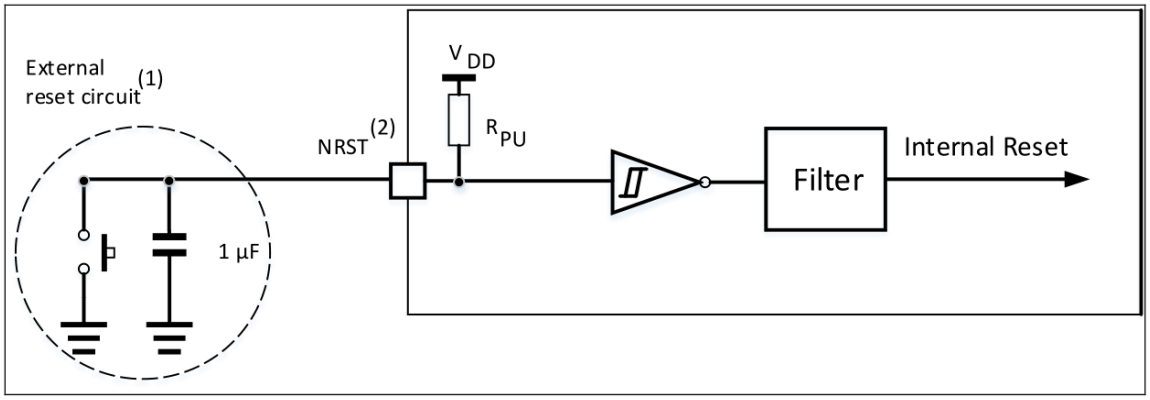
Unless otherwise specified, the parameters given in the table below are derived from tests performed under ambient temperature and VDD supply voltage conditions summarized in Table10.

Table30. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$(1)	NRST input low level voltage	-	-0.5	-	0.3*VDD	V
$V_{IH(NRST)}$(1)	NRST input high level voltage	-	0.7* VDD	-	5.5	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	600	-	mV
R_{PU}	Weak pull-up equivalent resistor	$V_{IN} = V_{SS}$	25	40	60	kΩ
$V_{F(NRST)}$(1)	NRST input filtered pulse	-	-		66	μs
$V_{NF(NRST)}$(1)	NRST input not filtered pulse	-	133		-	μs

Note1: *Guaranteed by design.*

Figure17. Recommended NRST pin protection



Note1: *The reset network protects the device against parasitic resets.*

Note2: *The user must ensure that the level on the NRST pin can go below the VIL (NRST) max level specified in Table 40. Otherwise the reset will not be taken into account by the device.*

5.3.12 TMR timer characteristics

The parameters given in the table below are guaranteed by design.

Refer to 5.3.10 for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table31. TMRx(1) characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TMR)}$	Timer resolution tim	-	1	-	$t_{TMRxCLK}$
		$f_{TMRxCLK}$ = 200 MHz	5	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	0	$f_{TMRxCLK}/2$	MHz
			0	50	MHz

Note1: *TMRx is used as a general term to refer to the TMR1 to TMR14.*

5.3.13 Communications interfaces

I2C interface characteristics

The V32G410x I2C interface meets the requirements of the standard I2C communication protocol with the following restrictions: the I/O pins SDA and SCL mapped to are not ”true” open-drain.

When configured as open-drain, the PMOS connected between the I/O pin and VDD is disabled, but is still present.

The I2C characteristics are described in the table below. Refer also to 5.3.12 I/O port

characteristics for more details on the input/output alternate function characteristics (SDA and SCL).

Table32. I2C characteristics

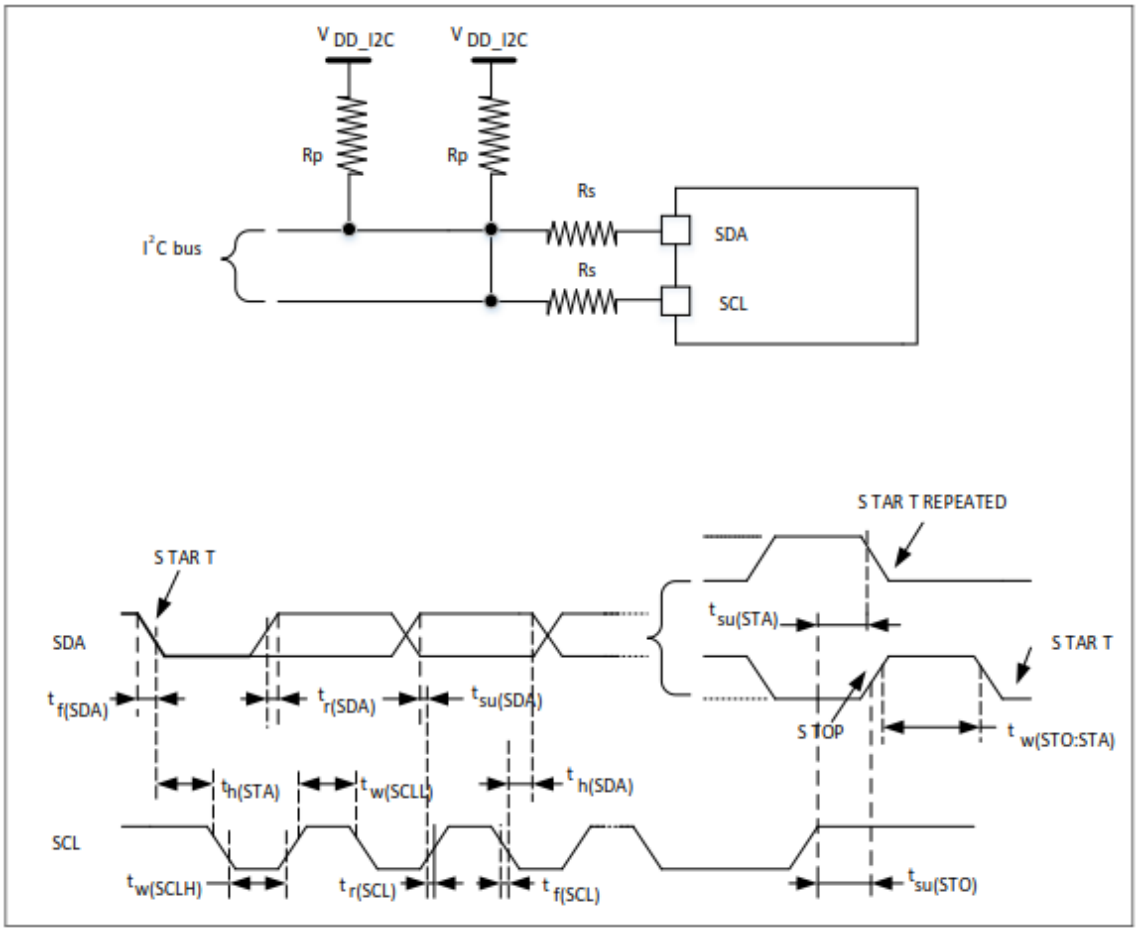
Symbol	Parameter	Standard mode I2C(1)(2)		Fast mode I2C(1)(2)		Unit
		Min	Max	Min	Max	
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	μs
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	
$t_{su(SDA)}$	SDA setup time	250	-	100	-	ns
$t_{h(SDA)}$	SDA data hold time	-	3450(3)	-	900(3)	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time	-	1000	-	300	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time	-	300	-	300	
$t_{h(STA)}$	Start condition hold time	4.0	-	0.6	-	μs
$t_{su(STA)}$	Repeated Start condition setup time	4.7	-	0.6	-	
$t_{su(STO)}$	Stop condition setup time	4.0	-	0.6	-	μs
$t_{w(STO:STA)}$	Stop to Start condition time (bus free)	4.7	-	1.3	-	μs
C_b	Capacitive load for each bus line	-	400	-	400	pF

Note1: *Guaranteed by design, not tested in production.*

Note2: *f_{PCLK1} must be at least 2 MHz to achieve standard mode I2C frequencies. It must be at least 4 MHz to achieve the fast mode I2C frequencies.*

Note3: *The device must internally provide a hold time of at least 300ns for the SDA signal in order to bridge the undefined region on the falling edge of SCL.*

Figure18. I2C bus AC waveforms and measurement circuit(1)



Note1: *Measurement points are done at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.*

Table33. SCL frequency (f_{PCLK1} = 36 MHz, VDD = 3.3 V)(1)(2)

f_{SCL}(kHz)	I2C_CLKCTRL value
	RP = 4.7 kΩ
400	0x801E
300	0x8028
200	0x803C
100	0x00B4
50	0x0168
20	0x0384

Note1: *R_P = External pull-up resistance, fSCL = I2C speed.*

Note2: *For speeds around 200 kHz, the tolerance on the achieved speed is of ±5%. For other speed ranges, the tolerance on the achieved speed ±2%. These variations depend on the accuracy of the external components used to design the application.*

SPI-I2S characteristics

Unless otherwise specified, the parameters given in Table 44 for SPI or in Table 45 for I2S are derived from tests performed under ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in Table10.

Refer to 5.3.10 for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI and WS, CK, SD for I2S).

Table34. SPI characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $(1/t_{c(SCK)})(1)$	SPI clock frequency(2)(3)	Master mode	-	50	MHz
		Slave mode	-	$f_{PCLK}/2$	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 30 pF	-	8	ns
$t_{su(NSS)}$ (1)	NSS setup time	Slave mode	$4t_{PCLK}$	-	ns
$t_{h(NSS)}$(1)	NSS hold time	Slave mode	$2t_{PCLK}$	-	ns
$t_{w(SCKH)}$(1) $t_{w(SCKL)}$(1)	SCK high and low time	Master mode, f_{PCLK} = 90 MHz, prescaler = 4	22	32	ns
$t_{su(MI)}$(1)	Data input setup time	Master mode	5	-	ns
$t_{su(SI)}$ (1)		Slave mode	5	-	
$t_{h(MI)}$(1)	Data input setup time	Master mode	5	-	ns
$t_{h(SI)}$ (1)		Slave mode	4	-	
$t_{a(SO)}$(1)(4)	Data output access time	Slave mode, fPCLK = 20 MHz	0	$3t_{PCLK}$	ns
$t_{dis(SO)}$(1)(5)	Data output disable time	Slave mode	2	10	ns
$t_{v(SO)}$(1)	Data output valid time	Slave mode (after enable edge)	-	25	ns
$t_{v(MO)}$(1)	Data output valid time	Master mode (after enable edge)	-	5	ns
$t_{h(SO)}$(1)	Data output hold time	Slave mode (after enable edge)	15	-	ns
$t_{h(MO)}$(1)		Master mode (after enable edge)	2	-	

Note1: *Guaranteed by characterization results, not tested in production.*

Note2: *Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.*

Note3: *Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z.*

Figure19. SPI timing diagram - slave mode and CPHA = 0

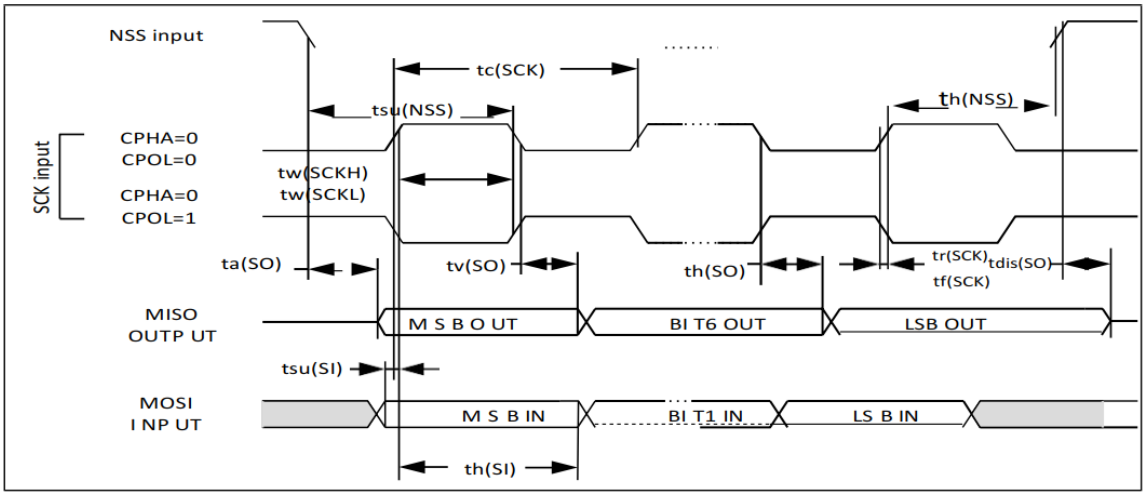
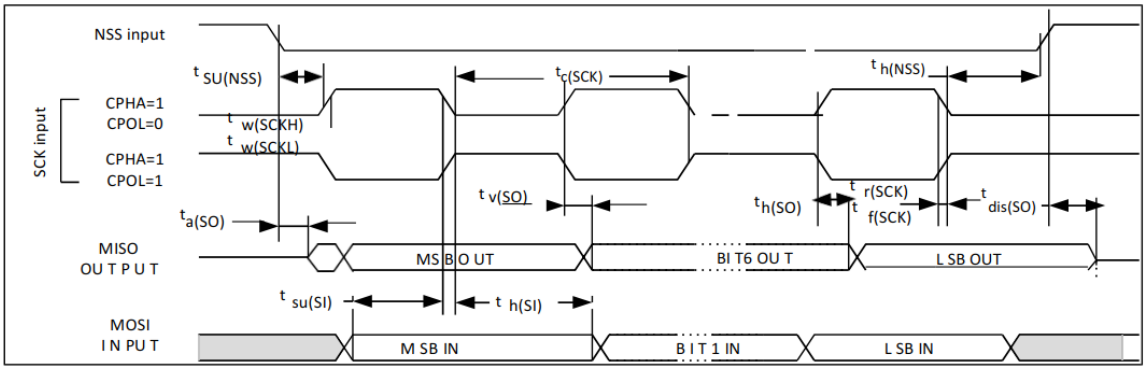
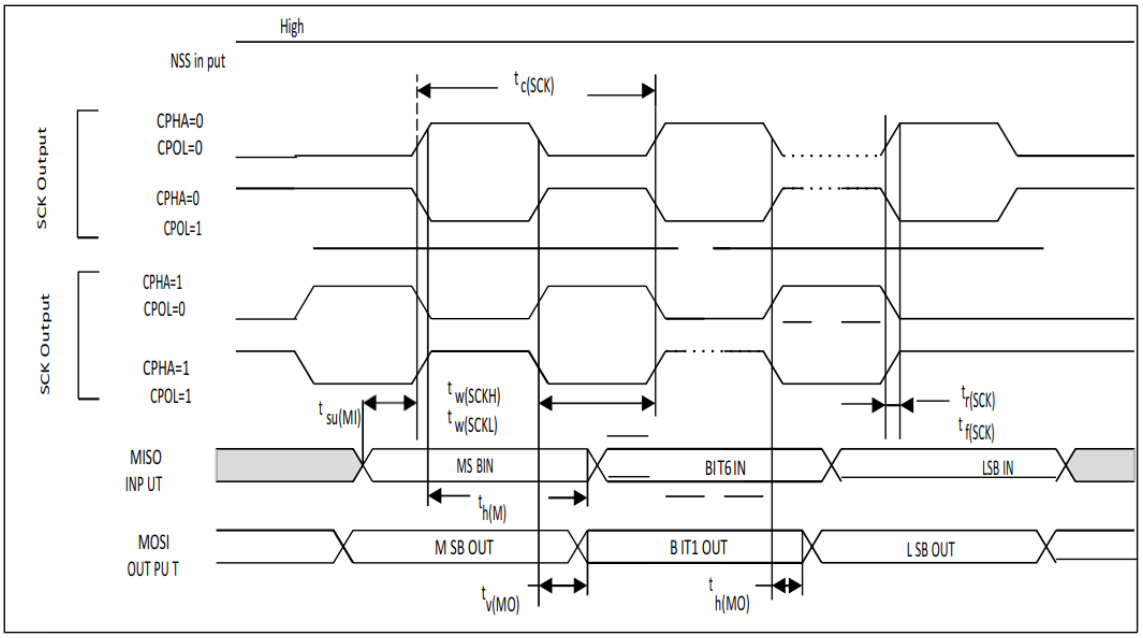


Figure20. SPI timing diagram - slave mode and CPHA = 1(1)



Note1: *Measurement points are done at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.*

Figure21. SPI timing diagram - master mode (1)



Note1: *Measurement points are done at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.*

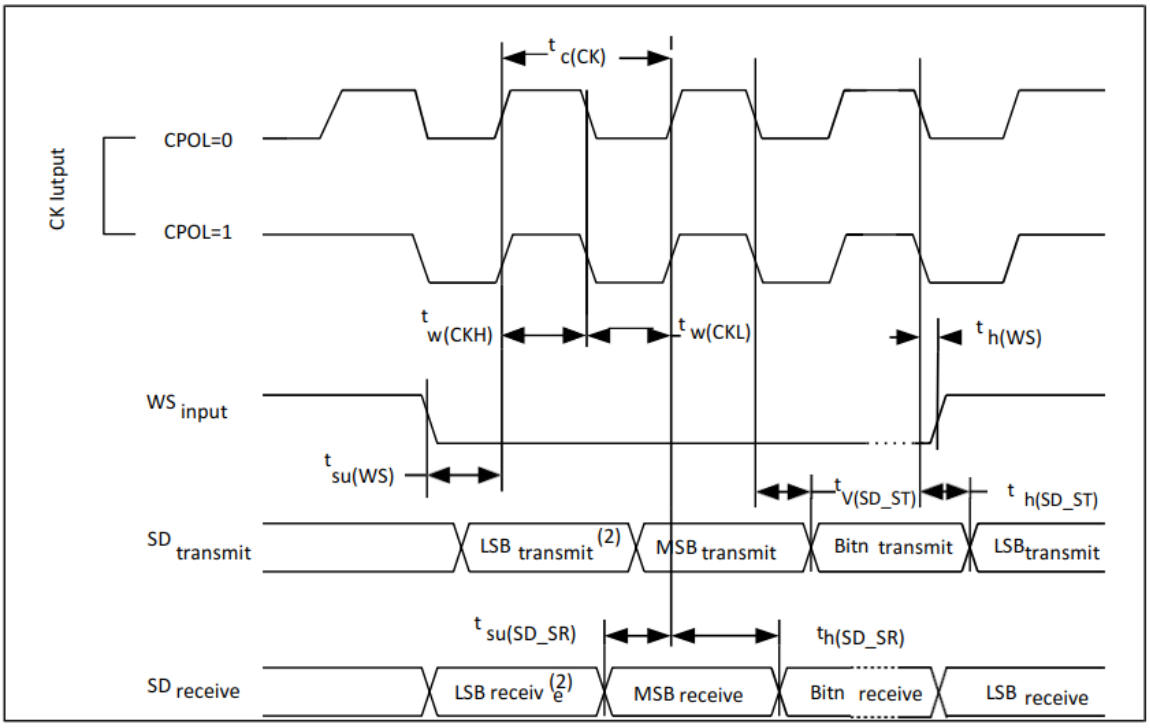
Table35. I2S characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{CK} $1/t_{c(CK)}$	I2S clock frequency	Master mode (data: 16 bits, audio frequency = 48 kHz)	1.522	1.525	MHz
		Slave mode	0	6.5	
$t_{r(CK)}$ $t_{f(CK)}$	I2S clock rise and fall time	Capacitive load: C = 50 pF	-	8	ns
$t_{v(WS)}$ (1)	WS valid time	Master mode	3	-	
$t_{h(WS)}$(1)	WS hold time	Master mode	2	-	
$t_{su(WS)}$(1)	WS setup time	Slave mode	4	-	
$t_{h(WS)}$(1)	WS hold time	Slave mode	0	-	
$t_{w(CKH)}$(1)	CK high and low time	Master fPCLK = 16 MHz, audio frequency = 48 kHz	312.5	-	
$t_{w(CKL)}$(1)			345	-	
$t_{su(SD\_MR)}$(1)	Data input setup time	Master receiver	6.5	-	
$t_{su(SD\_SR)}$(1)		Slave receiver	1.5	-	
$t_{h(SD\_MR)}$(1)(2)	Data input hold time	Master receiver	0	-	
$t_{h(SD\_SR)}$(1)(2)		Slave receiver	0.5	-	
$t_{v(SD\_ST)}$(1)(2)	Data output valid time	Slave transmitter (after enable edge)	-	18	
$t_{h(SD\_ST)}$(1)	Data output hold time	Slave transmitter (after enable edge)	11	-	
$t_{v(SD\_MT)}$(1)(2)	Data output valid time	Master transmitter (after enable edge)	-	3	
$t_{h(SD\_MT)}$(1)	Data output hold time	Master transmitter (after enable edge)	0	-	

Note1: *Guaranteed by design and/or characterization results.*

Note2: *Depends on f_{PCLK}. For example, if f_{PCLK}=8 MHz, then T_{PCLK} = 1/f_{PCLK} =125 ns.*

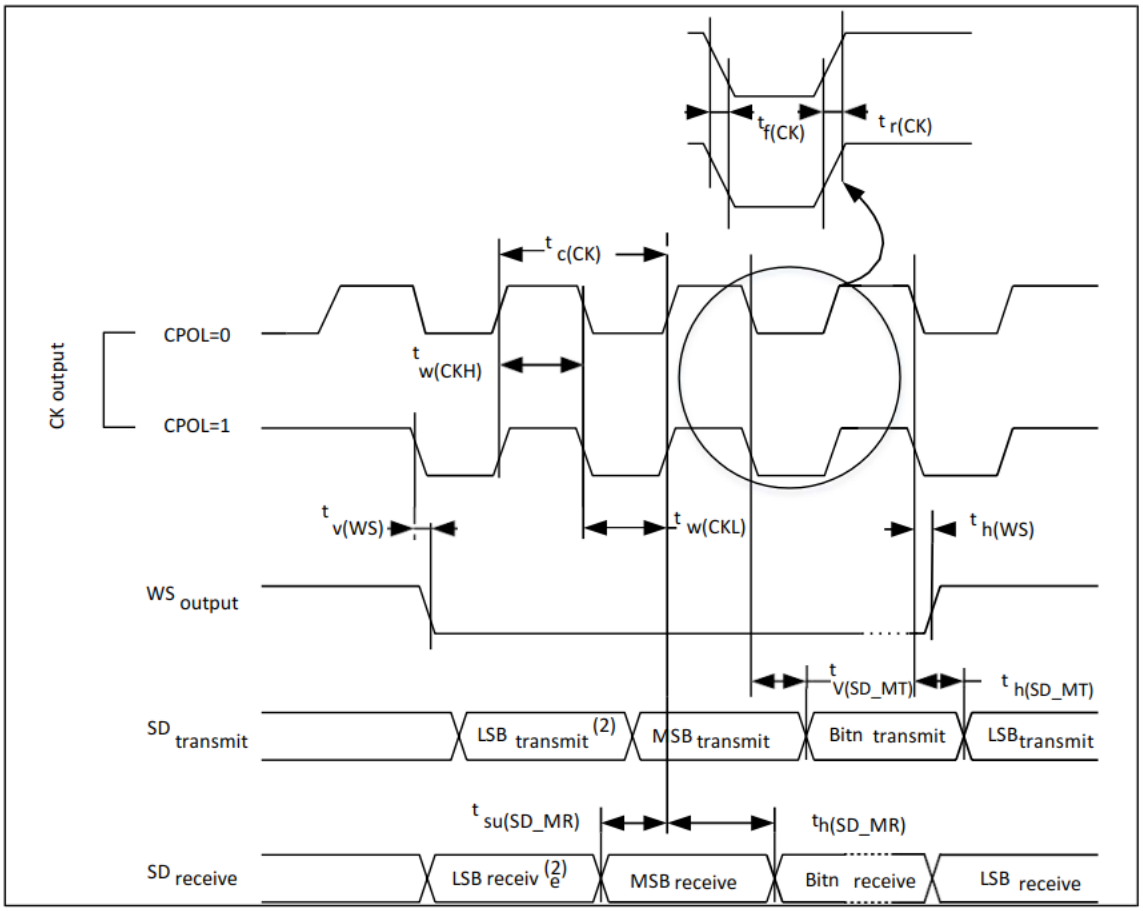
Figure22. I2S slave timing diagram (Philips protocol)(1)



Note1: *Measurement points are done at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.*

Note2: *LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.*

Figure23. I2S master timing diagram (Philips protocol)(1)



Note1: *Measurement points are done at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.*

Note2: *LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.*

CAN (controller area network) interface

Refer to 5.3.10 for more details on the input/output alternate function characteristics (CAN_TX and CAN_RX).

5.3.14 12-bit ADC characteristics

Table36. ADC Characteristics

Parameter	Condition	Minimum	Typical	Maximum	Unit
Power supply voltage					
AVDD_ADC	-	2.6	3.3	3.63	V
VDD_ADC	-	0.81	1.1	1.21	V
IAVDD_ADC	@ fs=2msps		500		uA
IVREFP_ADC	@ fs=2msps		80		uA
IVDD_ADC	@ fs=2msps		5		uA
PowerDown			30		nA
Reference voltage					
VEREFP_ADC	-	1.8	3.3	3.63	V

VREFN_ADC	-		0		V
Analog input					
Input range	ADC_SDIF=0	VREFN		VREFP	V
	ADC_SDIF=1	2* (VREFP-VREFN)			V
Input common mode		(VREFP-VREFN)/2			V
Input sampling capacitor	Single-ended		5		pF
Input equivalent impedance				1000	Ω
Time sequence					
Clock cycle (Ts)				3333	nS
Duty cycle		40%	50%	60%	Ts
SOC setup time			2		nS
SOC hold time			2		nS
Sampling time			1.5		Ts
Sampling + conversion time			14		Ts
Channel selection to EOC time		1.5		11	Ts
ADC Performance (Single Ended) 1					
THD			-75		dB
ENOB			10.5		bit
SNDR			65		dB
DNL			± 1.5		LSB
INL			± 2		LSB
Calibrable offset		-16		16	LSB
ADC Performance (Differential) 1					
THD			-75		dB
ENOB			11		bit
SNDR			68		dB
DNL			± 1.5		LSB
INL			± 2		LSB
Calibrable offset		-16		16	LSB

Note1: *Fin=100kHz, fs=28Msps, power supply voltage 2.97 ~ 3.63 V,-40 ℃ ~ 125 ℃;*

Note2: *In the case of single-ended input, the performance of odd channels passes through two-stage switches, and the performance decreases slightly;*

5.3.15 Temperature sensor characteristics

Table37. Temperature sensor characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{SENSE} linearity with temperature	-	±1	±2	ºC
Avg_Slope(1)(2)	Average slope		3.5		mV/ºC
V_{25}(1)(2)	Sample value at 25 ºC		1.05		

t_{START}(3)	Startup time	-	-	6	μs
T_{S_temp}(3)(4)	ADC sampling time when reading the temperature	2	-	-	μs

Note1: *Guaranteed by characterization results, not tested in production.*

Note2: *The temperature sensor output voltage changes linearly with temperature. The offset of this line varies from chip to chip due to process variation (up to 50 °C from one chip to another). The internal temperature sensor is more suited to applications that detect temperature variations instead of absolute temperatures. If accurate temperature readings are needed, an external temperature sensor part should be used.*

Note3: *Guaranteed by design, not tested in production.*

Note4: *Shortest sampling time can be determined in the application by multiple iterations.*

Obtain the temperature using the following formula:

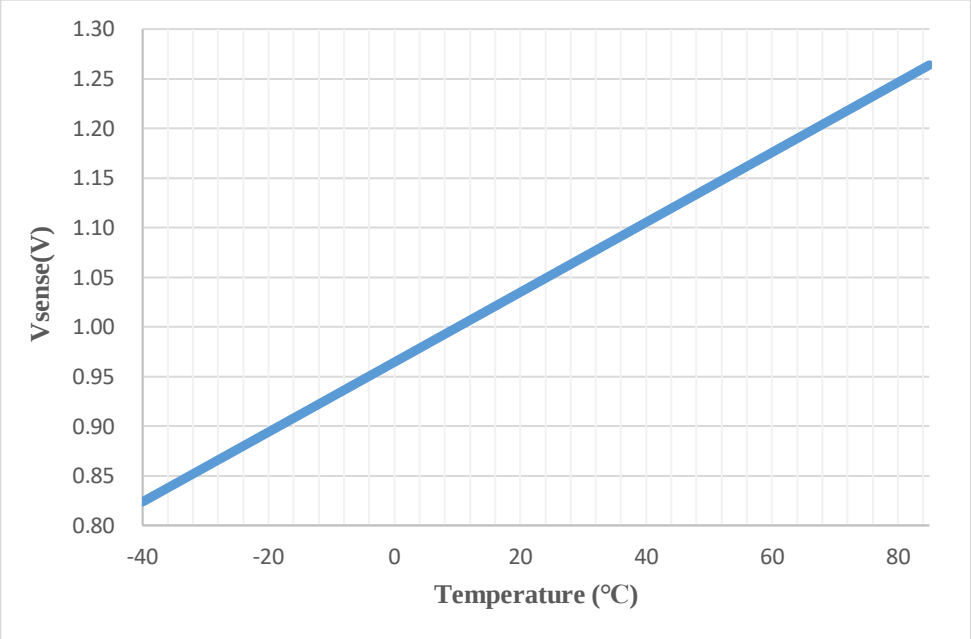
Temperature (in °C) = {(Vsense - V25) / Avg_Slope} +25

Where,

V_{25} = V_{SENSE} value for 25° C and

Avg_Slope = Average Slope for curve between Temperature vs. V_{SENSE} (given in mV/° C).

Figure24. V_{SENSE} vs. temperature



5.4 ESD electricial character

Table38. ESD electricial parameter

V_{ESD}	**Human Body Model(HBM)**	-4000	4000	V

	Charged Device Model(CDM)	-1000	1000	V

6 stroage

6.1 Hmidity sensitivity

Table39. MSL summary

MSL	Out-of-bag floor life	Comments
1	Unlimited	≤30°C / 85%RH
2	1 year	≤30°C / 60%RH
2a	4 weeks	≤30°C / 60%RH
3	168 hours	≤30°C / 60%RH
4	72 hours	≤30°C / 60%RH
5	48 hours	≤30°C / 60%RH
5a	24 hours	≤30°C / 60%RH
6	Time on Label(TOL)	≤30°C / 60%RH

Note1: *The moisture sensitivity level of V32G410x is MSL3.*

6.2 Storage conditions

Table40. Bagged storage conditions

Packaging method	method Vacuum
Storage temperature	-55°C ~150°C

7 Reflow soldering process

All Wangao chips provided to customers are lead-free RoHS compliant products.

The reflow soldering process recommended in this article is a lead-free reflow soldering process, which is suitable for the pure lead-free process of lead-free solder paste. If customers need to use lead solder paste, please contact the smart chip FAE connect.

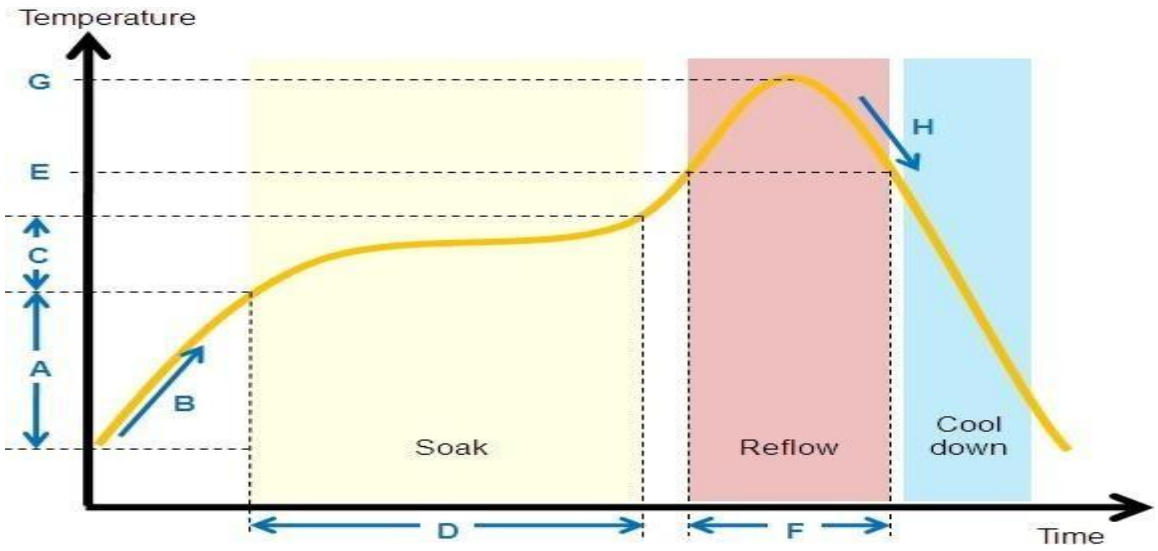
See Table41 for lead-free reflow profile conditions. This table is for reference only.

Table41. Reflow profile conditions

	QTI typical SMT reflow profile conditions(for reference only)	
	Step	**Reflow condition**
Environment	N2 purge reflow usage (yes/no)	Yes, N2 purge used
	If yes, O2 ppm level	O2 < 1500 ppm
A	Preheat ramp up temperature range	25°C -> 150°C
B	Preheat ramp up rate	1.5~2.5 °C /sec
C	Soak temperature range	150°C -> 190°C
D	Soak time	80~110 sec
E	Liquidus temperature	217°C
F	Time above liquidus	60-90 sec
G	Peak temperature	240-250°C
H	Cool down temperature rate	≤4°C /sec

The figure below shows a typical lead-free reflow mode.

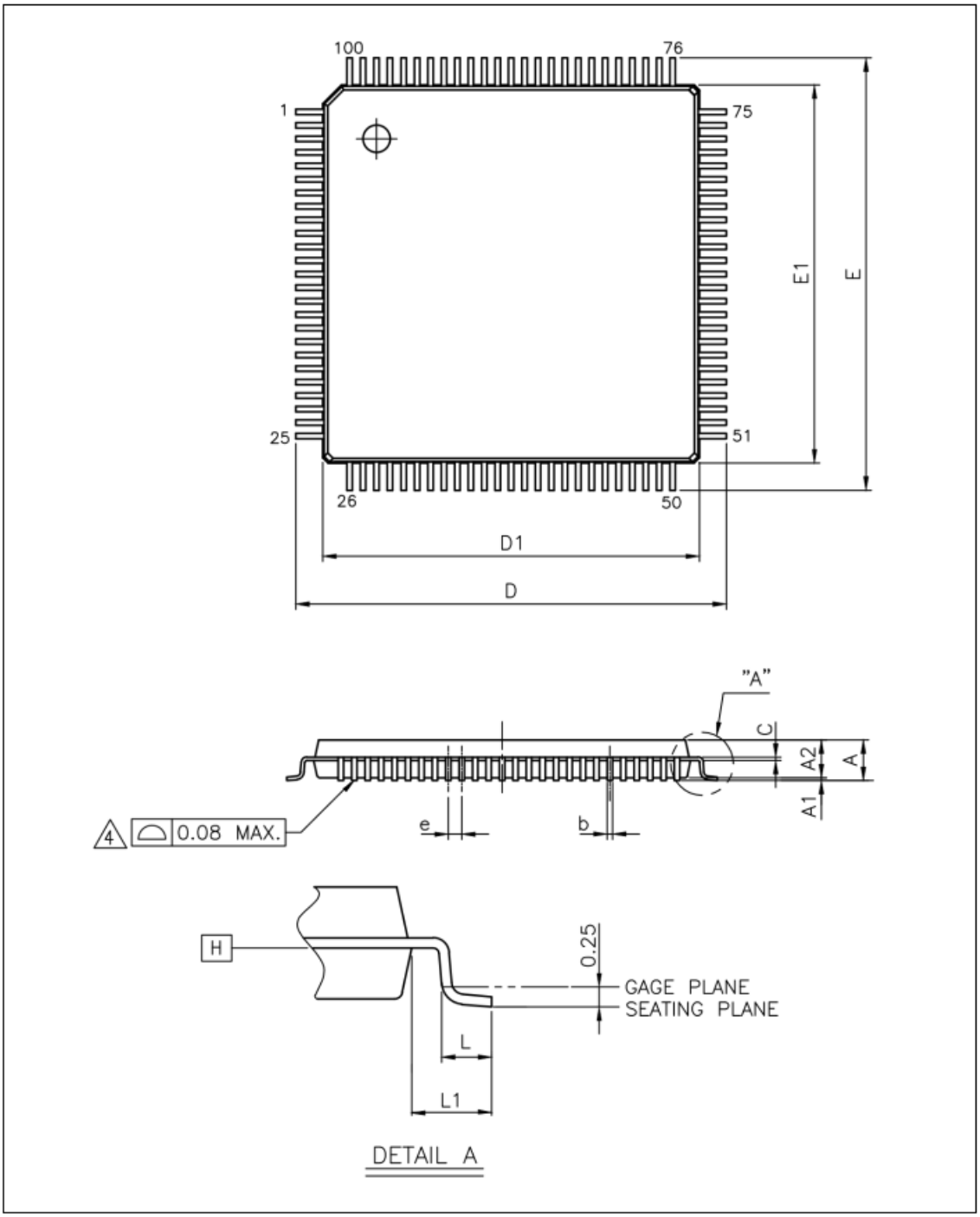
Figure25. A typical lead-free reflow mode


Temperature
G
E
C
A
B
H
Soak
Reflow
Cool
down
D
F
Time

8 Package information

8.1 LQFP100 14 x 14 mm package information

Figure26. LQFP100 – 14 x 14 mm 100 pin package outline



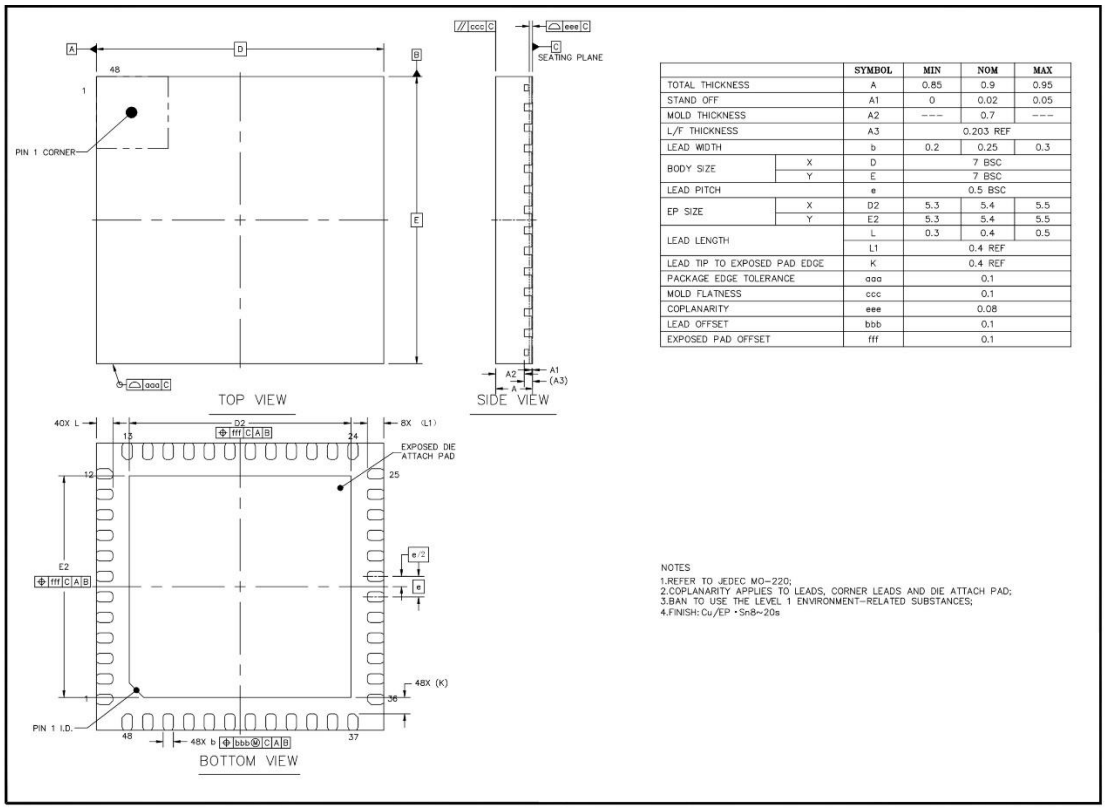
Note1: *Drawing is not in scale.*

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.60	-	-	0.063
A1	0.05	-	0.15	0.002	-	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.20	0.26	0.007	0.008	0.010
c	0.10	0.127	0.20	0.004	0.005	0.008
D	16.00 BSC.			0.630 BSC.		
D1	14.00 BSC.			0.551 BSC.		
E	16.00 BSC.			0.630 BSC.		
E1	14.00 BSC.			0.551 BSC.		
e	0.50 BSC.			0.020 BSC.		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF.			0.039 REF.		

Note1: *Values in inches are converted from mm and rounded to 3 decimal digits.*

8.3 QFN48 7 x 7 mm package information

Figure27. QFN48 – 7 x 7 mm 48 pin package outline

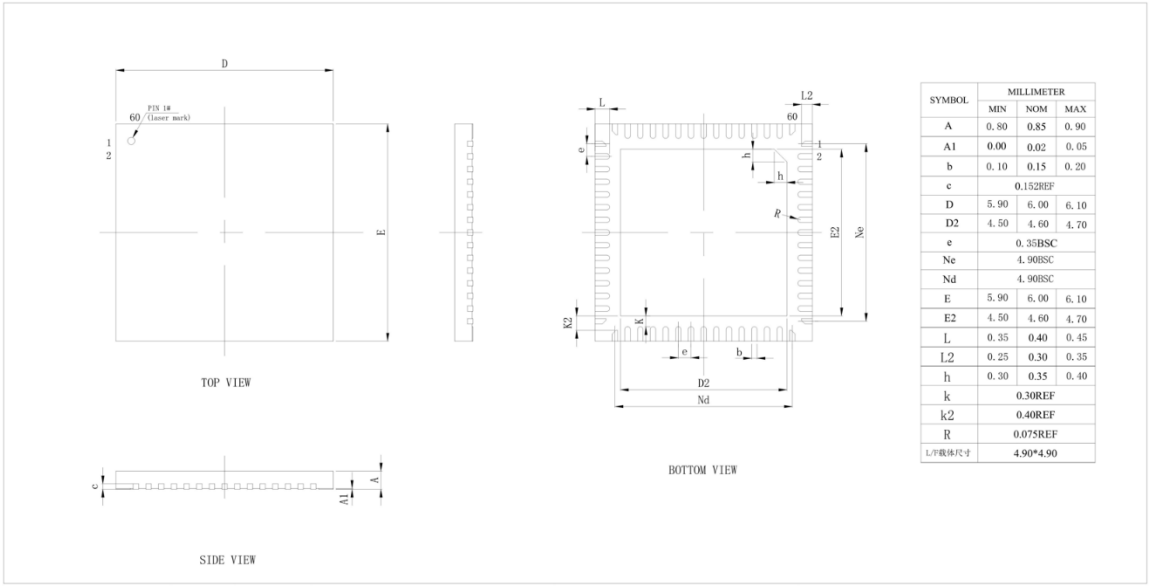


		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.85	0.9	0.95
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.7	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		7 BSC	
	Y	E		7 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	D2	5.3	5.4	5.5
	Y	E2	5.3	5.4	5.5
LEAD LENGTH		L	0.3	0.4	0.5
		L1		0.4 REF	
LEAD TIP TO EXPOSED PAD EDGE		K		0.4 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.1	
EXPOSED PAD OFFSET		fff		0.1	

NOTES
1.REFER TO JEDEC MO-220;
2.COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD;
3.BAN TO USE THE LEVEL 1 ENVIRONMENT-RELATED SUBSTANCES;
4.FINISH: Cu/EP • Sn8~20s

8.4 QFN60 6 x 6 mm package information

Figure28. QFN60 – 6 x 6 mm 60 pin package outline



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.10	0.15	0.20
e	0.152REF		
D	5.90	6.00	6.10
D2	4.50	4.60	4.70
e	0.35BSC		
Ne	4.90BSC		
Nd	4.90BSC		
E	5.90	6.00	6.10
E2	4.50	4.60	4.70
L	0.35	0.40	0.45
L2	0.25	0.30	0.35
h	0.30	0.35	0.40
k	0.30REF		
k2	0.40REF		
R	0.075REF		
L/F载体尺寸	4.90*4.90		

8.5 Thermal characteristics

The maximum chip junction temperature (T_{Jmax}) must never exceed the values given in Table9.

The maximum chip-junction temperature, TJmax, in degrees Celsius, may be calculated using the following equation:

$T_{jmax} = T_{amax} + (P_{dmax} \times \Theta_{JA})$

Where:

- Tamax is the maximum ambient temperature in °C,
- ΘJA is the package junction-to-ambient thermal resistance, in °C/W,
- Pdmax is the sum of PINTmax and PI/Omax (Pdmax = PINTmax + PI/Omax),
- PINTmax is the product of IDD and VDD, expressed in Watts. This is the maximum chip internal power.

$P_{I/Omax}$ represents the maximum power dissipation on output pins where:

$P_{I/Omax} = \Sigma(V_{OL} \times I_{OL}) + \Sigma((V_{DD} - V_{OH}) \times I_{OH})$,

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table42. Package thermal characteristics

symbol	Parameter	value	unit
Θ_{JA}	Thermal impedance from junction to environment	53.6	°C/W

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