V98XX Datasheet

Specifications are subject to change without notice.

Revision History

Date	Version	Description
2015.06.05	0.1	Initial release
2015.10.08	0.2	• Modified typical current load in sleeping mode from 10μA to 12μA • Modified "0b000" to "0b001" in Table 18-10 • Updated Table 4-3 Allocation of Info Area • Modified "SPC_FNC" to "SPCFNC" in Table 4-2 • Modified function description of "FWC" • Modified description of "CFWKEN" in Table 5-5
2015.11.12	0.3	• Updated Figure 4-2 Data Memory
2016.01.06	0.4	• Set the bit of "BGPCHOPN" to '0' in Table 18-10 BandGap Control Register (CtrlBGP, 0x2862) to improve the temperature measurement performance. • Modified the registers and related content of temperature measurement and temperature calibration. • Updated Table 17-10 RTC Timing Registers • Emphasized the setting of time information in sequence and at one time.
2016.10.01	0.5	• Modified "IOP14" to "P14WK", "PLLCNT" to "PLLCNTST" • Added V98XX Resource Comparison • Updated operating current in sleeping mode to 10μA and maximum current in sleeping mode to 14.5μA.
2016.12.02	0.6	• Updated pin8 to NC • Updated 10.16.3 Measuring Battery Voltage and External Voltage
2018.05.31	3.0	• Modify the formula of Phase Compensation • Add V9811S/V9811A/V9811B/V9821/V9821S/V9881D
2018.09.02	3.1	• Modify storage temperature to - 55 ~ 150 C • Modify the input range of current and voltage channels • Modify the maximum input voltage of analog comparator to LDO33 • Modify the LCD Drive Waveform
2021.03.01	3.2	• Modify V9811B Outline Dimensions

2021.04.15	3.3	• Update IEC Standard·
2021.06.02	3.4	• Update document format

General Description

V98XX is a single-phase energy metering SoC chip, featuring very low power consumption and high performance. It integrates Analog Front-End (AFE), energy metering architecture, enhanced 8052 MCU core, RTC, WDT, Flash memory, RAM, and LCD driver. It can be used for the single-phase multi-functional energy meter applications.

Features

- Optional power supply 3.3 V or 5 V, wide input range: 2.5 V to 5.5 V
- Reference voltage: 1.185 V (Typical drift 10 ppm/°C), interrupt triggered by external capacitor leakage
- Typical current load in full operation mode: 5.5 mA
- Typical current load in sleeping mode: 10 μA
- Supporting anti-tampering energy metering application
- Operating temperature: -40 °C ~ +85 °C
- Storage temperature: -55 °C ~ +150 °C
- Energy metering features:
  - Four independent oversampling Σ/Δ ADCs
    - ✓ One voltage channel
    - ✓ Two current channels, supporting shunt or CT for current sensing
    - ✓ One multifunctional channel for various signal measurements
  - High metering accuracy:
    - ✓ Exceeding requirements of IEC 62053-21:2020/ IEC 62053-22:2020 and IEC 62053-23:2020
    - ✓ Less than 0.1% error on active energy metering over dynamic range of 5000:1
    - ✓ Less than 0.1% error on reactive energy metering over dynamic range of 3000:1
    - ✓ Less than 0.5% error on current/voltage RMS calculation over dynamic range of 1000:1
  - Various measurements:
    - ✓ Raw waveform and DC component of current and voltage signals
    - ✓ Instantaneous/Average and active/reactive power
    - ✓ Positive/Negative and active/reactive energy
    - ✓ Average apparent power
    - ✓ Instantaneous/Average current and voltage RMS
    - ✓ Line frequency
    - ✓ Temperature with measurement accuracy of ±1°C
    - ✓ Battery voltage and external voltage signals
  - Two current inputs for active energy metering, or one current input for active and reactive energy metering
  - Programmable energy metering modes:
    - ✓ Accumulating power, current RMS, or a constant for energy metering
    - ✓ Accumulating energy at a configurable frequency

- Calibrating meters via software:
  - ✓ Phase compensation over a range of ±1.4° (min.), resolution of 0.0055°/lsb (min.).
  - ✓ Gain calibration of RMS and power, and offset calibration of power
  - ✓ Accelerating meter calibration when low current is applied
- CF pulse output and interrupt with configurable pulse width
- Zero-crossing interrupt
- Speeding current detection to lower power consumption
- Programmable threshold for no-load detection

– MCU and peripherals:

- High performance 8-bit 8052 MCU core, with programmable operation frequency, up to 26 MHz/6.5 mips
- One additional comparator
- Integrated oscillator, only one external 32768-Hz crystal is needed to generate crystal frequency
- Crystal supervised: Internal RC oscillator as a replacement when crystal oscillator stops running
- Integrated RTC and temperature sensor, digital crystal frequency compensation for calibration over temperature variation
- 128-KB Flash memory, ISP and IAP supported, with write protection and encryption function
- 4-KB extended SRAM memory
- Up to five UART serial interfaces, one supporting IR communication
- Up to two enhanced UART (EUART) serial interfaces, ISO/IEC 7816-3 compliant
- One GPSI (General-Purpose Serial Interface), I^2C compliant
- Up to 54 programmable GPIOs, with port interrupt
- Up to 16 fast IOs
- Up to 12 hardware timers
- Supporting PWM output
- LCD driver:
  - ✓ Up to 4×40, 6×38, or 8×36 segments
  - ✓ 1/3 bias or 1/4 bias ratio
  - ✓ Configurable frame frequency
  - ✓ Configurable drive voltage over a range of 2.7 V ~ 3.3 V, resolution 100 mV/lsb
- Various sleep/wakeup methods, configurable wakeup with reset
- Independent Watch-Dog Timer (WDT)
- Debugging via JTAG interfaces in real-time

V98XX Resource Comparison

Peripherals	V9801S	V9811S	V9811A	V9811B	V9821	V9821S	V9881D
Package	LQFP100	LQFP64	LQFP64	LQFP64(7*7)	TQFP48	TQFP48	SSOP24
Flash memory	128KB	128KB	64KB	64KB	64KB	64KB	64KB
SRAM	4KB	4KB	4KB	4KB	4KB	4KB	4KB

UART	Up to 5 UART serial interfaces, one supporting IR communication; up to 2 EUART, supporting ISO/IEC 7816-3 protocol	Up to 4 UART serial interfaces, one supporting IR communication	Up to 4 UART serial interfaces, one supporting IR communication	Up to 4 UART serial interfaces, one supporting IR communication	Up to 3 UART serial interfaces, one supporting IR communication	Up to 3 UART serial interfaces, one supporting IR communication	1 UART serial interfaces, supporting IR communication
GPIO	54	43	43	43	32	32	8
Rapid IO port	16	6	6	6	2	1	0
LCD	Up to 4×40/6×38/8×36 segments, 1/3 bias or 1/4 bias ratio	Up to 4×24/6×22/8×20 segments, 1/3 bias or 1/4 bias ratio	Up to 4×24/6×22/8×20 segments, 1/3 bias or 1/4 bias ratio	Up to 4×24/6×22/8×20 segments, 1/3 bias or 1/4 bias ratio	Up to 4×17/6×15/8×13 segments, 1/3 Bias or 1/4 Bias ratio	Up to 4×19/6×17/8×15 segments, 1/3 Bias or 1/4 Bias ratio	0

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1.Electrical Characteristics

1.1. Absolute Maximum Ratings

Operating circumstance exceeding **"Absolute Maximum Ratings"** may cause the permanent damage to the device.

Table 1-1 Absolut Maximum Ratings

Parameter	Min.	Max.	Unit	Description
Analog Power Supply	-0.3	+8.0	V	Relative to ground.
Analog Current Input	-0.3	+5.0	V	Relative to ground.
Analog Voltage Input	-0.3	+5.0	V	Relative to ground.
Operating Temperature	-40	+85	˚C	
Storage Temperature	-40	+125	˚C	
Junction Temperature	-	150	ºC	
Lead Temperature (Soldering, 10 s)	-	300	ºC	

1.2. Energy Metering Specifications

All typical specifications are at TA = 25 °C, VDD5 = 5.0 V ±10%, and f_{MTCLK} = 3.2768 MHz, unless otherwise noted.

Table 1-2 Energy Metering Specifications

Parameter	Typ.	Unit	Description
Phase Error Between Channels			
PF=0.8 Capacitive	±0.05	Degree	37° phase lead in current
PF=0.5 Inductive	±0.05	Degree	60° phase lag in current
Active Energy Metering			
Error	0.1	%	Dynamic range of 5000:1@25°C
Bandwidth	1.6	kHz	
Reactive Energy Metering			
Error	0.1	%	Dynamic range of 3000:1@25°C
Bandwidth	1.6	kHz	
Apparent Power Metering			

Parameter	Typ.	Unit	Description
Error	0.5	%	Dynamic range of 1000:1@25°C
Voltage/Current RMS Metering			
Error	0.5	%	Dynamic range of 1000:1@25°C
Bandwidth	1.6	kHz	
CF Pulse Output			
Maximum Output Frequency	6.4	kHz	
Duty Cycle	50%		When active high pulse width < 80 ms.
Active High Pulse Width	80	ms	Configurable
Frequency Measurement Resolution	0.05	Hz/lsb	Measurement range: 35 Hz ~ 75 Hz
Temperature Measurement Error	±1	°C	Measurement range: -40 °C ~ +85 °C

1.3. Analog Specifications

All maximum and minimum specifications apply over the entire recommended operation range (T = -40 °C ~ +85 °C, VDD5 = 3.3 V or 5.0 V), unless otherwise noted. All typical specifications are at TA = 25 °C and VDD5 = 5.0 V ±10%, unless otherwise noted.

Table 1-3 Analog Specifications

Parameter	Min.	Typ.	Max.	Unit	Description
Analog Power Supply (VDD5)	3.6	5.0	5.5	V	5 V powered
	2.5	3.3	3.6	V	3.3 V powered
LDO33 Output					
Voltage	2.8	3.3	3.5	V	$V_{VDD5} \geq 4$ V; I_{L33} = 16 mA Programmable
Load Current (I_{L33})			30	mA	Current dissipated on IOs should not be over the maximum driving capacity of LDO33.
Digital Power Supply					
Voltage	1.3	1.8	2.0	V	Programmable
Load Current (I_{LD})			35	mA	
POR/BOR Detection Threshold **("DVCC")**		1.4		V	Error: ±10%
Power-Down Detection Threshold ("VDCIN")					
Maximum Signal Level	0		VDD	V	

Parameter	Min.	Typ.	Max.	Unit	Description
Input Impedance (DC)		1.5		MΩ	
Detection Threshold for **"PWRDN"**		1.0		V	
Detection Threshold for **"PWRUP"**		1.1		V	
Analog Inputs					
Maximum Signal Levels	-200		+200	mV	Peak value
ADC Performance					
DC Offset			15	mV	
Effective Bits		20		BIT	Sign bits are excluded.
Bandwidth (-3dB)		1.6		kHz	
ADC Operating Current					
Voltage Channel		307		μA	f_{ADC} = 819.2 kHz
Current Channel		485		μA	
Measurement Channel		238		μA	
On-Chip Crystal Oscillator					
Crystal Frequency		32.768		kHz	
On-Chip Reference (BandGap)					
Reference Error	-18		18	mV	
Power Supply Rejection Ratio		80		dB	
Temperature Coefficient		10	30	ppm/°C	
Output Voltage		1.185		V	
Analog Comparator CB					
Input Voltage	0		VDD5 -0.8	V	
Load Current		186.2		nA	Bias current = 20 nA
Delay Time	2.7	3.0	4.0	μs	Square wave = 50 kHz
Load Current		664.6		nA	Bias current = 200 nA
Delay Time	0.20	0.37	0.60	μs	Square wave = 50 kHz

1.4. Digital Interface Specifications

All maximum and minimum specifications apply over the entire recommended operation range (T = -40 °C ~ +85 °C, VDD5 = 3.3 V or 5.0 V), unless otherwise noted.

Table 1-4 Digital Interface Specifications

Parameter	Min.	Typ.	Max.	Unit	Description
Digital IO, Output					
Output High Voltage, V_{OH}	2.4			V	12-mA current cannot damage the chip in a short period of time; Long duration of 10-mA or above current may cause damage to the chip.
I_{SOURCE}		10	12	mA	
Output Low Voltage, V_{OL}			0.4	V	
I_{SINK}		10	12	mA	
Digital IO, Input					
Input High Voltage, V_{INH}	2.0			V	
Input Low Voltage, V_{INL}			0.8	V	

1.5. Memory Specifications

All maximum and minimum specifications apply over the entire recommended operation range (T = -40 °C ~ +85 °C, VDD5 = 3.3 V or 5.0 V), unless otherwise noted. All typical specifications are at TA = 25 °C, VDD5 = 5.0 V ±10% or f_{MCU} = 13.1072 MHz, unless otherwise noted.

Table 1-5 Memory Specifications

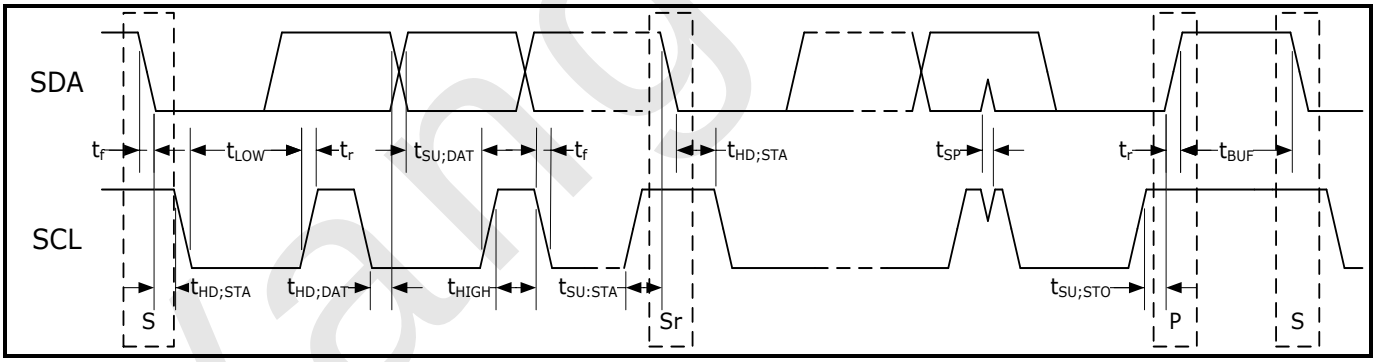
Parameter	Min.	Typ.	Max.	Unit	Description
Flash Memory					
Read Pulse Width		76		ns	
Endurance	20000			cycle	-40 °C ~ +85 °C
Data Retention	100			year	25°C
Data Retention	10			year	85°C
Write Time, per byte		40		μs	
Page Erase Time (512 bytes)		40		ms	
Mass Erase Time		40		ms	
RAM					
Data Retention Voltage	1.62			V	DVCC output voltage

1.6. GPSI Timing Specifications

All maximum and minimum specifications apply over the entire recommended operation range (T = -40 °C ~ +85 °C, VDD5 = 3.3 V or 5.0 V ±10%), unless otherwise noted.

Table 1-6 GPSI Timing Specifications

Parameter		Min.	Max.	Unit
f_{SCL}	SCL frequency		400	kHz
$t_{HD;STA}$	START condition hold time (Then, the first SCL pulse is generated.)	1.875		μs
t_{LOW}	SCL low pulse width	1.25		μs
t_{HIGH}	SCL high pulse width	1.25		μs
$t_{SU;STA}$	RESTART condition setup time	0.625		μs
$t_{HD;DAT}$	Data hold time	0.625		μs
$t_{SU;DAT}$	Data setup time	0.625		μs
t_r	Rising time of both SDA and SCL		50	ns
t_f	Falling time of both SDA and SCL		50	ns
$t_{SU;STO}$	STOP condition setup time	0.625		μs
t_{BUF}	Bus free time between STOP condition and START condition		N/A	
t_{SP}	Pulse width of spike suppressed		N/A	



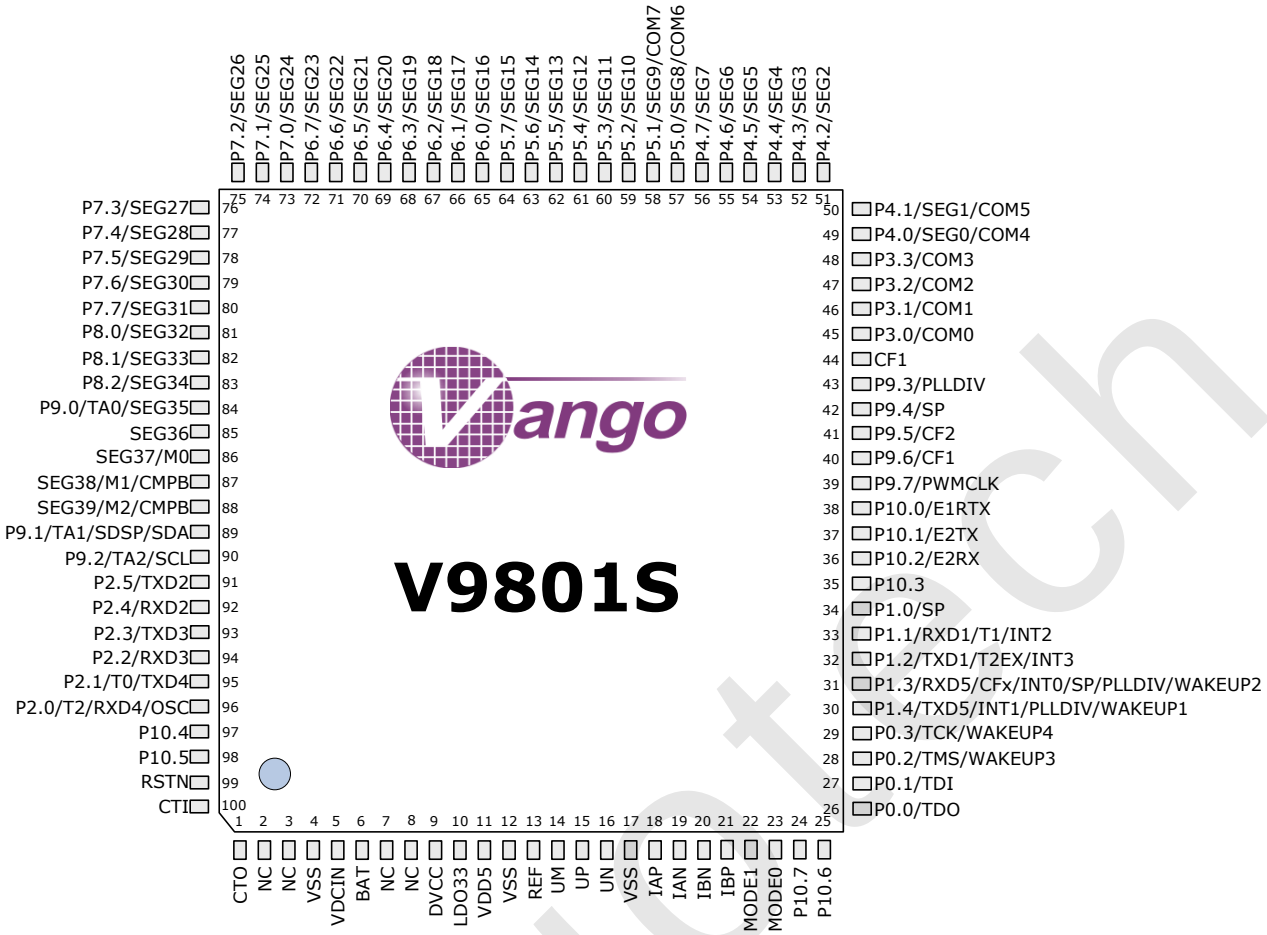
1.7. Typical Operating Current

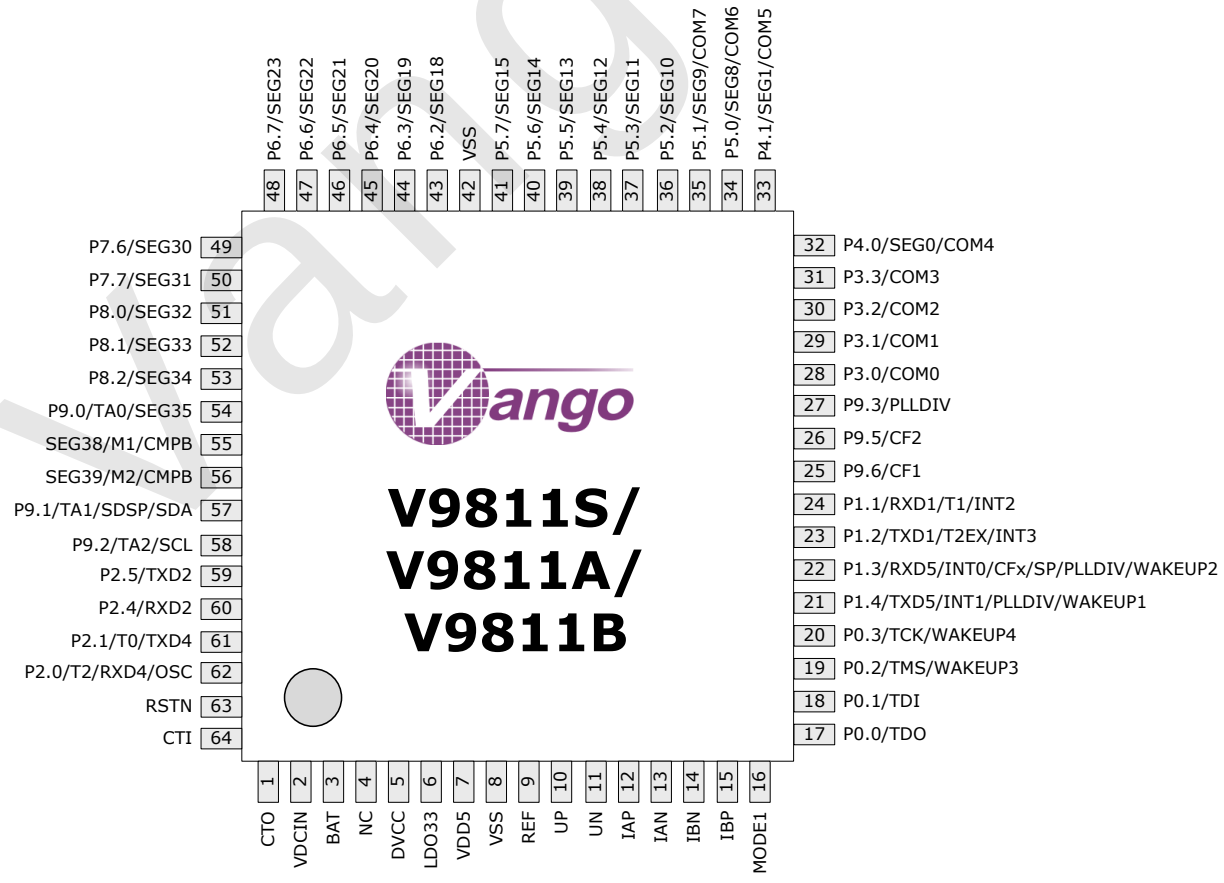
Table 1-7 Typical Operating Current

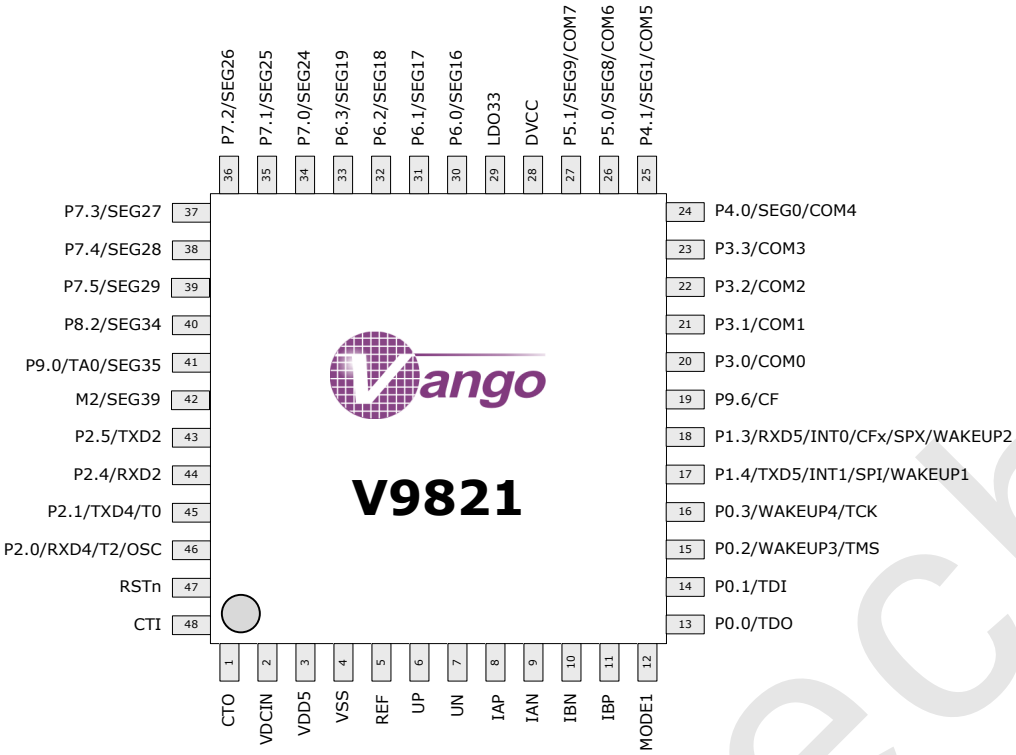
Mode	Typ.	Unit	Description
Full-operation	5.5	mA	f_{MCU} = 13.1072 MHz, f_{MTCLK} = 3276.8 kHz, f_{ADC} = 819.2 kHz, 4 ADC channels are enabled.
Sleeping	10	μA	Digital power supply is 1.8V; crystal oscillation circuit, RTC, system monitoring circuit, voltage monitoring circuit, and reset circuit keep working. RAM memory holds the data. Maximum current in sleeping mode:

Mode	Typ.	Unit	Description
			14.5μA.

2.Pin Descriptions



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P7.1/SEG25 35
P7.0/SEG24 34
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P6.2/SEG18 32
P6.1/SEG17 31
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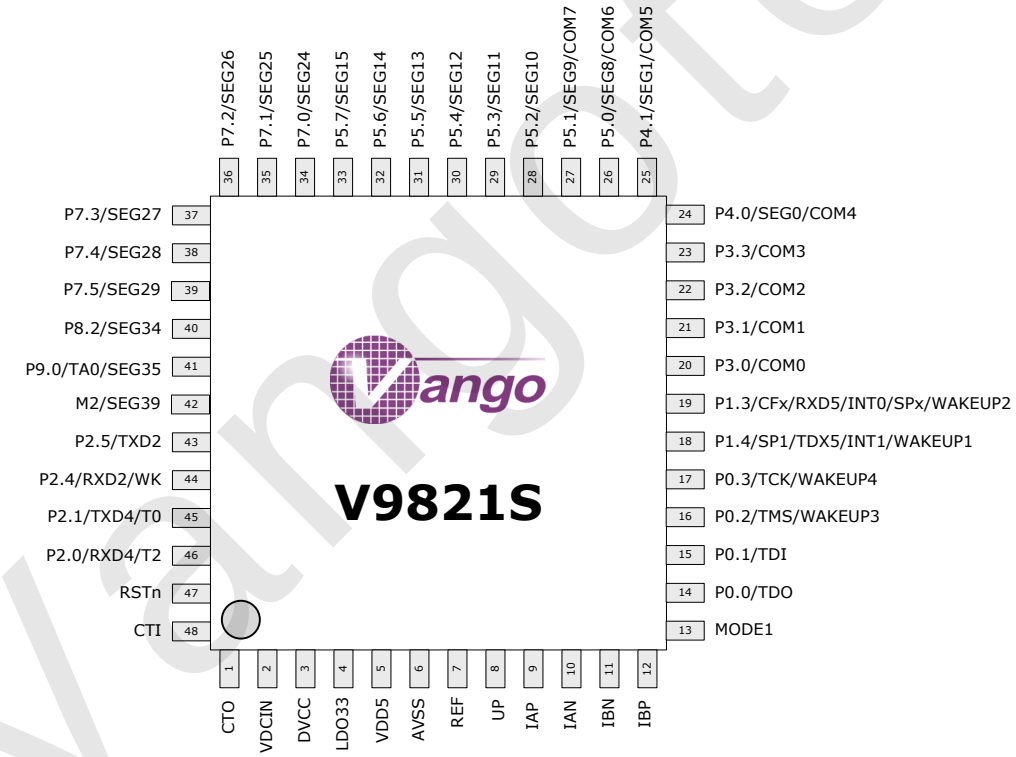
23 P3.3/COM3
22 P3.2/COM2
21 P3.1/COM1
20 P3.0/COM0
19 P9.6/CF
18 P1.3/RXD5/INT0/CFx/SPX/WAKEUP2
17 P1.4/TXD5/INT1/SPI/WAKEUP1
16 P0.3/WAKEUP4/TCK
15 P0.2/WAKEUP3/TMS
14 P0.1/TDI
13 P0.0/TDO
1 CTO
2 VDCIN
3 VDD5
4 VSS
5 REF
6 UP
7 UN
8 IAP
9 IAN
10 IBN
11 IBP
12 MODE1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23 P3.3/COM3
22 P3.2/COM2
21 P3.1/COM1
20 P3.0/COM0
19 P1.3/CFx/RXD5/INT0/SPx/WAKEUP2
18 P1.4/SP1/TDX5/INT1/WAKEUP1
17 P0.3/TCK/WAKEUP4
16 P0.2/TMS/WAKEUP3
15 P0.1/TDI
14 P0.0/TDO
13 MODE1
1 CTO
2 VDCIN
3 DVCC
4 LDO33
5 VDD5
6 AVSS
7 REF
8 UP
9 IAP
10 IAN
11 IBN
12 IBP

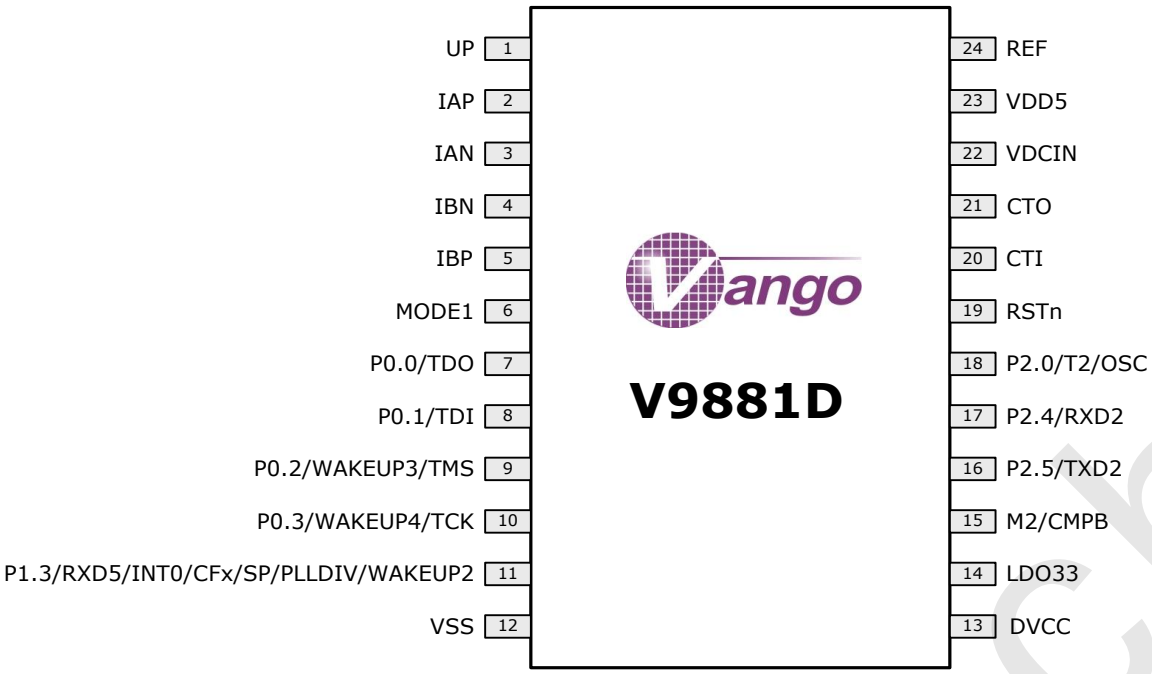


Figure 2-1 Pin Assignment

Table 2-1 Pin Descriptions (Pin type: "O"=Output, "I"= Input, "P"=Power, "G"=Ground)

V9801S	V9811B	V9811A/ V9811S/	V9821	V9821S	V9881D	Mnemonic	Type	Description
1	1		1	1	21	CTO	O	32768-Hz crystal output Connect a crystal around this pin and pin **"CTI"** to generate the **"OSC"** clock.
2~3						NC	-	Not connected
4					12	AVSS	G	Analog ground
5	2		2	2	22	VDCIN	I	Power supply supervisor input When the input voltage on this pin is higher than 1.1 V, the chip will be powered by 5-V main power. When the input voltage on this pin is lower than 1.0 V, the chip will be powered by batteries, or the power supply will be switched from 5-V main power to batteries.

V9801S	V9811B	V9811A/ V9811S/	V9821	V9821S	V9881D	Mnemonic	Type	Description
6	3					BAT	I	Analog input for battery voltage measurement The input voltage signal into this pin to be measured must be over the range of -200 mV ~ 3.8 V. When no battery is used, it is mandatory to float this pin, but not connect it to ground.
7~8	4					NC	-	Not connected
9	5		28		13	DVCC	P	Digital power output The internal power-on reset circuit supervises the output voltage on this pin: When the voltage is lower than 1.4 V, a power-on reset will occur. Connect a ≥ 4.7-μF capacitor in parallel with a 0.1-μF capacitor around this pin, and then connect it to the digital ground.
10	6		29	4	14	LDO33	P	Regulated 3.3-V analog voltage output Connect a ≥ 4.7-μF capacitor in parallel with a 0.1-μF capacitor around this pin, and then connect it to the analog ground. When the chip is 3.3 V powered, it is recommended to directly externally connect this pin to the pin **"VDD5"**.
11	7		3	5	23	VDD5	P	Power supply Connect a 10-μF capacitor to this pin, and then connect it to the ground. When the chip is 3.3 V powered, it is recommended to directly externally connect this pin to the pin **"LDO33"**.
12	8		4	6		AVSS	G	Analog ground
13	9		5	7	24	REF	I/O	On-chip reference Connect a 1-μF capacitor to this pin, and then connect it to analog ground.

V9801S	V9811B	V9811A/ V9811S/	V9821	V9821S	V9881D	Mnemonic	Type	Description
14						UM	I	Analog input for various signal measurements in Measurement (M) Channel The input voltage signal into this pin to be measured must be over the range of -200 mV ~ 3.4 V.
15	10		6	8	1	UP	I	Positive input for Voltage Channel
16	11		7			UN	I	Negative input for Voltage Channel
17						AVSS	G	Analog ground
18	12		8	9	2	IAP	I	Positive input for Current Channel IA
19	13		9	10	3	IAN	I	Negative input for Current Channel IA
20	14		10	11	4	IBN	I	Negative input for Current Channel IB
21	15		11	12	5	IBP	I	Positive input for Current Channel IB
22	16		12	13	6	MODE1	I	**"Logic 0"** is input to force the system into the debugging mode. **"Logic 1"** is input to force the system into the metering mode.
23						MODE0	I	Grounded/Float
24						P10.7	I/O	General-purpose input/output port (Fast IO)
25						P10.6	I/O	General-purpose input/output port (Fast IO)
26	17		13	14	7	P0.0 TDO	I/O	This pin is used as a general-purpose input/output port by default. But when **"logic 0"** is input to the pin **"MODE1"**, this pin will be used as a JTAG port for the test data output (**"TDO"**).
27	18		14	15	8	P0.1 TDI	I/O	This pin is used as a general-purpose input/output port by default. But when **"logic 0"** is input to the pin **"MODE1"**, this pin will be used as a JTAG port for the test data input (**"TDI"**).

V9801S	V9811B V9811A/ V9811S/	V9821	V9821S	V9881D	Mnemonic	Type	Description
28	19	15	16	9	P0.2 WAKEUP3 TMS	I/O	This pin is used as a general-purpose input/output port by default. When the bit **"IOP0"** (**"bit1"** of **"IOWK",** SFR 0xC9) is set to **'1'**, this pin will be used for the IO wakeup input, active on either transition (Configurable). When **"logic 0"** is input to the pin **"MODE1"**, this pin will be used as a JTAG port for the test mode selection (**"TMS"**).
29	20	16	17	10	P0.3 WAKEUP4 TCK	I/O	This pin is used as a general-purpose input/output port. When the bit **"IOP0"** (**"bit1"** of **"IOWK"**, SFR 0xC9) is set to **'1'**, this pin will be used for the IO wakeup input, active on either transition (configurable). When **"logic 0"** is input to the pin **"MODE1"**, this pin will be used as a JTAG port for the test clock input (**"TCK"**).
30	21	17	18		P1.4 TXD5 INT1 PLLDIV WAKEUP1	I/O	The function of this pin can be configured by the register **"P14FS"** (0x28C8): – General-purpose input/output port; – Transmitter data output of **"UART5"**; – IO interrupt input 1, active on high-to-low transition; – Pulse output proportional to the divided PLL clock frequency, which can be configured to output pulses of 1s width from the PLL counter. Besides, this pin can be used to wake up the system from the sleeping state, active on either transition (Configurable).

V9801S	V9811B	V9811A/ V9811S/	V9821	V9821S	V9881D	Mnemonic	Type	Description
31	22		18	19	11	P1.3 RXD5 INT0 CFx SP PLLDIV WAKEUP2	I/O	The function of this pin can be configured by the register **"P13FS"** (0x28C7): – General-purpose input/output port; – Receiver data input of **"UART5"**; – IO interrupt input 0, active on high-to-low transition; – Configurable CF pulse output; – Pulse per second (PPS) output from RTC. On calibrating RTC, every 30 seconds, from the 1st to 29th second, an un-calibrated pulse is output every second, and in the 30th second, a calibrated pulse is output which averages the cycle of each pulse in the 30 seconds to be 1s width; – Pulse output proportional to the divided PLL clock frequency, which can be configured to output pulses of 1s width from the PLL counter. Besides, this pin can be used to wake up the system from the sleeping state, active on either transition (Configurable).
32	23					P1.2 TXD1 T2EX INT3	I/O	The function of this pin can be configured by the register **"P12FS"** (0x28C6): – General-purpose input/output port; – Transmitter data output of **"UART1"**; – Timer2 capture or reload trigger input; IO interrupt input 3, active on high-to-low transition.

V9801S	V9811B	V9811A/ V9811S/	V9821	V9821S	V9881D	Mnemonic	Type	Description
33	24					P1.1 RXD1 T1 INT2	I/O	The function of this pin can be configured by the register **"P11FS"** (0x28C5): – General-purpose input/output port; – Receiver data input of **"UART1"**; – Timer1 external input; IO interrupt input 2, active on high-to-low transition.
34						P1.0 SP	I/O	The function of this pin can be configured by the register **"P10FS"** (0x28C4): – General-purpose input/output port; – Pulse per second (PPS) output from RTC. On calibrating RTC, every 30 seconds, from the 1st to 29th second, an un-calibrated pulse is output every second, and in the 30th second, a calibrated pulse is output which averages the cycle of each pulse in the 30 seconds to be 1s width.
35						P10.3	I/O	– General-purpose input/output port (Fast IO).
36						P10.2 E2RX	I/O	– This pin is used as a general-purpose input/output port (Fast IO) by default. When the bit **"ENABLE"** (**"bit0"** of **"CFGB"**, 0x2B05) is set to **'1',** this pin is used for the receiver data input of **"EUART2"**.
37						P10.1 E2TX	I/O	This pin is used as a general-purpose input/output port (Fast IO) by default. When the bit **"ENABLE"** (**"bit0"** of **"CFGB"**, 0x2B05) is set to **'1',** this pin is used for the transmitter data output of **"EUART2"**.

V9801S	V9811B	V9811A/ V9811S/	V9821	V9821S	V9881D	Mnemonic	Type	Description
38						P10.0 E1RTX	I/O	This pin is used as a general-purpose input/output port (Fast IO) by default. When the bit **"ENABLE"** (**"bit0"** of **"CFGA"**, 0x2A05) is set to **'1',** this pin is used for the data input and output of **"EUART1"**.
39						P9.7 PWMCLK	I/O	The function of this pin can be configured by the register **"P9FS"** (SFR 0xAD): – General-purpose input/output port (Fast IO); PWM pulse output. When the enhanced UART (EUART) ports are used for smart card communication, this pulse output is used as the clock input into the card for communication.
40	25		19			P9.6 CF1	I/O	The function of this pin can be configured by the register **"P9FS"** (SFR 0xAD): – General-purpose input/output port (Fast IO); CF pulse output of E1 path.
41	26					P9.5 CF2	I/O	The function of this pin can be configured by the register **"P9FS"** (SFR 0xAD): – General-purpose input/output port (Fast IO); – CF pulse output of E2 path.

V9801S	V9811B	V9811A/ V9811S/	V9821	V9821S	V9881D	Mnemonic	Type	Description
42						P9.4 SP	I/O	The function of this pin can be configured by the register **"P9FS"** (SFR 0xAD): – General-purpose input/output port (Fast IO); – Pulse per second (PPS) output from RTC On calibrating RTC, every 30 seconds, from the 1st to 29th second, an un-calibrated pulse is output every second, and in the 30th second, a calibrated pulse is output which averages the cycle of each pulse in the 30 seconds to be 1 second.
43	27					P9.3 PLLDIV	I/O	The function of this pin can be configured by the register **"P9FS"** (SFR 0xAD): – General-purpose input/output port (Fast IO); – Pulse output proportional to the divided PLL clock frequency, which can be configured to output pulses of 1s width from the PLL counter.
44						CF1	O	– CF pulse of E1 path
45~48	28~31		20~23	20~23		P3.0~P3.3 COM0~COM3	I/O	– These pins are used as general-purpose input/output ports by default. And they also can be used as backplanes of the LCD driver.
49	32		24	24		P4.0 SEG0 COM4	I/O	This pin is used as general-purpose input/output port by default, as SEG output for the LCD driver when bits **"LCDTYPE"** (**"bit[5:4]"** of **"LCDCtrl"**, 0x2C1E) are cleared, or as backplanes of the LCD driver when bits **"LCDTYPE"** are set to **'1', '2',** or **'3'**.

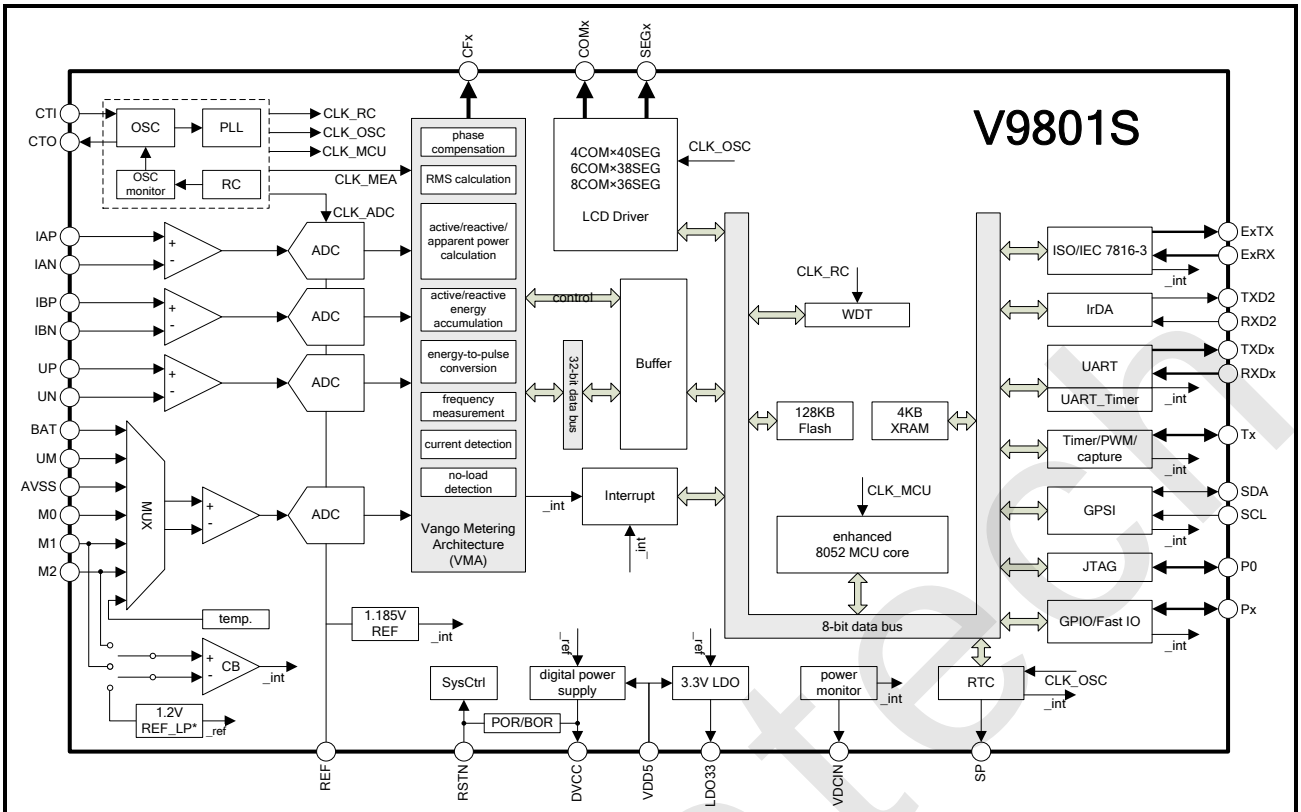
V9801S	V9811B V9811A/ V9811S/	V9821	V9821S	V9881D	Mnemonic	Type	Description
50	33	25	25		P4.1 SEG1 COM5	I/O	This pin is used as general-purpose input/output port by default, as SEG output for the LCD driver when bits **"LCDTYPE"** (**"bit[5:4]"** of **"LCDCtrl"**, 0x2C1E) are cleared, or as backplanes of the LCD driver when bits **"LCDTYPE"** are set to **'1', '2',** or **'3'**.
51~56					P4.2~P4.7 SEG2~SEG7	I/O	These pins are used as general-purpose input/output ports by default; or SEG output for the LCD driver when the corresponding bits in SEG control registers are set to 1s.
57	34	26	26		P5.0 SEG8 COM6	I/O	This pin is used as general-purpose input/output port by default, as SEG output for the LCD driver when bits **"LCDTYPE"** (**"bit[5:4]"** of **"LCDCtrl",** 0x2C1E) are cleared or set to **'1',** or as backplanes of the LCD driver when bits **"LCDTYPE"** are set to **'2**' or **'3'**.
58	35	27	27		P5.1 SEG9 COM7		This pin is used as general-purpose input/output port by default, as SEG output for the LCD driver when bits **"LCDTYPE"** (**"bit[5:4]"** of **"LCDCtrl",** 0x2C1E) are cleared or set to **'1',** or as backplanes of the LCD driver when bits **"LCDTYPE"** are set to **'2**' or **'3'**.
59~83	36~53	30-40	28~40		P5.2~P8.2 SEG10~SEG34	I/O	These pins are used as general-purpose input/output ports by default; or SEG output for the LCD driver when the corresponding bits in SEG control registers are set to 1s.
84	54	41	41		P9.0 TA0 SEG35	I/O	The function of this pin can be configured by the register **"P9FS"** (SFR 0xAD): – General-purpose input/output port (Fast IO); – TimerA port 0, to input/output the signals for TimerA Compare/Capture Module 0. Besides, this pin can be used for SEG output for the LCD driver

V9801S	V9811B	V9811A/ V9811S/	V9821	V9821S	V9881D	Mnemonic	Type	Description
85						SEG36	O	This pin is used for SEG output for the LCD driver.
86~88	55~56		42	42	15	SEG37~SEG39 M0~M2	I/O	These pins are used for SEG output for the LCD driver. And this pin also can be used for analog input for various measurements in Channel M. Both M1 and M2 can be used for analog signal input to the analog comparator CB for comparison. The input voltage signal into this pin to be measured must be over the range of -200 mV~3.4 V. When these pins are used for analog input to Channel M or the analog comparator CB, the SEG output on these pins must be disabled.
89	57					P9.1 TA1 SDSP SDA	I/O	The function of this pin can be configured by the register **"P9FS"** (SFR 0xAD): – General-purpose input/output port (Fast IO); – TimerA port 1, to input/output the signals for TimerA Compare/Capture Module 1. This pin can be used for reference pulse input of exact 1s width. When the bit **"GPSI"** (**"bit6"** of **"PRCtrl0"**, 0x2D00) is set to **'1'**, this pin will be used for serial data delivery for GPSI.

V9801S	V9811B	V9811A/ V9811S/	V9821	V9821S	V9881D	Mnemonic	Type	Description
90	58					P9.2 TA2 SCL	I/O	The function of this pin can be configured by the register **"P9FS"** (SFR 0xAD): – General-purpose input/output port (Fast IO); – TimerA port 2, to input/output the signals for TimerA Compare/Capture Module 2. When the bit **"GPSI"** ("**bit6"** of **"PRCtrl0"**, 0x2D00) is set to **'1',** this pin is used for serial clock delivery for GPSI.
91	59		43	43	16	P2.5 TXD2	I/O	The function of this pin can be configured by the register **"P25FS"** (0x28CE): – General-purpose input/output port; Transmitter data output of UART2. It can be configured to transmit 38-kHz carrier wave.
92	60		44	44	17	P2.4 RXD2	I/O	The function of this pin can be configured by the register **"P24FS"** (0x28CD): – General-purpose input/output port; Receiver data input of UART2. When this pin is used for IR communication, it should be connected to a demodulator externally.
93						P2.3 TXD3	I/O	The function of this pin can be configured by the register "P23FS" (0x28CC): – General-purpose input/output port; – Transmitter data output of UART3.
94						P2.2 RXD3	I/O	The function of this pin can be configured by the register **"P22FS"** (0x28CB): – General-purpose input/output port; – Receiver data input of UART3.

V9801S	V9811B	V9811A/ V9811S/	V9821	V9821S	V9881D	Mnemonic	Type	Description
95	61		45	45		P2.1 TXD4 T0	I/O	The function of this pin can be configured by the register **"P21FS"** (0x28CA): – General-purpose input/output port; – Transmitter data output of UART4; – Timer0 external input.
96	62		46	46	18	P2.0 RXD4 T2 OSC	I/O	The function of this pin can be configured by the register **"P20FS"** (0x28C9): – General-purpose input/output port; – Receiver data input of UART4; – Timer2 external input; – OSC clock waveform output.
97~98						P10.4~P10.5	I/O	– General-purpose input/output port (Fast IO)
99	63		47	47	19	RSTn	I	– Reset input, low active. Hold **"LOW"** at least 5 ms to generate a signal to reset the system.
100	64		48	48	20	CTI	I	32768-Hz crystal input Connect a crystal around this pin and pin **"CTO"** to generate a clock signal **"OSC"**.

3.Functional Block Diagram



*1.2V REF_LP represents the low power reference voltage unit (not the BandGap circuit). This unit works all the time until the chip is powered off. This unit provides the 3.3V LDO and digital power supply with 1.2V reference voltage, and it can be the negative input for the comparator CB.

4.8052 MCU Core Architecture

4.1. Memory Map

V98XX contains three memory blocks:

- 256 bytes of internal SRAM (IRAM), sharing the upper 128 bytes of its addresses with Special Function Registers (SFRs).
- 4-KB internal extended RAM (XRAM) and the memory of peripherals sharing the data memory area at addresses **"0000h" ~ "FFFFh"**.
- 128-KB on-chip Flash memory mapping the program memory area at addresses **"0000h" ~ "FFFFh".**

4.2. IRAM (Internal RAM) and SFRS (Special Function Registers)

The 256-byte internal SRAM (IRAM), located at addresses **"00h" ~ "FFh"**, is composed of two parts: the lower 128-byte RAM and the upper 128-byte RAM. When the output voltage of **"DVCC"** is higher than 1.62 V, IRAM holds the data in it even when MCU is reset to its default state.

The lower 128-byte internal RAM contains three distinct blocks: Register Bank 0~3 (**"00h" ~ "1Fh"**), Bit Address Area (**"20h" ~ "2Fh"**) and General RAM Area (**"30h" ~ "7Fh"**). All the lower 128-byte internal RAM can be accessed by direct or indirect addressing.

- Register Bank 0~3, 32 bytes from **"00h"** to **"1Fh"**, each is composed of 8 registers, R0~R7. Users can configure **"bit4"** (**"RS1"**) and **"bit3"** (**"RS0"**) of the register **"PSW"** (SFR 0xD0, Program Status Word SFR) to select the register bank to be used. By default Register Bank 0 is used.

Table 4-1 Select a Register Bank

Register	Bit	Default	Description
Program Status Word PSW SFR 0xD0	Bit[4:3] RS1/RS0	0	To select a register bank to be used 00: Register Bank 0, located at addresses 00h~07h; 01: Register Bank 1, located at addresses 08h~0Fh; 10: Register Bank 2, located at addresses 10h~17h; 11: Register Bank 3, located at addresses 18h~1Fh.

- Bit Address Area (**"20h" ~ "2Fh"**), each with bit addresses from **"00h"** to **"7Fh"**, is bit addressable.
- General RAM, from **"30h"** to **"7Fh"**, can be addressed directly.

The upper 128-byte internal RAM, located at addresses **"80h" ~ "FFh",** shares its addresses with a group of specific internal registers (Special Function Registers, SFRs), but they are accessed in different ways. SFRs are accessed via direct addressing, but the upper 128-byte internal RAM is accessed via

indirect addressing.

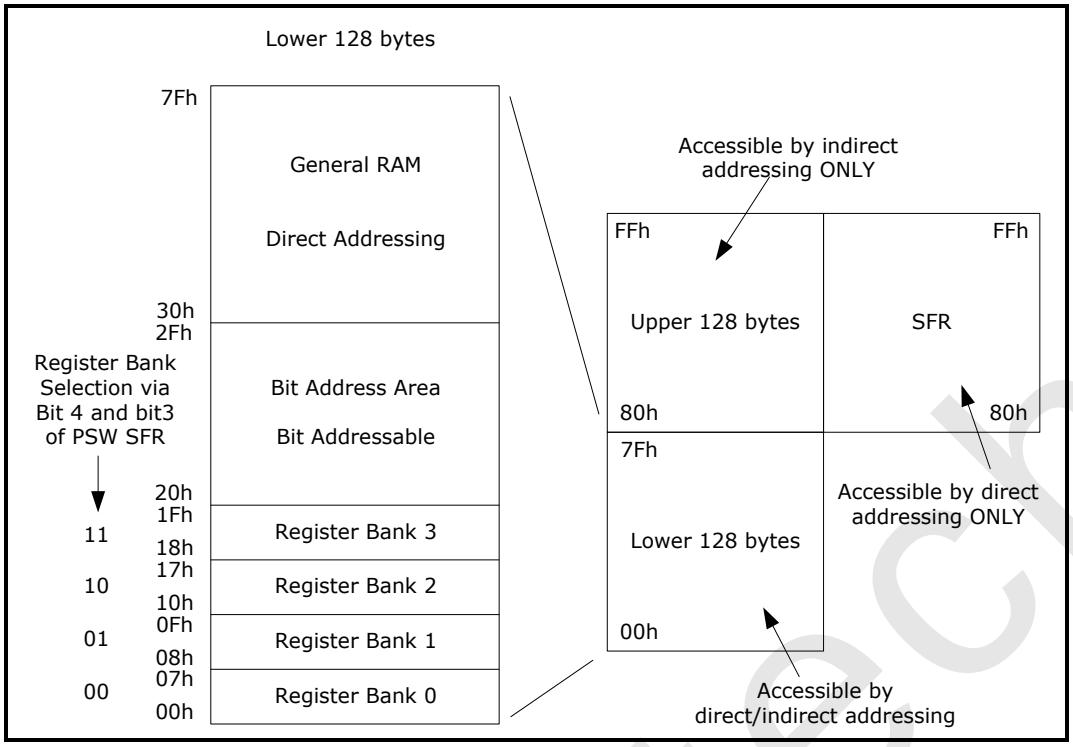


Figure 4-1 IRAM and SFR

Table 4-2 Special Function Registers (SFR)

Addr.	Register	Bit 7	bit 6	bit 5	bit 4	bit 3	Bit 2	bit 1	bit 0
80h	SysCtrl	MEAFRQ	FWC	FSC	PMG	LCDG	SLEEP1	SLEEP0	MCUFRQ
81h	SP	-	-	-	-	-	-	-	-
82h	DPL0	-	-	-	-	-	-	-	-
83h	DPH0	-	-	-	-	-	-	-	-
84h	DPL1	-	-	-	-	-	-	-	-
85h	DPH1	-	-	-	-	-	-	-	-
86h	DPS	0	0	0	0	0	0	0	SEL
87h	PCON	SMOD0	-	1	1	GF1	GF0	STOP	IDLE
88	TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

Addr.	Register	Bit 7	bit 6	bit 5	bit 4	bit 3	Bit 2	bit 1	bit 0
h									
89h	TMOD	GATE	C/T	M1	M0	GATE	C/T	M1	M0
8Ah	TL0	-	-	-	-	-	-	-	-
8Bh	TL1	-	-	-	-	-	-	-	-
8Ch	TH0	-	-	-	-	-	-	-	-
8Dh	TH1	-	-	-	-	-	-	-	-
8Eh	CKCON	-	-	T2M	T1M	T0M	MD2	MD1	MD0
8Fh	SPCFNC	0	0	0	0	0	0	0	WRS
90h	RTCPEN	-	-	-	-	-	-	-	-
91h	EXIF	IE5	IE4	IE3	IE2	1	0	0	0
92h	Reserved	-	-	-	-	-	-	-	-
93h	RTCYC	Y80	Y40	Y20	Y10	Y8	Y4	Y2	Y1
94h	RTCCH	-	-	C13	C12	C11	C10	C9	C8
95h	RTCCL	C7	C6	C5	C4	C3	C2	C1	C0
96h	INTRTC	-	-	-	-	-	RTC2	RTC1	RTC0
97h	RTCPWD		-	-	-	-	-	-	WE
98h	Reserved	-	-	-	-	-	-	-	-
99h	Reserved	-	-	-	-	-	-	-	-

Addr.	Register	Bit 7	bit 6	bit 5	bit 4	bit 3	Bit 2	bit 1	bit 0
9Ah	RTCSC	-	S40	S20	S10	S8	S4	S2	S1
9Bh	RTCMiC	-	M40	M20	M10	M8	M4	M2	M1
9Ch	RTCHC	-	-	H20	H10	H8	H4	H2	H1
9Dh	RTCDC	-	-	D20	D10	D8	D4	D2	D1
9Eh	RTCWC	-	-	-	-	W8	W4	W2	W1
9Fh	RTCMoC	-	-	-	Mo10	Mo8	Mo4	Mo2	Mo1
A0h	CBANK	-	-	-	-	-	-	B1	B0
A1h	Systate	-	P14WK	POR	-	IO	RTC/CF	PWRDN	PWRUP
A2h	Reserved	-	-	-	-	-	-	-	-
A3h	PLLLCK	-	-	-	-	-	-	-	PLLLCK
A4h	P9OE	P97OEN	P96OEN	P95OEN	P94OEN	P93OEN	P92OEN	P91OEN	P90OEN
A5h	P9IE	P97INEN	P96INEN	P95INEN	P94INEN	P93INEN	P92INEN	P91INEN	P90INEN
A6h	P9OD	-	-	-	-	-	-	-	-
A7h	P9ID	-	-	-	-	-	-	-	-
A8h	IE	EA	ES1	ET2	ES0	ET1	EX1	ET0	EX0
A9h	P10OE	P107OEN	P106OEN	P105OEN	P104OEN	P103OEN	P102OEN	P101OEN	P100OEN
AAh	P10IE	P107INEN	P106INEN	P105INEN	P104INEN	P103INEN	P102INEN	P101INEN	P100INEN
AB	P10OD								

Addr.	Register	Bit 7	bit 6	bit 5	bit 4	bit 3	Bit 2	bit 1	bit 0
h									
ACh	P10ID								
ADh	P9FS	P97FNC	P96FNC	P95FNC	P94FNC	P93FNC	P92FNC	P91FNC	P90FNC
AEh	Reserved	-	-	-	-	-	-	-	-
AFh	IOWKDET	-	-	-	-	CFWK	P03WK	P02WK	P14WK
B8h	IP	1	PS1	PT2	PS0	PT1	PX1	PT0	PX0
C0h	SCON1	SM0_1	SM1_1	SM2_1	REN_1	TB8_1	RB8_1	TI_1	RI_1
C1h	SBUF1	-	-	-	-	-	-	-	-
C7h	IOEDG	P03EDG <1>	P03EDG <0>	P02EDG <1>	P02EDG <0>	P14EDG <1>	P14EDG <0>	P13EDG <1>	P13EDG <0>
C8h	T2CON	TF2	EXF2	-	-	EXEN2	TR2	C/T2	CP/RL2
C9h	IOWK	-	-	-	-	-	CFWKEN	IOP0	IORSTN
CAh	RCAP2L	-	-	-	-	-	-	-	-
CBh	RCAP2H	-	-	-	-	-	-	-	-
CCh	TL2	-	-	-	-	-	-	-	-
CDh	TH2	-	-	-	-	-	-	-	-
CEh	WDTEN	-	-	-	-	-	-	-	-
CFh	WDTCLR	-	-	-	-	-	-	-	-
D0h	PSW	CY	AC	-	RS1	RS0	OV	-	P

Addr.	Register	Bit 7	bit 6	bit 5	bit 4	bit 3	Bit 2	bit 1	bit 0
D8h	EICON	SMOD1	1	-	-	PFI	0	0	0
D9h	Reserved	-	-	-	-	-	-	-	-
DAh	RDRTC	-	-	-	-	-	-	-	-
DBh	DIVTHH	DIV23	DIV22	DIV21	DIV20	DIV19	DIV18	DIV17	DIV16
DCh	DIVTHM	DIV15	DIV14	DIV13	DIV12	DIV11	DIV10	DIV9	DIV8
DDh	DIVTHL	DIV7	DIV6	DIV5	DIV4	DIV3	DIV2	DIV1	DIV0
DEh	PLLCNTST	-	-	-	-	-	-	STT1	STT0
DFh	SECINT	-	1	SEC5	SEC4	SEC3	SEC2	SEC1	SEC0
E0h	ACC	-	-	-	-	-	-	-	-
E8h	EIE	1	1	1	EWDI	EX5	EX4	EX3	EX2
F0h	B	-	-	-	-	-	-	-	-
F8h	EIP	1	1	1	PWDI	PX5	PX4	PX3	PX2

4.3. Data Memory

4096 bytes of XRAM and peripherals registers can be mapped to the data storage space. XRAM is located at addresses **"0000h" ~ "0FFFh"** that can be accessed limitless. The content of XRAM cannot be reset by any reset event, and it will hold the data in it until the output voltage of **"DVCC"** is lower than 1.62 V.

The bytes located at addresses **"0x3000" ~ "0x33FF"**, (Info area, read) are designed to store recommended configuration for analog registers , parameters for temperature measurement, and RTC calibration that are pre-programmed by Vango when the chips are being manufactured, see Figure 4-2 for details. The program can access the information within the address range in the same way as accessing the peripheral registers.

In Data storage space, in addition to the contents of the XRAM and Info area, all of the peripherals registers can be reset. Among them, the LCD/GPIO simulation control/registers related energy metering

can only be reset and are set to the default values by the Level 1 reset, other registers will be reset to the default values by the Level 1/2/3 reset. The contents of the Info area will not be reset, after a reset event of Level 1, the content of these bytes will be settled in 2 ms, and then CPU can execute the programs in Flash memory. These bytes are readable only, and MCU can read of these bytes as they are peripherals.

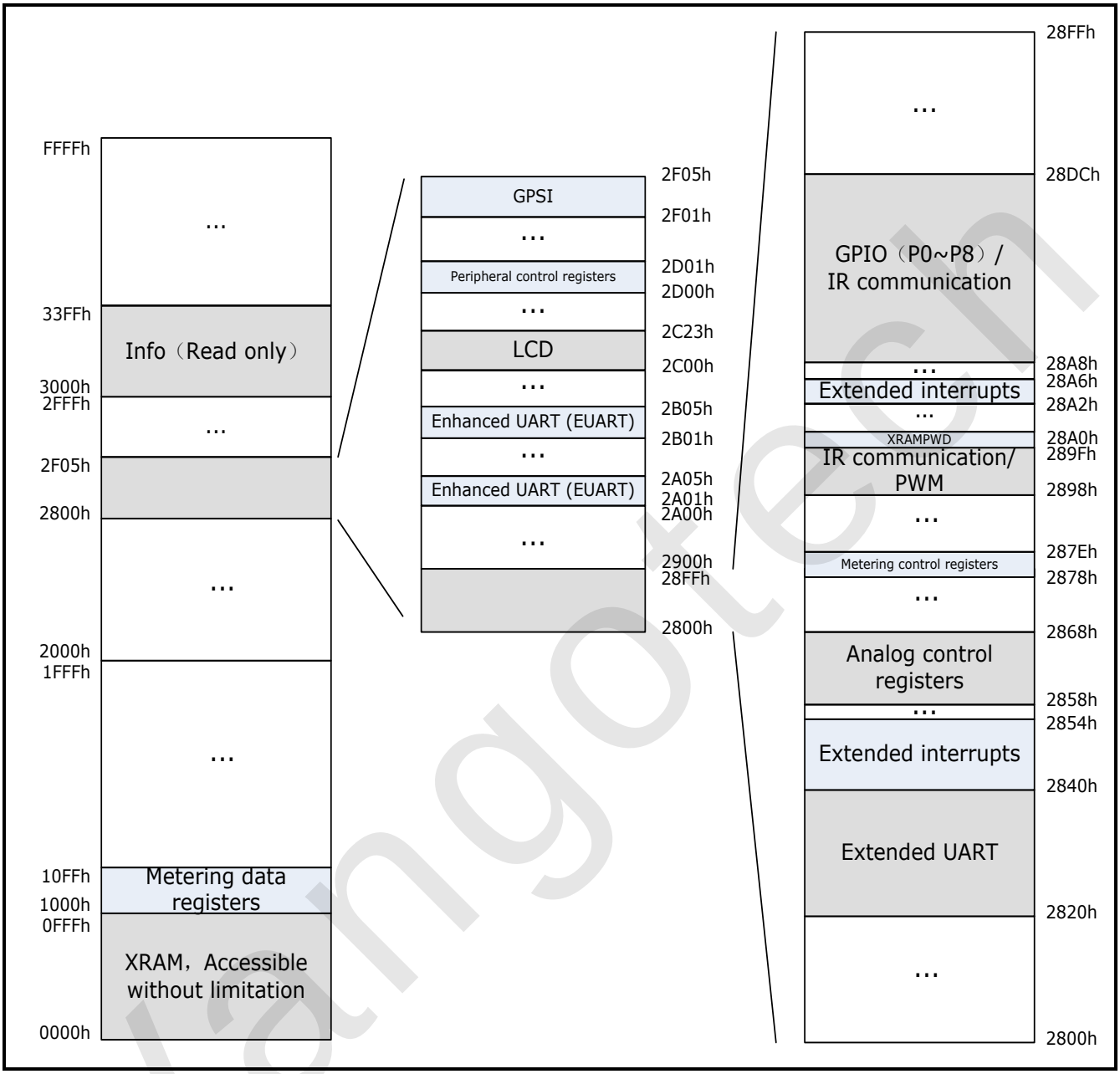


Figure 4-2 Data Memory

Table 4-3 Allocation of Info Area

Starting Address	Functional Description	Number of Byte	Endianness
0x 401	Noted additionally	2	Little-endian
0x 403	Noted additionally	2	Little-endian
0x 405	Noted additionally	2	Little-endian
0x 407	Noted additionally	4	Little-endian

Starting Address	Functional Description	Number of Byte	Endianness
0x 40B	Noted additionally	1	Little-endian
0x 40C	Noted additionally	4	Little-endian
0x 410	Noted additionally	2	Little-endian
0x 412	Noted additionally	2	Little-endian
0x 414	Noted additionally	1	Little-endian
0x 415	Noted additionally	1	Little-endian
0x 416	Noted additionally	2	Little-endian
0x 418	Noted additionally	1	Little-endian
0x 419	Noted additionally	1	Little-endian
0x 41A	Noted additionally	2	Little-endian
0x 41C	Noted additionally	1	Little-endian
0x 41D	Noted additionally	1	Little-endian
0x 41E	Noted additionally	2	Little-endian
0x420	a	4	Little-endian
0x 424	b	4	Little-endian
0x 428	c	4	Little-endian
0x 42C	d	4	Little-endian
0x 430	e	4	Little-endian
0x 434	ADD33 verification	2	Little-endian
0x 436	Reserved	2	Little-endian
0x 438	a	4	Little-endian
0x 43C	b	4	Little-endian
0x 440	c	4	Little-endian
0x 444	d	4	Little-endian
0x 448	e	4	Little-endian
0x 44C	ADD33 verification	2	Little-endian
0x 44E	Reserved	2	Little-endian
0x 450	a	4	Little-endian
0x 454	b	4	Little-endian
0x 458	c	4	Little-endian

Starting Address	Functional Description	Number of Byte	Endianness
0x 45C	d	4	Little-endian
0x 460	e	4	Little-endian
0x 464	ADD33 verification	2	Little-endian
0x 466	Reserved	2	Little-endian
0x 468	Reserved	4	Little-endian
0x 46C	Reserved	2	Little-endian
0x 46E	Reserved	2	Little-endian
0x 470	Reserved	4	Little-endian
0x 474	Reserved	2	Little-endian
0x 476	Reserved	2	Little-endian
0x 478	Reserved	4	Little-endian
0x 47C	Reserved	2	Little-endian
0x 47E	Reserved	2	Little-endian
0x 480	Backup 1 of temperature deviation	2	Big-endian
0x 482	ADD33 verification	2	Big-endian
0x 484	Backup 2 of temperature deviation	2	Big-endian
0x 486	ADD33 verification	2	Big-endian
0x 488	Backup 3 of temperature deviation	2	Big-endian
0x 48A	ADD33 verification	2	Big-endian
0x 48C	Backup 1 of RTC temperature deviation	2	Big-endian
0x 48E	ADD33 verification	2	Big-endian
0x 490	Backup 2 of RTC temperature deviation	2	Big-endian
0x 492	ADD33 verification	2	Big-endian
0x 494	Backup 3 of RTC temperature deviation	2	Big-endian
0x 496	ADD33 verification	2	Big-endian
0x 498	Backup 1 of parabolic	20	Big-endian

Starting Address	Functional Description	Number of Byte	Endianness
	coefficient B_{para} of crystal		
0x 4AC	ADD33 verification	2	Big-endian
0x 4AE	Backup 2 of parabolic coefficient B_{para} of crystal	20	Big-endian
0x 4C2	ADD33 verification	2	Big-endian
0x 4C4	Backup 3 of parabolic coefficient B_{para} of crystal	20	Big-endian
0x 4D8	ADD33 verification	2	Big-endian
0x 4DA	Backup 1 of crystal fixed-point temperature	2	Big-endian
0x 4DC	ADD33 verification	2	Big-endian
0x 4DE	Backup 2 of crystal fixed-point temperature	2	Big-endian
0x 4E0	ADD33 verification	2	Big-endian
0x 4E2	Backup 3 of crystal fixed-point temperature	2	Big-endian
0x 4E4	ADD33 verification	2	Big-endian
0x 4E6	Reserved	2	Big-endian
0x 4E8	Standard RTC capturing value	4	Big-endian
0x 4EC	Target chip RTC capturing value	4	Big-endian
0x 4F0	Reserved	4	Big-endian
0x 4F4	SD502 version number	4	Big-endian
0x 4F8	Ambient temperature during temperature calibration	4	Big-endian
0x 4FC	Temperature of target chip before temperature calibration	4	Big-endian
0x 500	Reserved	256	

*Users can read of these bytes and obtain the recommended configuration of the analog control registers, and then write them to the analog control registers.

See **"Measuring Temperature" for details of parameter A, B, C, D, E, and temperature error.

***When users are using the crystals provided by Vango, they can read these addresses to obtain the details of crystal frequency deviation Δ, parabolic coefficient Bpara, and turnover temperature of the crystal, to calibrate RTC. See the corresponding application notes for details.

4.4. Program Memory

In V98XX, the 128-KB on-chip Flash memory (Including program encryption bytes) and the Flash control registers are mapped to the MCU program memory at addresses **"0000h" ~ "FFFFh".** The Flash control registers mapped to the MCU program memory at addresses **"0x0401"** and **"0x0402"**, determining the programming mode and power consumption mode of the Flash memory.

Table 4-4 Flash Control Register 1 (FCtrl1, 0x0402)

0x0402, R/W, Flash Control Register 1, FCtrl1			
Bit		**Default**	**Description**
Bit7	-	-	Set this bit to **'1'** to activate write operation of other bits.
Bit6	CKSL	0	When the MCU clock frequency (f_{MCU}) is 3.2768 MHz, clear this bit to enable programming, page erase, and mass erase of Flash memory. When f_{MCU} is 13.1072 MHz, set this bit to **'1'** to enable programming, page erase, and mass erase of Flash memory.
Bit[5:0]	Reserved	0	These bits must hold their default values for proper operation.

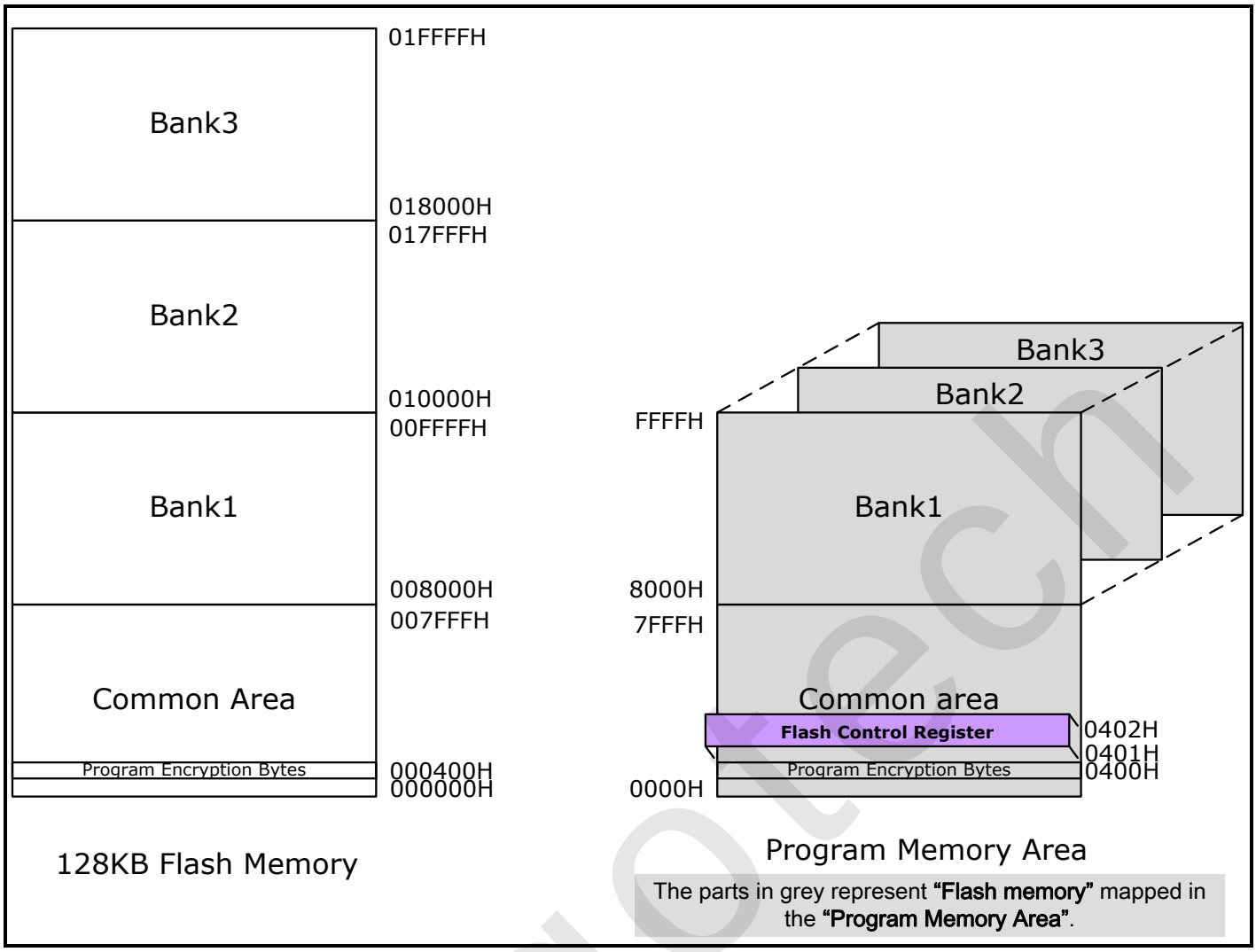


Figure 4-3 Flash Memory and Program Memory Area

The 128-KB on-chip Flash memory of V98XX is featured with write protection, program encryption, and ISP (In-System Programming), and IAP (In-Application Programming) supported.

The 8052 MCU core of V98XX can address up to 64-KB program memory area, **"0000h" ~ "FFFFh"**, but the Flash memory can store up to 128-KB codes. So to execute more than 64-KB program, the code banking technique should be used. Using this technique, the program can be divided into no more than four parts with no more than 64-KB codes each, and is allocated in different parts of the Flash memory:

- **"Common Area"**, at addresses **"0000h" ~ "7FFFh"**: To allocate the common codes, such as interrupt vectors, reset vectors, bank switching routines, interrupt service routines, and so on. It is always mapped to the program memory area at addresses **"0000h" ~ "7FFFh"**.
- **"Code Area"**, at addresses **"8000h" ~ "1FFFFh"**: To allocate the application codes; Bank 1, at addresses **"8000h" ~ "FFFFh"**; Bank2, at addresses **"10000h" ~ "17FFFh"**; Bank 3, at addresses **"18000h" ~ "1FFFFh"**. **Each bank can be mapped to the program memory area at addresses "8000h" ~ "FFFFh",** and the processor can access the register **"CBANK"** (SFR 0xA0) to switch the banks and execute the codes.

Table 4-5 Code Bank Register (CBANK, SFR 0xA0)

SFR 0xA0, R/W, Code Bank Register, CBANK			
Bit		**Default**	**Description**
bit[7:2]	Reserved	0	
bit[1:0]	B<1:0>	1	To select code bank to be mapped to the code area of the program memory space at addresses **"8000h" ~ "FFFFh"**. 01: Bank 1; 10: Bank 2; 11: Bank 3.

In V98XX, the on-chip Flash memory is divided into 256 pages with 512 bytes each. The codes in the Flash memory can be read, erased, or programmed in pages or mass erased.

Notes: The third page of the Flash memory, at addresses **"0400h" ~ "05FFh"**, is pre-programmed with codes by the manufacturer, so this part cannot be used for application codes.

When the low logic level is input on the pin **"MODE1"**, the chip will be in the debugging mode. In this mode, the 4 pins of Group P0 work as JTAG interfaces. Users can use the DLL codes and simulators provided by Vango to download and debug the applications in Keil µVision IDE or IAR IDE via the JTAG interfaces.

Notes:

Please comment the lines, like `switching the system clock source from PLL clock to OSC clock, and get to sleep`, out of the codes.

In the debugging mode, the system cannot get to **"Sleep"** or **"Deep Sleep"**, and the reset events, POR/BOR and WDT overflow, are masked. In the sleeping state, a power recovery event will occur immediately once the system goes to the debugging mode.

In the debugging mode, the TCK speed limit is 400 Kbps by default. The command **"0x22"** can increase it to the current PLL clock frequency, and the command **"0x23"** can recover it.

No capacitors should be connected to the JTAG interfaces to avoid the download failure of codes.

There is an encryption bit (**"bit0"** of byte located at address **"0x0400"**) in the Flash memory. The configuration of this bit has effect on the access to the Flash memory. When the high logic level is input on the pin **"MODE1"**, the chip will be in the metering mode. In this mode, the on-chip Flash memory is IAP supportive, and the access to the Flash memory will not be affected by the encryption bit configuration. When the low logic level is input on the pin **"MODE1"**, the chip will be in the metering mode. In this mode, the on-chip Flash memory is IAP and ISP supportive, and the encryption bit configuration will affect the access to the Flash memory.

Table 4-6 Programming Flash Memory

Programming	Flash memory	Write 0 to encryption bit	Write 1 to encryption bit

method		Mass erase	Write	Read	Page erase	Mass erase	Write	Read	Page erase
In debugging mode（IAP or ISP）	00000h~17FFFh	√	X	X	X	√	√	√	√
	18000h~1FFFFh		X	√	X				
IAP in metering mode	00000h~003FFh	X	X	√	X	X	X	√	X
	00400h~1FFFFh		√	√	√		√	√	√

Note: After ISP, the input logic low to the pin **"RSTn"** or power on the chip again to activate the ISP read encryption.

4.5. Instruction Set

The instruction set of the enhanced 8052 core is compatible with the industry standard 8051 MCU in binary code and the execution results are functionally equivalent. However, the number of clock cycles that each instruction cycle needs is different from that of the standard 8051 instruction set. And the execution timing of each instruction is also different from that of standard 8051 MCU. Each instruction cycle has four clock cycles.

Table 4-7 Instruction Set

Symbol	Description			
A	Accumulator			
Rn	Register R0 ~ R7			
direct	Internal direct addressable registers			
@Ri	Internal register pointed to by R0 or R1 (Except MOVX)			
rel	Two's complement offset byte			
bit	Direct bit address			
#data	8-bit constant			
#data 16	16-bit constant			
addr 16	16-bit destination address			
addr 11	11-bit destination address			
Mnemonic	**Description**	**Byte**	**Inst. Cycles**	**Hex Code**
Arithmetic				
ADD A, Rn	Add register to A	1	1	28 – 2F
ADD A, direct	Add direct byte to A	2	2	25

ADD A, @Ri	Add data memory to A	1	1	26 – 27
ADD A, #data	Add immediate to A	2	2	24
ADDC A, Rn	Add register to A with carry	1	1	38 – 3F
ADDC A, direct	Add direct byte to A with carry	2	2	35
ADDC A, @Ri	Add data memory to A with carry	1	1	36 – 37
ADDC A, #data	Add immediate to A with carry	2	2	34
SUBB A, Rn	Subtract register from A with borrow	1	1	98 – 9F
SUBB A, direct	Subtract direct byte from A with borrow	2	2	95
SUBB A, @Ri	Subtract data memory from A with borrow	1	1	96 – 97
SUBB A, #data	Subtract immediate from A with borrow	2	2	94
INC A	Increment A	1	1	04
INC Rn	Increment register	1	1	08 – 0F
INC direct	Increment direct byte	2	2	05
INC @Ri	Increment data memory	1	1	06 – 07
DEC A	Decrement A	1	1	14
DEC Rn	Decrement register	1	1	18 – 1F
DEC direct	Decrement direct byte	2	2	15
DEC @Ri	Decrement data memory	1	1	16 – 17
INC DPTR	Increment data pointer	1	3	A3
MUL AB	Multiply A by B	1	5	A4
DIV AB	Divide A by B	1	5	84
DA A	Decimal adjust A	1	1	D4
Logical				
ANL A, Rn	AND register to A	1	1	58 – 5F
ANL A, direct	AND direct byte to A	2	2	35
ANL A, @Ri	AND data memory to A	1	1	56 – 57
ANL A, #data	AND immediate to A	2	2	54
ANL direct, A	AND A to direct byte	2	2	52
ANL direct, #data	AND immediate data to direct byte	3	3	53
ORL A, Rn	OR register to A	1	1	48 – 4F
ORL A, direct	OR direct byte to A	2	2	45

ORL A, @Ri	OR data memory to A	1	1	46 – 47
ORL A, #data	OR immediate to A	2	2	44
ORL direct, A	OR A to direct byte	2	2	42
ORL direct, #data	OR immediate data to direct byte	3	3	43
XRL A, Rn	Exclusive-OR register to A	1	1	68 – 6F
XRL A, direct	Exclusive-OR direct byte to A	2	2	65
XRL A, @Ri	Exclusive-OR data memory to A	1	1	66 – 67
XRL A, #data	Exclusive-OR immediate to A	2	2	64
XRL direct, A	Exclusive-OR A to direct byte	2	2	62
XRL direct, #data	Exclusive-OR immediate to direct byte	3	3	63
CLR A	Clear A	1	1	E4
CPL A	Complement A	1	1	F4
SWAP A	Swap nibbles of A	1	1	C4
RL A	Rotate A left	1	1	23
RLC A	Rotate A left through carry	1	1	33
RR A	Rotate A right	1	1	03
RRC A	Rotate A right through carry	1	1	13
Data Transfer				
MOV A, Rn	Move register to A	1	1	E8 – EF
MOV A, direct	Move direct byte to A	2	2	E5
MOV A, @Ri	Move data memory to A	1	1	E6 – E7
MOV A, #data	Move immediate to A	2	2	74
MOV Rn, A	Move A to register	1	1	F8 – FF
MOV Rn, direct	Move direct byte to register	2	2	A8 – AF
MOV Rn, #data	Move immediate to register	2	2	78 – 7F
MOV direct, A	Move A to direct byte	2	2	F5
MOV direct, Rn	Move register to direct byte	2	2	88 – 8F
MOV direct, direct	Move direct byte to direct byte	3	3	85
MOV direct, @Ri	Move data memory to direct byte	2	2	86 – 87
MOV direct, #data	Move immediate to direct byte	3	3	75
MOV @Ri, A	MOV A to data memory	1	1	F6 – F7

MOV @Ri, direct	Move direct byte to data memory	2	2	A6 – A7
MOV @Ri, #data	Move immediate to data memory	2	2	76 – 77
MOV DPTR, #data	Move immediate to data pointer	3	3	90
MOVC A, @A+DPTR	Move code byte relative DPTR to A	1	3	93
MOVC A, @A+PC	Move code byte relative PC to A	1	3	83
MOVX A, @Ri	Move external data (A8) to A	1	2 – 9*	E2 – E3
MOVX A, @DPTR	Move external data (A16) to A	1	2 – 9*	E0
MOVX @Ri, A	Move A to external data (A8)	1	2 – 9*	F2 – F3
MOVX @DPTR, A	Move A to external data (A16)	1	2 – 9*	F0
PUSH direct	Push direct byte onto stack	2	2	C0
POP direct	Pop direct byte from stack	2	2	D0
XCH A, Rn	Exchange A and register	1	1	C8 – CF
XCH A, direct	Exchange A and direct byte	2	2	C5
XCH A, @Ri	Exchange A and data memory	1	1	C6 – C7
XCHD A, @Ri	Exchange A and data memory nibble	1	1	D6 – D7
* Number of cycles is user-selectable.				
Boolean				
CLR C	Clear carry	1	1	C3
CLR bit	Clear direct bit	2	2	C2
SETB C	Set carry	1	1	D3
SETB bit	Set direct bit	2	2	D2
CPL C	Complement carry	1	1	B3
CPL bit	Complement direct bit	2	2	B2
ANL C, bit	AND direct bit to carry	2	2	82
ANL C, /bit	AND direct bit inverse to carry	2	2	B0
ORL C, bit	OR direct bit to carry	2	2	72
ORL C, /bit	OR direct bit inverse to carry	2	2	A0
MOV C, bit	Move direct bit to carry	2	2	A2
MOV bit, C	Move carry to direct bit	2	2	92
Branching				
ACALL addr 11	Absolute call to subroutine	2	3	11 – F1

LCALL addr 16	Long call to subroutine	3	4	12
RET	Return from subroutine	1	4	22
RETI	Return from interrupt	1	4	32
AJMP addr 11	Absolute jump unconditional	2	3	01 – E1
LJMP addr 16	Long jump unconditional	3	4	02
SJMP rel	Short jump (relative address)	2	3	80
JC rel	Jump on carry = 1	2	3	40
JNC rel	Jump on carry = 0	2	3	50
JB bit, rel	Jump on direct bit = 1	3	4	20
JNB bit, rel	Jump on direct bit = 0	3	4	30
JBC bit, rel	Jump on direct bit = 1 and clear	3	4	10
JMP @A + DPTR	Jump indirect relative DPTR	1	3	73
JZ rel	Jump on accumulator = 0	2	3	60
JNZ rel	Jump on accumulator ≠ 0	2	3	70
CJNE A, direct, rel	Compare A, direct JNE relative	3	4	B5
CJNE A, #d, rel	Compare A, immediate JNE relative	3	4	B4
CJNE Rn, #d, rel	Compare reg, immediate JNE relative	3	4	B8 – BF
CJNE @Ri, #d, rel	Compare ind, immediate JNE relative	3	4	B6 – B7
DJNZ Rn, rel	Decrement register, JNZ relative	2	3	D8 – DF
DJNZ direct, rel	Decrement direct byte, JNZ relative	3	4	D5
Miscellaneous				
NOP	No operation	1	1	00
There is an additional reserved opcode (A5) that performs the same function as NOP.				

4.5.1. Programmable MOVX Timing

The programmable MOVX timing feature enables application to adjust the speed of the access to the data memory. CPU can execute the MOVX instruction in as little as two instruction cycles. However, it is sometimes desirable to stretch this value. **"Bit2" ~ "bit0"** (MD2~0) of **"CKCON"** (SFR 0x8E) control the stretch value, which can set the stretch value from **'0'** to **'7'**. A stretch value of **'0'** means no extra instruction cycles are added and the MOVX instructions will be executed in two instruction cycles. A stretch value of **'7'** means additional seven instruction cycles are added, and the MOVX instructions will be executed in nine instruction cycles. The stretch value is programmable. The stretch value will affect the width of the read/write strobe and all related timing. A higher stretch value results in a wider read/write strobe. By default the stretch value is **'1'**, meaning three instruction cycles are needed to execute the

MOVX instruction.

Table 4-8 Programmable MOVX Timing

Configuring the stretch value			Cycles to access the memory	Read/write strobe width (clocks)
MD2	MD1	MD0		
0	0	0	2	2
0	0	1	3 (default value)	4
0	1	0	4	8
0	1	1	5	12
1	0	0	6	16
1	0	1	7	20
1	1	0	8	24
1	1	1	9	28

4.5.2. Dual Data Pointers

Dual data pointers, standard data pointer **"DPTR0"** located at addresses **"SFR 0x82"** and **"SFR 0x83"**, and the second data pointer **"DPTR1"** located at addresses **"SFR 0x84"** and **"SFR 0x85"**, can improve the efficiency significantly when moving large blocks of data. The bit **"SEL"** (bit0) in the DPTR Select Register (DPS, SFR 0x86) is configured to select the active pointer. When **"SEL"** is cleared, **"DPL0"** (SFR 0x82) and **"DPH0"** (SFR 0x83) are selected. When **"SEL"** is set to **'1', "DPL1"** (SFR 0x84) and **"DPH1"** (SFR 0x85) are selected.

All DPTR-related instructions use the selected data pointer. Rewrite of the bit **"SEL"** to switch the pointer. The fastest way to do so is to use the increment instruction (INC DPS). Only one instruction is required to switch from the source address to the target address. When doing a block move, it is no need to save source and target addresses, which saves the number of application codes.

5.Reset

In V98XX, all circuits, except for the RTC calibration registers, RTC timing registers, IRAM, XRAM, and Info area, can be reset to their default states by an event of a specific reset level. Three levels of events are designed to reset different circuits of the system. They are:

- **Level 3:** The lowest level, including the debugging reset instruction.
  When the event of this level occurs, CPU, interrupt management circuits, timers, UART interfaces, and GPSI interfaces will be reset to their default states.
- **Level 2:** Including the power recovery (Power up), IO wakeup event, RTC wakeup event, and CF pulse wakeup event.
  When an event of this level occurs, **"Clock Switchover Control Register"** (**"SysCtrl"**, SFR 0x80), **"IO Wakeup Control Register"** (**"IOWK"**, SFR 0xC9), **"IO Wakeup Edge Control Register"** (**"IOEDG"**, SFR 0xC7), Flash control registers, watch-dog timer, and all the circuits that can be reset by events of Level 3 will be reset to their default states.
- **Level 1:** The highest level, including the RSTn pin input signal (RSTn pin reset), power-on reset (POR), brown-out reset (BOR), and WDT overflow event.
  When an event of this level occurs, the LCD driver, general-purpose I/O ports, **"System State Register"** (**"Systate"**, SFR 0xA1), **"P0 IO Wakeup Flag Register"** (**"IOWKDET"**, SFR 0xAF), analog control registers, the global energy metering architecture, and all the circuits that can be reset by events of Level 2 will be reset to their default states.

In V98XX, the reset management circuits are designed by following the rule that a reset event of higher level can reset the circuits that can be reset by a reset event of lower level, but not *vice versa*.

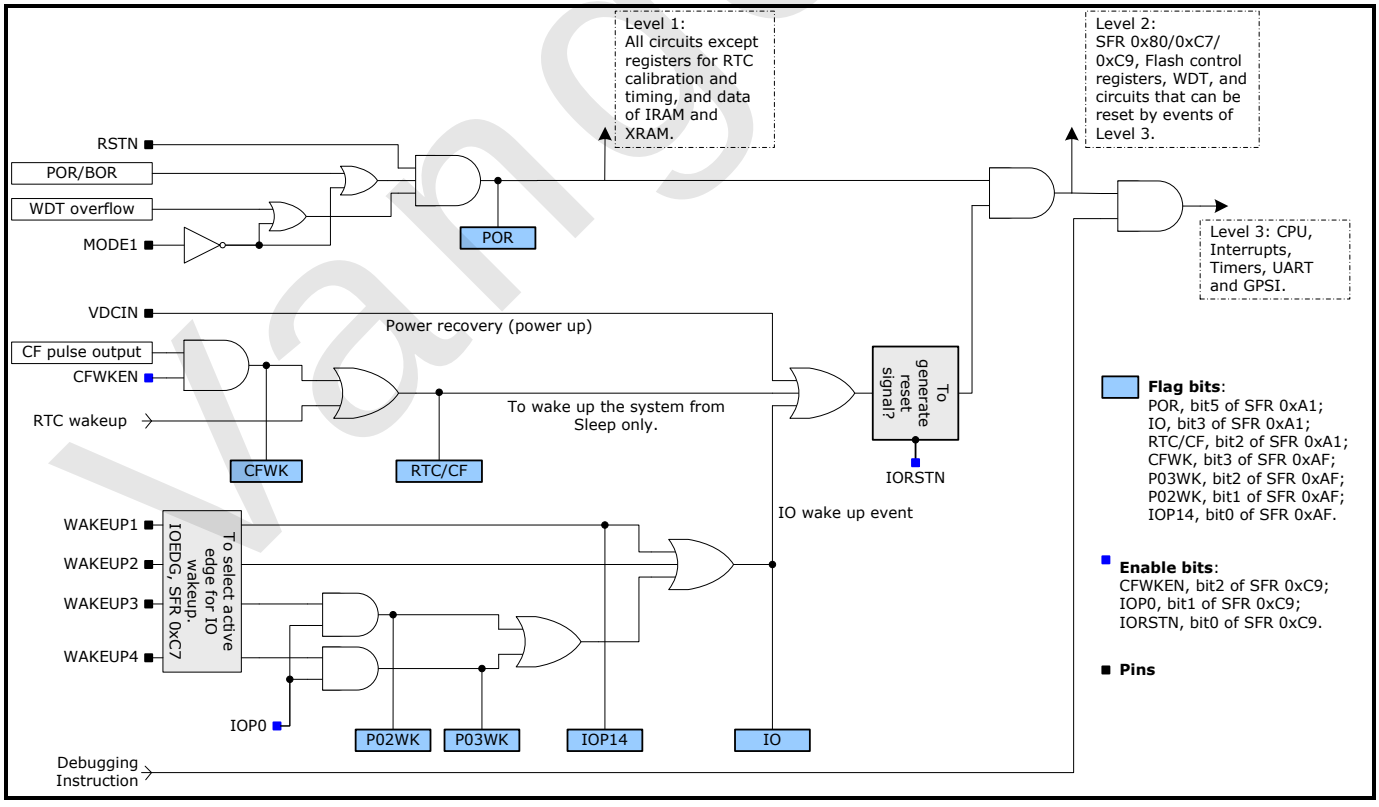


Figure 5-1 Reset Unit Diagram

Table 5-1 Circuits to Be Reset

Unit		Reset by		
		Events of Level 1	Events of Level 2	Events of Level 3
CPU		√	√	√
Interrupts		√	√	√
Timers		√	√	√
UART		√	√	√
GPSI		√	√	√
Flash control registers		√	√	X
SysCtrl (SFR 0x80)		√	√	X
IOEDG (SFR 0xC7)		√	√	X
IOWK (SFR 0xC9)		√	√	X
WDT		√	√	X
Systate (SFR 0xA1)		√	X	X
IOWKDET (SFR 0xAF)		√	X	X
Global Energy Metering Architecture (VMA)		√	X	X
Analog control registers		√	X	X
Electricity metering all registers about VMA		√	X	X
LCD driver		√	X	X
General-purpose I/O ports (GPIO)		√	X	X
RTC	Calibration registers	X	X	X
	Timing registers	X	X	X
	Other registers	√	X	X
IRAM		X	X	X
XRAM		X	X	X
Info area (0x3000~0x33FF)		X	X	X

5.1. Level 3

In V98XX, only the debugging reset instruction is designed as the reset event of Level 3. It can reset CPU, interrupt management circuits, timers, UART interfaces, and GPSI interfaces.

When **"logic 0"** is input to the pin **"MODE1"**, the system will enter the debugging mode. In this mode, when the debugging operation is enabled or the tab **"Reset"** in IDE is clicked, a debugging reset instruction will be executed to reset CPU and its peripherals.

5.2. Level 2

In V98XX, power recovery, IO wakeup event, RTC wakeup event, and CF pulse wakeup event are designed as the reset events of Level 2.

By default, any event of this level can wake up the system from **"Sleep"** or **"Deep Sleep"** and reset the system to OSC state. But if the bit **"IORSTN"** (**"bit0"** of **"IOWK**", SFR 0xC9) is set to **'1'**, any event of this level can wake up the system without reset, after wakeup, CPU keeps on executing programs; all circuits go back where the system enters the sleeping state, but **"bit[2:1]"** (**"SLEEP1"** and **"SLEEP0"**) and **"bit[6:5]"** (**"FWC"** and **"FSC"**) are cleared.

When **"IORSTN"** (**"bit0"** of **"IOWK"**, SFR 0 xc9) is cleared, in addition to the reset circuit which can be reset by Level 3 reset events, the wakeup events can reset the clock switch control register (**"SysCtrl"**, SFR 0 x80), IO dormancy awakening edge selection register (**"IOEDG"**, SFR 0 xc7), IO dormancy awakened control register (**"IOWK"**, SFR 0 xc9), FLASH control registers and WDT, please refer to Figure 5-1 for more detailed information.

5.2.1. Power Recovery (Power up)

In V98XX, when the voltage on the pin **"VDCIN"** rises from lower than 1.0 V to higher than 1.1 V, or when the voltage on the pin **"VDCIN"** is higher than 1.1 V after any reset event of Level 1, a power recovery event will occur. By default, this event wakes up the chip and resets it to the OSC state, and the reset signal holds 8 OSC clock cycles (About 244 μs). To lower the power consumption, users can set the bit **"IORSTN"** (**"bit0"** of **"IOWK"**, SFR 0xC9) to **'1'** to wake up the system without reset.

5.2.2. IO Wakeup Event

In V98XX, 4 pins, **"WAKEUP1 (P1.4)", "WAKEUP2 (P1.3)", "WAKEUP3 (P0.2)",** and **"WAKEUP4 (P0.3)"** can be used to wake up the chip from **"Sleep"** or **"Deep Sleep"**. Pins **"WAKEUP1"** and **"WAKEUP2"** can be used for the wakeup input all the time, but pins **"WAKEUP3"** and **"WAKEUP4"** can be used for the wakeup input only when the bit **"IOP0"** (**"bit1"** of **"IOWK"**, SFR 0xC9) is set to **'1'.** The wakeup input on these four I/O ports are independent.

If the four I/O ports are set to **"Input enabled"** before the chip enters **"Sleep"** or **"Deep Sleep"**, a transition (Either **"high-to-low"** or **"low-to-high"**, with more than four OSC clock cycles on both levels) on the pin in **"Sleep"** or **"Deep Sleep"** can wake up the system. Users can configure the register **"IOEDG"** (SFR 0xC7) to determine the active edge for the IO wakeup event. Any IO wakeup event can set

the bit **"IO"** (**"bit3**" of **"Systate"**, SFR 0xA1) to **'1'.** When the bit **"IO"** is set to **'1'**, users can read bits **"P14WK"**, **"P02WK",** and **"P03WK"** (**"bit[0:2]"** of **"IOWKDET"**, SFR 0xAF) to detect that the system is woken up by the transition on which pin.

By default, a transition on any one of the four I/O ports can wake up the system and reset it to the OSC state. To lower the power consumption, users can set the bit **"IORSTN"** (**"bit0"** of **"IOWK"**, SFR 0xC9) to **'1'** to wake up the system without reset.

5.2.3. RTC Wakeup Event

In V98XX, RTC can wake up the system from **"Sleep"** at an interval set in registers **"INTRTC"** (SFR 0x96) and **"SECINT"** (SFR 0xDF). When the system is woken up by an RTC event, the bit **"RTC/CF"** (**"bit2"** of **"Systate"**, SFR 0xA1) will be set to **'1'**, but the bit **"CFWK"** (**"bit3**" of **"IOWKDET"**, SFR 0xAF) will be cleared. Please refer to Figure 5-1 for more detailed information.

By default, RTC wakeup event can wake up the system from **"Sleep"** and reset it to the OSC state. The reset signal holds 8 OSC clock cycles. To lower the power consumption, users can set the bit **"IORSTN"** (**"bit0"** of **"IOWK**", SFR 0xC9) to **'1'** to wake up the system without reset.

5.2.4. CF Pulse Wakeup Event

In V98XX, the system may be woken up from **"Sleep"** by CF pulse output, if CF pulse output is enabled (**"CFENR"** = **'1'** or **"CFEN"** = **'1'**, **"bit[5:4]"** of **"PMCtrl4"**, 0x287D), and CF pulse output is enabled to be a wakeup event (**"CFWKEN"** = **'1'**, **"bit2"** of **"IOWK"**, SFR 0xC9) before the system enters **"Sleep".** When a CF pulse wakeup event occurs, both bits **"RTC/CF"** (**"bit2"** of **"Systate"**, SFR 0xA1) and **"CFWK"** (**"bit3"** of **"IOWKDET"**, SFR 0xAF) are set to 1s.

By default, a CF pulse wakeup event can wake up the system from **"Sleep"** and reset it to the OSC state. To lower the power consumption, users can set the bit **"IORSTN"** (**"bit0"** of **"IOWK",** SFR 0xC9) to **'1'** to wake up the system without reset.

5.3. Level 1

In V98XX, WDT overflow, RSTn pin input signal, Power-On Reset (POR), and Brown-Out Reset (BOR) are designed as the reset events of Level 1. When any one of these reset events occurs, the bit **"POR"** (**"bit5"** of **"Systate"**, SFR 0xA1) will be set to **'1'**.

5.3.1. RSTn Pin Reset

Holding logic low on the pin **"RSTn"** for more than 5 ms can trigger an RSTn pin reset signal to reset the system. After the logic is pulled high, the reset signal holds four more OSC clock cycles (About 122 μs) and then is released.

To prevent from the static disturbance, the input signal on the pin **"RSTn"** is filtered basing on the RC clock.

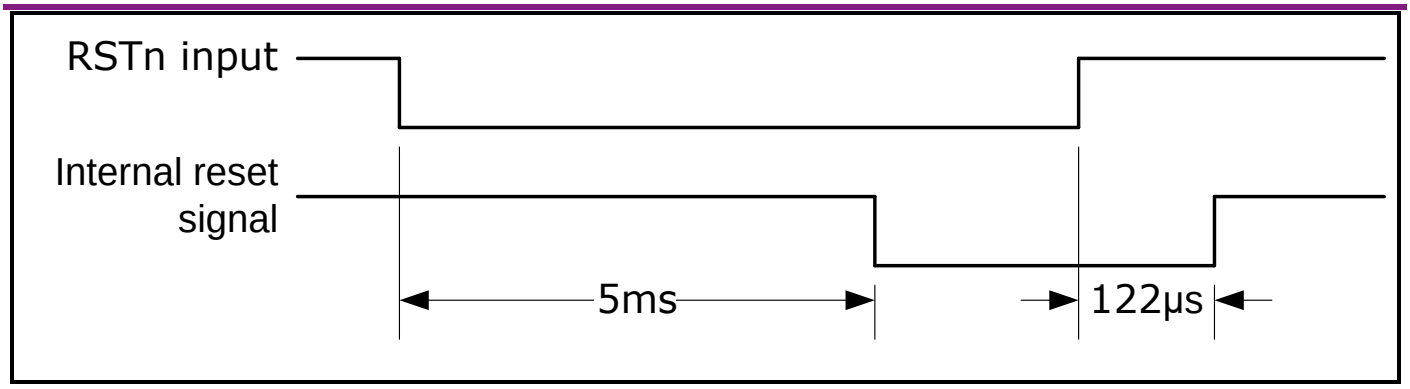


Figure 5-2 RSTn Pin Reset Timing

5.3.2. Power-On Reset (POR) and Brown-Out Reset (BOR)

In V98XX, the output voltage of the digital power supply (Via pin **"DVCC"**) is monitored by the power-on/brown-out reset circuit.

On power-up, a power-on reset signal will be generated to reset the system when the output voltage of pin **"DVCC"** is lower than 1.4 V. The system will stay in the reset state for four OSC clock cycles (About 122 μs) even when the voltage on the pin **"DVCC"** is higher than 1.4 V.

On power-down, when the output voltage on the pin **"DVCC"** is lower than 1.4 V, the brown-out reset circuit will generate a reset signal to reset the system.

When **"logic 0"** is input to the pin **"MODE1"**, POR/BOR will be masked.

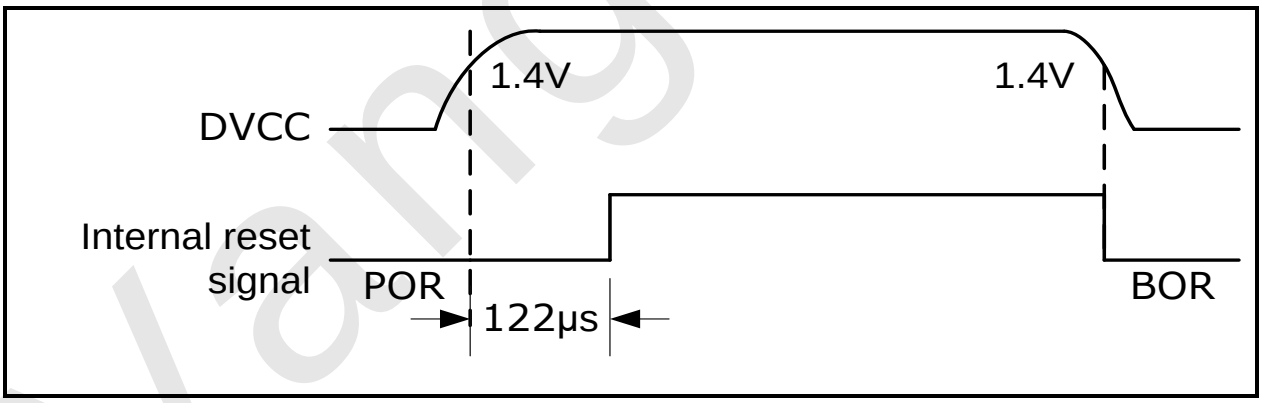


Figure 5-3 POR/BOR Timing

5.3.3. WDT Overflow Reset

In V98XX, when the WDT overflows, a reset signal will be generated and the system will be reset. The system will exit from the reset state in eight RC clock cycles (About 250 μs).

When **"logic 0"** is input to the pin **"MODE1"**, WDT overflow reset will be masked.

5.4. Registers

Table 5-2 System State Register, Systate (SFR 0xA1)

SFR 0xA1, R, System State Register, Systate		
Bit	**Default**	**Description**
Bit[7:6]		Reserved.
Bit5 POR	0	When this bit is read out as **'1',** it indicates the system is reset by an event of Level 1: POR/BOR, RSTn pin reset, or WDT overflow reset. This bit will be cleared when a reset event of other levels occurs.
Bit4	0	Reserved
Bit3 IO	0	When this bit is read out as **'1'**, it indicates the system is woken up from **"Sleep"** or **"Deep Sleep"** by an IO wakeup event.
Bit2 RTC/CF	0	When this bit is read out as **'1'**, but bit **"CFWK"** (**"bit3"** of **"IOWKDET"**, SFR 0xAF) is cleared, it indicates the system is woken up from **"Sleep"** by RTC wakeup event. If both this bit and bit **"CFWK"** are set to 1s, it indicates the system is woken up from **"Sleep"** by CF pulse wakeup event.
Bit1 PWRDN	0	When the input voltage on pin **"VDCIN"** is lower than 1.0 V, this bit is read out as **'1'**, indicating that the system is powered down. If the power down interrupt is enabled, an interrupt will be triggered when this bit is read out as **'1'**. When the input voltage on pin **"VDCIN"** is higher than 1.1 V, this bit holds its default value, indicating no power down event occurs.
Bit0 PWRUP	0	When the input voltage on pin **"VDCIN"** is higher than 1.1 V, this bit is read out as **'1',** indicating that the system is powered up by line power supply. When the input voltage on pin **"VDCIN"** is lower than 1.0 V, this bit holds its default value, indicating the system is powered up by the battery.

Table 5-3 P0 IO Wakeup Flag Register (IOWKDET, SFR 0xAF)

SFR 0xAF, R, P0 IO Wakeup Flag Register, IOWKDET				
Bit		**R/W**	**Default**	**Description**
Bit[7:4]	Reserved	-	-	
bit3	CFWK	R	0	If this bit is set to **'1'** when bit **"RTC/CF"** (**"bit2"** of **"Systate"**, SFR 0xA1) is read out as **'1',** it indicates that system is woken up from Sleep by CF pulse wakeup event.
Bit2	P03WK	R	0	If this bit is set to **'1'** when bit **"IO"** (**"bit3"** of **"Systate"**, SFR

SFR 0xAF, R, P0 IO Wakeup Flag Register, IOWKDET				
Bit		**R/W**	**Default**	**Description**
				0xA1) is read out as **'1',** it indicates the system is woken up from **"Sleep"** or **"Deep Sleep"** by a transition on pin **"WAKEUP4"** (P0.3).
Bit1	P02WK	R	0	If this bit is set to **'1'** when bit **"IO"** (**"bit3**" of **"Systate",** SFR 0xA1) is read out as **'1',** it indicates the system is woken up from **"Sleep"** or **"Deep Sleep"** by a transition on pin **"WAKEUP3"** (P0.2).
bit0	P14WK	R	0	If this bit is set to **'1'** when bit **"IO"** (**"bit3"** of **"Systate"**, SFR 0xA1) is read out as **'1',** it indicates the system is woken up from **"Sleep"** or **"Deep Sleep"** by a transition on pin **"WAKEUP1"** (P1.4).
When an event of reset Level 1 occurs, this register will be reset to its default state.				

Table 5-4 IO Wakeup Edge Control Register (IOEDG, SFR 0xC7)

SFR 0xC7, R/W, IO Wakeup Edge Control Register, IOEDG				
Bit		**R/W**	**Default**	**Description**
bit[7:6]	P03EDG	R/W	0	To set the active edge for pin **"WAKEUP4"** (P0.3) 00/11: high-to-low transition; 01: low-to-high transition; 10: either transition.
bit[5:4]	P02EDG	R/W	0	To set the active edge for pin **"WAKEUP3"** (P0.2) 00/11: high-to-low transition; 01: low-to-high transition; 10: either transition.
bit[3:2]	P14EDG	R/W	0	To set the active edge for pin **"WAKEUP1"** (P1.4) 00/11: high-to-low transition; 01: low-to-high transition; 10: either transition.
bit[1:0]	P13EDG	R/W	0	To set the active edge for pin **"WAKEUP2"** (P1.3) 00/11: high-to-low transition; 01: low-to-high transition; 10: either transition.

Table 5-5 IO Wakeup Control Register (IOWK, SFR 0xC9)

SFR 0xC9, R/W, IO Wakeup Control Register, IOWK				
Bit		**R/W**	**Default**	**Description**
Bit[7:3]	Reserved	-	-	
bit2	CFWKEN	R/W	0	1: to enable CF pulse output to wake up the system from **"Sleep"**; 0: to disable CF pulse output to wake up the system from **"Sleep"**.
Bit1	IOP0	R/W	0	1: to enable IO wakeup event on either pin **"WAKEUP4"** (P0.3) or **"WAKEUP3"** (P0.2); 0: to disable IO wakeup event on either pin **"WAKEUP4"** (P0.3) or **"WAKEUP3"** (P0.2).
Bit0	IORSTN	R/W	0	1: IO event wakes up but not reset the system. After wakeup, CPU keeps on executing programs; all circuits go back where the system entered the sleeping state, but **"bit[2:1]"** (**"SLEEP1"** and **"SLEEP0"**) and **"bit[6:5]"** (**"FWC"** and **"FSC"**) are cleared. 0: IO event wakes up and reset the system. After wakeup, the system goes to OSC state.

Table 5-6 Set RTC Wake-Up Interval

SFR 0x96, RTC Wake-up Interval Register, INTRTC				
Bit		**Default**	**R/W**	**Description**
bit[7:3]		0	R/W	
bit[2:0]	RTC<2:0>	0	R/W	000: 1 second; 001: 1 minute; 010: 1 hour; 011: 1 day; 100: 500ms; 101: 250ms; 110: 125ms; 111: 62.5ms.

Table 5-7 RTC Seconds Wake-up Interval Configuration Register (SECINT, SFR 0xDF)

SFR 0xDF, R/W, RTC Seconds Wake-up Interval Configuration Register, SECINT			
Bit	**R/W**	**Default**	**Description**
Bit7	R/W	0	Reserved
Bit6	R/W	0	It is mandatory to set register **"INTRTC"** (SFR 0x96) to **"0x07"**, and then set this bit to **'1'** to set interval in unit of second in **"bit[5:0]"** of this register.
Bit[5:0]	R/W	0	To set interval in unit of second for RTC to wake up the system from **"Sleep"**. The actual wakeup interval is equal to (bit[5:0]+1) seconds, of which **"bit[5:0]"** can be set to **'1' ~ '63'** (Decimal). Setting these **"bit[5:0]"** to **'0'** (Decimal) forces the interval to be 62.5 ms.

6.Clock

In V98XX, there are three clock generation circuits:

- **RC oscillator circuit:** To generate an RC clock (**"RCCLK"**). This circuit stops running only when the chip is powered off.
- **Crystal oscillator circuit:** To generate an OSC clock (**"OSCCLK"**). Generally, this circuit stops running only when the chip is powered off, but it also will stop running in some special circumstances. This circuit is monitored by the OSC monitoring circuit that is sourced by RC clock. When this crystal oscillator circuit stops running, the RC clock will replace the OSC clock to source all circuits that are sourced by the OSC clock, and the monitoring circuit will stimulate the crystal oscillator circuit until it runs again.
- **Phase-locked loop (PLL) circuit**: To generate a PLL clock (**"PLLCLK"**). The PLL locks onto a multiple of the **"OSCCLK"** frequency to provide a stable clock: **"PLLCLK"**. This circuit can be disabled.

The above three clocks can work as the clock sources for the functional units:

- Clock 1 (**"CLK1", "MCUCLK"**) provides clock pulses for MCU (Including CPU, RAM, Flash memory, interrupt circuits, timers/UART serial interfaces, GPSI, and IO ports). The OSC clock and PLL clock can be the optional source for **"CLK1"**. This clock is enabled by default, and it can be disabled.
- Clock 2 (**"CLK2", "MTCLK"**) provides clock pulses for the energy metering architecture. The OSC clock and PLL clock can be the optional source for **"CLK2"**. This clock is enabled by default, and it can be disabled.
- Clock 3 (**"CLK3", "LCDCLK"**) provides clock pulses for the LCD driver. The OSC clock is the source of this clock, and this clock is enabled by default, and it can be disabled only when PLL clock is selected as the source for **"CLK1"** and **"CLK2"**.
- Clock 4 (**"CLK4", "WDTCLK"**) provides clock pulses for WDT. The RC clock is the source of this clock. This clock is disabled and enabled together with **"CLK1"**.
- Clock 5 (**"CLK5", "RTCCLK"**) provides clock pulses for RTC. The OSC clock is the source of this clock. This clock cannot be disabled.

Figure 6-1 illustrates the clock system architecture of V98XX.

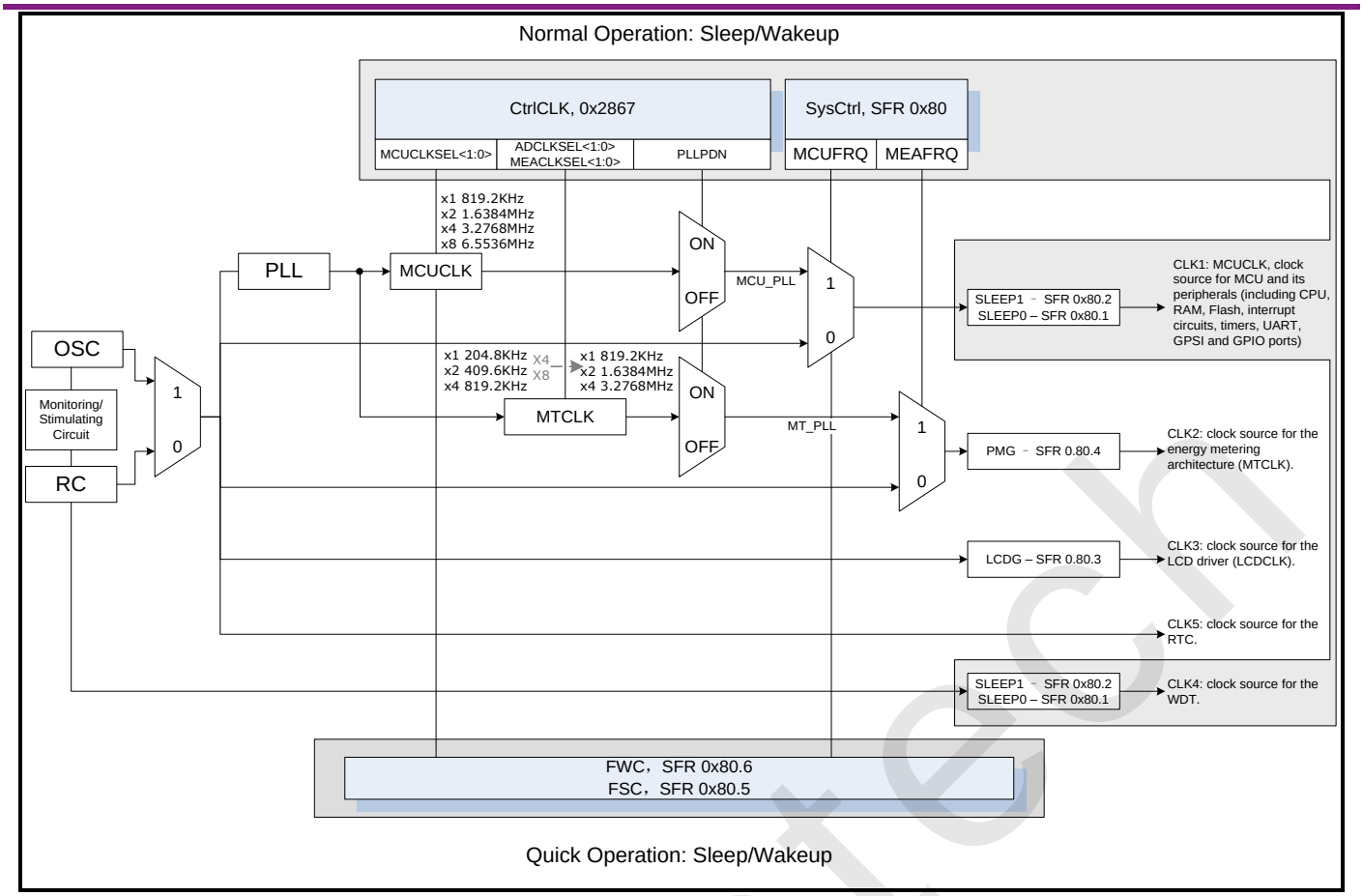


Figure 6-1 Clock System Architecture

6.1. RC Clock

In V98XX, there is an embedded RC oscillator circuit. It can generate an independent 32-kHz RC clock. It is the clock source for Clock 4 (**"CLK4"**) that provides clock pulses for WDT. The RC oscillator circuit will not stop running until the chip is powered off, but **"CLK4"** can be enabled or disabled together with **"CLK1"**.

There is a circuit monitoring the crystal oscillation and stimulating the oscillator to run again when it stops working. This circuit is sourced by the RC clock. When the crystal oscillator circuit stops running, the RC clock will immediately replace it to be the clock source for all circuits that are sourced by OSC clock. Users can read bit **"OSC"** (**"bit7"** of **"ANState"**, 0x286B) to detect whether the crystal stops running and has been replaced by RC clock to source all circuits.

6.2. OSC Clock

In V98XX, there is an embedded oscillator circuit with fixed capacitance of 12.5 pF. Connect this circuit to a 32768-Hz crystal around the pins **"CTO"** and **"CTI"** to compose a crystal oscillator circuit to generate a 32768-Hz OSC clock, an optional clock source for **"CLK1", "CLK2", "CLK3",** and **"CLK5"**. Users can configure the register **"P20FS"** (0x28C9) to measure the OSC clock waveform via pin **"P2.0"**. The clock frequency can be adjusted finely via configuring register **"CtrlCry1"** (0x2860) for the resistance and capacitance in the embedded oscillator circuit or connecting some additional capacitors around pins **"CTO"** and **"CTI"**. If RTC is used, bit **"XTRSEL<2:0>"** (**"bit[2:0]"** of **"CtrlCry1"**, 0x2860) must be set to

"0b011". It consumes 0.6 μA by default.

Generally, this circuit will not stop running until the chip is powered off, but some factors may cause the oscillator circuit to stop running. There is a circuit monitoring the crystal oscillation and stimulating it to run again when it stops working. This circuit is sourced by the RC clock. When the crystal oscillator circuit stops running, the RC clock will immediately replace it to be the clock source for all circuits that are sourced by OSC clock. Users can read bit **"OSC"** (**"bit7"** of **"ANState"**, 0x286B) to detect whether the crystal stops running and has been replaced with RC clock to source all circuits.

6.3. PLL Clock

The PLL circuit locks onto a multiple of the OSC clock frequency to provide some stable clock pulses, **"MEA_PLL"**, **"MCU_PLL",** and **"ADC_PLL",** for the energy metering architecture, MCU and its peripherals, and ADCs.

Start MCU and then enable the PLL circuit. When the PLL circuit is disabled, it will output the 32768-Hz OSC clock.

Users can enable the PLL circuit, and select the PLL clock as the source for **"CLK1"** and **"CLK2"** by following the steps:

1. Access to the register **"CtrlCLK"** (0x2867) to enable the PLL circuit, and configure the frequency of **"MCUCLK"** and **"MTCLK"**;
2. Wait for the configuration till PLL has locked. MCU can access to the register **"PLLLCK"** (SFR 0xA3) and read the bit **"PLLLCK"** to detect the state of the PLL circuit.
3. When the PLL circuit has locked, set the bit **"MCUFRQ"** or **"MEAFRQ**" (**"bit0"** or **"bit7"** of **"SysCtrl",** SFR 0x80) to **'1'** to select the PLL clock as the source for **"CLK1"** or **"CLK2"**. This duration spends one PLL clock cycle only.

Users must follow the steps to reconfigure the **"MTCLK"** frequency or **"MCUCLK"** frequency when PLL circuit is enabled:

1. Access to the register **"SysCtrl"** (SFR 0x80) to select the OSC clock as the source for **"CLK1"** or **"CLK2"**;
2. Access to the register **"CtrlCLK"** (0x2867) to adjust the frequency of **"MTCLK"** or **"MCUCLK"**;
3. Access to the register **"SysCtrl"** (SFR 0x80) to select the PLL clock as the source for **"CLK1"** or **"CLK2".**

V98XX is 50/60Hz-power-line supportive. By default the chip is applied for 50Hz-power-line. Users can set the bit **"PLLSEL"** ("**bit5**" of **"CtrlPLL"**, 0x2868) to '1' to configure the chip for the application in 60-Hz power grid. The PLL clock frequency in 60-Hz power grid is 1.2 times of that in 50-Hz power grid. In 60-Hz power grid, the parameters related to the clock frequency, such as the baud rate and timers, must be reconfigured. If not specifically noted, all information related to the clock frequency in this datasheet will be applied to 50-Hz power grid only.

In the full-speed operation, the **"MCUCLK"** frequency is 13.1072 MHz, **"MTCLK"** frequency is 3.2768 MHz, and **"ADCCLK"** frequency is 819.2 kHz which is a quarter of **"MTCLK"** frequency. The typical load current in the full-speed operation is 5.5 mA.

6.4. Switching Source for CLK1 and CLK2

In V98XX, there are two methods to switch the source for **"CLK1"**, and only one method to switch the source for **"CLK2"**.

- **Normal operation.** In this mode, MCU needs to access some registers to select the clock source for **"CLK1"** or **"CLK2"**, and/or to disable/enable the clock;
- **Quick operation.** In this mode, only one register is needed by MCU to access to trigger the hardware to enable/disable the PLL circuit, select the source for **"CLK1"**, and/or enable/disable "**CLK1"**. If this method is used to disable **"CLK1"**, the system will enter **"Sleep"** state, but not **"Deep Sleep"** state. If the chip is used for a low-power application, this method will be recommended.

6.4.1. Normal Operation

6.4.1.1. Switch Source for CLK1 and Disable CLK1

When the RSTn pin reset, POR/BOR, or WDT overflow reset occurs, the analog control registers and the register **"SysCtrl"** (SFR 0x80) are reset to their default states, which means the PLL circuit is disabled and "CLK1" is enabled and sourced by the OSC clock. After reset, access the analog control registers to enable the PLL circuit and configure the frequency of **"MCUCLK"**, and then set the bit **"MCUFRQ"** (**"bit0"** of **"SysCtrl"**, SFR 0x80) to **'1'** to select the PLL clock as the source for **"CLK1"**. Only one OSC clock cycle is needed for all the above processes.

It is mandatory to enable the PLL circuit before writing **'1'** to the bit **"MCUFRQ"** to select the source for **"CLK1"**. When **"CLK1"** is sourced by the PLL clock, the PLL clock frequency will change to 32768 Hz automatically if the PLL circuit is disabled anomaly, but the bit **"MCUFRQ"** is still read out as **'1'.** In this condition, MCU must read the bit **"PLLLCK"** ("**bit0"** of **"PLLLCK",** SFR 0xA3) to detect the state of the PLL circuit.

When **"CLK1"** is sourced by the PLL clock, clear the bit **"MCUFRQ"** (**"bit0"** of **"SysCtrl"**, SFR 0x80) to select the OSC clock as the source for **"CLK1**". This switchover needs no more than one OSC clock cycle. In this period, the write operation on the analog control registers is invalid. MCU can keep on reading this bit immediately once it is cleared. If this bit is read out as **'0'**, it indicates the switchover is finished.

When **"CLK1"** is sourced by the OSC clock, and the bit **"PWRUP"** (**"bit0"** of **"Systate"**, SFR 0xA1) is read out as **'0',** write **'1'** to the bit **"SLEEP0"** or **"SLEEP1"** (**"bit1"** or **"bit2"** of **"SysCtrl"**, SFR 0x80) to disable "CLK1" to force the system to enter "Deep Sleep" or "Sleep" state. When "CLK1" is disabled, MCU, including CPU, RAM, Flash memory, interrupt circuits, timers, UART interfaces, and GPIO ports, will stop working.

6.4.1.2. Switch Source for CLK2 and Disable CLK2

When the RSTn pin reset, POR/BOR, or WDT overflow reset occurs, the analog control registers and the register **"SysCtrl"** (SFR 0x80) will be reset to their default states, which means the PLL circuit is disabled; **"CLK2"** is enabled and sourced by the OSC clock. After the reset, access to the analog control registers

to enable the PLL circuit and configure the frequency of **"MTCLK",** and then set the bit **"MEAFRQ"** (**"bit7"** of **"SysCtrl"**, SFR 0x80) to **'1'** to select PLL clock as the source for **"CLK2"**. Only one OSC clock cycle is needed for all the above process.

It is mandatory to enable the PLL circuit and then to write **'1'** to the bit **"MEAFRQ"** to select the source for **"CLK2"**. When "**CLK2"** is sourced by the PLL clock, PLL clock frequency will change to 32768 Hz automatically if the PLL circuit is disabled anomaly, but the bit **"MEAFRQ"** is still read out as **'1'.** In this condition, MCU must read the bit **"PLLLCK"** (**"bit0"** of **"PLLLCK"**, SFR 0xA3) to detect the state of the PLL circuit.

When **"CLK2"** is sourced by PLL clock, clear the bit **"MEAFRQ"** (**"bit7"** of **"SysCtrl"**, SFR 0x80) to select the OSC clock as the source for **"CLK2"**. This switchover needs no more than one OSC clock cycle. In this period, the write operation on the analog control registers is invalid. MCU can keep on reading this bit immediately once it is cleared. When this bit is read out as '**0'**, it indicates the switchover is finished.

When **"CLK2"** is sourced by the OSC clock, write **'1'** to the bit **"PMG**" ("**bit4"** of **"SysCtrl"**, SFR 0x80) to disable **"CLK2"**. When **"CLK2"** is disabled, the energy metering architecture will stop working.

6.4.2. Quick Operation

This mode is applied to disable/enable the PLL circuit, select the source for **"CLK1"** and enable/disable **"CLK1"**. In this mode, only the register **"SysCtrl"** (SFR 0x80) needs to be accessed.

When the RSTn pin reset, POR/BOR, WDT overflow reset, power recovery event, or IO/RTC wakeup event occurs, the bits **"FWC"** and **"FSC" ("bit6"** and **"bit5"** of **"SysCtrl"**, SFR 0x80) are reset to 0s. So the program determines the state of the system, including the PLL circuit and the clock source for **"CLK1"**.

Clear the bit **"FSC"**, and then write **'1'** to the bit **"FWC"**, to enable the PLL circuit and select the PLL clock as the source for **"CLK1"** automatically. In this condition, the PLL clock frequency is 3.2768 MHz. The source for **"CLK1"** will be switched to PLL clock immediately once **'1'** is written to the bit **"FWC"**.

When the bit **"PWRUP"** (**"bit0"** of **"Systate"**, SFR 0xA1) is read out as **'0'**, write **'1'** to the bit "**FSC"** whatever the bit **"FWC"** is, to select the OSC clock to be the source for **"CLK1"**, to disable the PLL circuit, to disable **"CLK1"**, and to force the system to enter the **"Sleep"** state.

6.4.3. Normal Operation vs. Quick Operation

When the RSTn pin reset, POR/BOR, WDT overflow reset, power recovery event, or IO/RTC wakeup event occurs, the system will get into a temporary state in which the OSC clock is used as the clock source for **"CLK1"** and the energy accumulation unit can accumulate a constant only. In this state, the system consumes some power that should be diminished for the low-power-consumption applications. In the power-down state, the process of disabling the circuits consumes some power that should be also diminished.

In the normal operation, applications need to access analog control registers to get the system out of the temporary state or to disable the circuits in the power-down state. But in the quick operation, only the bits **"FSC"/"FWC"** need to be accessed. So, completing the above implementations in the quick operation is preferred.

But, as stated above, the clock source switchover in the normal operation and quick operation may affect each other:

- If the bits **"FSC"/"FWC"** are set to **"0b01"**, the configuration of the register **"CtrlCLK"** (0x2867) and the bit **"MCUFRQ"** (**"bit0"** of **"SysCtrl"**, SFR 0x80) cannot be activated, and the PLL clock frequency holds 3.2768 MHz.
- If the bit **"MCUFRQ"** is read out as **'1',** clearing the bits **"FSC"/"FWC"** cannot switch the clock source for **"CLK1"**.

To prevent MCU from the mis-operation, MCU can combine both methods, the combination operation: To enable the PLL circuit and switch the source for **"CLK1"** in the quick operation to lower the power consumption; and then, to hold the PLL clock frequency in the normal operation.

```
FWC = 1;          // Turn on PLL, and switch the clock source to PLL clock

MCUFRQ = 1;     // when PLL clock is the source for Clock 1
```

In the following table, the normal, quick, and combination operations are compared.

Table 6-1 Comparing Normal, Quick, and Combination Operation

Operation	Normal Operation	Quick Operation	Combination Operation
Enable PLL, and switch the source for CLK1 to PLL clock.	Access the analog control registers, enable the PLL circuit. MCUFRQ = 1;	FWC = 1	FWC = 1 MCUFRQ = 1
Switch source for CLK1 to OSC clock, disable PLL circuit, and disable CLK1.	MCUFRQ = 0; while(MCUFRQ == 1){;} access the analog control registers, disable PLL circuit. SLEEP0 = 1;	FSC = 1	MCUFRQ = 0 FSC = 1

The arrow in the following figure indicates the process from the IO wake-up event to completing the clock source switchover of **"CLK1"** to the 3.2768-MHz PLL clock, in the quick operation or combination operation, which lasts 800 μs ~ 900 μs, including the time to reset, to execute the initial long jump instruction, and to write **'1'** into **"FWC".**

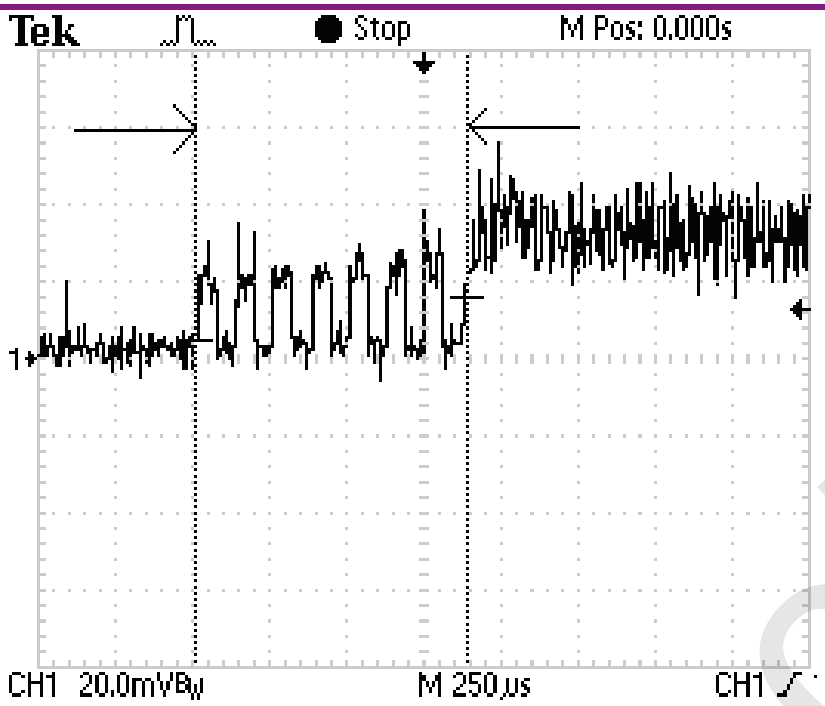


Figure 6-2 Enabling PLL Circuit and Clock Source Switchover to PLL in Quick Operation

The arrows in the following figure indicate the process from the clock source switchover of **"CLK1"** to **"OSC"** clock to disabling **"CLK1"**, in the quick or combination operation, which lasts less than 30 µs.

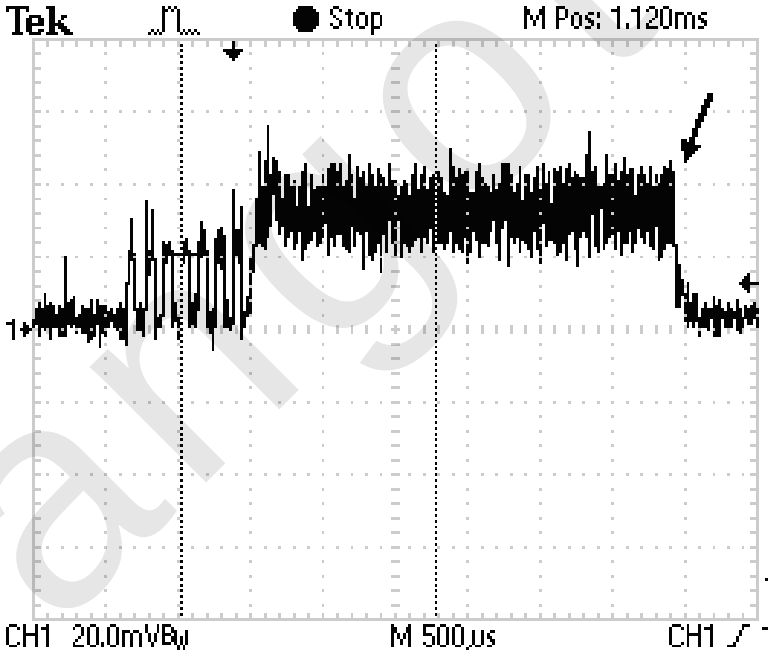


Figure 6-3 Clock Source Switchover to OSC, Disabling PLL Circuit, Disabling CLK1 in Quick Operation

6.5. Registers

Table 6-2 Clock Switchover Control Register (SysCtrl, SFR 0x80)

SFR 0x80, R/W, Clock Switchover Control Register, SysCtrl

Bit	Default	Description
bit7 MEAFRQ	0	To select the clock source for **"CLK2"** 0: OSC clock; 1: PLL clock. This bit is writable and readable. Configure this bit to switch the clock source for **"CLK2"**, and read this bit to acquire the current clock source for **"CLK2"**.
bit6 FWC	0	Only when the bit **"FSC"** is cleared will the configuration of **"FWC"** be activated. When the bit **"FSC"** is cleared, write **'1'** to this bit to enable the PLL circuit to start running and output a 3.2768-MHz PLL clock, and to select this clock to be the clock source for **"CLK1"**. When the bit **"FSC"** is cleared, write **'1'** to the bit **"FWC",** the clock setting will be locked. Writing **'0'** to the bit "**FWC"** will unlock the clock setting without switching the clock.
bit5 FSC	0	Write **'1'** to this bit to select the OSC clock as the clock source for **"CLK1"**, to disable the PLL clock, and to disable **"CLK1"**. If the bit **"PWRUP"** is read out as **'0'**, setting this bit to **'1'** will make the system enter **"Sleep"** state, but not **"Deep Sleep**". If the bit **"PWRUP"** is read out as '**1'**, setting this bit to **'1'** cannot force the system enter the "**Sleep"** state.
bit4 PMG	0	Set this bit to **'1'** to stop **"CLK2"**. By default this clock is running.
bit3 LCDG	0	Set this bit to **'1'** to stop **"CLK3"**. By default this clock is running. Only when the PLL clock is selected as the clock source for **"CLK1"** and **"CLK2"**, **"CLK3"** can be stopped.
bit2 SLEEP1 bit1 SLEEP0	0	When the bit **"PWRUP"** is read out as **'0',** write **'0'** to the bit **"MCUFRQ"**, and then: – Set **"SLEEP1"** and **"SLEEP0"** to **"0b11"** or **"0b01"** to stop **"CLK1**" (Together with **"CLK4"**) and force the system entering the "Sleep" state. – Set **"SLEEP1"** and **"SLEEP0"** to **"0b10"** to stop **"CLK1"** (Together with **"CLK4**") and force the system entering the **"Deep Sleep"** state.
bit0 MCUFRQ	0	To select the clock source for **"CLK1"** 0: OSC clock; 1: PLL clock. This bit is writable and readable. Configure this bit to switch the clock source for **"CLK1"**, and read this bit to acquire the current clock source for **"CLK1"**.

SFR 0x80, R/W, Clock Switchover Control Register, SysCtrl		
Bit	**Default**	**Description**
When bit **"IORSTN"** (**"bit0"** of **"IOWK"**, SFR 0xC9) is set to **'1',** any wakeup event can wake up the system from the sleeping state but cannot reset the system. After wakeup, CPU keeps on executing programs; all circuits hold their states where they were before sleeping; only **"bit[2:1]"** (**"SLEEP1"** and **"SLEEP0"**) and **"bit[6:5]"** (**"FWC"** and **"FSC"**) are cleared.		

Table 6-3 Peripheral Control Register 0 (PRCtrl0, 0x2D00)

0x2D00, R/W, Peripheral Control Register 0, PRCtrl0				
Bit		**R/W**	**Default**	**Description**
Bit7	PWMCLK	R/W	0	To enable or disable PWM clock generation circuit. 1: disable; 0: enable.
Bit6	GPSI	R/W	0	To enable or disable GPSI. 1: enable; 0: disable.
Bit5	P10	R/W	0	To enable or disable GPIOs Group P10. 1: disable; 0: enable.
Bit4	P9	R/W	0	To enable or disable GPIOs Group P9. 1: disable; 0: enable.
Bit3	P0P8	R/W	0	To enable or disable GPIOs Group P0~P8. 1: disable; 0: enable.
Bit2	EUART2	R/W	0	To enable or disable EUART2. 1: disable; 0: enable.
Bit1	EUART1	R/W	0	To enable or disable EUART1. 1: disable; 0: enable.
Bit0	TimerA	R/W	0	To enable or disable TimerA. 1: disable; 0: enable.

Table 6-4 Peripheral Control Register 1 (PRCtrl1, 0x2D01)

0x2D01, R/W, Peripheral Control Register 1, PRCtrl1				
Bit		R/W	Default	Description
Bit7	UART5	R/W	0	To enable or disable UART5. 1: disable; 0: enable.

Bit		R/W	Default	Description
Bit6	UART4	R/W	0	To enable or disable UART4. 1: disable; 0: enable.
Bit5	UART3	R/W	0	To enable or disable UART3. 1: disable; 0: enable.
Bit4	UART2	R/W	0	To enable or disable UART2. 1: disable; 0: enable.
Bit3	ExInt5	R/W	0	To enable or disable Interrupt 11. 1: disable; 0: enable.
Bit2	ExInt4	R/W	0	To enable or disable Interrupt 10. 1: disable; 0: enable.
Bit1	ExInt3	R/W	0	To enable or disable Interrupt 9. 1: disable; 0: enable.
Bit0	ExInt2	R/W	0	To enable or disable Interrupt 8. 1: disable; 0: enable.

Table 6-5 Register 1 to Adjust OSC Clock Frequency

0x2860, R/W, Crystal Control Register 1, CtrlCry1			
Bit		**Default**	**Description**
Bit[7:5]	Reserved	0	These bits must hold their default values for proper operation.
Bit4	CSEL	0	The fixed capacitance in the crystal oscillator circuit is 12.5 pF. Set this bit to **'1'** to decrease the capacitance by 2.35 pF.
Bit3	Reserved	0	These bits must hold their default values for proper operation.
Bit[2:0]	XTRSEL<2:0>	0	To adjust the resistance of the resistors in the internal crystal oscillator circuit. When RTC is used, these bits must be set to **"0b011"**, and the oscillation monitoring circuit must be enabled. Set bit **"XTRSEL<2>"** to **'1'** to increment the resistance to P end by 400 kΩ. **"XTRSEL<2:0>"** to adjust the resistance to N end: 00/01: Hold the resistance to N end. 10: Increment by 128 kΩ. 11: Increment by 64 kΩ.

Table 6-6 Register 2 to Adjust OSC Clock Frequency

0x2861, R/W, Crystal Control Register 2, CtrlCry2			
Bit		**Default**	**Description**
Bit7	REFLKEN	0	Set this bit to **'1'** to enable current leakage detection on BandGap circuit. When this bit is set to **'1',** an interrupt will be triggered when the reference voltage is lowered by more than 3% caused by the current leakage.
Bit6	Reserved	0	This bit must hold its default value for proper operation. By default this function is disabled.
bit5	XRESETEN	0	Set this bit to '1' to enable the oscillation monitor.
Bit4	CMPIT	0	To select the bias current input to the comparator CB 0: 20 nA; 1: 200 nA.
bit[3:2]	CMPSSELB<1:0>	0	To select the analog input to the comparator CB 00: M2 for positive input; REF_LP for negative input; 01: M1 for positive input; REF_LP for negative input; 10/11: M2 for positive input; M1 for negative input.
Bit[1:0]	Reserved	0	These bits must hold their default values for proper operation.

Table 6-7 PLL Clock State Register (PLLLCK, SFR 0xA3)

SFR 0xA3, R, PLL Clock State Register, PLLLCK			
Bit		**Default**	**Description**
bit[7:1]	Reserved	0	
bit0	PLLLCK	0	When this bit is read out as **'1'**, it indicates that the PLL has locked onto a certain frequency.

Table 6-8 Register 1 to Adjust Clock Frequency of Specific Functional Blocks

0x2867, R/W, Clock Control Register, CtrlCLK			
Bit		**Default**	**Description**
bit7	PLLPDN	0	To enable the PLL circuit 0: disable; 1: enable. Enable the BandGap circuit, and then enable the PLL circuit.

0x2867, R/W, Clock Control Register, CtrlCLK			
Bit		**Default**	**Description**
bit6	BGPPDN	0	To enable the BandGap circuit 0: disable; 1: enable. Enable the BandGap circuit, and then enable the PLL circuit.
bit[5:4]	ADCLKSEL<1:0>	0	To configure the sampling frequency of the oversampling ADCs (**"ADCCLK"**). Base: 204.8 kHz. 00: ×1; 01: ×2; 10: ×4.
bit[3:2]	MEACLKSEL<1:0>	0	To configure the clock frequency for the energy metering architecture (**"MTCLK"**). Base: 819.2 kHz. 00: ×1; 01: ×2; 10: ×4.
bit[1:0]	MCUCLKSEL<1:0>	0	To adjust the clock frequency for MCU (**"MCUCLK"**). Base: 819.2 kHz. 00: ×1; 01: ×2; 10: ×4; 11: ×8.

Table 6-9 Register 2 to Adjust Clock Frequency of Specific Functional Blocks

0x2868, R/W, PLL Control Register, CtrlPLL			
Bit		**Default**	**Description**
bit7	MCU26M	0	When the bit **"MCU13M"** is set to **'1'**, set this bit to **'1'** to double **"MCUCLK"** frequency further.
bit6	MCU13M	0	Set this bit to **'1'** to double **"MCUCLK"** frequency.

Table 6-10 OSC Clock State Register

0x286B, R, Analog Circuits State Register, ANState			
Bit		**Default**	**Description**
bit7	OSC	0	To indicate the state of the OSC clock 0: The crystal is working. 1: The crystal stops running, and all the circuits, including PLL circuit, sourced by the OSC clock now is being sourced by the internal RC clock.
Bit6	Reserved	-	
bit5	COMPB	0	To indicate the output of the comparator CB 1: the positive input is higher than the negative input; 0: the negative input is higher than the positive input.
bit[4:2]	Reserved	5	It is read out as **"0x5"**.
bit[1:0]	Reserved	-	

7.Power Management

V98XX has three system states according to the state of Clock 1:

- **OSC state:** When a reset event of Level 1 or Level 2 occurs, the system will go to the OSC state, in which Clock 1 runs and is sourced by the OSC clock.
- **Working state:** The PLL circuit is enabled, and the PLL clock is used as the source for Clock 1.
- **Sleeping state:** When the bit **"PWRUP"** (**"bit0"** of **"Systate"**, SFR 0xA1) is cleared, select the OSC clock as the source for Clock 1 and disable Clock 1, and then the system will enter the sleeping state. By default, the chip will be woken up with reset and be forced to go back to the OSC state. But when the bit **"IORSTN"** (**"bit0"** of **"IOWK"**, SFR 0xC9) is set to **'1',** the chip will be woken up without reset, which means the chip is woken up and goes back where it entered the sleeping state except that bits **"SLEEP1", "SLEEP0", "FWC",** and **"FSC"** (**"bits"** of **"SysCtrl"**, SFR 0x80) are cleared to 0s. The sleeping state is classified to 2 states: **"Sleep"** and **"Deep Sleep"**. An IO/RTC wakeup event, CF pulse output, or a power recovery event can wake up the system from **"Sleep"**. An IO wakeup event or a power recovery event can wake up the system from **"Deep Sleep"**.

7.1. Power Consumption

In V98XX, there are a lot of functional units, some of which can be disabled, but others cannot. The power consumption of these units may be affected by the digital power supply or the clock frequency as shown in Table 7-1.

Table 7-1 Factors Affecting Power Consumption of Each Unit

Unit	State When Powered On	Stoppable?	Factors Affecting Power Consumption.	
			Clock Frequency	Operation Voltage (DVCC Output)
LDO33	On	No	No	No
Digital Power Supply Circuit	On	No	No	No
OSC	On	No	No	No
MCU	On	Yes	Yes	Yes
REF_LP	On	No	No	No
RTC	On	No	No	No
PLL	Off	Yes	No	No
BandGap	Off	Yes	No	No

Unit	State When Powered On	Stoppable?	Factors Affecting Power Consumption.	
			Clock Frequency	Operation Voltage (DVCC Output)
Power Supervisor	On	No	No	No
Temperature Measurement Circuit	Off	Yes	No	No
Battery Voltage Measurement Circuit	Off	Yes	No	No
LCD Driver	COM/SEG driver circuit is disabled, and CLK3 is running.	Yes	No	No
ADCs	Off	Yes	Yes	No
Energy Metering Architecture	Digital signal inputs are disabled, and CLK2 is running.	Yes	Yes	No

7.1.1. OSC State

When a reset event of Level 1 or Level 2 occurs, the system will be reset to the OSC state. In this state, LDO33 is enabled, OSC clock is used as the source for **"CLK1"**, and MCU runs.

Table 7-2 OSC State of System

Module	State When Powered On	Stoppable?	State in OSC State
LDO33	On	No	On
Digital Power Supply Circuit	On	No	On
OSC	On	No	On
MCU	On	Yes	On

Module	State When Powered On	Stoppable?	State in OSC State
REF_LP	On	No	On
RTC	On	No	On

7.1.2. Working State

In the OSC state, enable the PLL circuit, select the PLL clock to work as the source for **"CLK1",** and then the system will enter the working state.

In the working state, users can configure the MCU clock (**"CLK1"**) frequency, and enable the required ADCs, the energy metering architecture, the LCD driver, and CPU and its peripherals according to the application.

In the working state, when the frequency of **"CLK1"** is set to 13.1072 MHz, that of **"CLK2"** is set to 3276.8 kHz, and sampling frequency of ADCs ("ADCCLK") is set to 819.2 kHz, the system will run at full speed. When the system works normally, the power consumption of the global system will be determined by the number of enabled ADCs, and the configuration of the metering architecture and the LCD driver.

Table 7-3 Power Consumption When System Working at Full Speed

Module	State When Powered on	Stoppable?	Current State
LDO33	On	No	On
Digital Power Supply Circuit	On	No	On
OSC	On	No	On
REF_LP	On	No	On
RTC	On	No	On
PLL	Off	Yes	On
BandGap	Off	Yes	On
Power Supervisor	On	No	On
Temperature Measurement Circuit	Off	Yes	Off
Battery Voltage Measurement Circuit	Off	Yes	Off
ADC	Off	Yes	4 ADCs are enabled.

Module	State When Powered on	Stoppable?	Current State
Energy Metering Architecture	Digital signal inputs are disabled, and CLK2 is running.	Yes	4 channels are enabled.
LCD Driver	COM/SEG driver circuit is disabled, and CLK3 is running.	Yes	On, no display screen
MCU	On	Yes	On
Power Consumption	5.5 mA		

7.1.3. Sleeping State

When the bit **"PWRUP"** (**"bit0"** of **"Systate"**, SFR 0xA1) is read out as **'0'**, switch the source for **"CLK1"** to the OSC clock and then disable **"CLK1"**, then the system will go to the sleeping state.

There are two types of sleeping state: **"Sleep"** and **"Deep Sleep"**.

In **"Sleep"** or **"Deep Sleep"**, RTC holds on; the memories, CPU and its peripherals stop working; but the LCD driver and the energy metering architecture will not stop working until they are disabled. If ADCs, PLL circuit, LCD driver, and energy metering architecture are disabled, and IOs are set to **"output, disabled; input, masked"** before entering **"Sleep"** or **"Deep Sleep"**, the system consumes the lowest power.

In **"Sleep"**, if IO/RTC wakeup event, CF pulse output, or power recovery event occurs, the system will be woken up and go back to the OSC state by default. In **"Deep Sleep"**, only an IO wakeup event or power recovery event can wake up the system and reset it to the OSC state by default. When the bit **"IORSTN"** (**"bit0"** of **"IOWK"**, SFR 0xC9) is set to **'1'**, any wakeup event can wake up the system from **"Sleep"** or **"Deep Sleep"** only but cannot reset the system to the OSC state. In this condition, the chip will go back where it entered the sleeping state, except that **"bit[6:5]"** (**"FWC"** and **"FSC"**) and **"bit[2:1]"** (**"SLEEP1"** and **"SLEEP0"**) will be cleared to 0s.

If the pin **"WAKEUP1", "WAKEUP2", "WAKEUP3",** or **"WAKEUP4"** is set to **"Input enabled"** before the system enters **"Sleep"** or **"Deep Sleep"**, a transition (Either high-to-low or low-to-high, with more than 4 OSC clock cycles on both levels) on the pin in **"Sleep"** or **"Deep Sleep"** can wake up the system. By default ports **"P0.2"** and **"P0.3"** are not used for the wakeup event input. Users must configure bit **"IOP0"** ("**bit1**" of **"IOWK"**, SFR 0xC9) to **'1'** to set both pins for the wakeup input. When the bit **"IO"** (**"bit3"** of **"Systate",** SFR 0xA1) is set to **'1'**, read states of bits **"P14WK"** (**"bit0"** of "**IOWKDET"**, SFR 0xAF), **"P02WK"** (**"bit1"** of **"IOWKDET"**, SFR 0xAF) and **"P03WK"** (**"bit2**" of **"IOWKDET"**, SFR 0xAF) to detect which IO wakeup event woke up the chip from the sleeping state.

If both bit **"RTC"** (**"bit2"** of **"Systate"**, SFR A1) and **"CFWK**" (**"bit3"** of **"IOWKDET"**, SFR 0xAF) are set to 1s, it indicates that the system was woken up by the CF pulse output. If the bit **"RTC"** is set to **'1',** but **"CFWK"** is cleared, it indicates that an RTC wakeup event occurred.

7.1.3.1. Sleep/Wake-Up

In V98XX, there are two methods to wake up the system from the sleeping state or make the system go to the sleeping state: Normal method and quick method.

1. Normal Method

The normal method for wakeup/sleep switchover is totally controlled by the program.

When the PLL clock is enabled and works as the source for the MCU clock (**"CLK1"**), users can follow steps illustrated in Figure 7-1 to force both MCU and energy metering architecture to go to the sleeping state, or force MCU to go to the sleeping state only but leave the energy metering architecture to accumulate a constant for the energy metering.

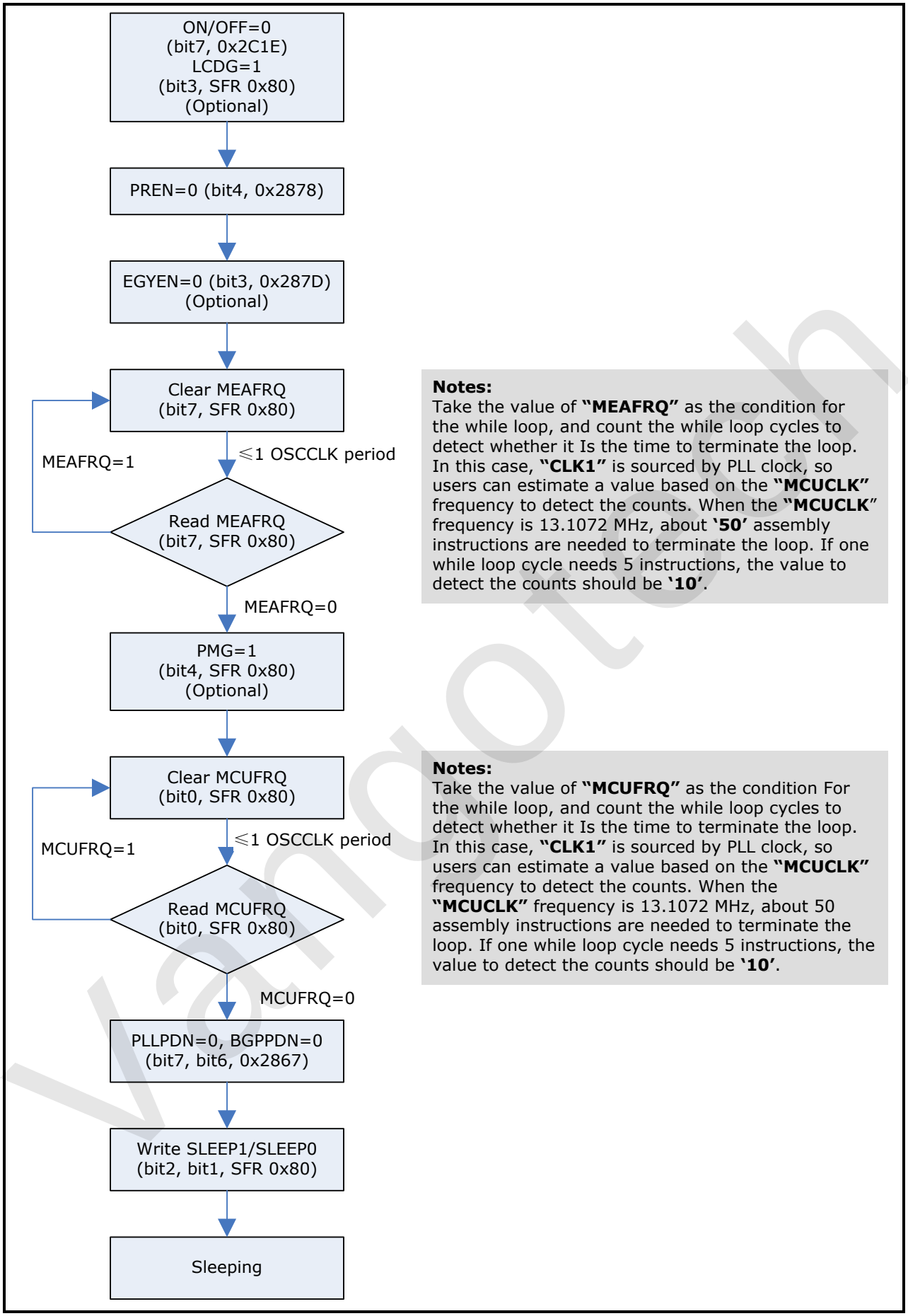


Figure 7-1 Go to Sleeping State (Normal Method, Disable PLL Clock)

When the PLL clock is enabled and works as the source for the MCU clock (**"CLK1"**), users can follow

steps illustrated in Figure 7-2 to force MCU to go to the sleeping state only but leave the energy metering architecture work normally.

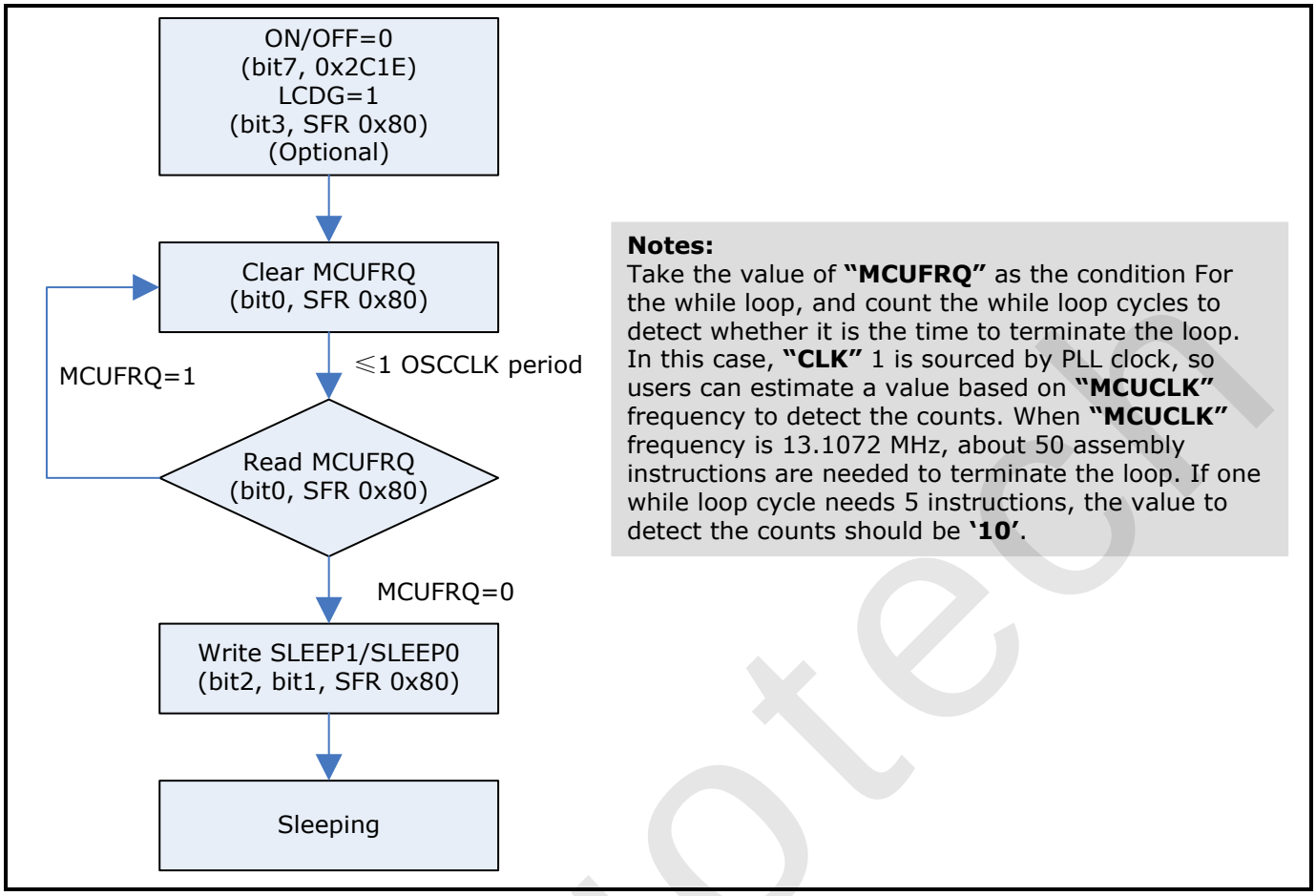


Figure 7-2 Go to Sleeping State (Normal Method, PLL Clock Holds on)

Table 7-4 Configuration for Sleeping State

Register	SLEEP1 (Bit 2)	SLEEP0 (Bit1)	System State
SysCtrl SFR 0x80	0	1	Sleep
	1	1	Sleep
	1	0	Deep Sleep

In **"Sleep"** or **"Deep Sleep"**, when IO/RTC wakeup event, CF pulse output, or power recovery event occurs, the system will be woken up from the sleeping state. If the wakeup with reset mode is applied, after a reset, users should use the normal operation to enable the PLL circuit and select it as the source for **"CLK1"** to make the system go to the working state.

2. Quick Method

In V98XX, the quick method can force the system to go to **"Sleep"**, but not **"Deep Sleep"**.

When the PLL clock is enabled and works as the source for the MCU clock (**"CLK1"**), users can follow steps illustrated in Figure 7-3 to force both MCU and energy metering architecture to go to **"Sleep"**, or force MCU to go to **"Sleep"** only but leave the energy metering architecture to accumulate a constant for energy metering. In this case, PLL clock will be disabled definitely.

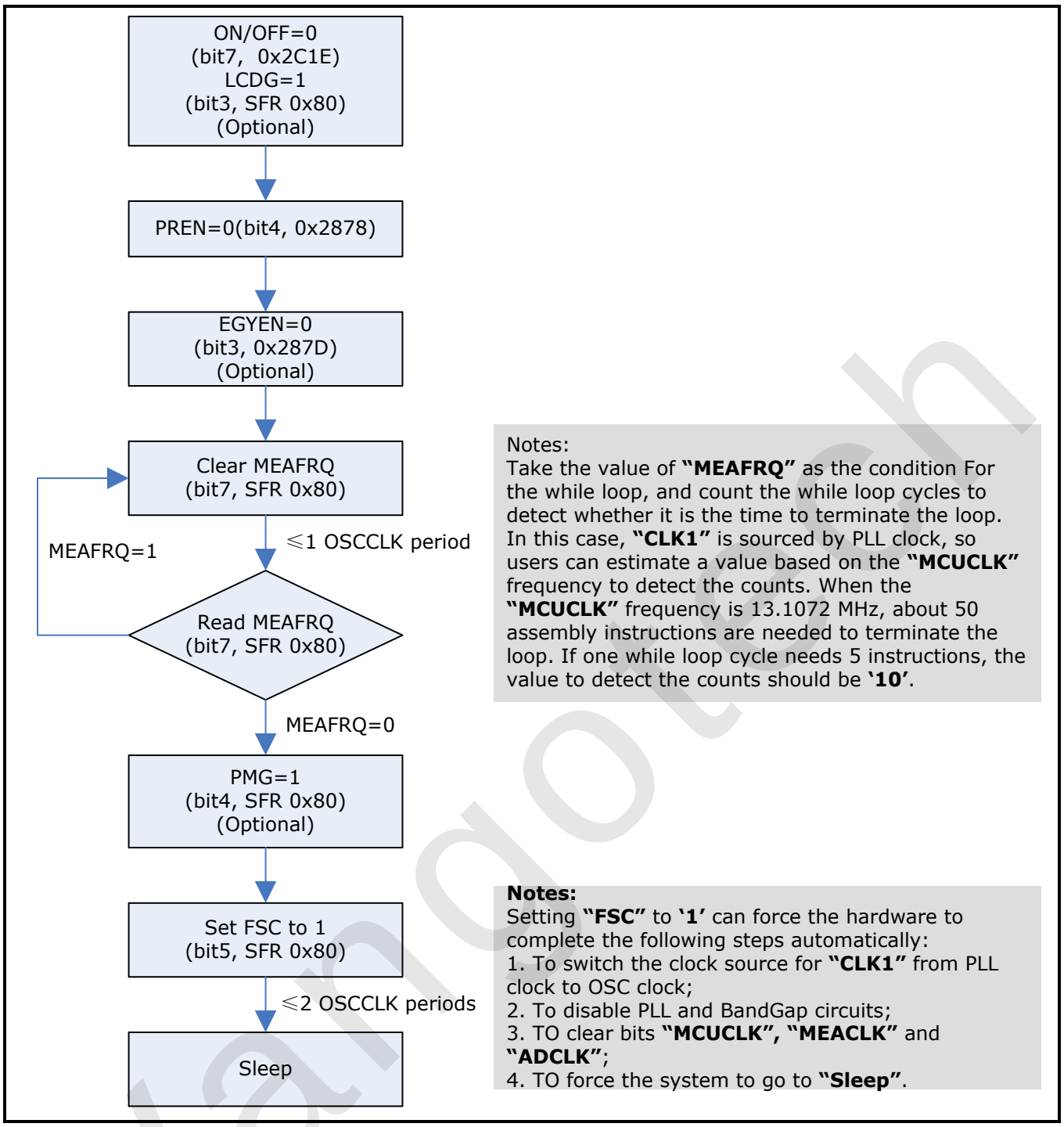


Figure 7-3 Go to Sleep (Quick Method)

In "Sleep", IO/RTC wakeup event, CF pulse output, or power recovery event can wake up the system. If the wakeup with reset mode is applied, users should use the quick operation to enable the PLL circuit and switch the source for "CLK1" to make the system go to the working state.

7.1.3.2. Power Consumption in Sleeping State

The following table shows the power consumption in the sleeping state when the LCD driver is disabled.

Table 7-5 Power Consumption in Sleeping State

Module	State When Powered On	Stoppable?
Digital Power Supply Circuit	On	No
OSC	On	No
REF_LP	On	No
RTC	On	No
Power Supervisor	On	No
RC Oscillator	On	No
Total	12 μA (Max. 16.2 μA; Min. 7.8 μA)	

7.2. Registers

Table 7-6 Register for Clock Control

SFR 0x80, R/W, Clock Switchover Control Register, SysCtrl		
Bit	**Default**	**Description**
bit7 MEAFRQ	0	To select the clock source for **"CLK2"** 0: OSC clock; 1: PLL clock. This bit is writable and readable. Configure this bit to switch the clock source for **"CLK2"**, and read this bit to acquire the current clock source for **"CLK2"**.
bit6 FWC	0	Only when the bit **"FSC"** is cleared, the configuration of **"FWC"** is activated. When the bit **"FSC"** is cleared, write **'1'** to the bit **"FWC"** to enable the PLL circuit to start running and output a 3.2768-MHz PLL clock, and to source **"CLK1"**. When the bit **"FSC"** is cleared, write **'1'** to the bit **"FWC",** the clock setting will be locked. Writing **'0'** to the bit "**FWC"** will unlock the clock setting without switching the clock.
bit5 FSC	0	Write **'1'** to this bit to select the OSC clock as the clock source for **"CLK1"**, to disable the PLL clock, and to disable **"CLK1"**. If the bit **"PWRUP"** is read out as '**0',** setting this bit to **'1'** will make the system enter the **"Sleep"** state, but not **"Deep Sleep"**. If the bit **"PWRUP"** is read out as **'1'**, setting this bit to **'1'** cannot force the system to enter the **"Sleep"** state.

SFR 0x80, R/W, Clock Switchover Control Register, SysCtrl		
Bit	**Default**	**Description**
bit4 PMG	0	Set this bit to **'1'** to stop **"CLK2"**. By default this clock is running.
bit3 LCDG	0	Set this bit to **'1'** to stop **"CLK3**". By default this clock is running. Only when the PLL clock is selected as the clock source for **"CLK1"** and **"CLK2"**, **"CLK3"** can be stopped.
bit2 SLEEP1 bit1 SLEEP0	0	When the bit **"PWRUP"** is read out as **'0',** write **'0'** to the bit **"MCUFRQ"**, and then: – Set **"SLEEP1"** and **"SLEEP0"** to **"0b11"** or **"0b01"** to stop **"CLK1"** (Together with **"CLK4"**) and force the system entering the **"Sleep"** state. – Set **"SLEEP1"** and **"SLEEP0"** to **"0b10"** to stop **"CLK1"** (Together with **"CLK4"**) and force the system entering the **"Deep Sleep"** state.
bit0 MCUFRQ	0	To select the clock source for **"CLK1"** 0: OSC clock; 1: PLL clock. This bit is writable and readable. Configure this bit to switch the clock source for **"CLK1"**, and read this bit to acquire the current clock source for **"CLK1"**.
When the bit **"IORSTN"** (**"bit0"** of **"IOWK"**, SFR 0xC9) is set to **'1'**, any wakeup event can wake up the system from the sleeping state without resetting the system. After wakeup, CPU keeps on executing programs; all circuits hold their states where they were before sleeping; only **"bit[2:1]"** (**"SLEEP1"** and **"SLEEP0"**) and **"bit[6:5]"** (**"FWC"** and **"FSC"**) are cleared.		

Table 7-7 Register to Indicate Power Supply State

SFR 0xA1, R, System State Register, Systate		
Bit	**Default**	**Description**
Bit[7:6]		Reserved.
Bit5 POR	0	When this bit is read out as **'1'**, it indicates the system is reset by an event of Level 1: POR/BOR, RSTn pin reset, or WDT overflow event. This bit will be cleared when a reset event of other levels occurs.
Bit4	0	Reserved.
Bit3 IO	0	When this bit is read out as **'1'**, it indicates the system is woken up from **"Sleep"** or "**Deep Sleep"** by an IO wakeup event.

SFR 0xA1, R, System State Register, Systate		
Bit	**Default**	**Description**
Bit2 RTC/CF	0	When this bit is read out as **'1',** but bit **"CFWK**" (**"bit3"** of **"IOWKDET"**, SFR 0xAF) is cleared, it indicates the system is woken up from **"Sleep"** by the RTC wakeup event. If both this bit and bit **"CFWK"** are set to 1s, it indicates the system is woken up from **"Sleep"** by the CF pulse wakeup event.
Bit1 PWRDN	0	When the input voltage on pin **"VDCIN"** is lower than 1.0 V, this bit is read out as '**1'**, indicating that the system is powered down. If the power down interrupt is enabled, an interrupt will be triggered when this bit is read out as '**1'**. When the input voltage on pin **"VDCIN"** is higher than 1.1 V, this bit holds its default value, indicating no power down event occurs.
Bit0 PWRUP	0	When the input voltage on pin **"VDCIN"** is higher than 1.1 V, this bit is read out as **'1',** indicating that the system is powered up by the line power supply. When the input voltage on pin **"VDCIN"** is lower than 1.0 V, this bit holds its default value, indicating the system is powered up by battery.

8.Power Supply

V98XX supports 5-V or 3.3-V power input on the pin **"VDD5"**. The power supply is supervised continuously. The internal analog circuits and general-purpose I/O (GPIO) ports are powered by the 3.3V regulator circuit (3.3V-LDO), and the peripheral circuits are powered by the LDO33 output voltage; the Vango metering architecture and PLL circuit are powered by the digital power supply circuit.

There is an internal power detection circuit in V98XX. By default this circuit is enabled. When the chip is 3.3 V powered, users must set bit **"PDDET"** (**"bit7"** of **"CtrlLDO",** 0x2866) to **'1'** to disable this circuit to protect the battery from the current leakage when a battery is connected. When the chip is 5 V powered, this bit must hold its default value.

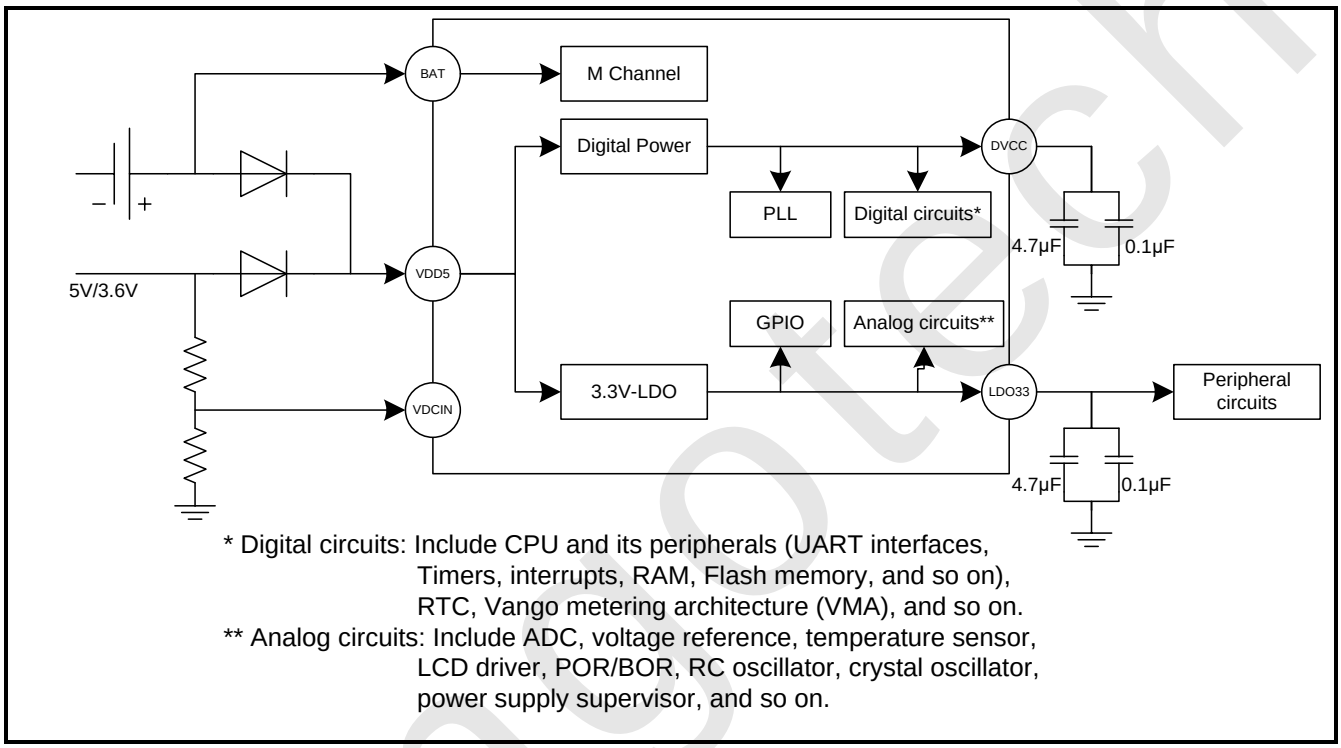


Figure 8-1 Power Supply Architecture

Note:

V98XX has an internal power supply detection circuit. The circuit is turned on by default. When the system is powered by a 3.3-V power source, users must set **"PDDET**" (**"bit7", "CtrlLDO",** 0x2866) to **'1'** to disable the power detection circuit, or when a battery is connected, the battery leakage may occur. The bit must be cleared when it is powered by 5-V power supply. By this way the battery leakage risk will not exist.

8.1. 3.3-V Regulator Circuit (LDO33)

In V98XX, the analog circuits and the GPIO ports are powered by the 3.3-V regulator circuit (**"LDO33"**), and the peripheral circuits are powered by the LDO33 output voltage. This LDO33 will not stop working until the chip is powered off. The LDO33 output voltage can be configurable via bits **"LDO3SEL"** (**"bit[5:3]"** of **"CtrlLDO"**, 0x2866).

This LDO33 has a driving capability of 30 mA. When the load current through the analog circuits and the

GPIO ports is less than 30 mA, the LDO33 output voltage holds 3.3 V; when the load current is higher than 30 mA, the higher the load current is, the lower voltage the LDO33 will output.

It is recommended to decouple the pin **"LDO33"** externally with a ≥ 4.7 μF capacitor in parallel with a 0.1-μF capacitor.

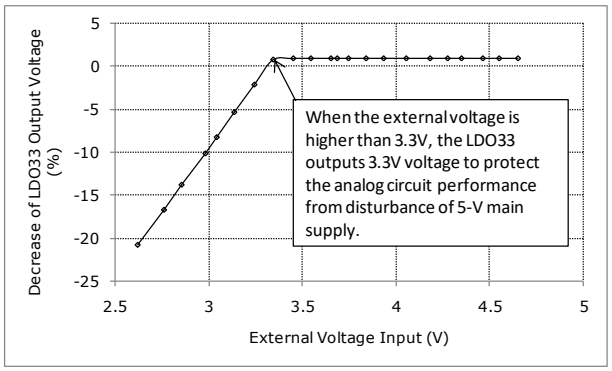


Figure 8-2 LDO33 Output and 5V Power Input

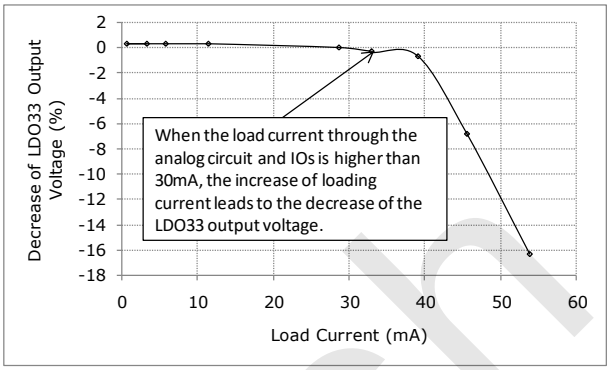


Figure 8-3 LDO33 output and the Load Current

8.2. Digital Power Supply

In V98XX, the PLL clock generation circuit and the Vango metering architecture (VMA) are powered by the digital power supply circuit. When the digital power supply output is 200 mA, being lower than the power input on the pin **"VDD5"**, it will output a stable voltage, avoiding the digital power fluctuation caused by the variation of the power input. The digital power supply output is configurable via the bit **"LDOV2SEL"** (**"bit[2:0]"** of **"CtrlLDO"**, 0x2866).

The digital power supply circuit has a driving capability of 35 mA. When the load current through the circuits is less than 35 mA, the digital power supply will be stable; when the load current is higher than 35 mA, the higher the load current is, the lower the digital power supply will be.

This power supply circuit will not stop working until the system is powered off.

It is recommended to decouple the pin **"DVCC"** externally with a ≥4.7 μF capacitor in parallel with a 0.1-μF capacitor.

8.3. Power Supply Supervisor

In V98XX, the 5-V main power is input into the pin **"VDCIN"** after a resistive divider. The input voltage on the pin **"VDCIN"** is monitored continuously by the power supply supervisor.

When the input voltage on the pin **"VDCIN"** is lower than 1 V, a power-down event will occur, the bit **"PWRDN"** (**"bit1"** of **"Systate"**, SFR 0xA1) will be set to **'1',** and a power-down interrupt will be generated to CPU.

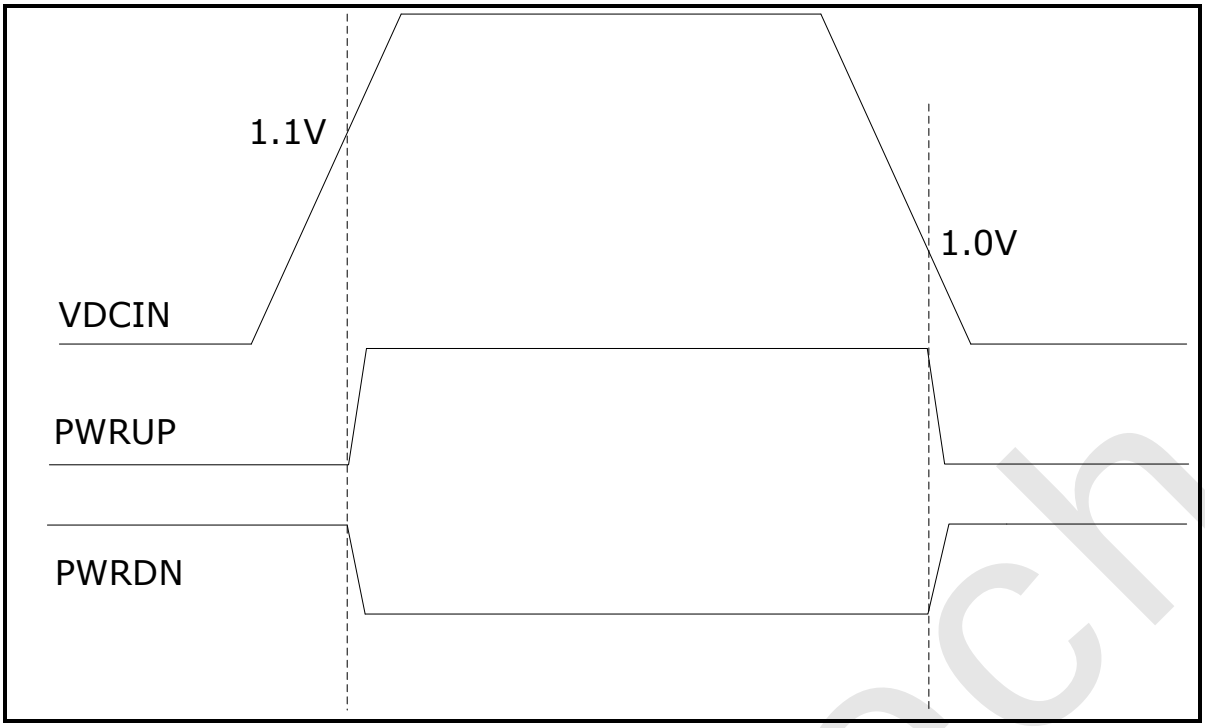


Figure 8-4 Relationship between VDCIN Input Signal and States of Flag Bits PWRUP and PWRDN

8.4. Battery Supply

V98XX can be powered by batteries. Users can read the value of the flag bit **"PWRUP"** (**"bit0"** of **"Systate"**, SFR 0xA1) to get the state of the power supply. When this bit is read out as **'0'**, it indicates the input voltage on the pin **"VDCIN"** is lower than 1.0 V, which means the system is powered by the battery, or the power supply has been switched from 5-V power to the battery.

When the chip is powered by batteries, please note that the battery will get passive when it is reactive for a long time. So users should set the bit **"BATDISC**" (**"bit0"** of **"CtrlBAT"**, 0x285C) to **'1'** at an interval to discharge the battery to protect them from passivation. During the battery discharge, the load current is 3 mA, and the period for battery discharge should not be too long to save power. After discharge, the bit **"BATDISC"** must be cleared.

9.Comparator

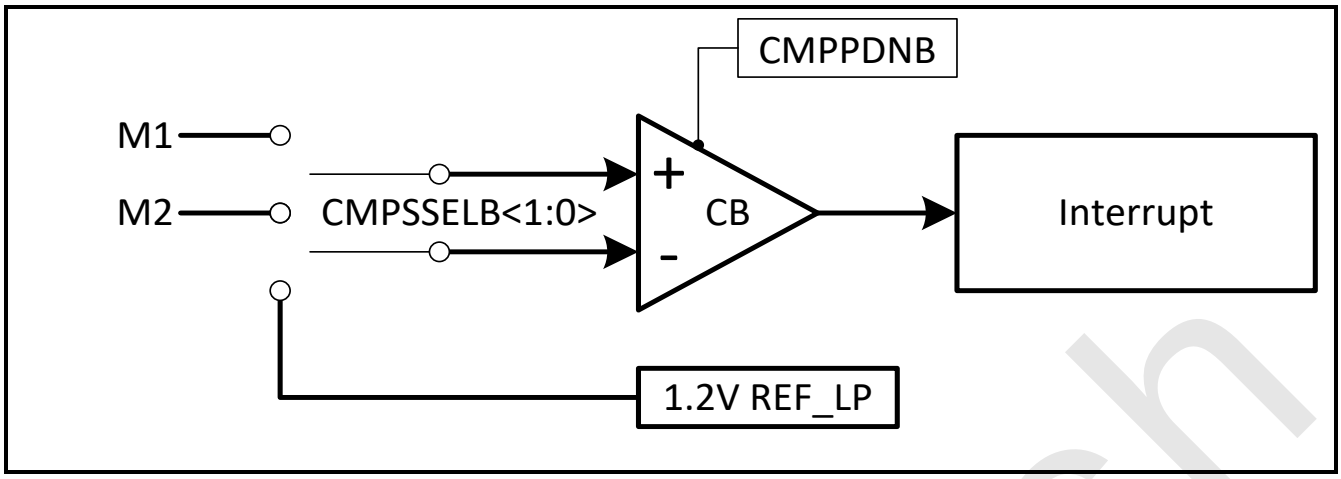


Figure 9-1 Comparator Architecture

V98XX integrates one additional comparator CB to compare the analog signals:

- Positive signal input on pin **"M1"** and negative signal input on pin **"M2"**;
- Positive signal input on pin **"M1"** and negative signal from internal low power reference circuit (REF_LP);
- Positive signal input on pin **"M2"** and negative signal from internal low power reference circuit (REF_LP).

When the RSTn pin reset, POR/BOR, or WDT overflow reset occurs, or the system is in **"Sleep"** or **"Deep Sleep"** state, this comparator will stop running.

When IE6=1 (**"bit6"** of **"0x28A5"**), EIE.3=1 (**"bit3"** of **"SFR 0xE8"**), and IE.7=1 (**"bit7"** of **"SFR 0xA8"**), the comparator interrupt will be enabled. In this state, the interrupt flag **"IR6**" (**"bit6"** of "**0x28A2"**) will be set to **'1'** when the output of the comparator changes, and the comparator will generate an interrupt to CPU. After the interrupt service, users can read bit **"COMPB"** (**"bit5"** of **"0x286B**") to detect the comparison result of the input signals.

Table 9-1 Registers Related to Comparator CB

Register	Bit		Default	Description
0x2861 CtrlCry2	Bit4	CMPIT	0	To select the bias current input to the comparator CB 0: 20 nA; 1: 200 nA.
	bit[3:2]	CMPSSELB<1:0>	0	To select the analog input to the comparator CB 00: M2 for positive input; REF_LP for negative input; 01: M1 for positive input; REF_LP for negative input; 10/11: M2 for positive input; M1 for negative input.

Register	Bit		Default	Description
0x2864 CtrlADC6	bit5	CMPPDNB	0	To enable the comparator CB. 0: Disable; 1: Enable.
0x286B ANState	bit5	COMPB	0	To indicate the output of the comparator CB 1: the positive input is higher than the negative input; 0: the negative input is higher than the positive input.

10. Energy Metering

The energy metering architecture in V98XX has features:

- Four independent oversampling Σ/Δ ADCs: One voltage channel (U), two current channels (I), and one multifunctional channel for various signal measurements.
- High metering accuracy:
  - Less than 0.1% error on active energy metering over dynamic range of 5000:1.
  - Less than 0.1% error on reactive energy metering over dynamic range of 3000:1.
  - Less than 0.5% error on current and voltage RMS calculation over dynamic range of 1000:1.
- Providing measurements:
  - Raw waveform and DC component of current/voltage signals
  - Instantaneous/Average and active/reactive power
  - Positive/Negative and active/reactive energy
  - Average apparent power
  - Instantaneous/average current/voltage RMS
  - Line frequency
  - Temperature with measurement accuracy of ±1°C
  - Battery voltage, system voltage, and external voltage signals
- Two current inputs for active energy, or one current input for active and reactive energy
- Programmable energy metering modes:
  - Accumulating power, current RMS, or a constant for energy metering
  - Accumulating energy at a configurable frequency
- Current detection, to lower power consumption
- CF pulse output and interrupt with configurable pulse width
- Zero-crossing interrupt
- Programmable threshold for no-load detection
- Calibrating meters via software:
  - Phase compensation supported, resolution 0.005°/lsb (min.), over a range of ±1.4° (min.)
  - Gain calibration of RMS and power, and offset calibration of power
  - Accelerating meter calibration when low current is applied.

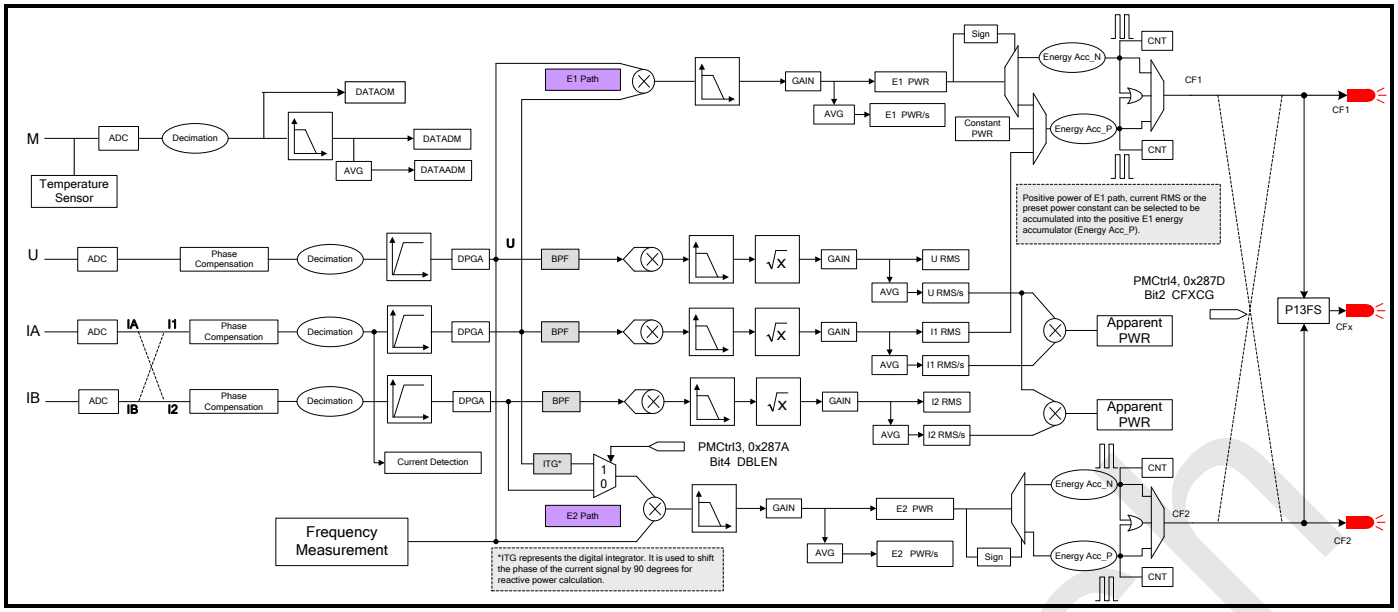


Figure 10-1 Digital Signal Processing in Vango Metering Architecture

10.1. Accessing to Registers for Vango Metering Architecture

In V98XX, MCU must write or read of the metering control, data and calibration registers through the buffer registers.

1. Buffer registers for write and read operation.

When a POR/BOR, RSTn pin reset, or WDT overflow reset event occurs, all buffer registers for the write and read operation on the registers for energy metering architecture will be reset to their default states.

Table 10-1 Buffer Registers and Data to Be Written or Read

Data	ACK	INVD	DATA[31:24]	DATA[23:16]	DATA[15:8]	DATA[7:0]
Buffer Register	BUFF5	BUFF4	BUFF3	BUFF2	BUFF1	BUFF0
Address	0x2885	0x2884	0x2883	0x2882	0x2881	0x2880

2. Read operation

MCU must read the registers for energy metering architecture following steps as illustrated:

a. Write **"0xCC"**, and then **"0s"** to the register **"INVD"** located at address **"0x2884"**;

b. Read the address of the target register;

c. When the flag bit **"ACK"** is read out as **'0'**, or in no more than 24 MTCLK clock periods, the content (DATA) of the target register will be loaded into the buffer registers in sequence as illustrated in the preceded table;

d. Read the buffer registers to acquire the content (DATA).

3. Write operation

MCU must write of the registers for energy metering architecture following steps as illustrated:

a. Write **"0xCC"**, and then **"0s"** to the register **"INVD"** located at address **"0x2884"**;

b. Write the data (DATA) to the buffer registers in sequence as illustrated in the preceded table;

c. Write of the address of the target register;

d. When the flag bit **"ACK"** is read out as **'0'**, or in no more than 24 MTCLK clock periods, the content (DATA) in the buffer registers will be loaded into the target registers.

10.2. Metering Clock

"CLK2" provides clock pulse for the energy metering architecture, including ADCs. It is sourced by OSC clock or PLL clock. When **"CLK2"** is disabled, the metering architecture stops running.

There is a specific bit (**"GT"**, **"bit7"** of **"IDET"**, 0x2886) to gate control the clock for the sampling circuits and RMS/power calculation circuits. When this bit is set to '1', the circuits stop working, but the energy accumulation unit keeps on running.

In working state, the PLL clock is enabled, and it is selected as the source for **"CLK2"**. In this condition, the metering clock frequency (f_{MTCLK}) and sampling frequency of ADCs (f_{ADC}) are configurable, and f_{MTCLK} must be 4 times of f_{ADC}.

Table 10-2 Configuration of CLK2

Register	Bit	Description
SysCtrl SFR 0x80	bit7 MEAFRQ	To select the clock source for CLK2. 0: OSC clock; 1: PLL clock. This bit is writable and readable. Configure this bit to switch the clock source for CLK2, and read this bit to acquire the current clock source for CLK2.
	bit4 PMG	Set this bit to 1 to stop CLK2. By default this clock is running.
CtrlCLK 0x2867	Bit[5:4] ADCLKSEL<1:0>	To configure the sampling frequency of the oversampling ADCs (ADCCLK). Base: 204.8kHz. 00: ×1; 01: ×2; 10: ×4.
	bit[3:2] MEACLKSEL<1:0>	To configure the clock frequency for the energy metering architecture (MTCLK). Base: 819.2kHz. 00: ×1; 01: ×2; 10: ×4.

10.3. Reference Voltage

In the V98XX, the BandGap circuit outputs a reference voltage (about 1.185V with a typical temperature drift of 10ppm/°C) and bias current for ADCs and PLL circuit. So users must enable the BandGap circuit

before enabling ADCs or PLL circuit.

Users can improve the BandGap performance via adjusting the temperature coefficient as follows:

1. Set bit BGPPDN (bit6 of CtrlCLK, 0x2867) to 1 to enable the BandGap circuit;
2. Ensure that the bit BGPCHOPN (bit0 of CtrlBGP, 0x2862) is cleared, which enables the chopper to remove the DC component of the BandGap circuit. When the chopper is enabled, the output voltage of the BandGap circuit varies over the range -50~+50mV, and the temperature coefficient is improved.
3. Configure bits REST<2:0> and RESTL<1:0> (bit[5:1] of CtrlBGP, 0x2862) to adjust the temperature coefficient to eliminate the temperature coefficient introduced by external components. A temperature coefficient drift of x in the BandGap circuit results in a drift of -2x in the meter measurement error.
4.

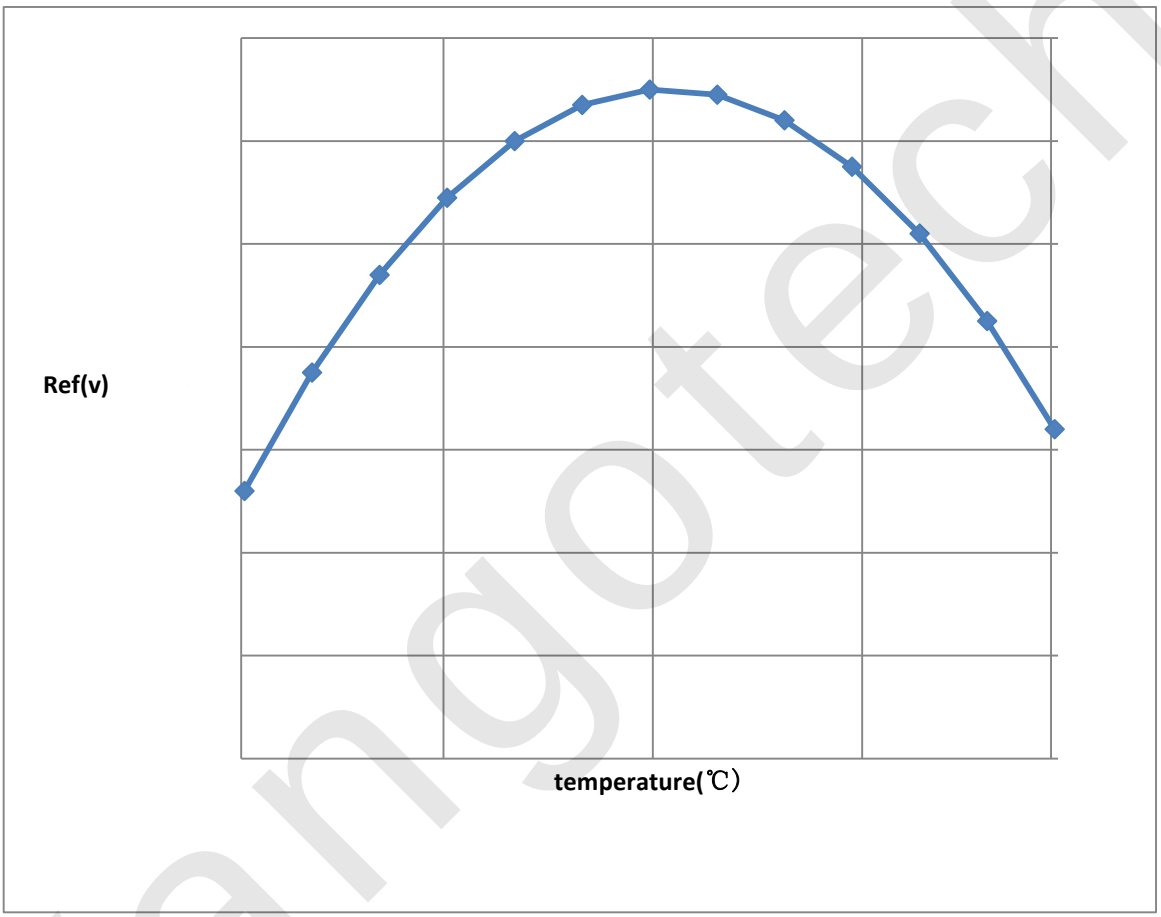


Figure 10-2 The temperature characteristic curve of reference voltage

In the V98XX, a circuit is designed to supervise the current leakage of the external decoupled capacitors connected to the pin REF. When bit REFLKEN (bit7 of CtrlCry2, 0x2861) is set to 1, an interrupt, REF leakage interrupt, will be triggered when the reference voltage is lowered by 3% caused by current leakage, and flag bit IR4 (bit4 of ExInt4IFG, 0x2850) is set to 1. When IE4=1 (bit4 of ExInt4IE, 0x2853), EIE.2=1 (bit2 of SFR 0xE8) and IE.7=1 (bit7 of SFR 0xA8), this circuit will generate an interrupt to CPU when flag bit IR4 is set to 1.

10.4. Analog Inputs

The V98XX has three pairs of analog inputs forming two current channels and one voltage channel. The current channels consist of two fully differential voltage inputs. And the voltage channel consists of a pseudo differential voltage input: UP is positive input for the voltage channel, and UN, grounded, is

negative input for the voltage channel. Each input has a maximum voltage of ±200mV, and each pair has a maximum differential voltage of ±400mV.

In a current channel, a current transformer (CT) or a shunt resistor can be used for analog inputs.

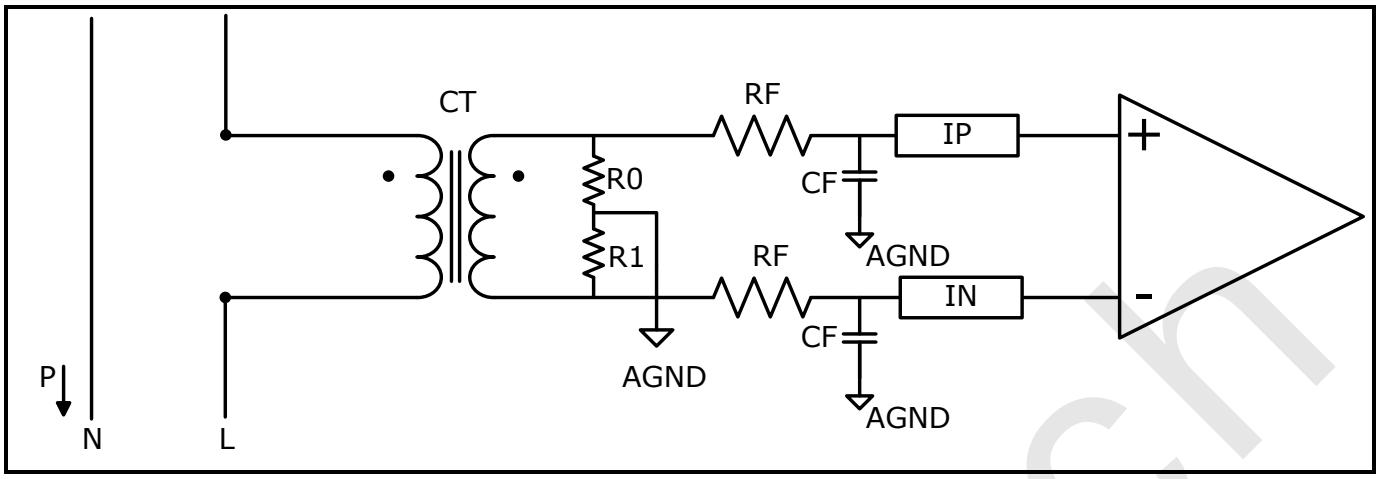


Figure 10-3 CT for Current Analog Input

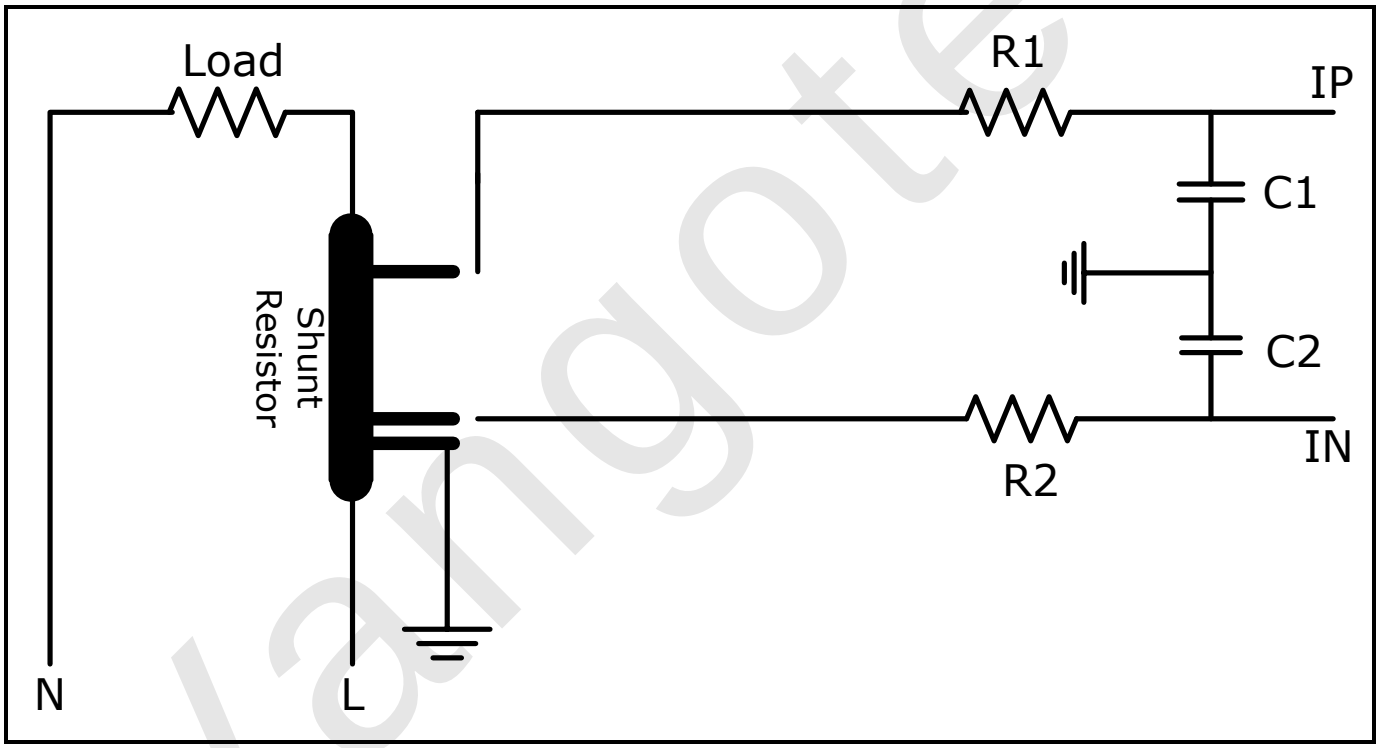


Figure 10-4 Shunt Resistor Network for Current Analog Input

In the voltage channel, a potential transformer (PT) or a resistor-divider network can be used for analog inputs.

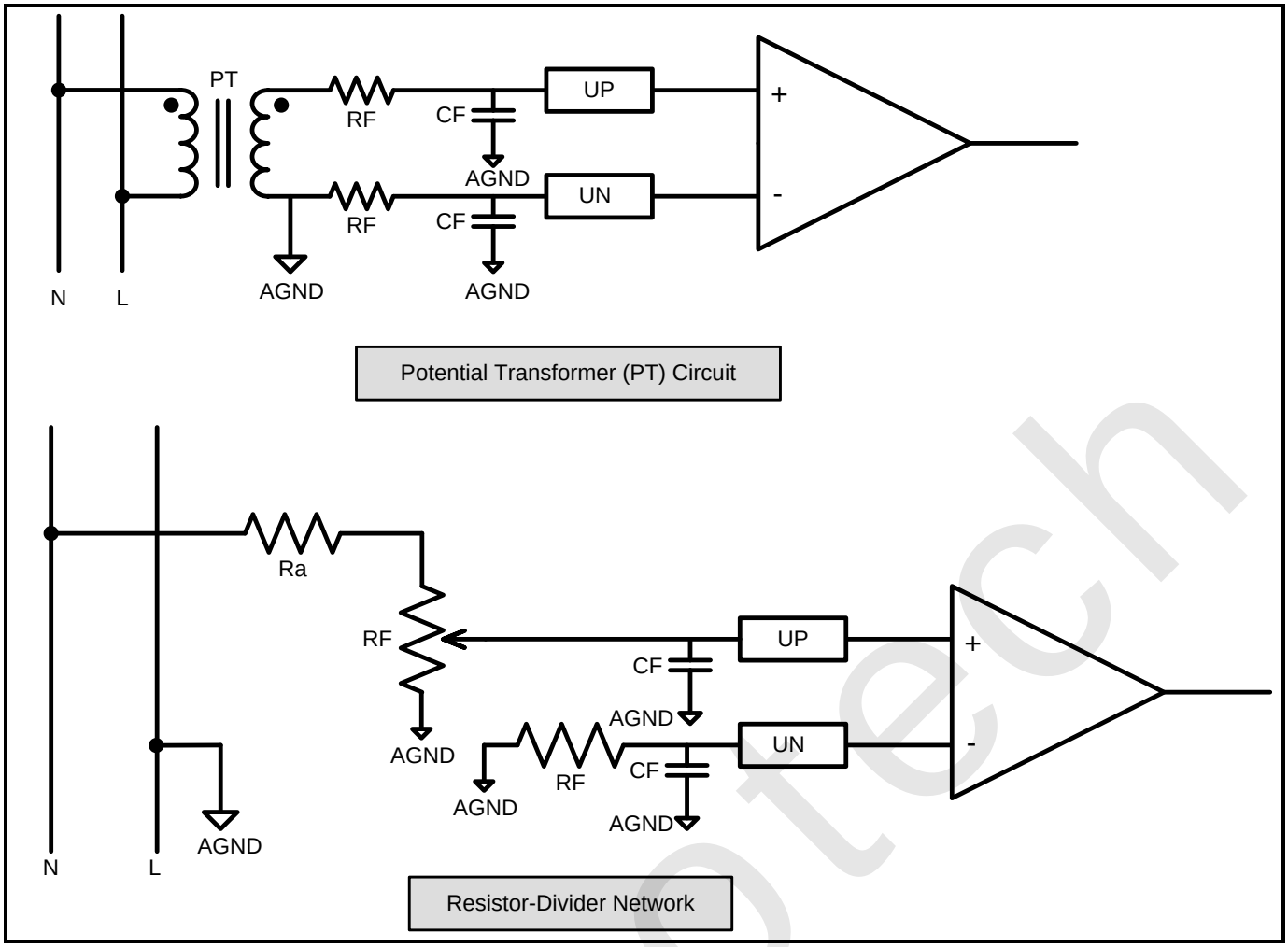


Figure 10-5 Analog Input of Voltage

The full measurement scale of ADCs is ±1.1 V. To match the output signal of the sensors with the measurement scale of ADCs, groups of Analog Programmable Gain Amplifiers (APGA) are set. The product of the analog input and the set APGA should not be over ±1.1 V.

Table 10-3 Analog PGA Gain Configuration for Current and Voltage Analog Input

Register	Bit	Default	Description
CtrlADC0 0x2858	Bit7 Reserved	0	These bits must hold their default values for proper operation.
	bit6 ADCGU	0	To set analog PGA gain for voltage input to Voltage Channel (U) ADC. It is mandatory to set this bit to its default value for proper operation. 0: ×1; 1: ×2.

Register	Bit	Default	Description
	bit[5:3] ADCGB<2:0>	0	To set analog PGA gain for current input to Current Channel B (IB) ADC 000: ×1; 001: ×4; 010: ×8; 011: ×16; 100/101/110/111: ×32. To match the output signal from the sensor to the measurement scale of the ADC, the default value should not be used.
	bit[2:0] ADCGA<2:0>	0	To set analog PGA gain for current input to Current Channel A (IA) ADC 000: ×1; 001: ×4; 010: ×8; 011: ×16; 100/101/110/111: ×32. To match the output signal from the sensor to the measurement scale of the ADC, the default value should not be used.

10.5. Analog-to-Digital Conversion

Second-order Σ-ΔADCs are designed in three channels of V98XX for analog-to-digital conversion, and their full measurement scale is ±1.1 V. By default, Σ-ΔADCs are disabled. Users can enable them via configuring **"CtrlADC6"** register (0x2864).

Note: It is mandatory to clear bit **"DCENN"** (**"bit7"** of **"CtrlLCDV"**, 0x285E) to add 10-mV direct voltage offset to the current input to current channel ADCs.

Table 10-4 Enable/Disable ADCs

Register	Bit		Default	Description
CtrlADC6 0x2864	bit2	ADCUPDN	0	To enable Channel U ADC 0: Disable. 1: Enable.
	bit1	ADCBPDN	0	To enable Channel IB ADC 0: Disable; 1: Enable.
	bit0	ADCAPDN	0	To enable Channel IA ADC 0: Disable; 1: Enable.

After analog-to-digital conversion, the analog signals are converted to be 1-bit code streams of 22-bit length with both **"bit21"** and **"bit20"** being the sign bits.

10.6. Switch of Current Channels

After analog-to-digital conversion, current IA or IB is sent to Current I1 or Channel I2, via configuring the bit **"SELI"** (**"bit5"** of **"PMCtrl1"**, 0x0100), for different signal processing.

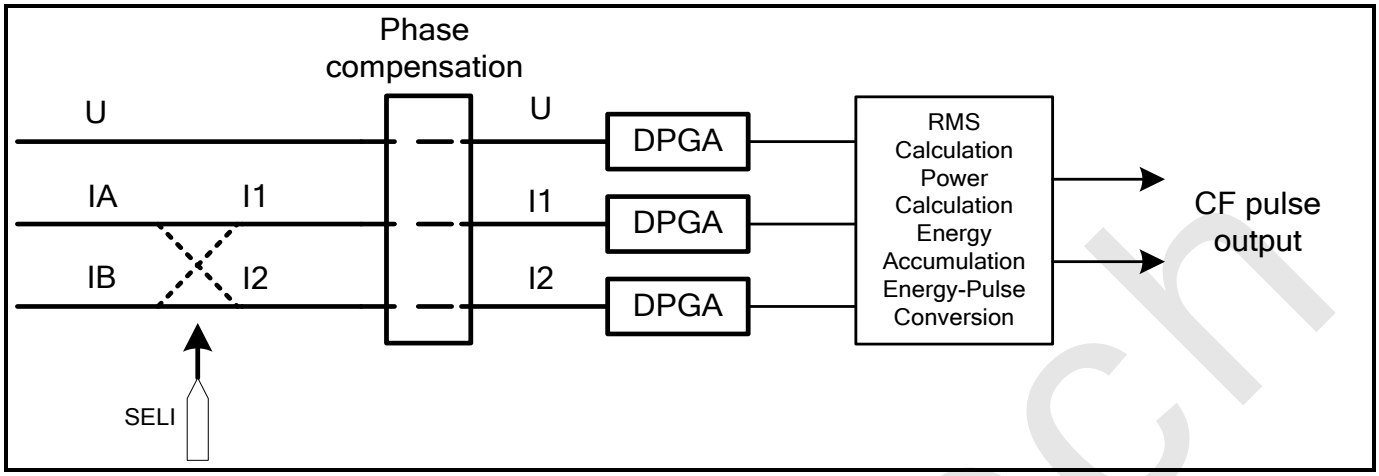


Figure 10-6 Exchange of Current Channels

Table 10-5 Control Bit for Switching Current Signals

Register	Bit	Description
0x2878 PMCtrl1	SELI Bit5	To exchange the current channels. By default this bit is cleared. 0: current IA is sent to Current I1 Channel for signal processing, and current IB is sent to Current I2 Channel for signal processing; 1: current IA is sent to Current I2 Channel for signal processing, and current IB is sent to Current I1 Channel for signal processing.

Then current (I1 and I2) and voltage signals must be input to a phase compensation circuit to correct the phase angle error between the current and voltage signals introduced by the transformers.

10.7. Phase Compensation

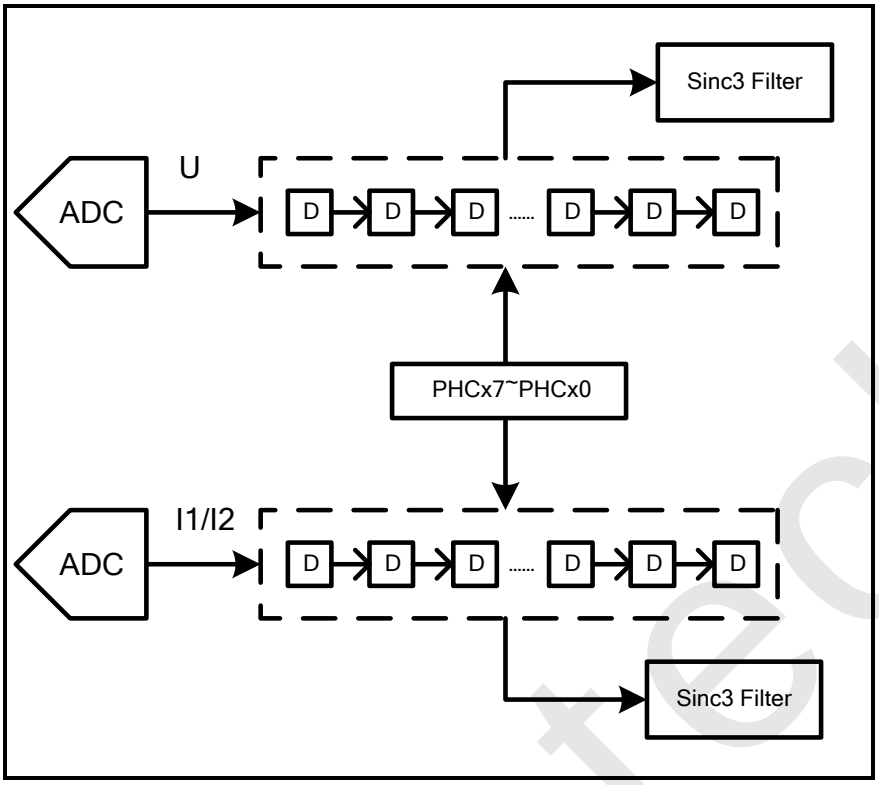


Figure 10-7 Phase Compensation Schematics

A phase compensation circuit composed of a time delay chain of fixed length is applied to correct the phase angle error via delaying the selected signal. Either current or voltage signals can be delayed.

By default phase compensation is disabled. Users can enable this function via configuring the bit **"PHCEN"** (**"bit6"** of **"PMCtrl1"**, 0x2878). When phase compensation is enabled, the phase angle error between I1 and U, and I2 and U, are corrected respectively. **"Bit [7:0]"** of register **"PHCCtrl1"** (0x287B) together with **"bit[1:0]"** (IAPHC) of register **"CRPST"** (0x287F) or **"bit[7:0]"** of register **"PHCCtrl2"** (0x287C) together with **"bit[3:2]"** (IBPHC) of register **"CRPST"** (0x287F) are used to calibrate the phase angle error between signal I1 or I2 and the voltage signal, see Table 10-7 for details.

In 50-Hz power grid, when the sampling frequency of the phase compensation circuit (f_{smpl}) is 3.2768 MHz, the calibration resolution is 0.0055°/lsb, and the maximum phase angle error to be corrected is 1.4°. The value of f_{smpl} is determined by the configuration of bits **"MEACLKSEL<1:0>"** (**"bit[3:2]"** of **"CtrlCLK"**, 0x2867).

At a lower power factor (PF), the phase angle error can cause greater energy metering error. So generally, the phase angle error is calibrated at PF=0.5L to ensure the metering accuracy. When PF=0.5L, users can use a simple equation as follows to calculate the value N.

$$N = Round(\frac{3011}{2} \times E \times \frac{f_{smpl}}{819200})$$ Equation 10-1where,

N is the value, signed, to be set to the phase compensation control registers to correct the phase angle error. A positive N indicates that current signal must be delayed, so "0" must be set to the sign bit; a negative N indicates that the voltage signal must be delayed, so "1" must be set to the sign bit;

E is the energy metering error displayed in LCD screen of the calibration equipment;

f_{smpl} is the sampling frequency of the phase compensation circuit, Hz.

Table 10-6 f_{smpl} Determines Phase Compensation Resolution and Correction Range

N	MEACLKSEL<1:0> Configuration		f_{smpl} (Hz)	Resolution (°/lsb)	Correction Range (°)
[-255, +255]	bit[3:2], 0x2867	00	819200	0.022	5.6
		01	1638400	0.011	2.8
		10	3276800	0.0055	1.4

Table 10-7 Registers for Phase Compensation

PHCCtrl1（0x287B）/PHCCtrl2（0x287C）								CRPST（0x287F）
bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	bit[3:2]/bit[1:0]
PHCx7	PHCx6	PHCx5	PHCx4	PHCx3	PHCx2	PHCx1	PHCx0	IxPHC
x=A or B. **"PHCx7"** is the sign bit, **"PHCx6"** is not used, and the other 8 bits are used to set the absolute value to correct the phase angle error.								

10.8. Digital Input

In V98XX, decimation filters are designed to reduce the noise of the 1-bit code stream output from the oversampling Σ/ΔADC and to reduce the sampling frequency to 1/256 of f_{ADC}.

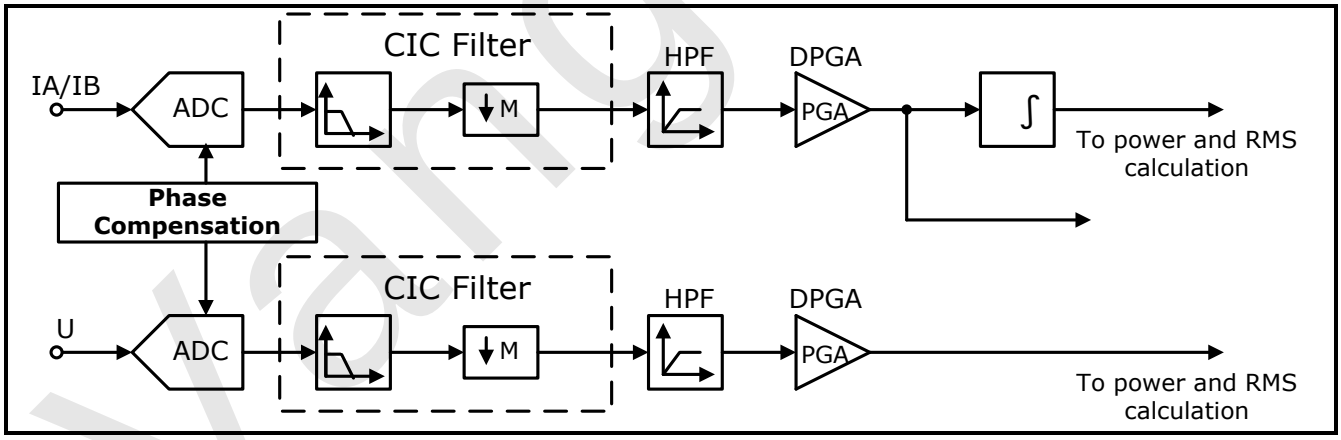


Figure 10-8 Digital Inputs

"Bit[2:0]" of the register **"PMCtrl1"** (0x2878) enables or disables the code stream input into the decimation filter. When this function is enabled, the code stream will be input to the filter; otherwise, 0s are input for digital signal processing.

Table 10-8 Enable/Disable Digital Inputs

Register	Bit	Description

Register	Bit	Description
0x2878 PMCtrl1	Bit2 ONI2	To enable digital signal input to the I2 channel. 0: disable; 0s are input to I2 channel. 1: enable.
	Bit1 ONI1	To enable digital signal input to the I1 channel. 0: disable; 0s are input to I1 channel. 1: enable.
	Bit0 ONU	To enable digital signal input to the U channel. 0: disable; 0s are input to U channel. 1: enable.

As depicted in the above figure, the signal output from the decimation filter in each channel will be sent to a high-pass filter (HPF) to remove the DC components introduced by the sensors and ADCs. In the V98XX, this high-pass filter cannot be disabled. When the **"ADCCLK"** frequency is 819.2 kHz, this filter will be settled in 60 ms in 50-Hz power grid, and in 50 ms in 60-Hz power grid.

Digital programmable gain amplifiers (DPGA) with possible gain selection via **"PMCtrl2"** (0x2879) and **"PMCtrl3"** (0x287A) are applied to digital signals output from the high-pass filters to amplify their capability of depressing truncation noise when a low signal was input. Please note the product of the analog input and the total PGA gains, including APGA and DPGA, should not be over the measurement scales of the ADCs.

Table 10-9 DPGA Gain Selection for Digital Signals

Register	Bit	Description
PMCtrl3 0x287A	PGANS Bit3	To set sign of the digital PGA gain for I2 signal. 0: positive; 1: negative.
	PGAN2~PGAN0 Bit[2:0]	To set the digital PGA gain for I2 signal. Gain=2^{PGANx}. PGANx is over the range of 0~5.
PMCtrl2 0x2879	PGACS Bit7	To set sign of the digital PGA gain for I1 signal. 0: positive; 1: negative.
	PGAC2~PGAC0 Bit[6:4]	To set the digital PGA gain for I1 signal. Gain=2^{PGACx}. PGACx is over the range of 0~5.

Register	Bit	Description
	PGAUS Bit3	To set sign of the digital PGA for U signal. 0: positive; 1: negative.
	PGAU2~PGAU0 Bit[2:0]	To set the digital PGA gain for U signal. Gain=2^{PGAUx}. PGAUx is over the range of 0~5. When bit LPFEN (bit5 of PMCtrl3, 0x287A) is set to 1, the digital PGA gain for U signal is lowered to 1/4 of its configuration. When bit LPFEN is cleared, the digital PGA gain for U signal is what it is configured.

The following equations describe the digital signals processed by the digital programmable gain amplifiers:

$$Ua = PGAdua \times PGAua \times \frac{Aua}{1.185} \times \sin \omega t = DUa \times \sin \omega t$$
$$Ia = PGAdia \times PGAia \times \frac{Aia}{1.185} \times \sin(\omega t + \psi) = DIa \times \sin(\omega t + \psi)$$

Equation 10-2

where, *PGAdua* and *PGAdia* are the DPGA gains; *PGAua* and *PGAia* are the APGA gains; *Aua* and *Aia* are the amplitude of current and voltage inputs; and 1.185 is the reference voltage.

10.9. Current Detection

To lower power consumption, a current detection circuit is designed in the V98XX to compare the AC component of the instantaneous I1 current signal with the preset threshold in register IDETTH (0x1002). Set bit DETON (bit4 of IDET, 0x2886) to 1 to enable current detection, and configure bit[3:0] of IDET (0x2886) for current detection window width ([IDLEN]+1). When ([IDLEN]+1) continuous current samples are detected to be higher than the preset threshold, it is defined a current signal is caught, and flag bit CST (bit6 of IDET, 0x2886) is set to 1. Users must set bit CLR (bit5 of IDET, 0x2886) to 1 or clear bit DETON to clear bit CST.

The configuration of bit IDLEN (bit[3:0] of IDET, 0x2886) and the current detection period have a relationship as follows:

$$t_{IDT} = \frac{256 \times ([IDLEN] + 1)}{f_{ADC}} \times 1000$$

Equation 10-3

where, 256 means the decimation filter (CIC) has reduced the sampling frequency to 1/256 of f_{ADC}, the sampling frequency of the oversampling ADC; [IDLEN] is the configuration of bits IDLEN; t_{IDT} is the current detection period, in unit of ms. To perform current detection, it is mandatory to enable the metering clock (MTCLK), and enable power/RMS calculation.

10.10. RMS Calculation and Calibration

The V98XX supports RMS calculation. By default this function is disabled. When RMS calculation is enabled, users can enable the band-pass filter in the RMS calculation circuit via bit BPFEN (bit6 of PMCtrl3,

0x287A) and configure the filter coefficient via register PARABPF (0x10EF) to improve calculation accuracy.

Table 10-10 Configuring for RMS Calculation and Calibration

Register	Bit	Description
IDET 0x2886	GT Bit7	Set this bit to 1 to disable the sampling circuits and power/RMS calculation circuits. In this case, the energy accumulation circuit keeps on working. So in an application to accumulate a constant for energy accumulation, it is recommended to set this bit to 1 to lower power consumption further. But please note the threshold for energy-to-pulse conversion must be set before setting this bit to 1.
PMCtrl1 0x2878	PREN Bit4	To enable active/reactive power calculation and RMS calculation, the apparent power calculation in M Channel. 0: disable; 1: enable. By default this function is disabled.
PMCtrl3 0x287A	BPFEN Bit6	To enable the band-pass filter in the voltage/current RMS calculation circuits. 0: disable (default); 1: enable. This filter can improve the RMS calculation accuracy, but will lead to harmonics loss. When a low signal is input, this filter will introduce greater truncation noise and prolong the period for the system to be settled.
PARABPF 0x10EF		To set the coefficient for the band-pass filter in the RMS calculation circuits. If MTCLK frequency is reduced to 819.2kHz, users must disable energy accumulation, CF pulse output and no-load detection, and then configure this register to 0x911D3C9C. When MTCLK frequency is reinstated to 3.2768MHz, this register must be set to its default value.

As illustrated in Figure 10-9, the current or voltage signal output from the high-pass filter is multiplied with itself in the multiplier to get the product with the second harmonic which can be removed by the low-pass filter, and then the signal processed output from the low-pass filter is sent to the circuit for rooting processing that produces a 32-bit datum, the raw RMS value of current or voltage. The raw RMS data will be gain calibrated and then stored in instantaneous RMS registers. Besides, the instantaneous RMS data will be averaged to acquire the average RMS data that are stored in average RMS registers.

If the raw RMS value is represented as RMS', the gain calibration value is represented as S, and the instantaneous RMS is represented as RMS, then the above three values have the relationship:

$$RMS=RMS'\times(1+S) \qquad \text{Equation 10-4}$$

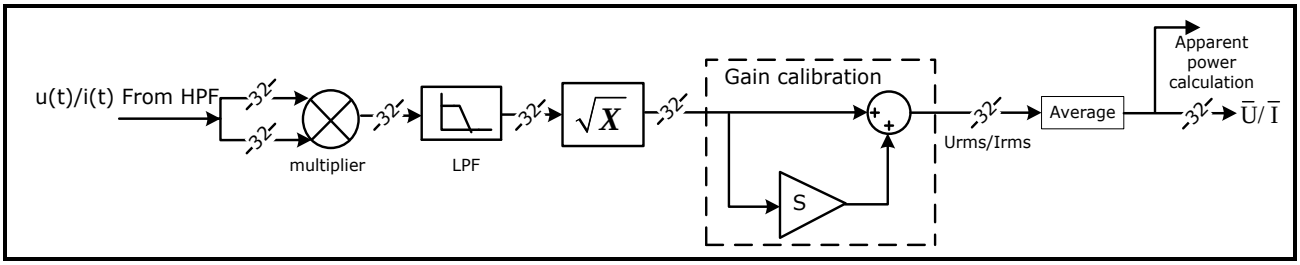


Figure 10-9 RMS Calculation and Calibration

The content of all the instantaneous and average RMS data registers are in the form of 32-bit 2'-complement. When POR/BOR, RSTn pin reset or WDT overflow reset occurs, these registers are reset to their default states.

10.11. Apparent Power Calculation

The V98XX supports apparent power calculation. This function is enabled or disabled together with RMS calculation.

In the V98XX, the average current and voltage RMS are multiplied to acquire the apparent power, as described in the following equation:

$$S = Irms \times Urms \qquad \text{Equation 10-5}$$

where, *S* represents apparent power; *Irms* and *Urms* are the average current and voltage RMS.

The content of the apparent power registers are in the form of 32-bit 2'-complement. When POR/BOR, RSTn pin reset or WDT overflow reset occurs, these registers are reset to their default states.

10.12. Power Calculation and Calibration

The V98XX supports active/reactive power calculation. This function is enabled or disabled together with the RMS calculation and apparent power calculation.

There are two paths for power calculation, energy accumulation and energy pulse generation: E1 path and E2 path. E1 path is used for active power calculation and energy accumulation only; but, E2 path can be configured for active or reactive power calculation and energy accumulation which is determined by bit DBLEN (bit4 of PMCtrl3, 0x287A). By default E2 path is used for reactive power calculation based on current I1.

Table 10-11 Functions of E2 Path

Register	Bit	Function Description

Register	Bit	Function Description
0x287A PMCtrl3	DBLEN Bit4	To select the function of E2 path. 0: for reactive power calculation and energy metering based on current I1. If positive current I1 is input to the path, the reactive power is negative, and it is accumulated to the negative energy accumulators; if negative current I1 is input to the path, the reactive power is positive, and it is accumulated to the positive energy accumulators. 1: for active power calculation and energy metering based on current I2.

10.12.1. Active Power Calculation and Calibration

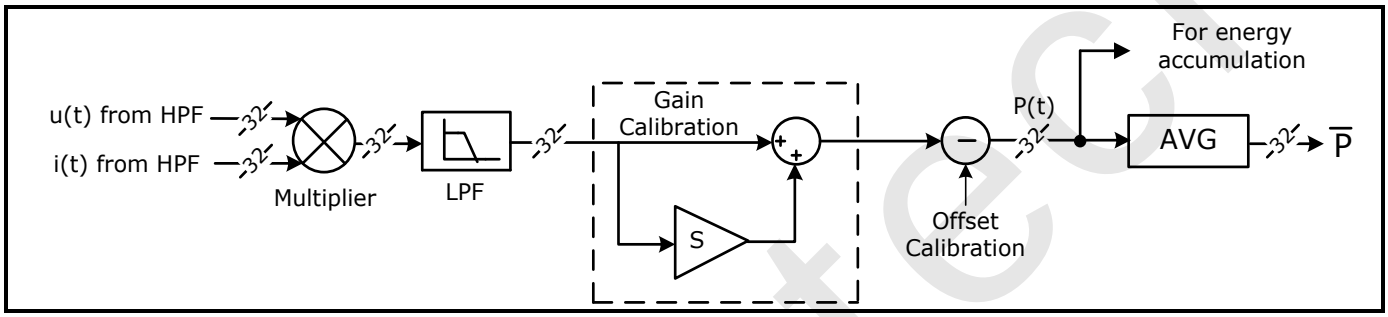


Figure 10-10 Signal Processing for Active Power Calculation and Calibration

In the V98XX, E1 path always calculates active power based on current I1. And when DBLEN is set to 1, E2 path is also used to calculate active power based on current I2.

As illustrated in the above figure, after being filtered by the high-pass filter (HPF), the current and voltage multiply each other. Then, the product is input to the low-pass filter (LPF) to remove the harmonics and the ripples caused by the noise, and the output of the LPF is the raw active power. This raw power is gain calibrated and then offset calibrated to acquire the instantaneous active power that is stored in the registers DATAIP (0x10D1, for active power calculated in E1 path) and DATAIQ (0x10D2, for active power calculated in E2 path). The instantaneous active power will be averaged to get the average active power that is stored in the registers DATAP (0x10D6, for active power in E1 path) and DATAQ (0x10D7, for active power in E2 path). The content of all the registers are in the form of 32-bit 2'-complement, and they will be reset to their default states when POR/BOR, RSTn pin reset or WDT overflow reset occurs.

Users can configure the registers SCP (0x10E8) and SCQ (0x10E9) for gain calibration over the range of -∞~+49.9%, and the registers PARAPC (0x10ED) and PARAQC (0x10EE) for offset calibration over the range of -50%~+50%. The content of these registers are in the form of 32-bit 2'-complement. When POR/BOR, RSTn pin reset or WDT overflow reset occurs, all the registers are reset to their default states.

10.12.2. Reactive Power and Calibration

By default the V98XX supports calculating active and reactive power based on current I1.

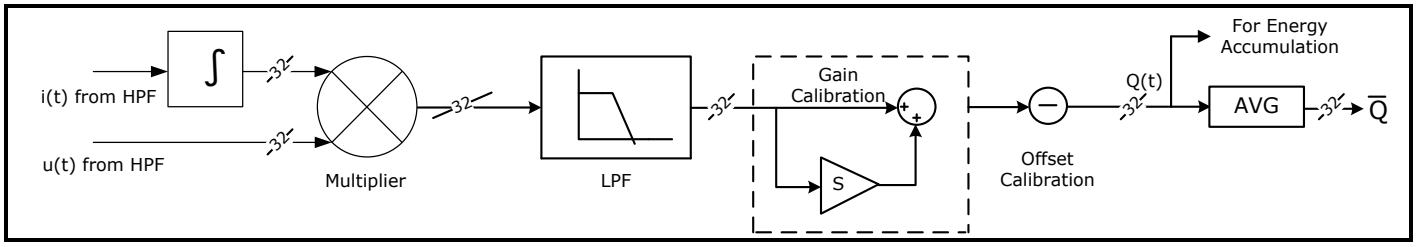


Figure 10-11 Signal Processing for Reactive Power Calculation and Calibration

As illustrated in the above figure, current I1, filtered by the high-pass filter (HPF), is input into a digital integrator to shift the phase by 90° (the integrator introduces an extra gain of 1.568 that can be eliminated via gain calibration). The filtered current signal is sent to the multiplier together with voltage to multiply each other. Then, the product is input to the low-pass filter (LPF) to remove the harmonics and the ripples caused by the noise, and the output of the LPF is the raw reactive power. This raw power is gain calibrated and offset calibrated to acquire the instantaneous reactive power, which is stored in the register DATAIQ (0x10D2, for reactive power calculated in E2 path). The instantaneous reactive power will be averaged to get the average reactive power, which is stored in the register DATAQ (0x10D7, for reactive power in E2 path). The content of the registers are in the form of 32-bit 2'-complement, and they will be reset to their default states when POR/BOR, RSTn pin reset or WDT overflow reset occurs.

Users can configure register SCQ (0x10E9) for gain calibration over the range of -∞~+49.9%, and register PARAQC (0x10EE) for offset calibration over the range of -50%~+50%. Both registers are in the form of 32-bit 2'-complement. When POR/BOR, RSTn pin reset or WDT overflow reset occurs, both registers are reset to their default states.

10.13. Energy Accumulation and CF Pulse Output

The V98XX supports energy accumulation and energy-to-pulse conversion. By default this function is disabled. Users can set bit EGYEN (bit3 of PMCtrl4, 0x287D) to 1 to enable energy accumulation and energy-to-pulse conversion.

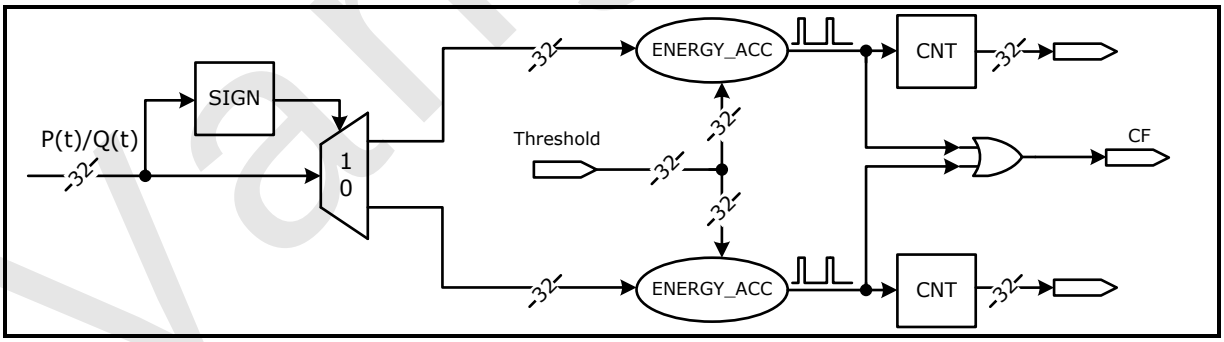


Figure 10-12 Energy Accumulation and CF Pulse Output

10.13.1. Energy Accumulation

In E1 path, positive and negative active powers are accumulated into the energy accumulators according to their signs; for example, positive active power is accumulated into PPCNT (0x10F0), and negative active power is accumulated into NPCNT (0x10F1). Besides, other data, such as I1 current RMS or a constant (preset in the register DATACP, 0x10FC), also can be selected to be accumulated into PPCNT

via configuring bits PSEL1~PSEL0 (bit[1:0] of PMCtrl4, 0x287D) when the chip is used for low power applications.

In E2 path, positive and negative active/reactive powers are accumulated into the energy accumulators according to their signs; for example, positive power is accumulated into PQCNT (0x10F6), and negative power is accumulated into NQCNT (0x10F7).

When MTCLK frequency is 3.2768MHz, 1.6384MHz or 819.2kHz, the energy accumulation frequency is 12.8kHz. When MTCLK frequency is 32768Hz, the energy accumulation frequency is 2979Hz.

The energy accumulators are of actual 42-bit length. But only the higher 32 bits are readable; and only the higher 32 bits are valid for write operation and the 10 least significant bits are padded with 0s in write operation. When POR/BOR, RSTn pin reset or WDT overflow reset occurs, all the energy accumulators are reset to default values, 0s.

Table 10-12 Register Configuration for Energy Accumulation

Register	Bit	Description
PMCtrl4 0x287D	Bit3 EGYEN	To enable energy accumulation and energy-to-pulse conversion. 0: disable; 1: enable.
	Bit[1:0] PSEL1~PSEL0	To select the source for positive active energy accumulation in E1 path. 00/11: active power calculated based on current I1; 01: I1 current RMS; 10: a constant preset in the register DATACP (0x10FC).

10.13.2. Energy Pulse Generation and CF Pulse Output

When energy accumulation and energy-to-pulse conversion is enabled, the energy will be accumulated at a certain rate. Preset a threshold in the register GATEP (0x10F4, for active energy accumulation in E1 path) or GATEQ (0x10FA, for active/reactive energy accumulation in E2 path), and when the content of energy accumulators in E1 or E2 path is higher than the preset threshold, the energy accumulator overflows, an energy pulse is generated, the energy pulse counter increments by 1, and a value equal to the threshold is subtracted from the energy accumulator.

When a low signal is input, users can reduce the energy threshold to increase the pulse generation rate to speed up energy calibration via configuring bits CFQR1~CFQR0 and CFQ1~CFQ0 (bit[7:4] of CFCtrl, 0x287E).

When CF pulse output is enabled, one CF pulse will be output every 2 counts of the pulse counter. When MTCLK frequency is 3.2768MHz, the maximum CF pulse output frequency is 6.4kHz, and the pulse width is configurable via bits CFWD (bit[5:4] of CRPST, 0x287F) and by default the width is 80ms.

In the V98XX, four pins, CF1, P9.5/CF2, P9.6/CF1 and P1.3/CFx, are used for CF pulse output.

- The pin CF1 is used for pulse output of E1 path only;
- When bit5 and bit6 of the register P9FS (SFR 0xAD) are set to 1s, the ports P9.5 and P9.6 are used

for CF pulse output of E1 and E2 path respectively;

- When the register P13FS (0x28C7) is set to 0x01, the port P1.3 is used for CF pulse output of E2 path; when the register is set to 0x04, the port P1.3 is used for CF pulse output of E1 path.

When bit CFWKEN (bit2 of IOWK, SFR 0xC9) is set to 1, CF pulse output can wake up the system from Sleep. By default CF pulse output can wake up and reset the system to OSC state. But when bit IORSTN (bit0 of IOWK, SFR 0xC9) is set to 1, this event can wake the system only but not reset the system. In this condition, after wakeup, the CPU keeps on executing the codes, and all circuits goes back where they were before sleeping, except that bits of SysCtrl (SFR 0x80), SLEEP1, SLEEP0, FWC and FSC, are cleared. When bits RTC/CF (bit2 of Systate, SFR 0xA1) and CFWK (bit3 of IOWKDET, SFR 0xAF) are read out as 1s, it indicates the system was woken up by CF pulse output.

Table 10-13 Configurations for Energy Pulse Generation Rate and CF Pulse Output

Register	Bit	Description
PMCtrl4 0x287D	Bit5, CFENR	To enable CF pulse output of E2 path. 0: disable; 1: enable.
	Bit4, CFEN	To enable CF pulse output of E1 path. 0: disable; 1: enable.
	Bit2 CFXCG	To select the pins for CF pulse output. 0: CF1 pin for E1 path; CF2 pin for E2 path; 1: CF2 pin for E1 path; CF1 pin for E2 path.
CFCtrl 0x287E	Bit[7:6], CFQR1~CFQR0	To adjust the energy pulse generation rate in E2 path. 00: ×1; 01: ×4; 10: ×8; 11: ×16.
	Bit[5:4], CFQ1~CFQ0	To adjust the energy pulse generation rate in E1 path. 00: ×1; 01: ×4; 10: ×8; 11: ×16.

Register	Bit	Description
	bit[3:2] CFSELR1~CFSELR0	To select the energy in E2 path to be converted into pulse. 01: positive active or reactive energy in E2 path; 10: negative active or reactive energy in E2 path; 00/11: the sum of the absolute values of the positive and negative active or reactive energy in E2 path.
	Bit[1:0] CFSEL1~CFSEL0	To select the energy in E1 path to be converted into pulse. 01: positive active energy in E1 path; 10: negative active energy in E1 path; 00/11: the sum of the absolute values of the positive and negative active energy in E1 path.
CRPST 0x287F	bit[5:4] CFWD	To adjust the CF pulse width. 00: 80ms; 01: 40ms; 10: 20ms; 11: 10ms.

10.14. No-Load Detection

The V98XX supports no-load detection on both E1 and E2 paths. By default this function is disabled, but users can enable it via configuring bits CRPENR and CRPEN (bit7 and bit6 of PMCtrl4, 0x287D).

There is an anti-creeping accumulator in the no-load detection circuit. When no-load detection is enabled, 1s are accumulated in this register constantly. When MTCLK frequency is 3.2768MHz, 1.6384MHz or 819.2kHz, the accumulation frequency is 12800Hz; and when MTCLK frequency is 32768Hz, the accumulation frequency is 2979Hz.

When no-load detection is enabled, constant 1s are accumulated into the embedded anti-creeping accumulator, and the energy accumulator in E1 or E2 path accumulates active or reactive power or a power constant. Preset a threshold for no-load detection in register GATECP (0x10F5) or GATECQ (0x10FB), and a threshold for energy-to-pulse conversion in register GATEP (0x10F4) or GATEQ (0x10FA). Compare the accumulation rate. If the energy accumulator overflows sooner, the anti-creeping accumulator is cleared, and E1 or E2 path starts to meter energy. Otherwise, E1 or E2 path enters creeping state. Users can read bit CRPST or CRPSTR (bit7 or bit6 of CRPST, 0x287F) to detect the state of the path.

When POR/BOR, RSTN pin reset or WDT overflow reset occurs, the mentioned threshold registers are reset to their default values, 0s.

The energy accumulators are of actual 42-bit length, but the threshold registers for energy-to-pulse conversion are of 32-bit length. So, the threshold registers will be padded with a string of 10 0s on the right to work as 42-bit registers.

Table 10-14 Configure for No-Load Detection

Register	Bit	Description
PMCtrl4 0x287D	CRPENR, Bit7	To enable no-load detection of E2 path. 0: disable (default); 1: enable.
	CRPEN, Bit6	To enable no-load detection of E1 path. 0: disable (default); 1: enable.
CRPST 0x287F	CRPST, Bit7	To indicate the state of E1 path. 0: metering energy; 1: creeping.
	CRPSTR, Bit6	To indicate the state of E2 path. 0: metering energy; 1: creeping.

10.15. Line Frequency Measurement

The V98XX supports line frequency measurement.

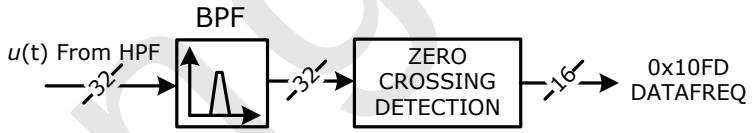


Figure 10-13 Signal Processing for Line Frequency Measurement

In the line frequency measurement circuit, the voltage signal, filtered by the high-pass filter, is input to a band-pass filter (BPF), which has a 50Hz center frequency with 25dB attenuation at 150Hz, for signal processing. The output signal from the BPF is detected for zero-crossing. The average number of the samples of the signal in 16 cycles is equal to the value of the register DATAFREQ (0x10FD). Then, the line frequency can be calculated via the following equation:

$$f = \frac{f_{ADC}}{FRQ} \qquad \text{Equation 10-6}$$

where, *f* is the line frequency to be measured; *FRQ* is the content of register DATAFREQ (0x10FD) in the form of decimal.

The line frequency register is a 16-bit, unsigned register. When POR/BOR, RSTn pin reset or WDT overflow reset occurs, this register is reset to its default state. The measurement resolution is 0.05Hz/lsb, and the measurement range is over 35~75Hz. When MTCLK frequency is 3.2768MHz, this register is updated in 320ms, and is settled in 500ms.

Note: When MTCLK frequency is lowered to 819.2kHz, the sampling frequency of the enabled band-pass filter in the RMS calculation circuit is changed to 800Hz and the center frequency is changed to 12.5Hz, which has a greater attenuation on 50Hz signals and will reduce the accuracy of the RMS calculation and line frequency measurement. So, if MTCLK frequency is reduced to 819.2kHz, users must disable energy accumulation, CF pulse output and no-load detection, and then configure this register to 0x911D3C9C.

10.16. Measuring Various Signals in M Channel

10.16.1. Architecture of M Channel

The M Channel can be used to measure the ground, temperature, battery voltage and external voltage signals. As illustrated in the following figure, there is only one ADC in M Channel, so users must configure registers to use this channel to measure one signal at a time.

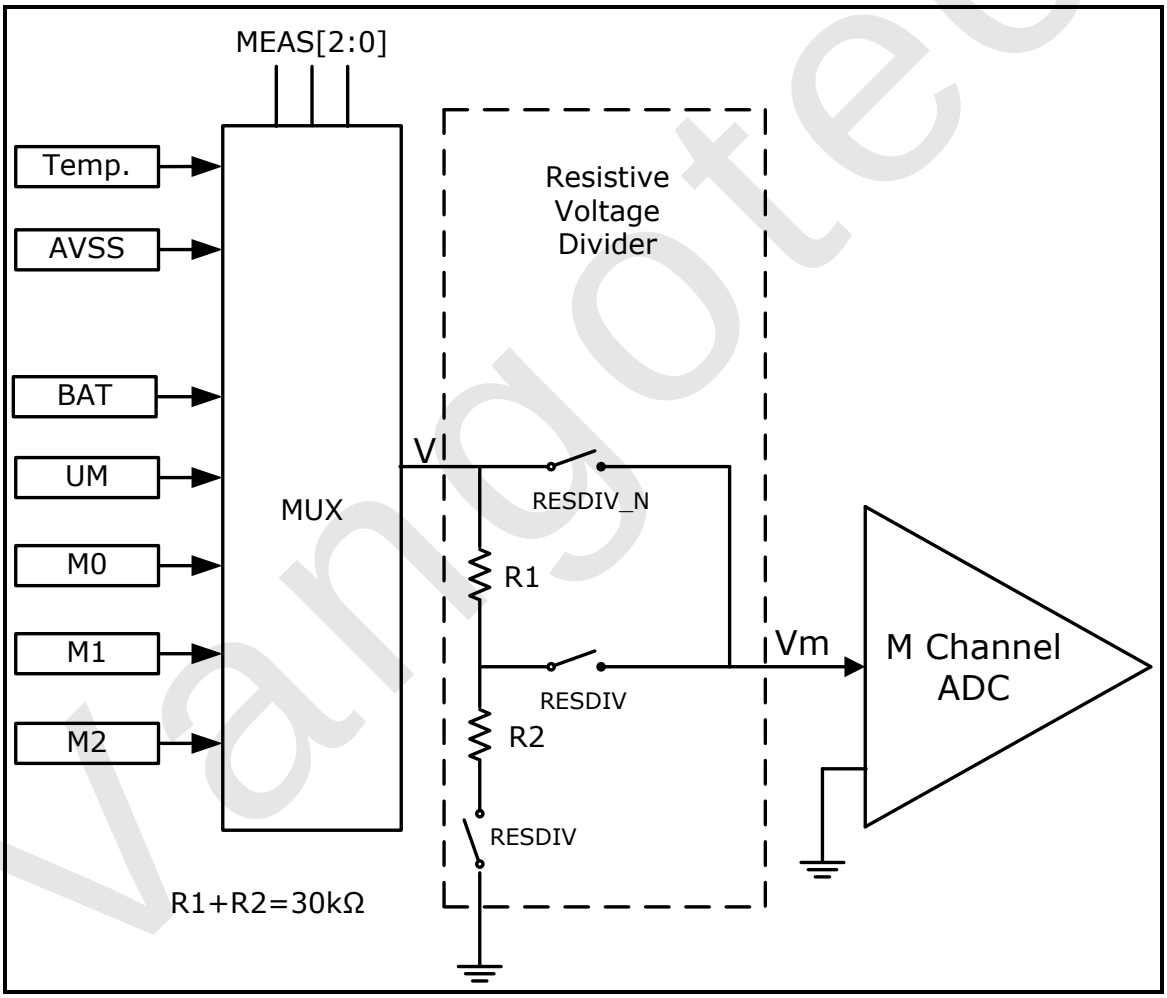


Figure 10-14 M Channel Architecture

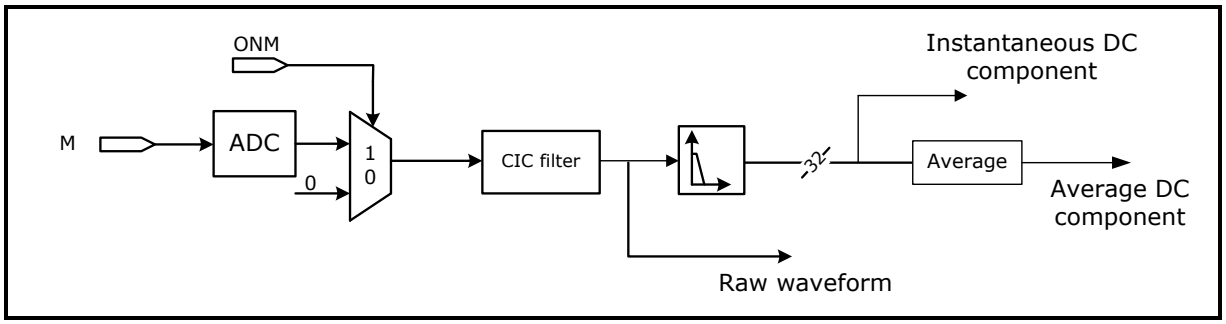


Figure 10-15 Signal Processing in M Channel

There are three data registers of M Channel, DATAOM (0x10CE) for raw waveform of the various signal input, DATADM (0x10CF) for instantaneous DC component of the signal, and DATAADM (0x10D0) for average DC component of the signal. The content of these registers are in the form of 32-bit 2' complement. When POR/BOR, RSTn pin reset or WDT overflow reset occurs, these registers are reset to their default states.

In 50Hz power grid, when MTCLK frequency is 3.2768MHz, DATAOM is updated in 0.3ms and settled in 10ms; DATADM is updated in 20ms and settled in 70ms; DATAADM is updated in 1.28s and settled in 3s. If MTCLK frequency is divided by a coefficient K, the update and settle time is K times of that for 3.2768MHz MTCLK frequency.

10.16.2. Measuring Temperature

M Channel is used to measure temperature. The temperature measurement range is over -40~+85°C with a measurement error of ±1°C.

It is recommended to measure temperature following steps:

1. Enable M Channel ADC: ADCMPDN=1 (bit3 of CtrlADC6, 0x2864). It is mandatory to enable BandGap circuit before M Channel ADC;
2. Configure the register CtrlADC5 (0x2863) as follows:
   - To disable the internal resistive divider: RESDIV=0 (bit4);
   - To enable M Channel to measure temperature: MEAS<2:0>= 001 (bit[2:0]).
3. Set bit MADCHOPN (bit0 of CtrlM, 0x2865) to 1 to stop removing DC offset in M Channel ADC;
4. Enable the sampling circuits and power/RMS calculation circuits: GT=0 (bit7 of IDET, 0x2886);
5. Configure the register PMCtrl1 (0x2878) as follows:
   - Set bit ONM (bit3) to 1 to enable digital signal input to M Channel for digital signal processing;
   - Set bit PREN (bit4) to 1 to enable digital signal processing.
6. Wait for 70ms (f_{MTCLK}=3.2768MHz) or 280ms (f_{MTCLK}=819.2kHz), and then read the register DATADM (0x10CF) and calculate the nominal temperature T' (in unit of °C):

$$T' = \frac{B \times (D \times \frac{x_0}{2^{16}} + C)^{\frac{1}{2}} - A}{E}$$ Equation 10-7

where x_0 is the reading of register DATADM (in hexadecimal); A/B/C/D/E is the parameters of the temperature curve, which can be read in bytes located at addresses 0x420~0x433 (in small endian format). There are another two bytes used for the checksum.

7. Calibrate temperature:
   - There is a constant error ΔT between the nominal temperature T' and the actual temperature T:

$$\Delta T = \frac{x_1}{10}$$ Equation 10-8

where x_1 is the content of bytes located at addresses 0x480~0x481 (There are another two bytes used for the checksum.) (in hexadecimal, and in small endian format), 10 times of the actual temperature error ΔT. The unit of ΔT is 0.1 °C.

   - Calculate the actual temperature according to the following equation:

$$T = T' + \Delta T$$ Equation 10-9

10.16.3. Measuring Battery Voltage and External Voltage

In the V98XX, pin BAT can be used to input battery voltage or external voltage signals to be measured, and the voltage signal must be over the range of -200mV~3.8V; pin UM, M0, M1 or M2 can be used to input external voltage signals to be measured, and the voltage signal must be over the range of -200mV~3.4V.

It is recommended to measure the battery voltage or external voltage signals following steps:

1. Enable M Channel ADC: ADCMPDN=1 (bit3 of CtrlADC6, 0x2864). It is mandatory to enable BandGap circuit before M Channel ADC;
2. Configure the register CtrlADC5 (0x2863) as follows:
   - To configure the internal resistive divider:
     - When the input voltage signal is over the range of -200mV~1.1V, it is mandatory to set RESDIV=0 (bit4);
     - When the input voltage signal is over the range of 1.1V~3.8V (for BAT) or 1.1V~3.4V (for UM/M0/M1/M2), it is mandatory to set either bit GDE4 or bit RESDIV to 1;
   - To enable M Channel to measure battery voltage or external voltage signals.
3. Set bit MADCHOPN (bit0 of CtrlM, 0x2865) to 1 to stop removing DC offset in M Channel ADC;
4. Enable the sampling circuits and power/RMS calculation circuits: GT=0 (bit7 of IDET, 0x2886);
5. Configure the register PMCtrl1 (0x2878) as follows:
   - Set bit ONM (bit3) to 1 to enable digital signal input to M Channel for digital signal processing;
   - Set bit PREN (bit4) to 1 to enable digital signal processing.

Wait for 10ms (f_{MTCLK}=3.2768MHz) or 40ms (f_{MTCLK}=819.2kHz), and then read the register DATAOM (0x10CE) and RESDIV configuration,then calculate the amplitude of the voltage signal V_{DC} (in unit of mV):

- When the voltage signal is over the range of -200mV~1.1V:

$$V_{DC} = \frac{\frac{x_R}{2^{16}} + 198.42}{27210} \qquad \text{Equation 10-10}$$

- When the voltage signal is over the range of 1.1V~3.8V (for BAT) or 3.4V (UM/M0/M1/M2), and RESDIV=1:

$$V_{DC} = \frac{\frac{x_R}{2^{16}} + 50.693}{5959.9} \qquad \text{Equation 10-11}$$

Because there are 30kΩ resistors in the internal resistive divider network, this network consumes power:

$$P = U_D \times I_D = V \times \frac{V}{R1 + R2} = \frac{V^2}{30} \qquad \text{Equation 10-12}$$

- When the voltage signal is over the range of 1.1V~3.8V (for BAT) or 3.4V (UM/M0/M1/M2), and RESDIV=0:

$$V_{DC} = \frac{\frac{x_R}{2^{16}} + 21.034}{7118.3} \qquad \text{Equation 10-13}$$

In the above equations, x_R is the content of register DATAOM (0x10CE).

10.17. Initializing Energy Metering Architecture

To ensure the performance of the energy metering architecture, it must be initialized as follows:

1. Clear the bits CRPEN, CFEN and EGYEN (bit5~bit3 of PMCtrl4, 0x287D) to disable energy accumulation, CF pulse output and no-load detection; clear the bit PREN (bit4 of PMCtrl1, 0x2878) and bits ONx (bit3~bit0 of PMCtrl1, 0x2878) to disable the signal input to Channel I1/I2/U/M and stop the digital signal processing.
2. Enable the ADCs.
3. When f_{ADC} is 819.2kHz, write 0x889374BC to the register PARABPF (0x10EF); When f_{ADC} is 204.8kHz, write 0x911D3C9C to the register PARABPF (0x10EF).
4. Write 1 to bit PREN (bit4 of PMCtrl1, 0x2878) to enable power and RMS calculation.
5. Wait for 70ms (f_{ADC}=819.2kHz) or 250ms (f_{ADC}=204.8kHz) until the registers for waveform registers are read out as 0s, and then clear the read/write buffer registers located at addresses 0x2880~0x2885, and clear the registers located at addresses 0x1059~0x106A.
6. Configure the calibration registers (except the PARABPF and current detection threshold register).
7. Access to the energy metering control registers:
   - Configure the bit SELI (bit5 of PMCtrl1, 0x2878) to switch the current channels.
   - Configure the bit PHCEN (bit6 of PMCtrl1, 0x2878) to enable phase compensation, and configure the registers PHCCtrl1 (0x287B), PHCCtrl2 (0x287C) and bits IBPHC and IAPHC (bit[3:0] of CRPST, 0x287F) to set which and how the signal to be delayed.

- Configure the digital PGA gain for current and voltage signals.
- Configure the bit DBLEN (bit4 of PMCtrl3, 0x287A) to select the function of E2 path.
- Configure the bits LPFEN and BPFEN (bit5 and bit6 of PMCtrl3, 0x287A) to enable the low-pass filter and band-pass filter.
- Configure the bits PSEL1 and PSEL0 (bit1 and bit0 of PMCtrl4, 0x287D) to select the signal to be accumulated to the positive energy accumulator in E1 path.
- Configure the register CFCtrl (0x287E) for CF pulse output.
- Write 1s to bit6 and bit7 of PMCtrl4 (0x287D) to enable no-load detection in E1 and E2 paths.

8. Write 1s to the bits ONx (bit3~bit0 of PMCtrl1, 0x2878) to enable the signal input to Channel I1/I2/U/M.
9. Wait for 250ms (f_{ADC}=819.2kHz), or 900ms (f_{ADC}=204.8kHz).
10. Write the stored values of the energy accumulators and energy pulse counters into themselves. If the values are 0s, it is equal to clearing the registers.
11. Read of the threshold registers for energy-to-pulse conversion and no-load detection. If the value is anomaly, reconfigure the registers.
12. Configure registers to enable CF pulse interrupt (optional).
13. Write 1s to the bits CRPEN, CFEN and EGYEN (bit5~bit3 of PMCtrl4, 0x287D) to enable energy accumulation, CF pulse output and no-load detection.

10.18. Calibration

10.18.1. Registers for Meter Calibration

Table 10-15 Registers for Meter Calibration

Address	Register		R/W	Format
0x10F4	GATEP	To set a threshold for active energy-to-pulse conversion in E1 path.	R/W	Unsigned
0x10F5	GATECP	To set a threshold for no-load detection in E1 path.	R/W	Unsigned
0x10FA	GATEQ	To set a threshold for active or reactive energy-to-pulse conversion in E2 path.	R/W	Unsigned
0x10FB	GATECQ	To set a threshold for no-load detection in E2 path.	R/W	Unsigned
0x10E8	SCP	To set a value to gain calibrate active power in E1 path.	R/W	2’ complement
0x10EB	SCI1	To set a value to gain calibrate current I1 RMS.	R/W	2’ complement

Address	Register		R/W	Format
0x10E9	SCQ	To set a value to gain calibrate active/reactive power in E2 path.	R/W	2' complement
0x10EC	SCI2	To set a value to gain calibrate current I2 RMS.	R/W	2' complement
0x10EA	SCU	To set a value to gain calibrate voltage RMS.	R/W	2' complement
0x287B	PHCCtrl1	Phase Compensation Control Register 1	R/W	
0x287C	PHCCtrl2	Phase Compensation Control Register 2	R/W	
0x287F	CRPST	Bit[3:0] of CRPST: IBPHC and IAPHC, for phase compensation	R/W	
0x10ED	PARAPC	To set a value to offset calibrate active power in E1 path.	R/W	2' complement
0x10EE	PARAQC	To set a value to offset calibrate active/reactive power in E2 path.	R/W	2' complement
0x10D6	DATAP	Average active power in E1 path.	R	2' complement
0x10D7	DATAQ	Average active or reactive power calculated in E2 path.	R	2' complement
0x10D8	RMSU	Average voltage RMS.	R	2' complement
0x10D9	RMSI1	Average current I1 RMS.	R	2' complement
0x10DA	RMSI2	Average current I2 RMS.	R	2' complement

10.18.2. Equations for Calibration

1. Equation for current/voltage RMS registers.

$$RMS = V \times G \times K \qquad \text{Equation 10-14}$$

where, *V* is the RMS value of the input signal (mV); *G* is the gain; and *K* is a constant, 1.8117×10^9.

2. Equation for power registers.

$$P = Vi \times Gi \times Vv \times Gv \times B \times C \qquad \text{Equation 10-15}$$

where, *Vi* and *Vv* are the input current and voltage; *Gi* and *Gv* are the gains for current and voltage respectively; C=*cosθ* for active power calculation, C=sinθ for reactive power calculation; *B* is a coefficient, 1.5413×10^9 for active power calculation or 2.4167×10^9 for reactive power calculation.

3. Equation for ratio factor of RMS and power.

The value acquired by Equation 10-14 or Equation 10-15 is the theoretical value of the register of the RMS or power. It must be multiplied by a ratio factor to get the actual value (accurate to the second decimal place).

$$D = \frac{V_n}{Value} \qquad \text{Equation 10-16}$$

where, *Value* is the theoretical value of the registers acquired by Equation 10-14 or Equation 10-15; *D* is the ratio factor; and V_n is the rated voltage/current/power.

4. Equation for registers for phase compensation.

Please note that phase compensation must be executed after power calibration.

At a lower power factor (PF), the phase angle error can cause greater energy metering error. So generally, the phase angle error is calibrated at PF=0.5L to ensure the metering accuracy. When PF=0.5L, users can use a simple equation as follows to calculate the value N.

$$N = Round(\frac{3011}{2} \times E \times \frac{f_{smpl}}{819200}) \qquad \text{Equation 10-17}$$

where,

N is the value, signed, to be set to the phase compensation control registers to correct the phase angle error. A positive N indicates that current signal must be delayed, so "0" must be set to the sign bit; a negative N indicates that the voltage signal must be delayed, so "1" must be set to the sign bit;

E is the energy metering error displayed in LCD screen of the calibration equipment;

f_{smpl} is the sampling frequency of the phase compensation circuit, Hz.

5. Equation for energy accumulation threshold.

$$PGAT = \frac{P \times T \times 6400}{1024} \qquad \text{Equation 10-18}$$

where *P* is the power calculated by Equation 10-15; *T* is a time constant acquired via the equation:

$$T = \frac{3600 \times 1000}{PulseConstant \times U_n \times I_n} \qquad \text{Equation 10-19}$$

6. Equation for the gain calibration registers.

$$S = 2^{31}(\frac{1}{1+e} - 1) + S_1(\frac{1}{1+e}) \qquad \text{Equation 10-20}$$

where, *S* is the content to be set in the registers for gain calibration of active/reactive power or current/voltage RMS, in the form of 2'-complement; S_1 is the original value of the registers; *e* is the error: when this equation is used for power gain calibration, *e* is equal to the error displayed in LCD screen of the calibration equipment (*E*); when this equation is used for RMS gain calibration, *e* is equal to the error (E_u/E_i) calculated by the following equations:

$$E_u = \frac{U_1 - U_n}{U_n} \qquad \text{Equation 10-21}$$

$$E_i = \frac{I_1 - I_b}{I_b}$$ Equation 10-22

where U_1/I_1 is the voltage/current RMS displayed in LCD screen of the meter to be calibrated, U_n is the rated voltage, and I_b is the base current.

7. Equation for power offset calibration registers.

$$C = a\% \times E_1 \times P$$ Equation 10-23

where E_1 is the error displayed in LCD screen of the calibration equipment when $a\%I_b$ is applied at power factor 1.0; generally, a=1; and P is the power calculated by Equation 10-15.

8. Equation for no-load detection threshold registers.

Generally, the period for the first pulse output is used as the threshold for no-load detection, so the threshold can be calculated as follows:

$$GATECP = T' \times \frac{1}{2} \times f_{overflow} = \frac{3600 \times 1000}{PulseConstant \times U_n \times \frac{1}{2} I_s} \times \frac{1}{2} \times f_{overflow}$$ Equation 10-24where,

U_n: rated voltage;

I_s: starting current. Generally, $I_s=0.4\%I_b$, and $\frac{1}{2}I_s$ is used for no-load detection;

$f_{overflow}$: accumulation frequency of the energy accumulator. When f_{MTCLK}=3.2768MHz, $f_{overflow}$=12800Hz; when f_{MTCLK}=32768Hz, $f_{overflow}$=2979Hz.

10.18.3. Steps for Calibration

10.18.3.1. Parameters Configuration

Users must determine the following parameters when designing an energy meter:

- Parameters for a meter, including basic current, rated voltage, pulse constant and accuracy class.
- Parameters for design, including the current and voltage RMS when rated current and rated voltage are applied.
- The analog PGA gains of the current and voltage channels.
- The ratio factor (D) of RMS and power calculated via Equation 10-16.
- The threshold for energy-to-pulse conversion calculated via Equation 10-18.
- The threshold for no-load detection calculated via Equation 10-24.

When the above parameters are determined, no changes should be done to them.

10.18.3.2. Calibrating Active Energy

1. Gain calibration

At power fact of 1.0, apply 100% U_n and 100% I_b to the calibration equipment.

Before calibration, read the error displayed in LCD screen of the calibration equipment (*E*), and read the value of the gain calibration register (SCP, 0x10E8), S_1, and then calculate the value for gain calibration via Equation 10-20 and write it to the register SCP (0x10E8). After having written, if the error displayed in LCD screen of the calibration equipment (E) is over the range of standard, indicating the difference ratio correction is succeding.

2. Phase compensation

After gain calibration of power, apply 100%I_b and 100%U_n to the calibration equipment when PF=0.5L, to correct the phase angle error between the current and voltage signals.

Clear bit[5:0] of PHCCtrl1 (0x287B) and bit[2:1] of CRPST (0x287F) or bit[5:0] of PHCCtrl2 (0x287C) and bit[4:3] of CRPST (0x287F), and then write the values calculated by Equation 10-17 to the register. If N is positive, the sign bit is "0"; if N is negative, the sign bit is "1".

3. Offset calibration

Apply 5%I_b or 2% I_b and 100%U_n to the calibration equipment when PF=1.0. Read the error (E) displayed in LCD screen and calculate the value for power offset calibration by Equation 10-23, and write them to the registers for power offset calibration.

10.18.3.3. Calibrating Current RMS

1. Clear the register SCI1 (0x10EB).
2. Apply 100%I_b to the calibration equipment at PF=1.0.
3. Read the current RMS I_1 shown in the LCD screen of the calibration equipment (I_1 is the product of the value of the gain calibration register and the coefficient D).
4. Calculate the value to gain calibrate the current signal of Channel I1 via Equation 10-20.

Note: When the current through the energy meter is less than the starting current, the current RMS I_1 is not shown in the LCD.

10.18.3.4. Calibrating Voltage RMS

1. Clear the register SCU (0x10EA).
2. Apply 100% U_n to the calibration equipment.
3. Read the voltage RMS U_1 shown in the LCD screen of the calibration equipment (U_1 is the product of the value of the gain calibration register and the coefficient D).
4. Calculate the value to gain calibrate the voltage signal of Channel U via Equation 10-20.

11. Interrupt

When POR/BOR, RSTn pin reset, WDT overflow event, power recovery event, IO/RTC wakeup event or debugging event occurs, the interrupt control module is reset to its default state.

CLK1 provides clock pulses for the interrupt control module, so when the system enters Sleep or Deep Sleep state, the interrupt control module stops running to save power. Each extended interrupt can be gate controlled independently via configuring register PRCtrl1 (0x2D01).

11.1. Interrupt Sources

In the V98XX 41 events can trigger interrupts:

- 4 IO interrupts on low or high-to-low transitions;
- 4 transmitter data output interrupt of UART, and 2 transmitter data output interrupt of enhanced UART;
- 4 receiver data input interrupt of UART, and 2 receiver data input interrupt of enhanced UART;
- 4 timer overflow interrupts;
- 3 timer capture interrupts (TimerA);
- 2 overflow interrupt of enhanced UART;
- 2 CF pulse output interrupts;
- 1 pulse per second (PPS) output interrupt;
- 1 RTC illegal data interrupt;
- 1 zero-crossing interrupt;
- 1 power-down interrupt;
- 1 GPSI illegal data interrupt;
- 1 GPSI transmit interrupt;
- 1 comparator interrupt;
- 1 REF leakage interrupt.

In the V98XX the interrupts triggered by peripheral events are called *"Extended Interrupt"*. They are named after the polling sequence; for example, Interrupt 8 is named because the polling sequence of the extended interrupt handler located at 43h is 8. Additionally, an extended interrupt may be triggered by more than one event (interrupt sources); for example, both transmitter data output interrupt and receiver data input interrupt of UART2 can trigger the program execution to service the interrupt handler located at 43h (Interrupt 8).

Take Interrupt 8 as an example to introduce how to trigger an interrupt, service and clear the interrupt flag, and detect the event that triggers an extended interrupt. Only when the global enable bit IE.7 and the enable bit for Interrupt 8 (EIE.0) is set to 1, will Interrupt 8 be triggered if any one enabled peripheral event occurs and the flag bits of Interrupt 8 and the interrupt event is set bit. The program has to detect the interrupt source depending on the flags and enable bits of the peripheral event when the program enters to the interrupt subroutine located at address 43h. The processor can respond to the interrupt event by polling or interrupt handling. When an extended interrupt is responded, the program must clear the flag of the peripheral event firstly, and then the flag of Interrupt 8.

In the V98XX, there are two tiers of interrupts: Interrupt Priority 1 and Interrupt Priority 0. Registers IP (SFR 0xB8) and EIP (SFR 0xF8) can configure the priority of the interrupts. Interrupt Priority 1 takes precedence over Interrupt Priority 0. In addition to an assigned priority level (1 or 0), each interrupt has a polling sequence. An interrupt with a small polling sequence number means that it must be serviced firstly when two interrupts of the same tier occur simultaneously. If two interrupts of different priority occur, the one of Interrupt Priority 1 is serviced firstly. Only an interrupt of higher priority level can break the service routine of the interrupt currently being serviced; when the new interrupt is serviced, the program will go back where it was interrupted and serve the last interrupt.

Table 11-1 Interrupt Sources

Polling sequence	Vector address	Interrupt No.[1]	Description	Enable bit of interrupt	Enable bit of peripheral event	Flag of interrupt	Flag of peripheral event
0 (highest)	33h	6	Reserved.				
1	03h	0	IO interrupt 0 (INT0), triggered on low level or high-to-low transition.	IE.0		TCON.1	
2	0Bh	1	Timer0 interrupt (TF0).	IE.1		TCON.5	
3	13h	2	IO interrupt 1 (INT1), triggered on low level or high-to-low transition.	IE.2		TCON.3	
4	1Bh	3	Timer1 interrupt (TF1).	IE.3		TCON.7	
5	23h	4	Reserved.				
6	2Bh	5	Timer2 interrupt (TF2, EXF2).	IE.5		T2CON.7	
7	3Bh	7	Receiver data input interrupt of UART1 (RI1).	IE.6		SCON1.0	
			Transmitter data output interrupt of UART1 (TI1).			SCON1.1	
8	43h	8	Transmitter data output interrupt of UART2.	EIE.0	ExInt2IE.0	EXIF.4	ExInt2IFG.0

[1] When Keil IDE is applied, users must use Interrupt No. to check the interrupts.

Polling sequence	Vector address	Interrupt No.[1]	Description	Enable bit of interrupt	Enable bit of peripheral event	Flag of interrupt	Flag of peripheral event
			Receiver data input interrupt of UART2.		ExInt2IE.1		ExInt2IFG.1
			Transmitter data output interrupt of UART4.		ExInt2IE.2		ExInt2IFG.2
			Receiver data input interrupt of UART4.		ExInt2IE.3		ExInt2IFG.3
			Timer overflow interrupt of UART2.		ExInt2IE.4		ExInt2IFG.4
			Timer overflow interrupt of UART4.		ExInt2IE.5		ExInt2IFG.5
			Reserved.				
			CF pulse output interrupt of E1 path		ExInt2IE.7		ExInt2IFG.7
9	4Bh	9	Transmitter data output interrupt of UART3.	EIE.1		EXIF.5	
			Receiver data input interrupt of UART3.				
			Transmitter data output interrupt of UART5.		ExInt3IE.2		ExInt3IFG.2
			Receiver data input interrupt of UART5.		ExInt3IE.3		ExInt3IFG.3
			Timer overflow interrupt of UART3.				
			Timer overflow interrupt of UART5.		ExInt3IE.5		ExInt3IFG.5
			Pulse per second (PPS) output interrupt of RTC.		ExInt3IE.6		ExInt3IFG.6
			CF pulse output interrupt of E2 path.		ExInt3IE.7		ExInt3IFG.7
10	53h	10	Illegal data interrupt of RTC.	EIE.2	ExInt4IE.0	EXIF.6	ExInt4IFG.0

Polling sequence	Vector address	Interrupt No.[1]	Description	Enable bit of interrupt	Enable bit of peripheral event	Flag of interrupt	Flag of peripheral event
			Transmitter data output interrupt, receiver data input output, and overflow interrupt of EUART1 RIF/SIF/OVIF (0x2A04)		RCIE SDIE ExInt4IE.1		ExInt4IFG.1
			IO interrupt 2 (INT2), triggered on high-to-low transition.		ExInt4IE.2		ExInt4IFG.2
			IO interrupt 3 (INT3), triggered on high-to-low transition.		ExInt4IE.3		ExInt4IFG.3
			REF leakage interrupt.		ExInt4IE.4		ExInt4IFG.4
			Zero-crossing interrupt.		X0EN (bit7 of 0x287A) ExInt4IE.5		ExInt4IFG.5
			Transmitter data output interrupt, receiver data input output, and overflow interrupt of EUART2 RIF/SIF/OVIF (0x2B04)		RCIE SDIE ExInt4IE.6		ExInt4IFG.6
			Reserved.				
11	5Bh	11	TimerA overflow interrupt.	EIE.3	ExInt5IE.0	EXIF.7	ExInt5IFG.0
			TimerA capture interrupt 0.		ExInt5IE.1		ExInt5IFG.1
			TimerA capture interrupt 1.		ExInt5IE.2		ExInt5IFG.2
			TimerA capture interrupt 2.		ExInt5IE.3		ExInt5IFG.3

Polling sequence	Vector address	Interrupt No.[1]	Description	Enable bit of interrupt	Enable bit of peripheral event	Flag of interrupt	Flag of peripheral event
			Illegal data interrupt of GPSI.		ExInt5IE.4		ExInt5IFG.4
			Transmit interrupt of GPSI.		ExInt5IE.5		ExInt5IFG.5
			Comparator interrupt.		ExInt5IE.6		ExInt5IFG.6
			Reserved.				
12 (lowest)	63h	12	Power-down interrupt.	EIE.4		EICON.3	

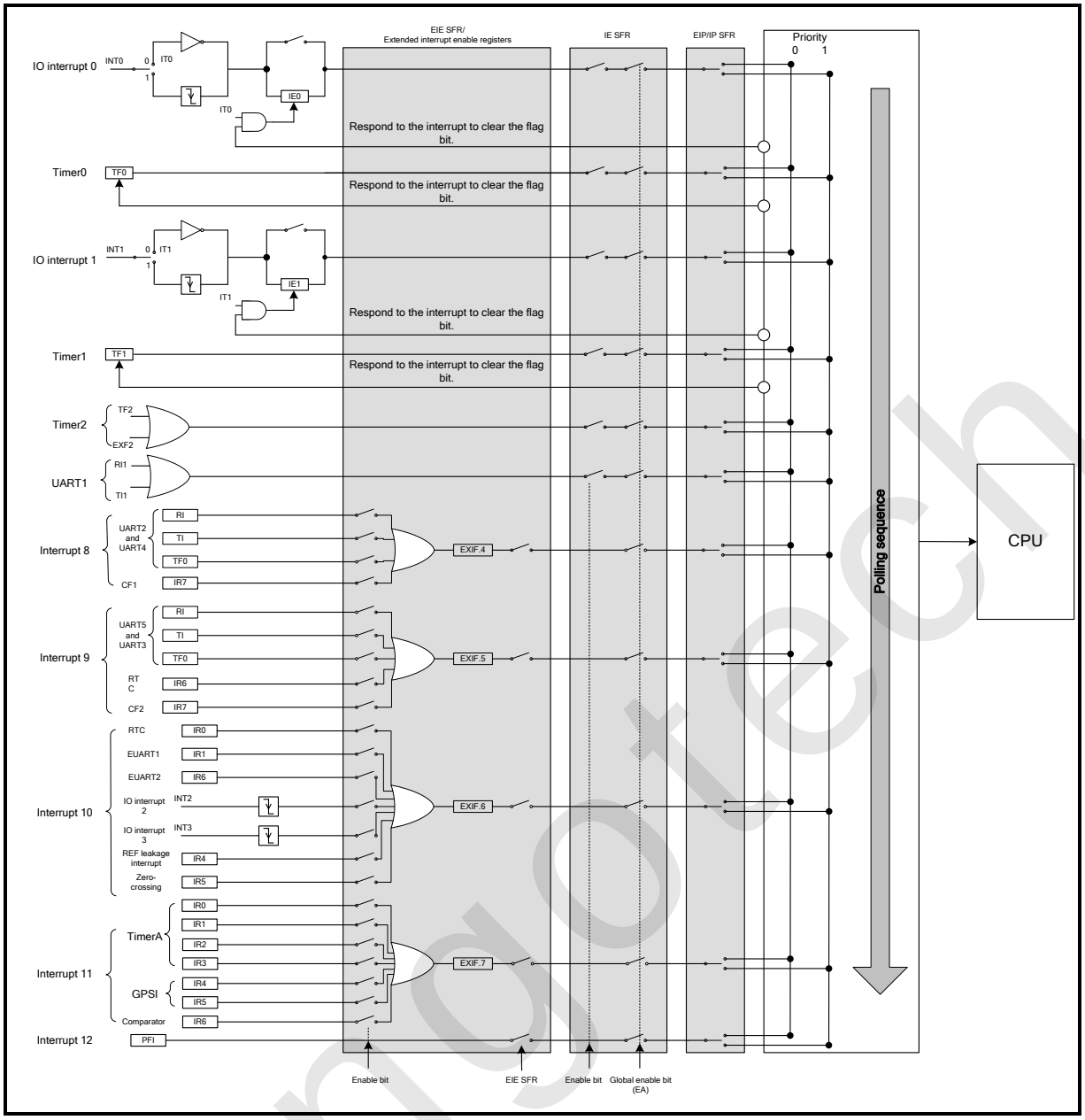


Figure 11-1 Interrupt Logic

11.2. Interrupt Control Registers

Table 11-2 IE (SFR 0xA8)

Bit		Description
IE.7	EA	Global interrupt enable bit. EA overrides individual interrupt enable bit. 0: to disable all interrupts. 1: indicating that each interrupt is enabled or disabled by its individual enable bit.

Bit		Description
IE.6	ES1	UART1 interrupt enable bit. 1: to enable transmitter data output interrupt of UART1 triggered by the flag TI1 or receiver data interrupt of UART1 triggered by the flag RI1. 0: to disable the UART1 interrupt.
IE.5	ET2	Timer2 interrupt enable bit. 0: to disable Timer2 interrupt (TF2 or EXF2). 1: to enable the interrupt triggered by flag TF2 or EXF2.
IE.4	ES0	Reserved
IE.3	ET1	Timer1 interrupt enable bit. 0: to disable Timer1 interrupt (TF1). 1: to enable the interrupt generated by the flag TF1.
IE.2	EX1	IO Interrupt 1 enable bit. 0: to disable IO Interrupt 1. 1: to enable the interrupt triggered by high-to-low transition or low level on the port INT1.
IE.1	ET0	Timer0 interrupt enable bit. 0: to disable Timer0 interrupt (TF0). 1: to enable the interrupt triggered by the flag TF0.
IE.0	EX0	IO Interrupt 0 enable bit. 0: to disable IO Interrupt 0. 1: to enable the interrupt triggered by high-to-low transition or low level on the port INT0.

Table 11-3 EIE (SFR 0xE8)

Bit	Description
EIE.7-5	Reserved. Read out as 1.
EIE.4	Interrupt 12 (Power-down Interrupt, PFI) enable bit. 0: disable; 1: enable.
EIE.3	Interrupt 11 enable bit. 0: disable; 1: enable.

Bit	Description
EIE.2	Interrupt 10 enable bit. 0: disable; 1: enable.
EIE.1	Interrupt 9 enable bit. 0: disable; 1: enable.
EIE.0	Interrupt 8 enable bit. 0: disable; 1: enable.

Table 11-4 EXIF (SFR 0x91)

Bit		Description
EXIF.7	IE5	Interrupt 11 flag. When this bit is set to 1, it indicates that Interrupt 11 was triggered. IE5 must be cleared by software. When Interrupt 11 was enabled, setting IE5 by software can trigger an interrupt.
EXIF.6	IE4	Interrupt 10 flag. When this bit is set to 1, it indicates that Interrupt 10 was triggered. IE4 must be cleared by software. When Interrupt 10 was enabled, setting IE4 by software can trigger an interrupt.
EXIF.5	IE3	Interrupt 9 flag. When this bit is set to 1, it indicates that Interrupt 9 was triggered. IE3 must be cleared by software. When Interrupt 9 was enabled, setting IE3 by software can trigger an interrupt.
EXIF.4	IE2	Interrupt 8 flag. When this bit is set to 1, it indicates that Interrupt 8 was triggered. IE3 must be cleared by software. When Interrupt 8 was enabled, setting IE2 by software can trigger an interrupt.
EXIF.3	Reserved	Read out as 1.
EXIF.2-0	Reserved	Read out as 0.

Table 11-5 EICON (SFR 0xD8)

Bit		Description
EICON.7	SMOD1	UART1 baud rate double enable bit. Set this bit to 1 to double the baud rate for UART1 serial interface.
EICON.6	Reserved	Read out as 1.
EICON.5	Reserved.	
EICON.4	Reserved.	

Bit		Description
EICON.3	PFI	Power-down Interrupt (Interrupt 12) flag. When this bit is set to 1, it indicates that a power-down interrupt was triggered. This flag must be cleared by software before exiting the interrupt service routine. Otherwise, the interrupt will occur again. When Interrupt 12 was enabled, setting this flag by software can trigger a power-down interrupt.
EICON.2-0	Reserved.	Read out as 0.

Table 11-6 IP (SFR 0xB8)

Bit		Description
IP.7	Reserved.	Read out as 1.
IP.6	PS1	Set this bit to 1 to configure UART1 transmit or receive interrupt (RI1 or TI1) to Interrupt Priority 1. Clear this bit to configure it to Interrupt Priority 0.
IP.5	PT2	Set this bit to 1 to configure Timer2 interrupt (TF2 or EXF2) to Interrupt Priority 1. Clear this bit to configure it to Interrupt Priority 0.
IP.4	PS0	Reserved
IP.3	PT1	Set this bit to 1 to configure Timer1 interrupt (TF1) to Interrupt Priority 1. Clear this bit to configure it to Interrupt Priority 0.
IP.2	PX1	Set this bit to 1 to configure IO Interrupt 1 to Interrupt Priority 1. Clear this bit to configure it to Interrupt Priority 0.
IP.1	PT0	Set this bit to 1 to configure Timer0 interrupt (TF0) to Interrupt Priority 1. Clear this bit to configure it to Interrupt Priority 0.
IP.0	PX0	Set this bit to 1 to configure IO Interrupt 0 to Interrupt Priority 1. Clear this bit to configure it to Interrupt Priority 0.

Table 11-7 EIP (SFR 0xF8)

Bit	Description
EIP.7-5	Reserved. Read out as 1.
EIP.4	Set this bit to 1 to configure Interrupt 12 (Power-down interrupt) Interrupt Priority 1. Clear this bit to configure it to Interrupt Priority 0.
EIP.3	Set this bit to 1 to configure Interrupt 11 Interrupt Priority 1. Clear this bit to configure it to Interrupt Priority 0.
EIP.2	Set this bit to 1 to configure Interrupt 10 Interrupt Priority 1. Clear this bit to configure it to Interrupt Priority 0.
EIP.1	Set this bit to 1 to configure Interrupt 9 Interrupt Priority 1. Clear this bit to configure it to Interrupt Priority 0.
EIP.0	Set this bit to 1 to configure Interrupt 8 Interrupt Priority 1. Clear this bit to configure it to Interrupt Priority 0.

11.3. Interrupt Processing

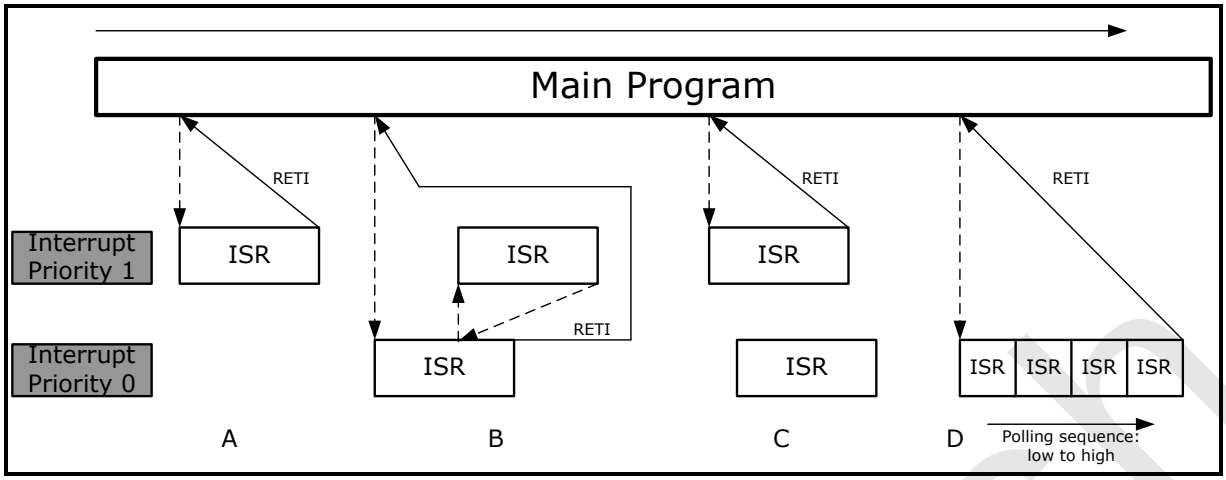


Figure 11-2 Interrupt Processing

The preceding figure illustrates the interrupt processing in the V98XX. When an enabled interrupt occurs,

- The program jumps to the interrupt vector address to execute the interrupt service routine (ISR) of the interrupt. An ISR being executed can only be interrupted by one of the interrupt with higher priority. Each ISR ends with an *RETI* (return from interrupt) instruction, as shown as *A* in the preceding figure.
- After executing the *RETI*, the program returns to the place where it was interrupted, as if it did not leave off, to execute the next instruction that would have been executed if the interrupt had not occurred. The program always completes an instruction in progress before servicing an interrupt. If an instruction executed in progress is *RETI*, or a write operation to registers including IP SFR, IE SFR, EIP SFR, and EIE SFR, the program will complete one additional instruction before servicing the ISR.
- In the V98XX, Interrupt Priority 1 has higher priority than Interrupt Priority 0. So, the ISR of Interrupt Priority 0 only can be interrupted by the ISR of Interrupt Priority 1, as shown as B and C in the preceding figure.
- An ISR of Interrupt Priority 0 can be intruded by one of Interrupt Priority 1. When the latter one is executed, the program will return to the place at the vector address of the former one where it was interrupted to execute the ISR, and then, execute the instruction *RETI* to finish the ISR, as shown as B in the preceding figure.
- When two interrupts of the same tier (Interrupt Priority 1 or Interrupt Priority 0) occur simultaneously, the polling sequence of them is observed, as shown as D in the preceding figure.
- Interrupt latency depends on the current state of the MCU.
  - The shortest interrupt latency is equal to five instruction cycles: one to detect the interrupt, and four to perform the *LCALL* to the ISR.
  - The longest latency (equal to thirteen instruction cycles) occurs when the MCU is currently executing an *RETI* instruction followed by a *MUL* or *DIV* instruction. The thirteen instruction cycles in this case are: one to detect the interrupt, three to complete the *RETI*, five to execute the *DIV* or *MUL*, and four to execute the *LCALL* to the ISR. For an interrupt with the maximum latency, the interrupt latency is 52 (13x4) clock cycles.
- To ensure that high-to-low-transition-triggered interrupts can be detected, such as IO Interrupt 0/1/2/3, the level on the corresponding ports should be held high for at least four clock cycles and then low for no less than four clock cycles. If a level-triggered interrupt occurs when the flag has not been set bit, or an interrupt with higher priority is in process which blocks the program jumping to the interrupt vector address to execute its ISR, the interrupt signal will hold until it is to be serviced.

11.4. Extended Interrupts

11.4.1. Interrupt 8

Interrupt 8 can be triggered by 7 interrupt events which are listed in the following table. Bit ExInt2 (bit0 of PRCtrl1, 0x2D01) gate controls Interrupt 8.

Table 11-8 Interrupt Events to Trigger Interrupt 8

Interrupt 8			Interrupt Event	Enable bit	Flag (R/W)
Vector Address	Enable Bit	Flag (R/W)			
43h	IE.7 EIE.0	EXIF.4 (IE2)	Transmitter data output interrupt of UART2	ExInt2IE.0	ExInt2IFG.0
			Receiver data input interrupt of UART2	ExInt2IE.1	ExInt2IFG.1
			Transmitter data output interrupt of UART4	ExInt2IE.2	ExInt2IFG.2
			Receiver data input interrupt of UART4	ExInt2IE.3	ExInt2IFG.3
			Timer overflow interrupt of UART2	ExInt2IE.4	ExInt2IFG.4
			Timer overflow interrupt of UART4	ExInt2IE.5	ExInt2IFG.5
			CF pulse interrupt of E1 path	ExInt2IE.7	ExInt2IFG.7

Table 11-9 Extended Interrupt Flag (Request) Register (ExInt2IFG, 0x2840)

0x2840, R/W, Extended Interrupt Flag (Request) Register, ExInt2IFG								
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
	IR7	-	IR5	IR4	IR3	IR2	IR1	IR0
Default	0	X	0	0	0	0	0	0
1: an interrupt request occurred; 0: no interrupt request occurred; X: do not care. A flag bit can be set to 1 only when the corresponding interrupt was enabled. When an interrupt was enabled, writing 1 to the corresponding flag bit can trigger the interrupt. Otherwise, however, cannot. Write 0 to a bit can clear the corresponding interrupt flag.								

Table 11-10 Extended Interrupt Input Type Register (ExInt2IN, 0x2841)

0x2841, R/W, Extended Interrupt Input Type Register, ExInt2IN

	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
	EDG7I	-	EDG5I	EDG4I	EDG3I	EDG2I	EDG1I	EDG0I
Default	1	X	1	1	1	1	1	1
These bits must be set to their default values for proper operation.								

Table 11-11 Extended Interrupt Output Type Register (ExInt2OUT, 0x2842)

0x2842, R/W, Extended Interrupt Output Type Register, ExInt2OUT								
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
	-	-	-	-	-	-	-	EDGO
Default	-	-	-	-	-	-	-	1
These bits must be set to their default values for proper operation.								

Table 11-12 Extended Interrupt Enable Register (ExInt2IE, 0x2843)

0x2843, R/W, Extended Interrupt Enable Register, ExInt2IE								
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
	IE7	-	IE5	IE4	IE3	IE2	IE1	IE0
Default	0	X	0	0	0	0	0	0
1: enable; 0: disable; X: do not care.								

Table 11-13 Extended Interrupt Pending Register (ExInt2OV, 0x2844)

0x2844, R/W, Extended Interrupt Pending Register, ExInt2OV								
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
	IPND7	-	IPND5	IPND4	IPND3	IPND2	IPND1	IPND0
Default	0	X	0	0	0	0	0	0
If an interrupt is triggered again when the corresponding flag in the register ExInt2IFG has not been cleared yet, the corresponding pending bit of this register will be set to 1. The pending bit is just an indication flag, nothing to do with the interrupt. It must be cleared by the program.								

11.4.2. Interrupt 9

Interrupt 9 can be triggered by 8 interrupt events which are listed in the following table. Bit ExInt3 (bit1 of PRCtrl1, 0x2D01) gate controls Interrupt 9.

Table 11-14 Interrupt Event to Trigger Interrupt 9

Interrupt 9			Interrupt Event	Enable Bit	Flag (R/W)
Vector Address	Enable Bit	Flag (R/W)			

Interrupt 9			Interrupt Event	Enable Bit	Flag (R/W)
Vector Address	Enable Bit	Flag (R/W)			
4Bh	IE.7 EIE.1	EXIF.5 (IE3)	Transmitter data output interrupt of UART3(V98XX)	ExInt3IE.0	ExInt3IFG.0
			Receiver data input interrupt of UART3(V98XX)	ExInt3IE.1	ExInt3IFG.1
			Transmitter data output interrupt of UART5	ExInt3IE.2	ExInt3IFG.2
			Receiver data input interrupt of UART5	ExInt3IE.3	ExInt3IFG.3
			Timer overflow interrupt of UART3(V98XX)	ExInt3IE.4	ExInt3IFG.4
			Timer overflow interrupt of UART5	ExInt3IE.5	ExInt3IFG.5
			Pulse per second interrupt of RTC	ExInt3IE.6	ExInt3IFG.6
			CF pulse interrupt of E2 path	ExInt3IE.7	ExInt3IFG.7

Table 11-15 Extended Interrupt Flag (Request) Register (ExInt3IFG, 0x2848)

0x2848, R/W, Extended Interrupt Flag (Request) Register, ExInt3IFG								
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
	IR7	IR6	IR5	IR4	IR3	IR2	IR1	IR0
Default	0	0	0	0	0	0	0	0
1: an interrupt request occurred; 0: no interrupt request occurred; X: do not care. A flag bit can be set to 1 only when the corresponding interrupt was enabled. When an interrupt was enabled, writing 1 to the corresponding flag bit can trigger the interrupt. Otherwise, however, cannot. Write 0 to a bit can clear the corresponding interrupt flag.								

Table 11-16 Extended Interrupt Input Type Register (ExInt3IN, 0x2849)

0x2849, R/W, Extended Interrupt Input Type Register, ExInt3IN								
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
	EDG7I	EDG6I	EDG5I	EDG4I	EDG3I	EDG2I	EDG1I	EDG0I
Default	1	1	1	1	1	1	1	1
These bits must be set to their default values for proper operation.								

Table 11-17 Extended Interrupt Output Type Register (ExInt3OUT, 0x284A)

0x284A, R/W, Extended Interrupt Output Type Register, ExInt3OUT

	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
	-	-	-	-	-	-	-	EDGO
Default	-	-	-	-	-	-	-	1
These bits must be set to their default values for proper operation.								

Table 11-18 Extended Interrupt Enable Register (ExInt3IE, 0x284B)

0x284B, R/W, Extended Interrupt Enable Register, ExInt3IE								
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
	IE7	IE6	IE5	IE4	IE3	IE2	IE1	IE0
Default	0	0	0	0	0	0	0	0
1: enable; 0: disable; X: do not care.								

Table 11-19 Extended Interrupt Pending Register (ExInt3OV, 0x284C)

0x284C, R/W, Extended Interrupt Pending Register, ExInt3OV								
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
	IPND7	IPND6	IPND5	IPND4	IPND3	IPND2	IPND1	IPND0
Default	0	0	0	0	0	0	0	0
If an interrupt occurs again when the corresponding flag in the register ExInt3IFG has not been cleared yet, the corresponding pending bit of this register will be set to 1. The pending bit is just an indication flag, nothing to do with the interrupt. It must be cleared by the program.								

11.4.3. Interrupt 10

Interrupt 10 can be triggered by 7 interrupt/ 5 interrupt events/which are listed in the following table. Bit ExInt4 (bit2 of PRCtrl1, 0x2D01) gate controls Interrupt 10.

Table 11-20 Interrupt Events to Trigger Interrupt 10

Interrupt 10			Interrupt Event	Enable Bit	Flag (R/W)
Vector Address	Enable Bit	Flag (R/W)			
53h	IE.7 EIE.2	EXIF.6 (IE4)	RTC illegal data interrupt	ExInt4IE.0	ExInt4IFG.0
			Transmitter data output interrupt, receiver data input interrupt and timer overflow interrupt of EUART1(V98XX)	ExInt4IE.1	ExInt4IFG.1
			IO Interrupt 2 (INT2), triggered on high-to-low transition	ExInt4IE.2	ExInt4IFG.2

Interrupt 10			Interrupt Event	Enable Bit	Flag (R/W)
Vector Address	Enable Bit	Flag (R/W)			
			IO Interrupt 3 (INT3), triggered on high-to-low transition	ExInt4IE.3	ExInt4IFG.3
			REF leakage interrupt	ExInt4IE.4	ExInt4IFG.4
			Zero-crossing interrupt	ExInt4IE.5	ExInt4IFG.5
			Transmitter data output interrupt, receiver data input interrupt and timer overflow interrupt of EUART2	ExInt4IE.6	ExInt4IFG.6

Table 11-21 Extended Interrupt Flag (Request) Register (ExInt4IFG, 0x2850)

0x2850, R/W, Extended Interrupt Flag (Request) Register, ExInt4IFG								
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
	-	IR6	IR5	IR4	IR3	IR2	IR1	IR0
Default	X	0	0	0	0	0	0	0
1: an interrupt request occurred; 0: no interrupt request occurred; X: do not care. A flag bit can be set to 1 only when the corresponding interrupt was enabled. When an interrupt was enabled, writing 1 to the corresponding flag bit can trigger the interrupt. Otherwise, however, cannot. Write 0 to a bit can clear the corresponding interrupt flag.								

Table 11-22 Extended Interrupt Input Type Register (ExInt4IN, 0x2851)

0x2851, R/W, Extended Interrupt Input Type Register, ExInt4IN								
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
	-	EDG6I	EDG5I	EDG4I	EDG3I	EDG2I	EDG1I	EDG0I
Default	X	1	1	1	1	1	1	1
These bits must be set to their default values for proper operation.								

Table 11-23 Extended Interrupt Output Type Register (ExInt4OUT, 0x2852)

0x2852, R/W, Extended Interrupt Output Type Register, ExInt4OUT								
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
	-	-	-	-	-	-	-	EDGO
Default	-	-	-	-	-	-	-	1
These bits must be set to their default values for proper operation.								

Table 11-24 Extended Interrupt Enable Register (ExInt4IE, 0x2853)

0x2853, R/W, Extended Interrupt Enable Register, ExInt4IE								
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
	-	IE6	IE5	IE4	IE3	IE2	IE1	IE0
Default	X	0	0	0	0	0	0	0
1: enable; 0: disable; X: do not care.								

Table 11-25 Extended Interrupt Pending Register (ExInt4OV, 0x2854)

0x2854, R/W, Extended Interrupt Pending Register, ExInt4OV								
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
	-	IPND6	IPND5	IPND4	IPND3	IPND2	IPND1	IPND0
Default	X	0	0	0	0	0	0	0
If an interrupt occurs again when the corresponding flag in the register ExInt4IFG has not been cleared yet, the corresponding pending bit of this register will be set to 1. The pending bit is just an indication flag, nothing to do with the interrupt. It must be cleared by the program.								

11.4.4. Interrupt 11

Interrupt 11 can be triggered by 7 interrupt events which are listed in the following table. Bit ExInt5 (bit3 of PRCtrl1, 0x2D01) gate controls Interrupt 11.

Table 11-26 Interrupt Events to Trigger Interrupt 11

Interrupt 11			Interrupt Event	Enable Bit	Flag (R/W)
Vector Address	Enable Bit	Flag (R/W)			
5Bh	IE.7 EIE.3	EXIF.7 (IE5)	TimerA overflow interrupt	ExInt5IE.0	ExInt5IFG.0
			TimerA capture interrupt 0	ExInt5IE.1	ExInt5IFG.1
			TimerA capture interrupt 1	ExInt5IE.2	ExInt5IFG.2
			TimerA capture interrupt 2	ExInt5IE.3	ExInt5IFG.3
			Illegal data interrupt of GPSI*	ExInt5IE.4	ExInt5IFG.4
			Transmit interrupt of GPSI*	ExInt5IE.5	ExInt5IFG.5
			Comparator interrupt	ExInt5IE.6	ExInt5IFG.6
*When bit GPSI (bit6 of PRCtrl0, 0x2D00) is set to 1, GPSI (general-purpose serial interface) is enabled. Writing of illegal data or transmit completion will trigger interrupt to CPU.					

Table 11-27 Extended Interrupt Flag (Request) Register (ExInt5IFG, 0x28A2)

0x28A2, R/W, Extended Interrupt Flag (Request) Register, ExInt4IFG

	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
	-	IR6	IR5	IR4	IR3	IR2	IR1	IR0
Default	X	0	0	0	0	0	0	0

1: an interrupt request occurred; 0: no interrupt request occurred; X: do not care.

A flag bit can be set to 1 only when the corresponding interrupt was enabled. When an interrupt was enabled, writing 1 to the corresponding flag bit can trigger the interrupt. Otherwise, however, cannot.

Write 0 to a bit can clear the corresponding interrupt flag.

Table 11-28 Extended Interrupt Input Type Register (ExInt5IN, 0x28A3)

0x28A3, R/W, Extended Interrupt Input Type Register, ExInt5IN

	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
	-	EDG6I	EDG5I	EDG4I	EDG3I	EDG2I	EDG1I	EDG0I
Default	X	1	1	1	1	1	1	1

These bits must be set to their default values for proper operation.

Table 11-29 Extended Interrupt Output Type Register (ExInt5OUT, 0x28A4)

0x2852, R/W, Extended Interrupt Output Type Register, ExInt4OUT

	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
	-	-	-	-	-	-	-	EDGO
Default	-	-	-	-	-	-	-	1

These bits must be set to their default values for proper operation.

Table 11-30 Extended Interrupt Enable Register (ExInt5IE, 0x28A5)

0x28A5, R/W, Extended Interrupt Enable Register, ExInt4IE

	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
	-	IE6	IE5	IE4	IE3	IE2	IE1	IE0
Default	X	0	0	0	0	0	0	0

1: enable; 0: disable; X: do not care.

Table 11-31 Extended Interrupt Pending Register (ExInt5OV, 0x28A6)

0x28A6, R/W, Extended Interrupt Pending Register, ExInt5OV

	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
	-	IPND6	IPND5	IPND4	IPND3	IPND2	IPND1	IPND0
Default	X	0	0	0	0	0	0	0

0x28A6, R/W, Extended Interrupt Pending Register, ExInt5OV								
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
If an interrupt occurs again when the corresponding flag in the register ExInt5IFG has not been cleared yet, the corresponding pending bit of this register will be set to 1. The pending bit is just an indication flag, nothing to do with the interrupt. It must be cleared by the program.								

12. UART/Timers

When power-on or brown out reset (POR/BOR), RSTn pin reset, WDT overflow, power recovery event, IO/RTC wakeup event or debugging reset occurs, all the timers and the UART serial interfaces are reset to their default states. In Sleep or Deep Sleep, they stop working. Each extended UART serial interface and TimerA can be gate controlled independently via configuring register PRCtrl0 (0x2D00) and PRCtrl1 (0x2D01).

12.1. Timers/Counters

The V98XX can provide users with timers listed as follows:

- TimerA, a 16-bit timer, with 3 compare/capture modules, gate controlled independently;
- Timer0, Timer1 and Timer2 of 8052 microcontroller. They work as general timers; furthermore, Timer1 can work as the baud rate generator of UART1;
- The general timer and specific baud rate generator of each extended UART serial interface (UART2/UART3(V98XX)/UART4/UART5). Each interface can be gate controlled independently. The general timer has the same function with Timer0, an overflow event of which will set the flag bit to 1, which will be cleared by executing interrupt service routine (ISR) or by polling interrupt sources, and generate an interrupt to the CPU. The specific baud rate generator has the same function with Timer1: it can be used as a general timer, an overflow event of which can set the flag bit to 1 but cannot generate an interrupt to the CPU.

In this section, only TimerA, Timer0, Timer1 and Timer2 are introduced. The general timers in extended UART serial interfaces are introduced in “UART”.

12.1.1. TimerA

TimerA is a 16-bit timer/counter, and has 4 operation modes. It has 3 compare/capture modules, and 3 configurable output units with 8 output modes. Bit TimerA (bit0 of PRCtrl0, 0x2D00) gate controls TimerA.

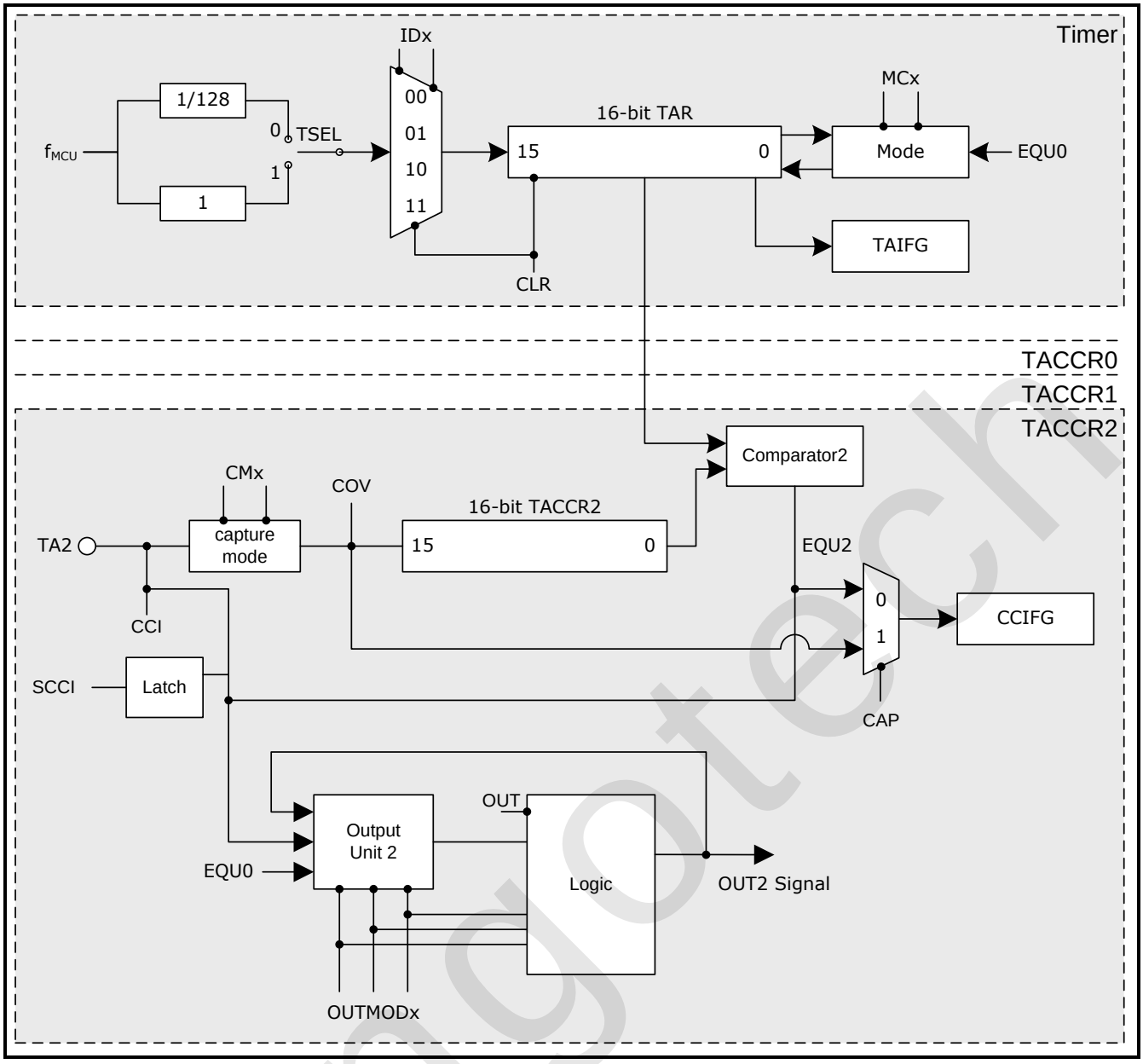


Figure 12-1 TimerA Architecture

Table 12-1 TimerA-Related Registers

Address	Description		
0x2900	TACTL, Timer A Control Register		R/W
0x2902	Low byte	TAR, TimerA Timer/Counter Register	R
0x2903	High byte		
0x2904	TACCTL0, low byte	Timer A Compare/Capture Control Register 0	R/W
0x2905	TACCTH0, high byte		
0x2906	TACCTL1, low byte	Timer A Compare/Capture Control Register 1	R/W

Address	Description		
0x2907	TACCTH1, high byte		
0x2908	TACCTL2, low byte	Timer A Compare/Capture Control Register 2	R/W
0x2909	TACCTH2, high byte		
0x290A~0x290B	TACCR0, Timer A Compare/Capture Register 0		R/W
0x290C~0x290D	TACCR1, Timer A Compare/Capture Register 1		R/W
0x290E~0x290F	TACCR2, Timer A Compare/Capture Register 2		R/W

Table 12-2 Timer A Counter/Timer Register (TAR, 0x2902~0x2903)

0x2902~0x2903, R, Timer A Timer/Counter Register, TAR			
Bit		Default	Description
0x2903	Bit[7:0]	0	The registers give the value of TimerA (TAR), of which the low byte is in the register located at address 0x2902, and the high byte is in 0x2903. It is read-only, and can be reset by software. When TimerA overflows, an interrupt is generated to the CPU.
0x2902	Bit[7:0]		

Table 12-3 Timer A Control Register (TACTL, 0x2900)

<table>
<tr><td colspan="4">0x2900, R/W, TimerA Control Register, TACTL</td></tr>
<tr><td colspan="2">Bit</td><td>Default</td><td>Description</td></tr>
<tr><td>Bit7</td><td>ID1</td><td rowspan="2">0</td><td>These bits are used to select the divider for the input clock.
ID1 ID0 Description
0 0 The input clock is divided by 2;
0 1 The input clock is divided by 4;
1 0 The input clock is divided by 8;
1 1 The input clock is divided by 16.</td></tr>
<tr><td>Bit6</td><td>ID0</td></tr>
<tr><td>Bit5</td><td>MC1</td><td>0</td><td>To select operation mode, as illustrated in figure “Operation Modes for TimerA”.
MC1 MC0 Description
0 0 Stop Mode: the timer is halted.</td></tr>
</table>

0x2900, R/W, TimerA Control Register, TACTL			
Bit		Default	Description
Bit4	MC0		0 1 Up Mode: the timer counts up to the value of TACCR0, and recount from 0000h. 1 0 Continuous Mode: the timer counts up to FFFFh, and recounts from 0000h. 1 1 Up/Down Mode: the timer counts up to the value of TACCR0, and then, back down to 0000h.
Bit3	TSEL	-	To select the clock source for the timer. 0: f_{MCU} /128; 1: f_{MCU}.
Bit2	CLR	0	Set the bit CLR to 1 to clear the register TAR, meanwhile, [ID1, ID0]=00; if the timer works in Up/Down mode, the timer rolls over to 0000h, and back up to the value of TACCR0.
Bit1	TAIE	0	When the bit EX3 (EIE.3) is set to 1, set this bit to 1 to enable TimerA overflow interrupt. When this bit is cleared, the interrupt is disabled.
Bit0	TAIFG	0	TimerA overflow interrupt flag. In the Up Mode, when the timer rolls over to 0000h from the value of TACCR0, TAIFG is set bit. In the Continuous Mode, when the timer rolls over to 0000h from FFFFh, TAIFG is set bit. In the Up/Down Mode, when the timer counts down to 0000h from 0001h, TAIFG is set bit.

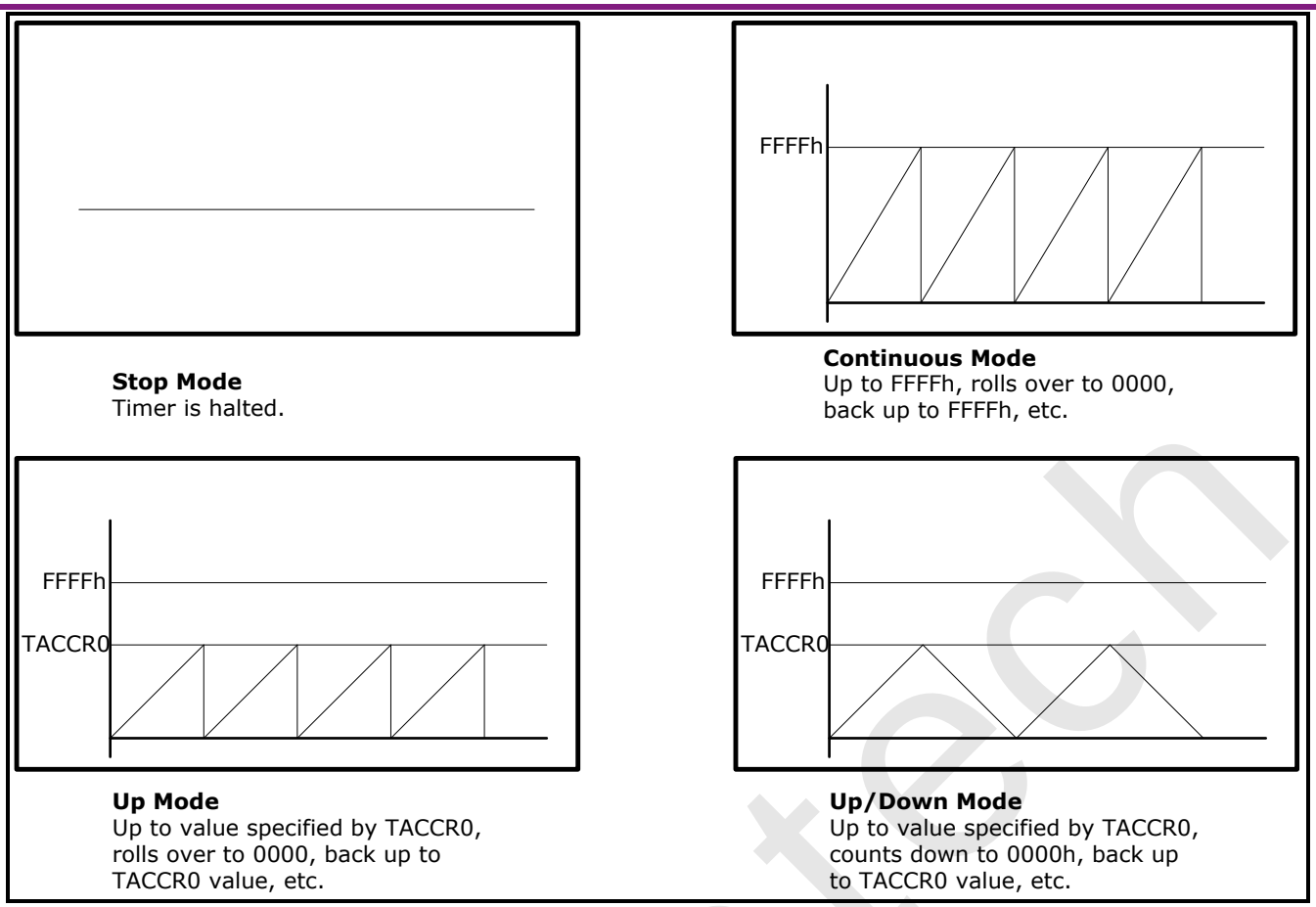


Figure 12-2 Operation Modes for TimerA

When either bit MC1 or MC0 is not cleared, or the clock source is active, the timer starts counting. In Up or Up/Down Mode, when the register TACCR0 is cleared, the timer stops running, and it may then be restarted counting in the up direction from zero when a non-zero value is written into the register TACCR0.

In Up Mode, when the value of the register TACCR0 is changed while the timer is running,

- if the new value is not less than the former value or current counts, the timer will count up to the new TACCR0 value, and then rolls over to 0000h;
- if the new value is less than current counts, the timer will count to the former value firstly, rolls over to 0000h, and then counts to the new TACCR0 value.

In Up/Down Mode,

- when the value of the register TACCR0 is changed while the timer is counting in the down direction, the timer continues its direction until it counts down to 0000h, and then it counts up to the new value of TACCR0 from 0000h;
- when the value of the register TACCR0 is changed while the timer is counting in the up direction:
  - if the new value is not less than the former value or current counts, the timer counts up to the new TACCR0 value before counting down;
  - if the new value is less than current counts, the timer will count to the former value firstly, counts back to 0000h, and then counts up to the new TACCR0 value.

In Continuous Mode, the output frequency is configurable, as illustrated in the following figure. This operation mode can be used to generate independent output frequencies.

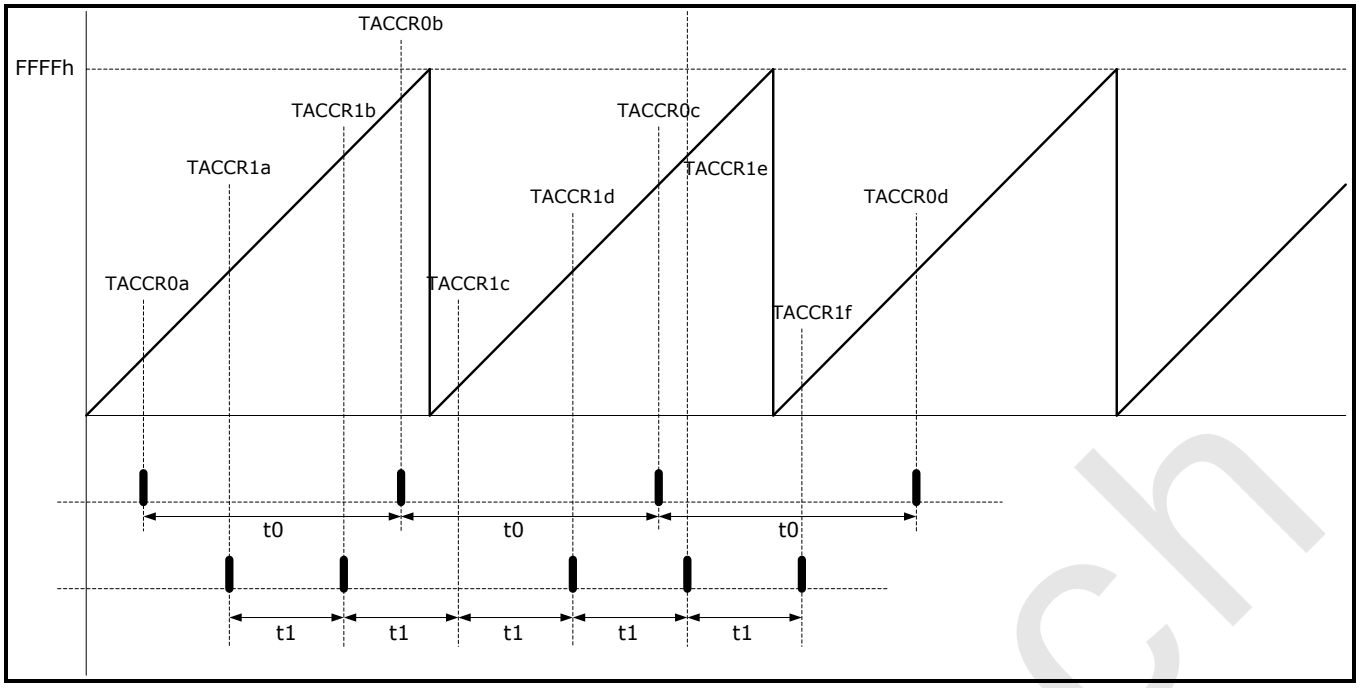


Figure 12-3 Configuring Output Frequency in Continuous Mode

As illustrated in the above figure, TACCR0a and TACCR1a are the values of the registers TACCR0 and TACCR1 at the moment of Ta0 and Ta1, and TACCR0b and TACCR1b are the values of the registers TACCR0 and TACCR1 at the moment of Tb0 (Tb0=Ta0+t0) and Tb1 (Tb1=Ta1+t1), and so forth. When the interrupt is enabled (CCIE=1, Bit4, TACCTLx), an interrupt will be generated at the moment of Ta0 and Ta1 independently and at an interval (t0 or t1). The interrupt flags CCIFG (Bit0 of TACCTLx, x=0 and 1) are set bit respectively. Up to 3 independent output frequencies can be generated using all capture/compare registers. In this application, when the timer rolls over to 0000h from FFFFh, the bit TAIFG is still set.

Table 12-4 Timer A Compare/Capture Control Registers (0x2904~0x2909)

<table>
<tr><th colspan="5">0x2904~0x2905/0x2906~0x2907/0x2908~0x2909, R/W, TimerA Compare/Capture Control Register x[2], TACCTLx~TACCTHx</th></tr>
<tr><th>Byte</th><th colspan="2">Bit</th><th>Default</th><th>Description</th></tr>
<tr><td rowspan="4">High byte
TACCTHx
0x2905
0x2907
0x2909</td><td>Bit15</td><td>CM1</td><td rowspan="2">0</td><td rowspan="2">To select the capture mode.
CM1 CM0 Description
0 0 To disable capture mode.
0 1 To capture signals on the rising edge.
1 0 To capture signals on the falling edge.
1 1 To capture signals on both edges.</td></tr>
<tr><td>Bit14</td><td>CM0</td></tr>
<tr><td>Bit[13:11]</td><td>Reserved</td><td>0</td><td>Read only.</td></tr>
<tr><td>Bit10</td><td>SCCI</td><td>0</td><td>To latch the input signal (determined by bits CCISx) with the EQUx signal, and read it via the bit CCI.</td></tr>
</table>

[2] x can be equal to 0/1/2 to represent the TimerA Capture/Compare Module 0/1/2 control register.

0x2904~0x2905/0x2906~0x2907/0x2908~0x2909, R/W, TimerA Compare/Capture Control Register x², TACCTLx~TACCTHx

<table>
<tr><th>Byte</th><th colspan="2">Bit</th><th>Default</th><th colspan="5">Description</th></tr>
<tr><td></td><td></td><td></td><td></td><td colspan="5">Note: when the value of TAR is equal to the value of TACCRx, TimerA output the EQUx signal, of which x can be 0, 1 or 2.</td></tr>
<tr><td></td><td>Bit9</td><td>Reserved</td><td>0</td><td colspan="5">Read-only. This bit is read out as 0 all the time.</td></tr>
<tr><td></td><td>Bit8</td><td>CAP</td><td>0</td><td colspan="5">To select capture or compare mode.
0: Compare Mode;
1: Capture Mode.</td></tr>
<tr><td rowspan="6">Low byte
TACCTLx
0x2904
0x2906
0x2908</td><td>Bit7</td><td>OUTMOD2</td><td rowspan="6">0</td><td colspan="5" rowspan="2">To select the output mode, see figure Output on Pin TA1 in Up Mode for description of the pulse output.</td></tr>
<tr><td rowspan="2">Bit6</td><td rowspan="2">OUTMOD1</td></tr>
<tr><td rowspan="4">Bit5</td><td rowspan="4">OUTMOD0</td><td>Bit7</td><td>Bit6</td><td>Bit5</td><td>Mode</td><td>Description</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Output</td><td>To output the value of the bit OUT on the pin TAx.</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Set</td><td>When TAR=TACCRx (x=0~2), the output on the corresponding pin TAx is set bit. It remains the state until a reset of the timer, or until another output mode is selected.</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Toggle
Reset</td><td>When TAR= TACCRx (x=1~2), the output on the corresponding pin TAx is toggled. When TAR=TACCR0, the output on the corresponding pin TAx is reset.
And this mode is not for the output on the pin TA0.</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Set
Reset</td><td>When TAR= TACCRx (x=1~2), the output on the corresponding pin TAx is set. When TAR=TACCR0, the output on the corresponding pin TAx is reset.
This mode is not for the output on the pin TA0.</td></tr>
</table>

0x2904~0x2905/0x2906~0x2907/0x2908~0x2909, R/W, TimerA Compare/Capture Control Register x², TACCTLx~TACCTHx

Byte	Bit		Default	Description				
				1	0	0	Toggle	When TAR= TACCRx (x=0~2), the output on the corresponding pin TAx is toggled.
				1	0	1	Reset	When TAR= TACCRx (x=0~2), the output on the corresponding pin TAx is reset. It remains reset until another output mode is selected.
				1	1	0	Toggle Set	When TAR= TACCRx (x=1~2), the output on the corresponding pin TAx is toggled. When TAR=TACCR0, the output on the corresponding pin TAx is set. This mode is not for the output on the pin TA0.
				1	1	1	Reset Set	When TAR= TACCRx (x=1~2), the output on the corresponding pin TAx is reset. When TAR=TACCR0, the output on the corresponding pin TAx is set. This mode is not for the output on the pin TA0.
	Bit4	CCIE	0	Interrupt enable bit, to enable TimerA compare/capture interrupt. 0: disable; 1: enable.				
	Bit3	CCI	0	To read the captured input signal (via configuring the bits CCIS1/CCIS0).				
	Bit2	OUT	0	When the bits OUTMOD2, OUTMOD1 and OUTMOD0 are cleared, the value of this is output on the pins TAx (x=0~2).				
	Bit1	COV	0	Capture overflow flag.				

0x2904~0x2905/0x2906~0x2907/0x2908~0x2909, R/W, TimerA Compare/Capture Control Register x², TACCTLx~TACCTHx				
Byte	**Bit**		**Default**	**Description**
				In capture mode, when COV is read out as 0, the capture signal is reset, and the capture event cannot set this bit to 1. In capture mode, when COV is read out as 1, if a capture event occurs when the value of the last capture has not been read out, COV is set bit. This bit must be reset by program. Reading the captured signal cannot reset this bit.
	Bit0	CCIFG	0	Compare / capture interrupt flag. In capture mode: when the value of the register TAR is captured into the registers TACCR0/1/2, this flag bit will be set bit. In compare mode: when the value of the register TAR is equal to that of the registers TACCR0/1/2 (EQUx signal), this flag bit will be set bit. In Compare/Capture Module 0, when the interrupt request is responded, this flag bit will be reset automatically. In Compare/Capture Module 1/2, when the interrupt request is responded, the CCIFG flag is reset; if the corresponding enable bit is cleared, this flag bit still will be set bit, which must be cleared by program, but no interrupt will be generated.

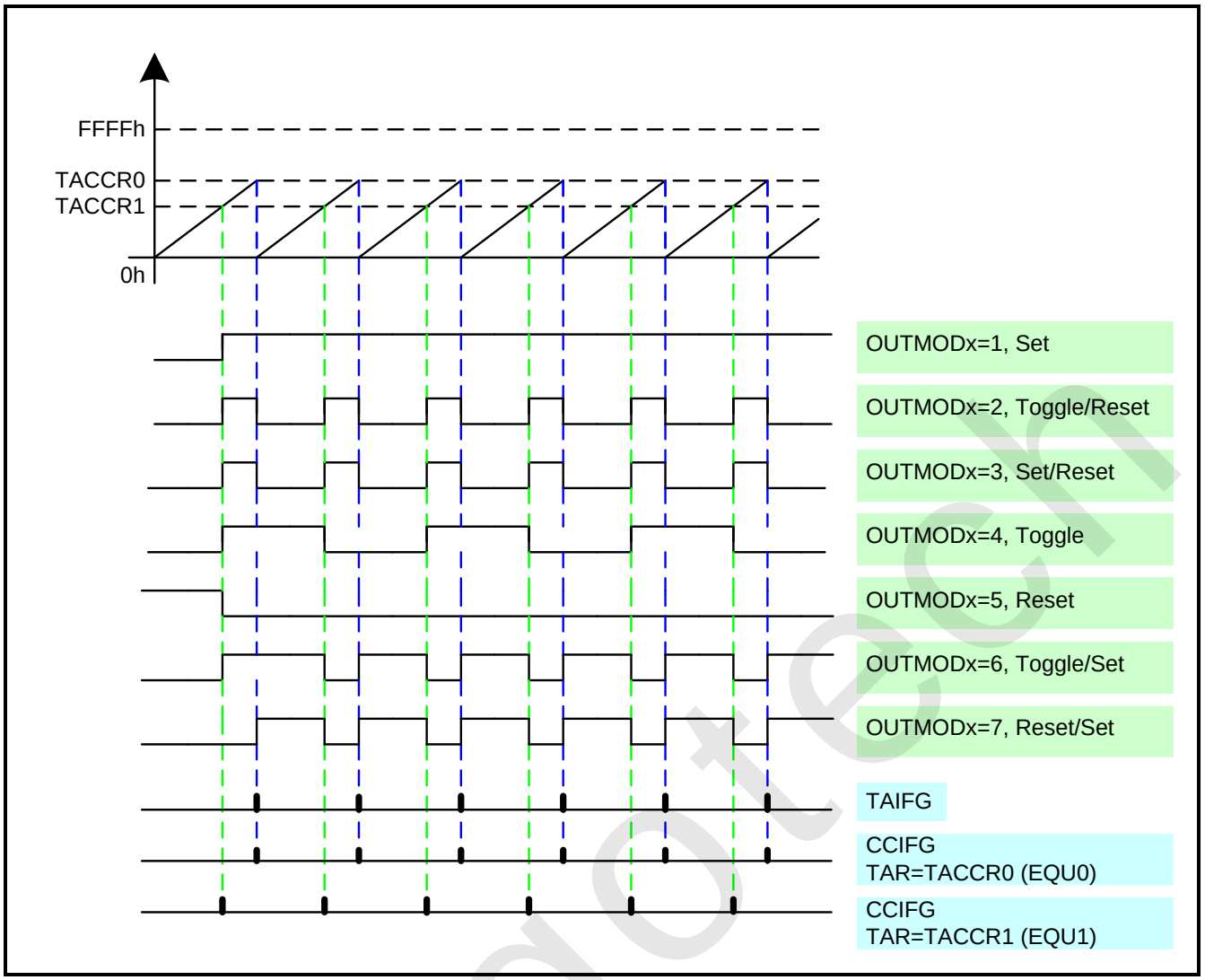


Figure 12-4 Output on Pin TA1 in Up Mode

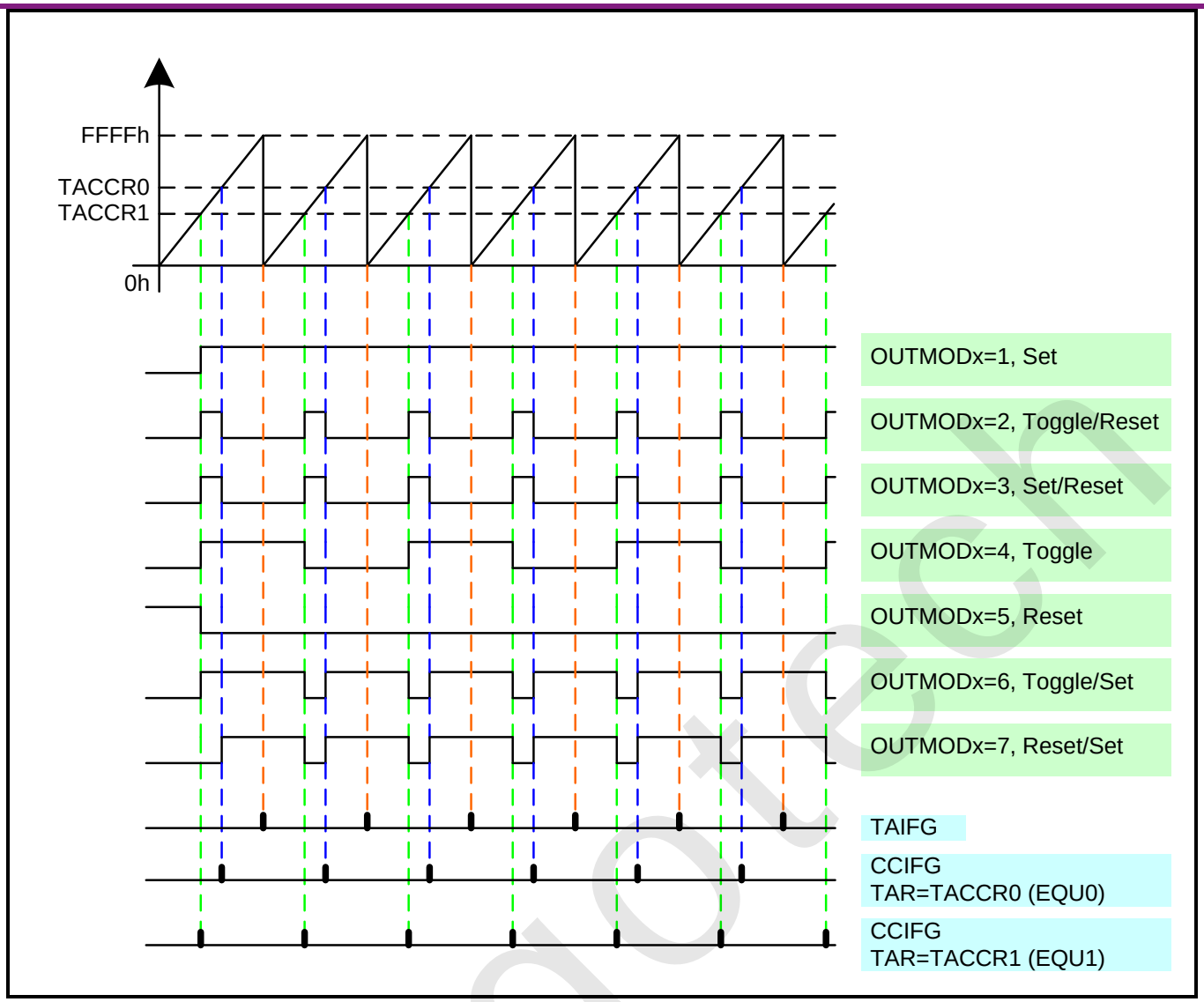


Figure 12-5 Output on Pin TA1 in Continuous Mode

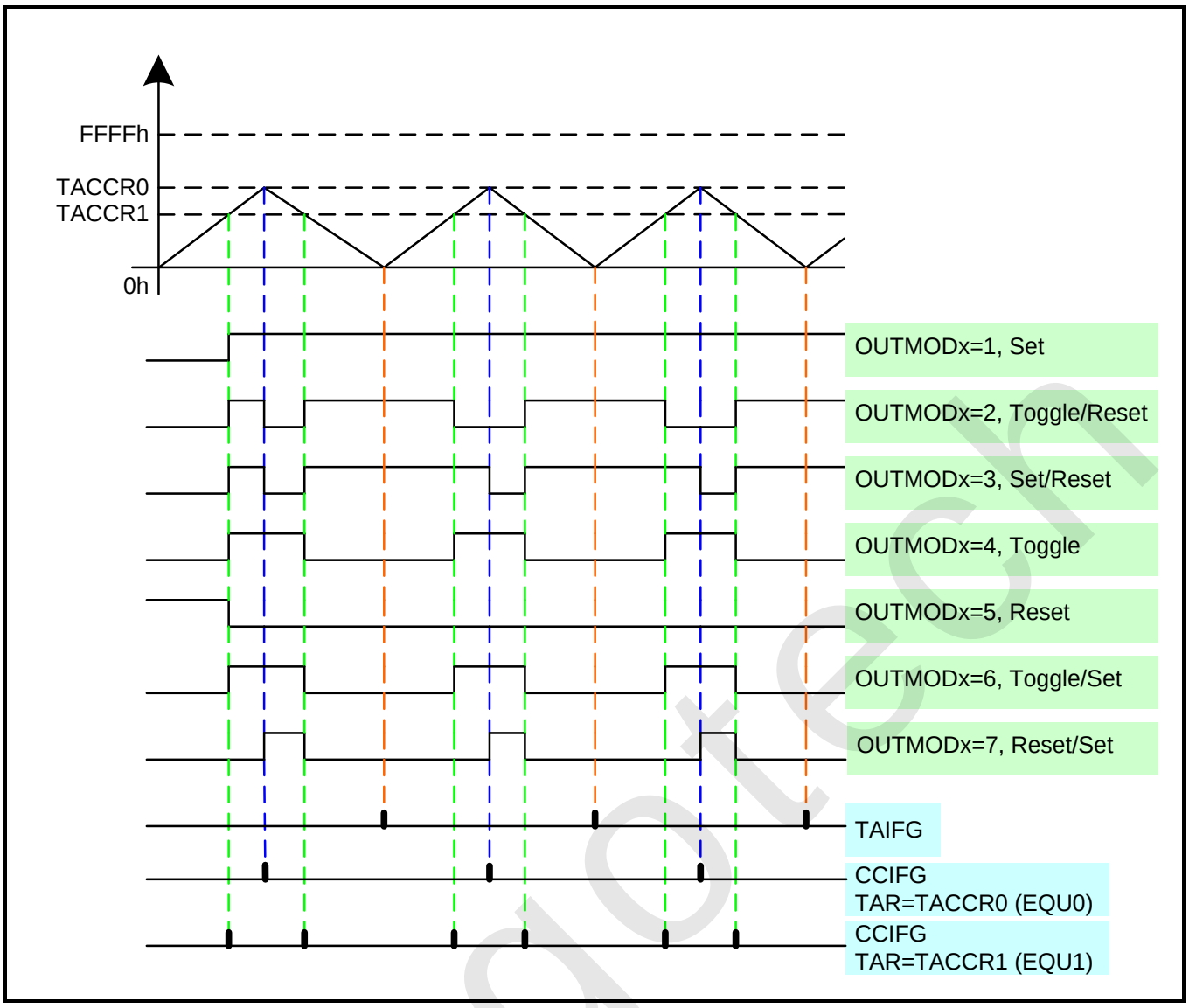


Figure 12-6 Output on Pin TA1 in Up/Down Mode

As illustrated in the above figures, users can configure the bits OUTMOD2, OUTMOD1 and OUTMOD0 to select the output mode. When these bits are set to 0b010/011/100/110/111, the frequency and duty cycle of the output pulse changes, generating PWM signals (pulse width modulation).

12.1.2. Timer0/Timer1/Timer2

12.1.2.1. Timer Rate Control

When the bits in CKCON (SFR 0x8E), CKCON.5, CKCON.4 and CKCON.3, are set bit, the associated timers increment by ones every clock cycle (clk). When they are cleared, the associated timers increment by ones every 12 clock cycles (clk/12). The timers are independent of each other. By default the above three bits are cleared.

Table 12-5 Bit Description of CKCON (SFR 0x8E)

Bit	Description

Bit	Description
CKCON.5	T2M – to select the clock source for Timer2. When T2M = 0, clk/12 is used; when T2M = 1, clk is used.
CKCON.4	T1M – to select the clock source for Timer1. When T1M = 0, clk/12 is used; when T1M = 1, clk is used.
CKCON.3	T0M – to select the clock source for Timer0. When T0M = 0, clk/12 is used; when T0M = 1, clk is used.

12.1.2.2. Timer0/Timer1

Timer0 and Timer1 are two of three embedded timers of 8052 microcontroller. Both timers can act as a timer to count the MCU clock frequency, or act as a counter to count the input signals. Furthermore, Timer1 also can act as a baud rate generator of UART1 for serial communication.

There are 4 operation modes for Timer0 and Timer1. They are determined by TMOD (SFR 0x89) and TCON (SFR 0x88). The four modes are:

- 13-bit timer/counter (Mode 0).
- 16-bit timer/counter (Mode 1).
- 8-bit timer/counter in auto-reload mode (Mode 2).
- Split timer/counter mode (Mode 3, only for Timer0).

The SFRs associated with Timer0/Timer1 are:

- TL0 (SFR 0x8A) and TH0 (SFR 0x8C), the lower byte and higher byte of Timer0.
- TL1 (SFR 0x8B) and TH1 (SFR 0x8D), the lower byte and higher byte of Timer1.

Table 12-6 Timer0/1 Mode Control Special Function Register (TMOD, SFR 0x89)

Bit		Description
Bit7 TMOD.7	GATE	Timer1 gate control bit. If the bit TR1 (TCON.6) is set bit and the signal on the pin INT1 is high, Timer1 runs when this bit is set to 1. If this bit is cleared, Timer1 runs when TR1 is set to 1, regardless of the state of the pin INT1.
Bit6 TMOD.6	C/T	When this bit is cleared, Timer1 acts as a timer to count the clock pulse (clk or clk/12, depending on the bit T1M, CKCON.4). When this bit is set bit, Timer1 acts as a counter driven by the input signal on the pin T1 and counts the 1-0 transitions of the input signal.

Bit		Description
Bit5 TMOD.5	M1	To determine the operation mode for Timer1. M1 M0 Mode 0 0 Mode 0: 13-bit timer/counter. 0 1 Mode 1: 16-bit timer/counter. 1 0 Mode 2: 8-bit timer/counter in auto-reload mode. 1 1 Mode 3: Split timer/counter.
Bit4 TMOD.4	M0	
Bit3 TMOD.3	GATE	Timer0 gate control bit. If the bit TR0 (TCON.4) is set bit and the signal on the pin INT0 is high, Timer0 runs when this bit is set bit. If this bit is cleared, Timer0 runs when TR0 is set bit, regardless of the state of the pin INT0.
Bit2 TMOD.2	C/T	Timer or counter select bit. When this bit is cleared, Timer0 acts as a timer to count the clock pulse (clk or clk/12, depending on the bit T0M, CKCON.3). When this bit is set bit, Timer0 acts as a counter driven by the input signal on the pin T0 and counts the 1-0 transitions of the input signal.
Bit1 TMOD.1	M1	M1 M0 Mode 0 0 Mode 0: 13-bit timer/counter. 0 1 Mode 1: 16-bit timer/counter. 1 0 Mode 2: 8-bit timer/counter in auto-reload mode. 1 1 Mode 3: Split timer/counter mode.
Bit0 TMOD.0	M0	

Table 12-7 Timer0/1 Control Special Function Register (TCON, SFR 0x88)

Bit		Description
Bit7 TCON.7	TF1	Timer 1 overflow flag. It is set bit when Timer1 overflows. It is cleared when the processor vectors to execute interrupt service routine located at program address 0x001B ("Interrupt Resources").
Bit6 TCON.6	TR1	Timer1 run control bit. Set this bit to 1 to enable Timer1 to run.
Bit5 TCON.5	TF0	Timer0 overflow flag. It is set bit when Timer0 overflows. It is cleared when the processor vectors to execute interrupt service routine located at program address 0x000B ("Interrupt Resources").
Bit4 TCON.4	TR0	Timer0 run control bit. Set this bit to 1 to enable Timer0 to run.

Bit		Description
Bit3 TCON.3	IE1	IO Interrupt 1 edge flag. If IO Interrupt 1 is configured to be edge-sensitive (IT1 is set bit), IE1 is set bit when a 1-to-0 transition is detected on the input signal on the pin INT1, but automatically cleared when the processor vectors to execute the corresponding interrupt service routine located at program address 0x0013 ("Interrupt Resources"). In edge-sensitive mode, IE1 also can be cleared by program. If IO Interrupt 1 is configured to be level-sensitive (IT1 is cleared), IE1 is set bit when the level on the pin INT1 is low, but cleared when the level on the pin INT1 is high. In level-sensitive mode, the program cannot write of IE1.
Bit2 TCON.2	IT1	IO Interrupt 1 signal type control bit. When IT1 is set bit, IO Interrupt 1 is triggered when a 1-to-0 transition of the input signal is detected on the pin INT1. When IT1 is cleared, IO Interrupt 1 is triggered when a low level input signal is detected on the pin INT1.
Bit1 TCON.1	IE0	IO Interrupt 0 edge flag. If IO Interrupt 0 is configured to be edge-sensitive (IT0 is set to 1), IE0 is set bit when a 1-to-0 transition is detected on the input signal on the pin INT0, but is automatically cleared when the processor vectors to execute the corresponding interrupt service routine located at program address 0x0003 ("Interrupt Resources"). In edge-sensitive mode, IE0 also can be cleared by program. If IO Interrupt 0 is configured to be level-sensitive (IT0 is cleared), IE0 is set bit when the level on the pin INT0 is low, but cleared when the level on the pin INT0 is high. In level-sensitive mode, the program cannot write of IE0.
Bit0 TCON.0	IT0	IO Interrupt 0 signal type control bit. When IT0 is set bit, IO Interrupt 0 is triggered when a 1-to-0 transition of the input signal is detected on the pin INT0. When IT0 is cleared, IO Interrupt 0 is triggered when a low level input signal is detected on the pin INT0.

12.1.2.2.1. Timer0/1, Mode 0

In Mode 0, Timer0 and Timer1 act as a 13-bit timer/counter. In this mode, the lower byte of Timer0/Timer1 (TLx, SFR 0x8A or SFR 0x8B) counts from 0 to 31. When it increments from 31, TLx SFR (x=0~1) is cleared, and the higher byte of the timer (THx, SFR 0x8C or SFR 0x8D) increments by 1. In this mode, only 13 bits of Timer0/Timer1, Bit0~Bit4 of TLx SFR and all 8 bits of THx SFR, are active. The upper three bits of TLx SFR are indeterminate in Mode 0 and must be masked when the software evaluates the register.

Users can configure the bit (TR0 or TR1, Bit4 or Bit6 of TCON SFR) to run Timer0 or Timer1. In the V98XX, according to the value of the bit C/T (Bit6 or Bit2 of TMOD SFR), Timer0 or Timer1 can act as a timer or a counter.

When the bit GATE (Bit7 or Bit3 of TMOD SFR) is cleared or set bit, and the input signal on the pin INT0 or INT1 is active, Timer0 or Timer1 runs when TRx (x=0~1, TCON.4 or TCON.6) is set bit.

When the 13-bit timer increments from 0x1FFF, it rolls over to all zeros, and then the bit TF0 (TCON.5) or TF1 (TCON.7) is set bit, and an interrupt is generated to CPU.

12.1.2.2.2. Timer0/1, Mode 1

In Mode 1, Timer0 and Timer1 act as 16-bit timers/counters. In this mode, all eight bits of the lower byte of the timers, TL0 (SFR 0x8A) or TL1 (SFR 0x8B), are active, so, TLx SFR increments from 0 to 255. When the TLx SFR increments from 255, it is cleared, and the higher byte of the timer, THx SFR (TH0 SFR or TH1 SFR), increments by 1. The timer will roll over to all zeros when the timer/counter increments from 0xFFFF.

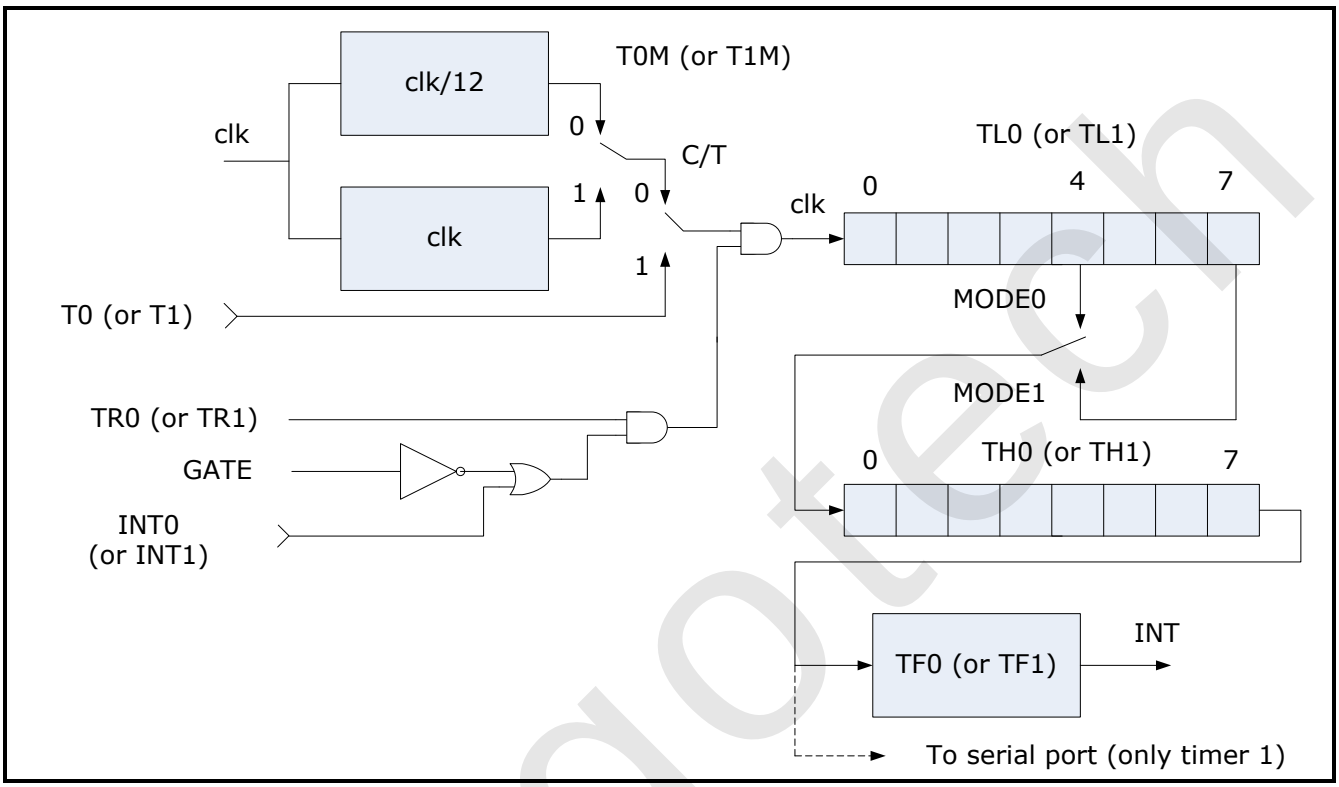


Figure 12-7 Timer 0/1, Mode 0/1

12.1.2.2.3. Timer0/1, Mode 2

In Mode 2, only the lower byte of Timer0/Timer1 (TLx SFR, x=0~1) acts as an 8-bit timer/counter, while the higher byte of it (THx SFR, x=0~1) holds a value that will be loaded into TLx SFR every time TLx SFR overflows. When the value is loaded into the TLx SFR, the timer will increment from the loaded value.

For example, TH1 SFR is set to 200, and when TL1 SFR increments from 255, it rolls to 200, and recounts from 200 to 255, and then to 200, and repeats.

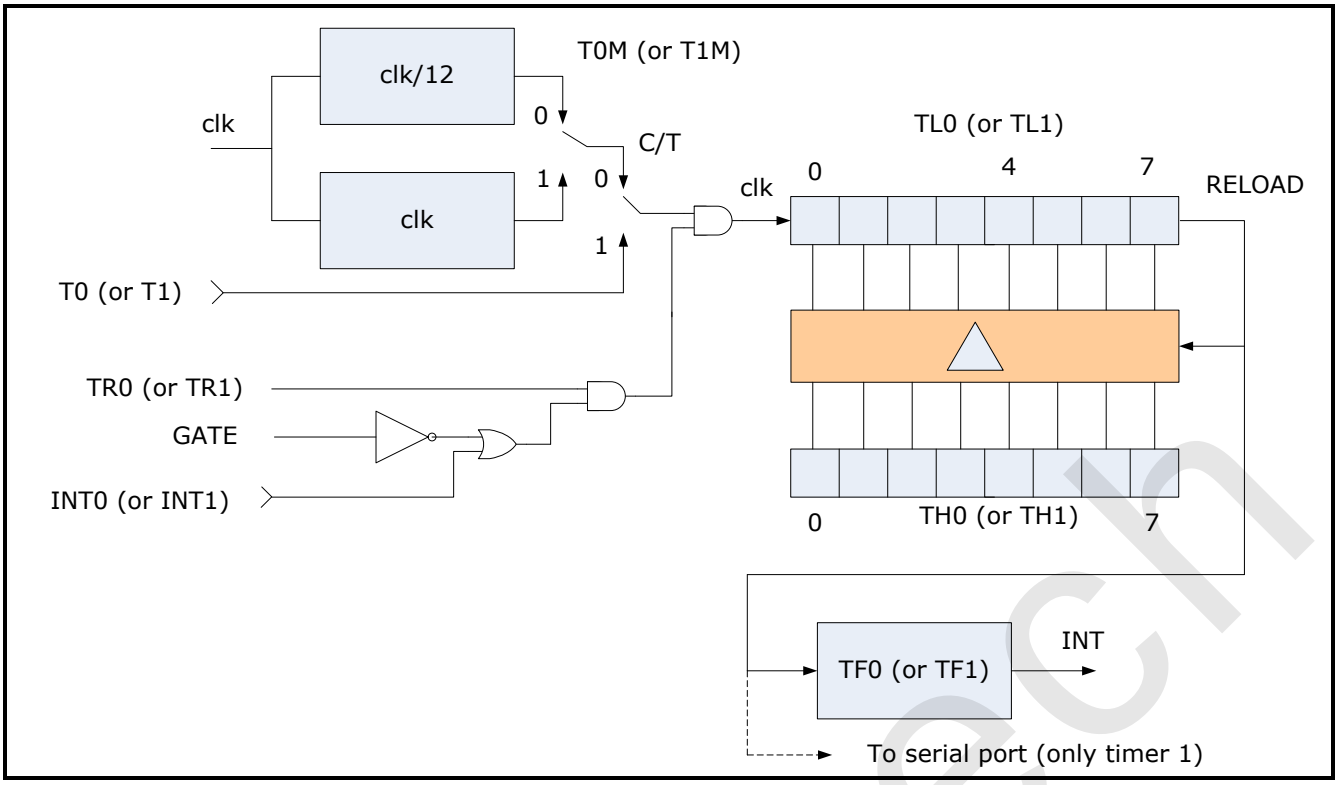


Figure 12-8 Timer 0/1, Mode 2

12.1.2.2.4. Timer0/1, Mode 3

In Mode 3, Timer0 becomes two completely separate 8-bit timers/counters. When Timer0 is set to work in this mode, TR0 (TCON.4) and TF0 (TCON.5) are used by TL0 SFR, but TR1 (TCON.6) and TF1 (TCON.7) are used by TH0 SFR, so Timer1 stops running as a general timer but still can be used as a baud rate generator.

When Timer0 works in Mode3, Timer1 still can be enabled via configuring its operation mode to Mode 0/1/2, but no interrupt will be generated by it, because the flag TF1 is used by Timer0. When Timer1 is configured to work in Mode 3, it stops running, but holds its counts.

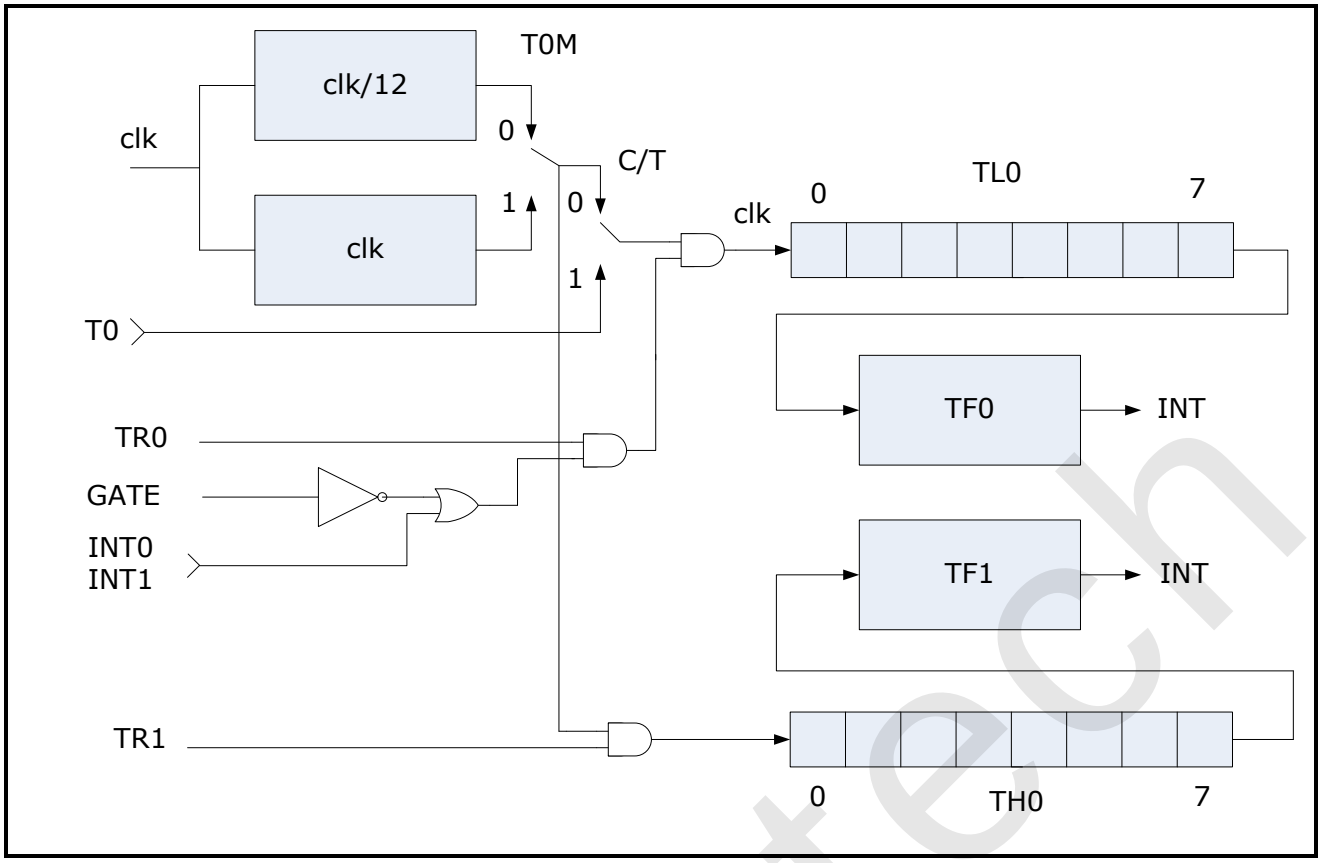


Figure 12-9 Timer 0, Mode 3

12.1.2.3. Timer2

Besides Timer0 and Timer1, there is a third timer, Timer2, in 8052 microcontroller, a 16-bit timer, has a number of new functions. The modes for Timer2 are:

- 16-bit timer/counter.
- 16-bit timer/counter in capture mode.
- 16-bit timer/counter in auto-reload mode.

The SFRs associated with Timer 2 are:

- T2CON (SFR 0xC8).
- TL2 (SFR 0xCC) – Lower byte of Timer2.
- TH2 (SFR 0xCD) – Higher byte of Timer2.
- RCAP2L (SFR 0xCA) – To capture the value of TL2 SFR when Timer 2 is configured in capture mode, or, to hold the lower byte of the loaded value when Timer 2 is configured in auto-reload mode.
- RCAP2H (SFR 0xCB) –To capture the value of TH2 SFR when Timer 2 is configured in capture mode, or, to hold the higher byte of the loaded value when Timer 2 is configured in auto-reload mode.

Table 12-8 Timer2 Control Special Function Register (T2CON, SFR 0xC8)

Bit		Description
Bit7 T2CON.7	TF2	Timer2 overflow flag. The bit TF2 is set bit when Timer2 overflows from FFFFh. TF2 must be cleared by the program. Only when both RCLK and TCLK are cleared, TF2 will be set bit. Writing 1 to TF2 can force the Timer2 interrupt if it is enabled.
Bit6 T2CON.6	EXF2	Timer2 external interrupt flag. When EXEN2 is set bit, EXF2 will be set bit when a 1-to-0 transition of the input signal on the pin T2EX is detected, which can trigger an auto-reload or capture event. EXF2 must be cleared by the program. Writing 1 to EXF2 can force the Timer 2 external interrupt if it is enabled.
Bit5 T2CON.5	RCLK	Reserved. By default it is 0.
Bit4 T2CON.4	TCLK	Reserved. By default it is 0.
Bit3 T2CON.3	EXEN2	Timer2 external interrupt enable bit. When EXEN2 is set bit, an auto-reload or capture event will be triggered when a 1-to-0 transition of the input signal on the pin T2EX is detected. When EXEN2 is cleared, no interrupt will be generated whatever the input signal on the pin T2EX is.
Bit2 T2CON.2	TR2	Timer2 run control flag. 1: Timer2 runs. 0: Timer2 stops.
Bit1 T2CON.1	C/T2	Timer or counter select bit. When C/T2 is cleared, Timer2 acts as a timer to count the clock pulses (clk or clk/12, depending on the bit T2M, CKCON.5). When C/T2 is set bit, Timer2 acts as a counter driven by the input signal on the pin T2 and counts the 1-to-0 transitions of the input signals.
Bit0 T2CON.0	CP/RL2	Capture/reload flag. When CP/RL2 and EXEN2 are set bit, the current counts will be captured into the registers RCAP2L SFR and RCAP2H SFR when a 1-to-0 transition of the input signal on the pin T2EX is detected. When CP/RL2 is cleared, but EXEN2 is set bit, an auto-reload event will occur when a 1-to-0 transition of the input signal on the pin T2EX is detected. If either RCLK or TCLK is set bit, CP/RL2 cannot work, and Timer2 can operate in auto-reload mode on overflow.

Table 12-9 Timer 2 Mode

RCLK	TCLK	CP/RL2	TR2	Mode

RCLK	TCLK	CP/RL2	TR2	Mode
0	0	1	1	16-bit timer/counter in capture mode.
0	0	0	1	16-bit timer/counter in auto-reload mode.
1	X	X	1	Reserved.
X	1	X	1	Reserved.
X	X	X	0	Stop working

12.1.2.3.1. Timer2, 16-Bit Timer/Counter Mode

In this mode, users can configure the register T2CON SFR to enable Timer2 to act as a 16-bit timer or a 16-bit counter (C/T2, T2CON.1), and to enable Timer2 to run (TR2, T2CON.2). In this mode, Timer2 increments from 0000h to FFFFh, and then rolls over to all zeros, setting the flag TF2 (T2CON.7) to 1, which generate an interrupt to CPU.

12.1.2.3.2. Timer2, 16-Bit Timer/Counter in Capture Mode

When CP/RL2 (T2CON.0) and EXEN2 (T2CON.3) are set bit, the values of TH2 SFR and TL2 SFR are captured and loaded into the registers RCAP2L SFR and RCAP2H SFR when a 1-to-0 transition of the input signal on the pin T2EX is detected. At the same time, the flag EXF2 (T2CON.6) is set bit, which will generate an interrupt to the processor if it is enabled.

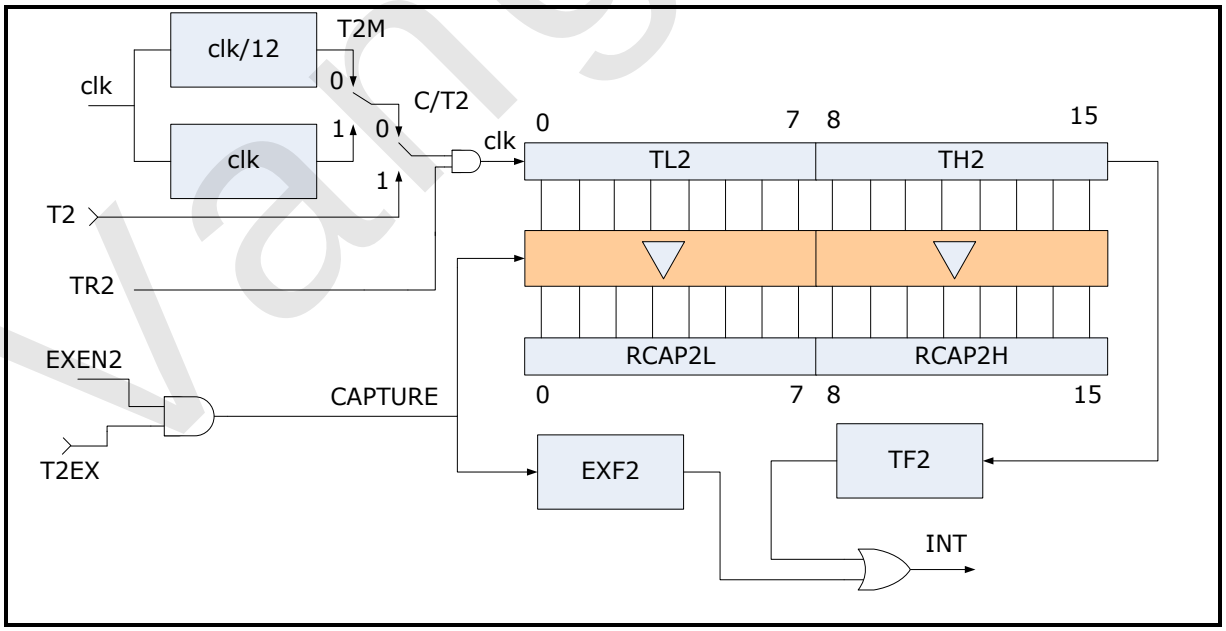


Figure 12-10 Timer2, 16-bit Timer/ Counter in Capture Mode

12.1.2.3.3. Timer2, 16-Bit Timer/Counter in Auto-Reload Mode

When CP/RL2 (T2CON.0) is cleared, Timer2 acts as a 16-bit counter/timer in auto-reload mode.

In this mode, the CPU must write the reload value to the registers RCAP2L (SFR 0xCA) and RCAP2H (SFR 0xCB). When the timer increments from FFFFh, the value stored in RCAP2L will be reloaded into the register TL2 (SFR 0xCC), and the value stored in RCAP2H will be reloaded into the register TH2 (SFR 0xCD), at the same time, TF2 is set bit, which will generate an interrupt to the processor if it is enabled.

When CP/RL2 is cleared, but EXEN2 (T2CON.3) is set bit, an auto-reload event occurs when a 1-to-0 transition of the input signal on the pin T2EX is detected, at the same time, the flag EXF2 (T2CON.6) is set bit, which will generate an external interrupt to the processor if it is enabled.

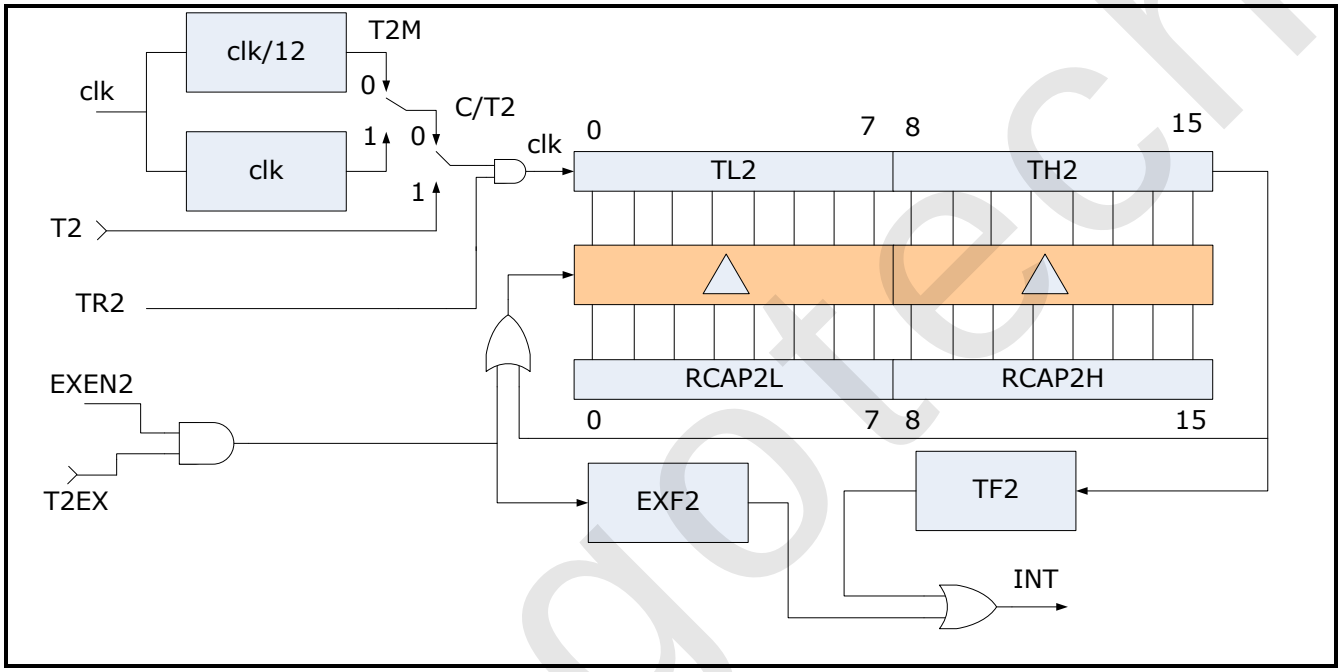


Figure 12-11 Timer2, 16-Bit Timer/Counter in Auto-Reload Mode

12.2. UART

In V98XX, there are 5 active UART serial interfaces on the chip, including UART1 of 8052 microcontroller and the extended UART2 /UART3/UART4/ UART5 serial interfaces. Bits UART2 (bit4)/ UART3(bit5), UART4(bit6) and UART5(bit7) (bit4~bit7 of PRCtrl1, 0x2D01) gate controls the corresponding UART serial interfaces.

The UART serial interfaces can work in 4 modes. In Mode 0, the serial interface can only receive data on the RXD port and output shifting clock on the TXD port. In other modes, the extended UART serial interfaces can work like UART1 serial interfaces of 8052 microcontroller.

It is recommended to use extended UART interfaces for serial communication.

12.2.1. UART1

UART1 uses Timer1 to generate baud rate, and the bit SMOD1 (EICON.7) controls doubling the baud

rate of UART1.

The SFRs associated with UART1 are:

- SCON1 (SFR 0xC0) – UART1 Control Register.
- SBUF1 (SFR 0xC1) – UART1 Buffer Register.

Table 12-10 UART1 Control Special Function Register (SCON1, SFR 0xC0)

Bit		Description
Bit7 SCON1.7	SM0_1	To determine the mode for UART1. SM0_1 SM1_1 Mode 0 0 0: 8-bit shift register; baud rate=clk or clk/12. 0 1 1: 8-bit UART; baud rate, determined by Timer1. 1 0 2: 9-bit UART; baud rate = clk/32 or clk/64. 1 1 3: 9-bit UART; baud rate, determined by Timer1.
Bit6 SCON1.6	SM1_1	
Bit5 SCON1.5	SM2_1	Multiprocessor communication enable bit. In Mode2 and Mode3, SM2_1 enables the multiprocessor communication. In Mode2 and Mode3, when SM2_1 is set bit, RI_1 cannot be set bit in case that the received 9th bit is 0. In Mode1, when SM2_1 is set bit, RI_1 will be set bit only if a valid stop bit is received. In Mode0, SM2_1 establishes the baud rate: when SM2_1 is cleared, the baud rate is clk/12; when SM2_1 is set to 1, the baud rate is clk.
Bit4 SCON1.4	REN_1	Receive enable bit. When REN_1 is set bit, data reception is enabled.
Bit3 SCON1.3	TB8_1	To define the 9th bit to be transmitted in Mode2 or Mode3.
Bit2 SCON1.2	RB8_1	In Mode2 and Mode3, RB8_1 is to store the received 9th bit. In Mode1, the stop bit is stored as the RB8_1. In Mode0, RB8_1 is not used.
Bit1 SCON1.1	TI_1	Transmit interrupt flag. If this bit is set bit, it indicates that the transmit data has been shifted out. In Mode0, TI_1 is set bit at the end of the 8th bit. In other modes, TI_1 is set bit when the stop bit is placed on the pin TXD1. TI_1 must be cleared by the program.
Bit0 SCON1.0	RI_1	Receive interrupt flag. If this bit is set bit, it indicates that a serial data has been received. In Mode 0, RI_1 is set bit at the end of the 8th data bit. In Mode1, according to the state of SM2_1, RI_1 is set bit after the last sample of the incoming stop bit. In Mode2 and Mode3, RI_1 is set bit at the end of the last sample of the 9th bit. RI_1 must be cleared by the program.

12.2.2. Extended UART Serial Interfaces

All the extended UART serial interfaces have the same architecture, but only UART2 has an optional 38-kHz carrier wave modulator.

In each extended UART serial interface, there are a general timer (compatible with Timer0) and a baud rate generator (compatible with Timer1). The overflow of general timer can set a flag bit which will be cleared by executing interrupt service routine (ISR) or by polling interrupt sources, and generate an interrupt to the CPU. When the baud rate generator is used as a general timer, it can set the related overflow flag to 1, but cannot generate an overflow interrupt. As an extended peripheral, there is a specific control/status register for each UART interface, which can control the baud rate, select the clock sources for the timers, disable or enable the timers, and show the overflow state of the timers.

12.2.2.1. Registers

Table 12-11 Extended UART Serial Interfaces Registers

0x2820, R/W	TCON2, UART2 Control / Status Register
0x2821, R/W	TMOD2, UART2 Timers Mode Control Register
0x2822, R/W	TH20, Higher Byte of General Timer of UART2
0x2823, R/W	TH21, Higher Byte of Baud Rate Generator of UART2
0x2824, R/W	TL20, Lower Byte of General Timer of UART2
0x2825, R/W	TL21, Lower Byte of Baud Rate Generator of UART2
0x2826, R/W	SCON2, UART2 Control Register
0x2827, R/W	SBUF2, UART2 Buffer Register
0x2828, R/W(V98XX)	TCON3, UART3 Control / Status Register
0x2829, R/W(V98XX)	TMOD3, UART3 Timers Mode Control Register
0x282A, R/W(V98XX)	TH30, Higher Byte of General Timer of UART3
0x282B, R/W(V98XX)	TH31, Higher Byte of Baud Rate Generator of UART3
0x282C, R/W(V98XX)	TL30, Lower Byte of General Timer of UART3

0x282D, R/W(V98XX)	TL31, Lower Byte of Baud Rate Generator of UART3
0x282E, R/W(V98XX)	SCON3, UART3 Control Register
0x282F, R/W(V98XX)	SBUF3, UART3 Buffer Register
0x2830, R/W	TCON4, UART4 Control / Status Register
0x2831, R/W	TMOD4, UART4 Timers Mode Control Register
0x2832, R/W	TH40, Higher Byte of General Timer of UART4
0x2833, R/W	TH41, Higher Byte of Baud Rate Generator of UART4
0x2834, R/W	TL40, Lower Byte of General Timer of UART4
0x2835, R/W	TL41, Lower Byte of Baud Rate Generator of UART4
0x2836, R/W	SCON4, UART4 Control Register
0x2837, R/W	SBUF4, UART4 Buffer Register
0x2838, R/W	TCON5, UART5 Control / Status Register
0x2839, R/W	TMOD5, UART5 Timers Mode Control Register
0x283A, R/W	TH50, Higher Byte of General Timer of UART5
0x283B, R/W	TH51, Higher Byte of Baud Rate Generator of UART5
0x283C, R/W	TL50, Lower Byte of General Timer of UART5
0x283D, R/W	TL51, Lower Byte of Baud Rate Generator of UART5
0x283E, R/W	SCON5, UART5 Control Register
0x283F, R/W	SBUF5, UART5 Buffer Register

Table 12-12 UARTx Control/Status Register (TCON2/TCON3/TCON4/TCON5)

Bit		Default	Description
Bit7	SMOD	0	When this bit is set to 1, the baud rate of UARTx is doubled.
Bit6	Reserved		

Bit		Default	Description
Bit5	T1M	0	To select the clock source for the baud rate generator. 0: clk/12; 1: clk.
Bit4	T0M	0	To select the clock source for the general timer. 0: clk/12; 1: clk.
Bit3	TF1	0	Overflow flag of the baud rate generator. When an overflow occurs to the baud rate generator, this bit will be set bit, but no overflow interrupt will be generated.
Bit2	TF0	0	Overflow flag of the general timer. When an overflow occurs to the general timer, this bit will be set bit, and an overflow interrupt will be generated to CPU if the interrupt is enabled.
Bit1	TR1	0	Baud rate generator run control bit. 1: to run; 0: to stop.
Bit0	TR0	0	General timer run control bit. 1: to run; 0: to stop.

Table 12-13 UARTx Timers Mode Control Register (TMOD2/TMOD3/TMOD4/TMOD5)

Bit		Description
Bit7 TMOD2.7	GATE1	This bit must be cleared for proper operation. In this case, the baud rate generator runs when TR1 (Bit1 of TCONx) is set.
Bit6 TMOD2.6	C/T1	This bit must be cleared for proper operation. In this case, the clock source for the baud rate generator is determined by the bit T1M (bit5 of TCONx).
Bit5 TMOD2.5	T1M1	To select the mode for the baud rate generator. T1M1 T1M0 Mode 0 0 Mode0: 13-bit timer. 0 1 Mode1: 16-bit timer. 1 0 Mode2: 8-bit timer in auto-reload mode. 1 1 Mode3: Split timer mode.
Bit4 TMOD2.4	T1M0	

Bit		Description
Bit3 TMOD2.3	GATE0	This bit must be cleared for proper operation. In this case, the general timer runs when TR0 (Bit0 of TCONx) is set.
Bit2 TMOD2.2	C/T0	This bit must be cleared for proper operation. In this case, the clock source for the baud rate generator is determined by the bit T0M (bit4 of TCONx).
Bit1 TMOD2.1	T0M1	To select the mode for the general timer. T0M1 T0M0 Mode 0 0 Mode0: 13-bit timer. 0 1 Mode1: 16-bit timer. 1 0 Mode2: 8-bit timer in auto-reload mode. 1 1 Mode3: Split timer mode.
Bit0 TMOD2.0	T0M0	

Table 12-14 UARTx Control Register (SCON2/SCON3/SCON4/SCON5)

Bit		Description
Bit7 SCON2.7	SM0	To select the mode for UARTx. SM0 SM1 Mode 0 0 Mode0: 8-bit shift register; baud rate =clk or clk/12. 0 1 Mode1: 8-bit UART; baud rate, determined by the baud rate generator. 1 0 Mode2: 9-bit UART; baud rate =clk/32 or clk/64. 1 1 Mode3: 9-bit UART; baud rate, determined by the baud rate generator.
Bit6 SCON2.6	SM1	
Bit5 SCON2.5	SM2	Multiprocessor communication enable bit. In Mode2 and Mode3, SM2 enables the multiprocessor communication. In Mode2 or Mode3, when SM2 is set bit, RI cannot be set bit in case that the received 9th bit is 0. In Mode1, when SM2 is set bit, RI will be set bit only if a valid stop bit is received. In Mode0, SM2 determines the baud rate: when SM2 is cleared, the baud rate is clk/12; when SM2 is set bit, the baud rate is clk.
Bit4 SCON2.4	REN	Receive enable bit. When REN is set bit, data reception is enabled.
Bit3 SCON2.3	TB8	To define the 9th bit transmitted in Mode2 and Mode3.
Bit2 SCON2.2	RB8	In Mode2 and Mode3, RB8 stores the received 9th bit. In Mode 1, RB8 stores the received stop bit. In Mode0, RB8 is not used.

Bit		Description
Bit1 SCON2.1	TI	Transmit interrupt flag. If this flag is set bit, it indicates that the transmit data has been shifted out. In Mode0, TI is set at the end of the 8th bit. In other modes, TI is set when the stop bit is placed on the pin TXD2. TI must be cleared by the program.
Bit0 SCON2.0	RI	Receive interrupt flag. If this flag is set, it indicates that a serial data has been received. In Mode0, RI is set at the end of the 8th bit. In Mode1, according to the state of SM2, RI is set after the last sample of the incoming stop bit. In Mode2 and Mode3, RI is set at the end of the last sample of the 9th bit. RI must be cleared by the program.

Table 12-15 UARTx Buffer Register (SBUF2/SBUF3/SBUF4/SBUF5)

Register	R/W	Bit	Default	Description
SBUFx	R/W	Bit[7:0]	0	SBUFx is physically two registers. One is written only and is used to hold data to be transmitted out of the MCU via the pin TXD2. The other is read only and is used to hold received data from external sources via the pin RXD2. Both mutually exclusive registers use one address. When UARTx works in the asynchronous and full-duplex communication mode, it can be used for "read" and "write" simultaneously.

12.2.2.2. Carrier Wave Modulation on UART2

UART2 has a 38 kHz carrier wave modulator controlled by TXD2 Type Register (Txd2FS). When bit TXD2CARRY (bit0 of Txd2FS, 0x28CF) is cleared, pin TXD2 will output modulated signals. Users can write of the carrier wave generation registers to configure the carrier wave frequency and its duty cycle:

$$f_{CARR} = \frac{f_{MCU}}{CARRH + CARRL} \qquad \text{Equation 12-1}$$

$$Duty_{CARR} = \frac{CARRH}{CARRL} \qquad \text{Equation 12-2}$$

where, f_{CARR} is the carrier wave frequency; f_{MCU} is MCU clock frequency; $Duty_{CARR}$ is the duty cycle of the carrier wave; *CARRH* is the value of registers CARRHH and CARRHL; *CARRL* is the value of registers CARRLH and CARRLL.

When the level on the pin TXD2 is low, the modulated signal is output.

Table 12-16 TXD2 Type Register (Txd2FS, 0x28CF)

0x28CF, R/W, TXD2 Type Register, Txd2FS			
Bit		Default	Description
Bit[7:1]	Reserved	X	

Bit0	TXD2CARRY	0	0: with 38-kHz carrier wave; 1: without 38-kHz carrier wave.

Table 12-17 Carrier Wave Generation Registers

Register		Description	R/W	Bit	Default
0x2898	CARRHH	Higher byte of Carrier Wave Generation Register 1: Duty Cycle Control, High Pulse Duration	R/W	Bit[7:0]	0
0x2899	CARRHL	Lower byte of Carrier Wave Generation Register 1: Duty Cycle Control, High Pulse Duration	R/W	Bit[7:0]	0
0x289A	CARRLH	Higher Byte of Carrier Wave Generation Register 2: Duty Cycle Control, Low Pulse Duration	R/W	Bit[7:0]	0
0x289B	CARRLL	Lower Byte of Carrier Wave Generation Register 2: Duty Cycle Control, Low Pulse Duration	R/W	Bit[7:0]	0

12.2.2.3. UART Modes

The UART serial interfaces can work in 4 modes via configuring the mode select bits, for example, SM1 and SM2 of the register SCON2 (0x2826).

Table 12-18 UART Modes

Mode		Sync. Or Async.	Baud rate	Data	Start or Stop Bit	The 9th Bit
0	8-bit shift register	Sync.	clk or clk/12	8-bit	None	None
1	8-bit UART	Async.	Determined by baud rate generator	8-bit	1 start, 1 stop	None
2	9-bit UART	Async.	clk/32 or clk/64	9-bit	1 start, 1 stop	Parity bit
3	9-bit UART	Async.	Determined by baud rate generator	9-bit	1 start, 1 stop	Parity bit

All the UART serial interfaces have the same architecture and functions except that:

- Only UART2 has 38-kHz carrier wave with its TXD.

- UART1 uses Timer1 as its baud rate generator.

So take UART2 for an example to introduce the work modes for UART serial interfaces.

12.2.2.3.1. Mode0

In Mode0, UART2 receives data on the pin RXD2, and outputs shift clock on the pin TXD2. Data can be received as soon as the bit REN (bit4 of SCON2, 0x2826) is set bit and the bit RI (bit0 of SCON2, 0x2826) is cleared. The shift clock is activated and the UART shifts data in on each rising edge of the shift clock until eight bits have been received. The 8th bit was shifted in, and one machine cycle later, the bit RI is set bit and the reception stops until the bit RI is cleared by the program.

12.2.2.3.2. Mode1

Mode1 provides standard asynchronous and full-duplex communication. In this mode, a data frame contains ten bits: one start bit, eight bits of data, and one stop bit. When a data frame is received, the stop bit is stored in the bit RB8 (bit2 of SCON2, 0x2826). On receive and transmit operation, start with the LSB.

In Mode1, the baud rate is determined by the baud rate generator overflow frequency. UART2 uses a dedicated baud rate generator, which is compatible with Timer 1. When the baud rate generator overflows, it generates a clock which is then divided by 16 to generate the baud rate.

$$BaudRate = \frac{2^{SMODx}}{32} \times Overflow \qquad \text{Equation 12-3}$$

Where,

Overflow is the baud rate generator overflow frequency. As for UART1, Timer1 is the baud rate generator; as for the extended UART serial interfaces, the specific baud rate generator is used. SMODx, the value of the bit SMOD0/1, determines to double the baud rate or not.

Generally, the baud rate generator works in the mode of 8-bit timer with auto-reload. The reload value is stored in the register TH21 (0x2823), which makes the above equation for baud rate (clk/12 is used as the clock source):

$$BaudRate = \frac{2^{SMODx}}{32} \times \frac{clk}{12 \times (256 - TH21)} \qquad \text{Equation 12-4}$$

where, clk is the MCU clock, and TH21 is the reload value of the register TH21 (0x2823).

The bit T1M (TCON2.5) determines the clock source for the baud rate generator of UART2. When T1M is set bit, clk is used as the clock source:

$$BaudRate = \frac{2^{SMODx}}{32} \times \frac{clk}{(256 - TH21)} \qquad \text{Equation 12-5}$$

Users can obtain the value of TH21 via the equation:

$$TH21 = 256 - \frac{2^{SMODx} \times clk}{32 \times BaudRate} \qquad \text{Equation 12-6}$$

When T1M is cleared, and the baud rate is known, users can obtain the value of TH21 via the following

equation:

$$TH21 = 256 - \frac{2^{SMODx} \times clk}{384 \times BaudRate}$$ Equation 12-7

In Mode1, UART2 begins to transmit data after the program writing data into the register SBUF2 (0x2827). UART2 transmits data on the pin TXD2 in the following order: start bit, eight data bits (LSB first), stop bit. The bit TI (bit1 of SCON2, 0x2826) will be set bit two clock cycles after the stop bit is transmitted.

In Mode1, UART2 starts to receive data at the falling edge of a start bit received on the pin RXD2, when the REN (bit4 of SCON2, 0x2826) bit is set. To achieve this, every bit on the pin RXD2 should be sampled sixteen times at any baud rate. When a falling edge of a start bit is detected, the timer used to generate the receive clock is reset to synchronize with the received bits. To reject noise, the serial port detects the values of the three consecutive samples in the middle of each bit. Only more than two same values can decide the received data bit to be valid. This is especially true for the start bit. If the falling edge on the pin RXD2 is not verified by a majority decision of three consecutive samples, then the serial port stops receiving data and waits for another falling edge on RXD2.

When RI (bit0 of SCON2, 0x2826) is cleared, SM2 (bit5 of SCON2, 0x2826) is set bit, and the stop bit is 1 (if SM2 is cleared, the state of stop bit does not matter), the serial port will write the received byte to the register SBUF2 (0x2827), load the stop bit into RB8 (bit2 of SCON2, 0x2826), and set the bit RI to 1. Otherwise, the received data lose; they cannot load data into the register SBUF2 and the bit RB8; and the bit RI cannot be set bit.

12.2.2.3.3. Mode2

Mode2 provides asynchronous and full-duplex communication. In this mode, the data frame contains eleven bits: one start bit, eight data bits, one programmable 9th bit, and one stop bit.

When data bits are received or transmitted, start with LSB. As to the transmitting operation, the 9th bit is determined by the value of the bit TB8 (bit3 of SCON2, 0x2826). If the 9th bit is used as a parity bit, the value of the P bit (Bit 0 of PSW SFR) should be moved to TB8.

In Mode2, the baud rate is either clk/32 or clk/64, determined by the bit SMOD (Bit7 of TCON2, 0x2820). It can be calculated as follows:

$$BaudRate = \frac{2^{SMODx} \times clk}{64}$$ Equation 12-8

In Mode2, UART2 starts transmitting data after the software writing data into the register SBUF2 (0x2827). UART2 transmits data on the pin TXD2 in the following order: the start bit, eight data bits (LSB first), the 9th bit, then the stop bit. The bit TI (bit1 of SCON2, 0x2826) is set bit when the stop bit has been transmitted.

In Mode2, receiving data begins at the falling edge of a start bit received on the pin RXD2, when the bit REN=1 (bit4 of SCON2, 0x2826). To achieve it, every bit on the pin RXD2 should be sampled sixteen times at any baud rate. When a falling edge of a start bit is detected, the timer used to generate the receive clock is reset to synchronize with the received bits. To reject noise, the serial port detects the values of the three consecutive samples in the middle of every bit. Only more than two same values can decide the received data bit to be valid. This is especially true for the start bit. If the falling edge on the pin RXD2 is not verified by a majority decision of three consecutive samples, then the serial port stops receiving data

and waits for another falling edge on RXD2.

When RI (bit0 of SCON2) is cleared, SM2 (bit5 of SCON2) is set bit, and the stop bit is 1 (if SM2 is cleared, the state of stop bit does not matter), the serial port will write the received byte to the register SBUF2 (0x2827), load the stop bit into RB8 (bit2 of SCON2), and set the bit RI. Otherwise, the received data lose; they cannot load data into the register SBUF2 and the bit RB8; and the bit RI cannot be set bit.

12.2.2.3.4. Mode3

Mode3 provides asynchronous and full-duplex communication. In this mode, the data frame contains eleven bits: one start bit, eight data bits, one programmable 9th bit, and one stop bit. When data bits are received and transmitted, start with LSB.

In Mode3, the data is transmitted or received in the same way that in Mode2. In Mode3, the baud rate generation is identical to that in Mode1. That is, Mode3 is a combination of the communication protocol in Mode2 and the baud rate generation in Mode1.

12.2.2.3.5. Multiprocessor Communication

The multiprocessor communication is enabled in Mode2 and Mode3 when the bit SM2 (bit5 of SCON2, 0x2826) is set bit. In the multiprocessor communication mode, the received 9th bit is stored in the bit RB8 (bit2 of SCON2, 0x2826), and, after the stop bit has been received, UART2 receive interrupt is activated if RB8 is set bit.

The multiprocessor communication is used to send a block of data from a master to one slave. The master first transmits an address byte that identifies the target slave. When transmitting an address byte, the master sets the 9th bit to 1; when transmitting data bytes, the master clears the 9th bit.

When SM2 is set bit, no slave can generate an interrupt when a data byte has been received. However, all slaves can generate interrupts when an address byte is received. Every slave can examine the received address byte to determine whether it is the slave being addressed. Address decoding must be done by the program during the interrupt service routine. The slave being addressed clears the bit SM2 and prepares to receive the data bytes. The slaves that are not being addressed leave the bit SM2 set and ignore the incoming data bytes.

12.3. Enhanced UART Serial Interfaces (EUART)

Besides the above general UART serial interfaces, there are two enhanced UART serial interfaces (EUART1 and EUART2) which have features as follows:

- ISO/IEC 7816-3 compliant;
- asynchronous and half-duplex communication;
- programmable baud rate;
- re-transmitting automatically.

The EUART interface receives and transmits a data frame composed of 10 bits: 1-bit start bit (START,

low level), 8-bit data (DATA, from MSB to LSB) and 1-bit check bit (CK). When the 8-bit DATA are received and transmitted, the MSB is first. Bits EUART1 and EUART2 (bit1~bit2 of PRCtrl0, 0x2D00) gate controls the corresponding enhanced UART serial interfaces.

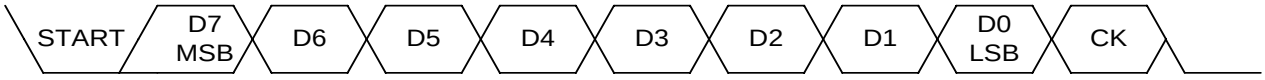


Figure 12-12 Data Frame in EUART Communication

12.3.1. Registers

In the V98XX, the EUART related registers are located at addresses 0x2A00~0x2A05 (for EUART1) and 0x2B00~0x2B05 (for EUART2).

Table 12-19 EUART Baud Rate Generators

Register			Bit	Default	Description
0x2A01 0x2B01	Lower byte of EUART1/2 baud rate generator	DIVLA DIVLB	bit[7:0] DIV<7:0>	0	See "EUART Baud Rate Generation" for details
0x2A02 0x2B02	Higher byte of EUART1/2 baud rate generator	DIVHA DIVHB	bit[7:0] DIV<15:8>	0	

Table 12-20 EUART Buffer Register (DATAA/DATAB, 0x2A03/0x2B03)

0x2A03/0x2B03, R/W, EUART1/2 Buffer Register, DATAA/DATAB		
Bit	Default	Description
bit[7:0] D<7:0>	0	The buffer register is physically two registers. One register is read-only. When an EUART receive interrupt was triggered, the read-only register holds the received data, which will be read out via reading operation of this register. When the bit OVIE (bit7 of CFGA/CFGB, 0x2A05/0x2B05) is set bit, an overflow interrupt will be triggered if another data is received when the former received data has not been read out. The other register is write-only. Writing of the write-only register will activate data transmission. Writing of this register cannot overlap the received data stored in the read-only buffer register.

Table 12-21 EUART Information Register (INFOA/INFOB, 0x2A04/0x2B04)

0x2A04/0x2B04, R/W, EUART1/2 Information Register, INFOA/INFOB		
Bit	Default	Description

0x2A04/0x2B04, R/W, EUART1/2 Information Register, INFOA/INFOB		
Bit	Default	Description
bit7 OVIF	0	Overflow interrupt flag. When another byte is received before the former one was read out, this bit will be set to 1 and an overflow interrupt will be generated to CPU.
bit6 SIF	0	Transmit interrupt flag. A transmit interrupt will be generated to CPU at the end of reading the bit CKACK.
bit5 RIF	0	Receive interrupt flag. A receive interrupt will be generated to CPU at the end of transmission of the signal CKACK.
bit4	0	Reserved.
bit3 SERR	0	Transmit error flag. On data transmission, if the signal CKACK received by the transmitter is low, a transmit error will be triggered and this bit will be set to 1.
bit2 RERR	0	Receive error flag. On data receiving, if the received checksum bit (CK) is not equal to that automatically computed by the system, a receive error will be triggered and this bit will be set to 1.
bit1 CHKSUM	0	The automatically computed checksum based on the received or transmitted 8-bit data (DATA).
bit0 CKACK	0	CKACK signal transmitted by the receiver at the end of data frame transmission. If the receiver cannot start receiving data automatically at the end of data frame transmission, this bit is read out as 1. If the receiver can start receiving data automatically at the end of data frame transmission, this bit will be set bit if the data are valid, or cleared if the data are invalid.

Table 12-22 EUART Configuration Register (CFGA/CFGB, 0x2A05/0x2B05)

0x2A05/0x2B05, R/W, EUART1/2 Configuration Register, CFGA/CFGB		
Bit	Default	Description
bit7 OVIE	0	Set this bit to 1 to enable receive overflow interrupt. By default the interrupt is disabled.

0x2A05/0x2B05, R/W, EUART1/2 Configuration Register, CFGA/CFGB		
Bit	Default	Description
bit6 SDIE	0	Set this bit to 1 to enable transmit interrupt. By default the interrupt is disabled.
bit5 RCIE	0	Set this bit to enable receive interrupt. By default the interrupt is disabled.
bit4 ACKLEN	0	When the V98XX works as a slave, this bit gives the period the bit CKACK stays 0 when a receive error occurs. 0: 1-byte length; 1: 2-byte length.
bit3 AUTOSD	0	If this bit is set to 1 and the V98XX works as a mater, the master will automatically transmit another character when a low level CKACK was received at the end of the former character. By default this function is disabled.
bit2 AUTORC	0	If this bit is set to 1 and the V98XX works as a slave, when the slave received invalid data, it will automatically transmit a low level CKACK to the master to ask it to transmit the data again.
bit1 CHKP	0	Parity bit. 0: even; 1: odd.
bit0 ENABLE	0	Set the bit ENABLE of CFGA to 1 to enable the port P10.0 for EUART1 data transmission and receive. Set the bit ENABLE of CFGB to 1 to enable the port P10.1 for EUART2 data transmission, and P10.2 for EUART2 data receive. By default the EURAT interfaces are idle.
According to the ISO/IEC 7816-3 protocol, the data should not be automatically re-transmitted more than three times. For example, the program must disable the automatic re-transmitting after two failures of re-transmitting.		

12.3.2. EUART Communication Timing

On EUART communication, the period for transmitting or receiving 1 bit is defined as the elementary time unit (ETU). When a data frame was transmitted, a period is needed by the receiver to check the received data before the transmitter sends another data frame. This period is defined as the guard time (GT). Generally, 1 GT is equal to 3 ETU.

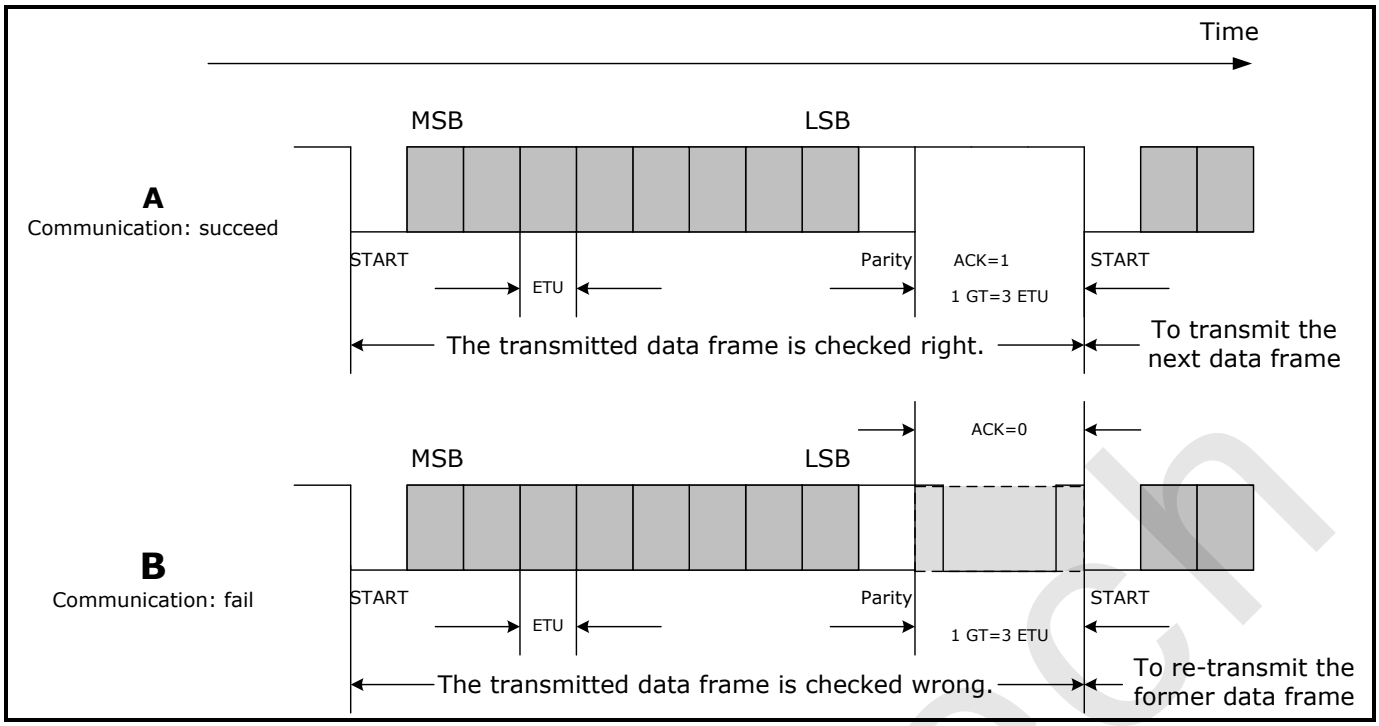


Figure 12-13 EUART Communication Timing

As shown in A, the transmitter sends a 10-bit data frame to the receiver, including 1-bit START, 8-bit DATA and 1-bit CK. At the end of transmission, the receiver sends a check signal CKACK of 1 to 2 ETU length. If a high level CKACK is transmitted, it indicates the received data frame is valid; in this condition, the transmitter and receiver will remain at high state for at least 1 ETU, and then the transmitter will send the next data frame.

As shown in B, the transmitter sends a 10-bit data frame to the receiver, including 1-bit START, 8-bit DATA and 1-bit CK. At the end of the transmission, the receiver sends a check signal CKACK of 1 to 2 ETU length. If a low level CKACK is transmitted, the signal will be driven to low from high at the moment of 9.5 ETU, and then pulled high at the moment of 11.5 or 12.5 ETU, which is determined by the configuration of the bit ACKLEN (bit4 of CFG), and holds high for 0.5 ETU. Then the transmitter will send the data frame again.

EUART interfaces support half-duplex communication. When the transmitter is sending a data frame, the receive port of the transmitter receives logic "1" all the time; when the receiver sent a signal CKACK to the transmitter at the end of the data frame transmission, the receive port of the transmitter receives the CKACK.

12.3.3. EUART Baud Rate Generation

In the V98XX, each EUART has a 16-bit timer for baud rate generation, DIVLA/DIVHA and DIVLB/DIVHB. The timer counts the MCU clock cycles. When the timer overflows, the transmitter is enabled to transmit 1-bit data. The baud rate can be calculated as follows:

$$\text{Baudrate} = \frac{f_{MCU}}{10000h - DIV} = \frac{1}{ETU} \qquad \text{Equation 12-9}$$

where, f_{MCU} is the MCU clock frequency, DIV is the preset value of the timer (DIVLA/DIVHA or DIVLB/DIVHB).

To ensure that the receiver can receive reliable data, the data receive is enabled at the moment of 0.5 ETU after the transmission started.

12.3.4. Data Transmission and Reception

By default the EUART serial interfaces stay IDLE.

12.3.4.1. Data Transmission

In the state IDLE, writing of the buffer register DATAA/DATAB (0x2A03/0x2B03) will enable data transmission. The transmission has 7 steps, each lasting 1 ETU:

1. transmitting the bit START (0);
2. transmiting 8-bit DATA, from MSB to LSB;
3. transmitting 1-bit CK;
4. reading the CKACK signal transmitted by the receiver, and then generating a transmit interrupt if the bit SDIE was set bit;
5. waiting state 1 (1 ETU);
6. waiting state 2 (1 ETU);
7. if a high level CKACK is transmitted by the receiver, or the automatic re-transmitting is disabled (AUTOSD is cleared, bit3 of CFGA/B, 0x2A05/0x2B05), the EUART interface gets back to IDLE state; if a low level CKACK is transmitted by the receiver, and the automatic re-transmitting is enabled, the EUART interface starts to transmit the start bit (START) of the former data frame again.

12.3.4.2. Data Reception

When the V98XX works as a slave, the EUART interface starts to receive a data frame when a 1-to-0 transition of the signal was detected. The data reception includes steps as follows, each lasting 1 ETU:

1. receiving the bit START (0);
2. receiving 8-bit DATA, from MSB to LSB;
3. receiving 1-bit CK;
4. transmitting a CKACK signal to the transmitter. If the received CK is equal to that automatically computed by the chip, or the automatic re-receiving is disabled (AUTORC is cleared, bit2 of CFGA/CFGB, 0x2A05/0x2B05), CKACK is high level; otherwise, CKACK is low level.
5. Transmitting the CKACK signal to the transmitter again. If the received CK is equal to that automatically computed by the chip, or the automatic re-receiving is disabled (AUTORC is cleared, bit2 of CFGA/CFGB, 0x2A05/0x2B05), CKACK is high level; otherwise, CKACK is low level. After this step, an interrupt is generated to CPU.
6. getting back to the IDLE state.

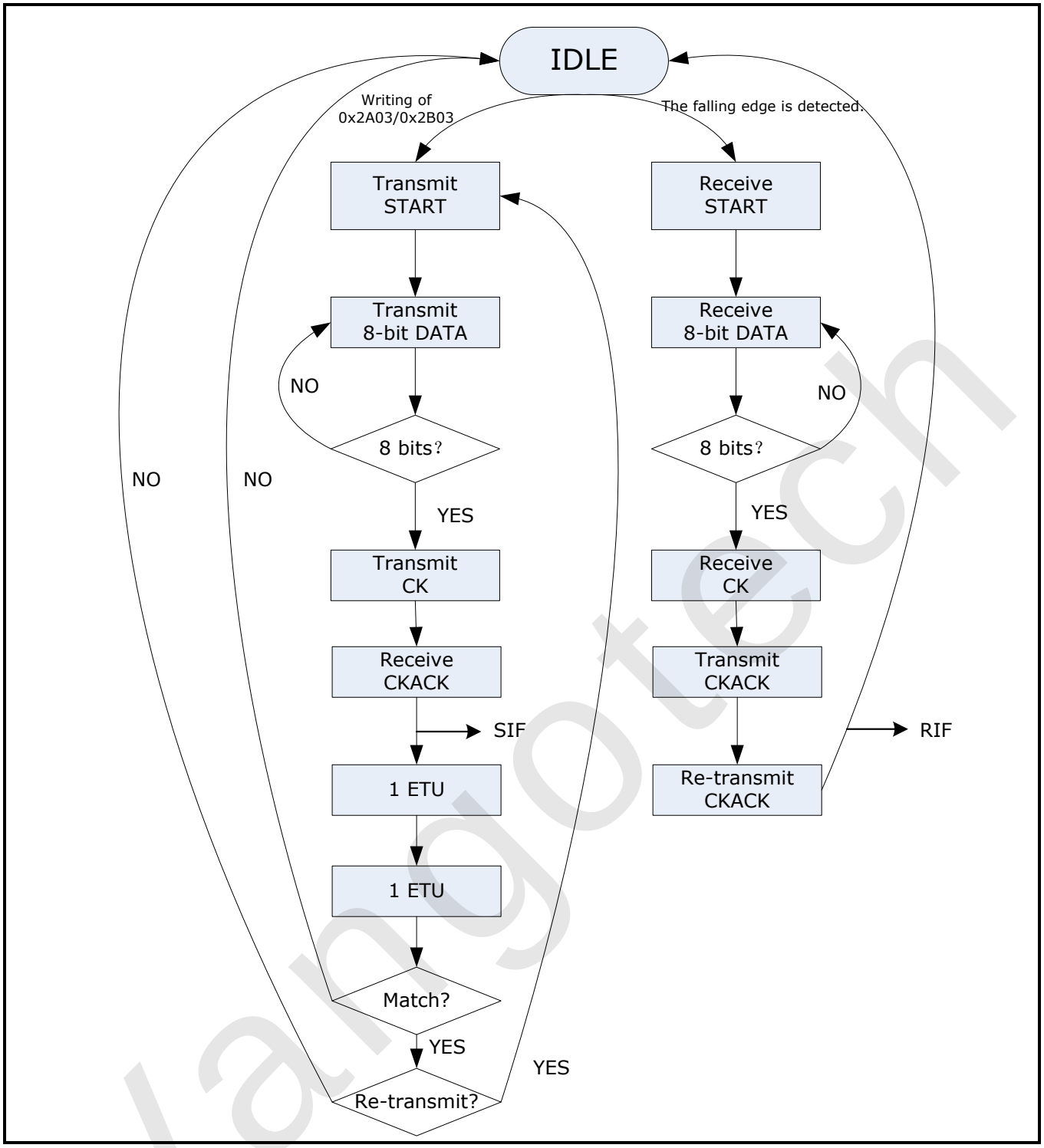


Figure 12-14 Data Transmission and Reception

12.3.5. EUART for Smart Card Communication

Both EUART interfaces are ISO/IEC 7816-3 compliant, so they can be used for smart card communication.

When the EUART interface is used for smart card communication, the pulse width modulation clock (PWM clock) output from the pin P9.7 will be used as the smart card clock input. The pulse width can be configured via the registers listed in the following table. Bit PWMCLK (bit7 of PRCtrl0, 0x2D00) gate controls the PWM clock generator.

Users can write of pulse width modulation clock generators to configure the PWM clock frequency and its duty cycle:

$$f_{PWMCLK} = \frac{f_{MCU}}{PWMCLK1 + PWMCLK2} \quad \text{Equation 12-10}$$

$$Duty_{PWM} = \frac{PWMCLK1}{PWMCLK2} \quad \text{Equation 12-11}$$

where, f_{PWMCLK} is PWM clock frequency; f_{MCU} is MCU clock frequency; $Duty_{PWM}$ is the duty cycle of PWM clock; *PWMCLK1* is the value of registers PWMCLK1H and PWMCLK1L; *PWMCLK2* is the value of registers PWMCLK2H and PWMCLK2L.

Table 12-23 Pulse Width Modulation Clock Generators

Register	Address	R/W	Bit	Default	Description
PWMCLK1H	0x289C	R/W	bit[7:0]	0	Higher byte of pulse width modulation clock generator 1, to control duration of state high in the duty cycle
PWMCLK1L	0x289D	R/W	bit[7:0]	0	Lower byte of pulse width modulation clock generator 1, to control duration of state high in the duty cycle
PWMCLK2H	0x289E	R/W	bit[7:0]	0	Higher byte of pulse width modulation clock generator 2 , to control duration of state low in the duty cycle
PWMCLK2L	0x289F	R/W	bit[7:0]	0	Lower byte of pulse width modulation clock generator 2, to control duration of state low in the duty cycle

13. General-Purpose Serial Interface (GPSI)

V98XX integrates a general-purpose serial interface (GPSI) that is compliant with the I^2C protocol. When the bit **"GPSI"** (**"bit6"** of **"PRCtrl0"**, 0x2D00) is set to **'1'**, pins **"P9.1"** and **"P9.2"** work as the two wires of the general-purpose serial interface: **"P9.1"** for serial data (**"SDA"**), and **"P9.2"** for serial clock (**"SCL"**). When pins **"P9.1"** and **"P9.2"** is used for GPSI wires, **"P9.1"** must be configured to **"Input enabled"**, but no mandatory requirement on the output enable register of **"P9.1"**; and **"P9.2"** is **"Output enabled"** automatically.

13.1. Frame Structure

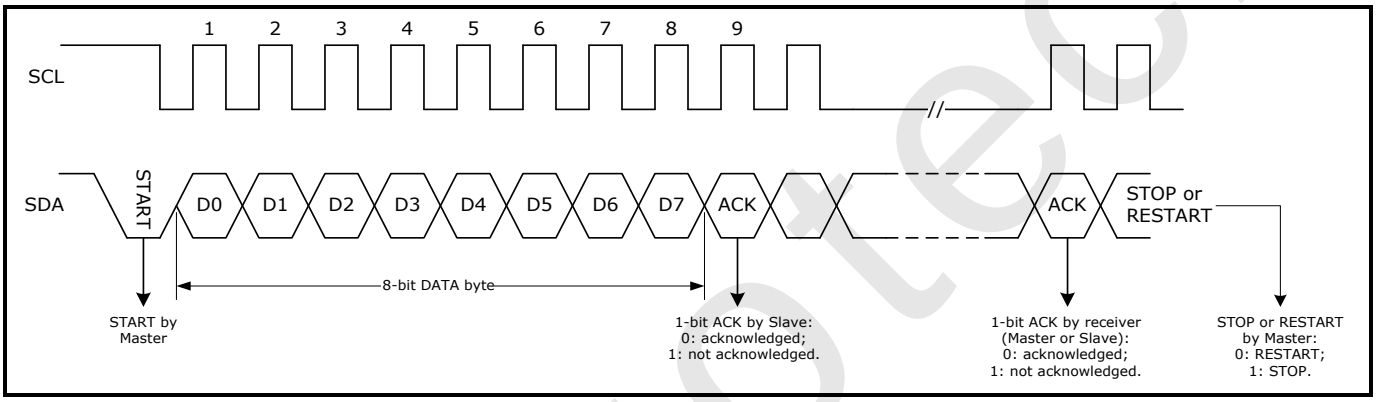


Figure 13-1 Frame Structure on SDA

As illustrated in Figure 13-1, a frame through the wire **"SDA"** is composed of some of the following parts.

- **1-bit START**: A falling edge on **"SDA"** when **"SCL"** holding **"HIGH"** sets up a START condition. This bit must be sent by Master.
- **8-bit DATA byte**: 1 bit DATA transferred on 1 SCL clock. A DATA bit is prepared on the falling edge of each SCL clock, and sampled on the rising edge of each SCL clock. The endian of byte transfer is defined by the bit **"Endian"** (**"bit4"** of **"SICFG"**, 0x2F01). 8-bit DATA byte must be followed by 1-bit **"ACK"**.
- **1-bit ACK**: The **"ACK"** bit is prepared on the falling edge of an **"SCL"** clock, and sampled on the rising edge of an **"SCL"** clock. Only the **"ACK"** bit transferred by the receiver is valid. **"HIGH"** indicates **"Not acknowledged"**; **"LOW"** indicates **"Acknowledged"**. 1-bit ACK must be preceded by 8-bit DATA.
- **1-bit STOP or RESTART**, when **"SCL"** holds **"HIGH"**, the SDA signal will generate a rising edge (**"STOP"**) or falling edge (**"RESTART"**). Preparing **"SDA"** data in the **"SCL"** falling edge, Sampling **"SDA"** data in a **"SCL"** rising edge. So, Before **"STOP"** or **"RESTART"**, SCL signal must produce a falling edge, while ensuring the SDA level on the rising edge of **"SCL"**: If users want to generate **"STOP"**, users should ensure that the SDA signal is low; If you want to generate RESTART, should ensure that the SDA is high level. STOP or RESTART must be issued by by Master device.

Bit[3:0] of register SICFG (0x2F01) defines the structure of the frame to be transmitted or received.

Table 13-1 Description of Different Frame Structures

#	START	DATA+ACK	STOP/RESTART	Description
0	○	○	○	Not valid.
1	○	○	X	To receive or transmit the starting frame.
2	○	X	○	Not valid.
3	○	X	X	To receive or transmit START bit only.
4	X	○	○	To receive or transmit the last frame composed of 8-bit DATA, 1-bit ACK and 1-bit STOP.
5	X	○	X	To receive or transmit 8-bit DATA and 1-bit ACK only.
6	X	X	○	To receive or transmit 1-bit STOP only.
7	X	X	X	Not valid.
○: to receive or transmit; X: not to receive or transmit.				

13.2. Serial Clock Generation

When a START condition is set up, the 16-bit timer embedded in the GPSI unit starts to count the MCU clock pulses to generate the serial clock (f_{SCL}). The f_{SCL} is defined by the following equation:

$$f_{SCL} = \frac{f_{MCU}}{4 \times (TH+1)} \qquad \text{Equation 13-1}$$

where f_{MCU} is the clock frequency for MCU operation; *TH* is the threshold preset in registers SITHH (0x2F03) and SITHL (0x2F02); f_{SCL} is the serial clock (SCL) frequency, and the maximum f_{SCL} is 400kHz.

13.3. Receive and Transmit Data

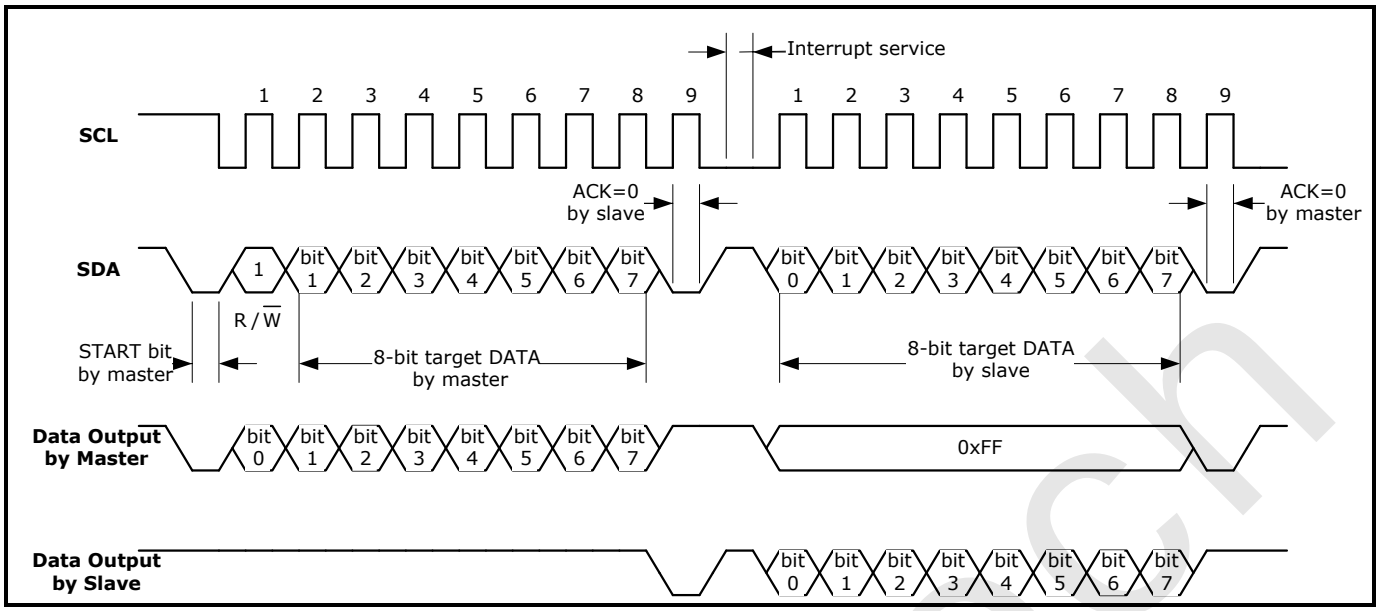


Figure 13-2 Receive and Transmit Data

When the V98XX communicate with other devices via GPSI, it transmits and receives data simultaneously.

The data on the wire SDA is in the format of Wire-AND, which means the data is the data from receiver and transmitter in "AND" logic, but not the state of either. The MCU can read the register SIDAT (0x2F04) and bit ACK (bit0 of SIFLG, 0x2F05) to acquire the data of the SDA. When GPSI is idle (BUSY, bit1 of SIFLG, 0x2F05, is cleared), writing of register SIDAT (0x2F04) triggers data receive and transmit.

When bit BUSY (bit1 of SIFLG, 0x2F05) is cleared, writing 0xFF or a specific data byte to be transmitted to register SIDAT (0x2F04) triggers data receive and transmit. Then bit BUSY is set to 1. After data transmit and receive, bit BUSY is cleared again, and read register SIDAT and bit ACK (bit0 of SIFLG, 0x2F05) to acquire the data from SDA.

13.4. GPSI Interrupt

When IE4=1 (bit4 of ExInt5IE, 0x28A5), EIE.3=1 (SFR 0xE8) and IE.7=1 (SFR 0xA8), a transmit interrupt will be triggered every time a frame (structure defined by register SICFG) is transmitted, and CPU will service the interrupt, read bit ACK, and prepares for the next frame transmission.

When IE5=1 (bit5 of ExInt5IE, 0x28A5), EIE.3=1 (SFR 0xE8) and IE.7=1 (SFR 0xA8), writing of registers located at addresses 0x2F01~0x2F04 when bit BUSY (bit1 of SIACK, 0x2F05) is set to 1, an illegal data interrupt will be triggered and the write operation is invalid.

SCL holds LOW on interrupt service.

13.5. For I²C Application

The GPSI is I²C compliant. When it is used for I²C application, the V98XX works as Master device to

communicate with other devices connected to the I²C bus. In this case, the starting frame is to select the target slave, of which bit[7:1] of 8-bit DATA is slave address byte, and bit0 is read/write control bit ("1" read; "0" write).

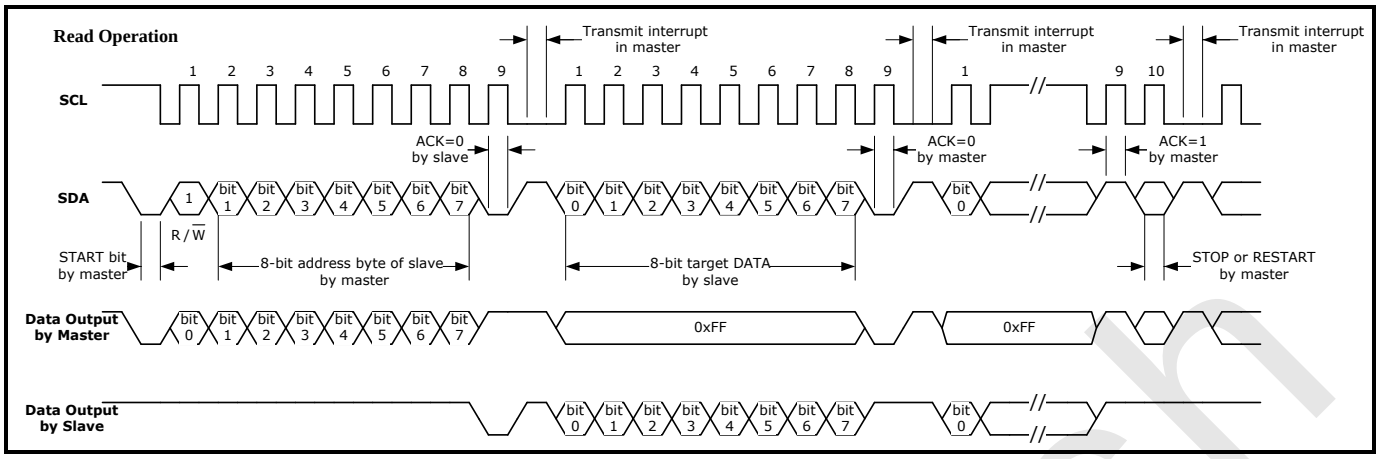


Figure 13-3 Read Operation

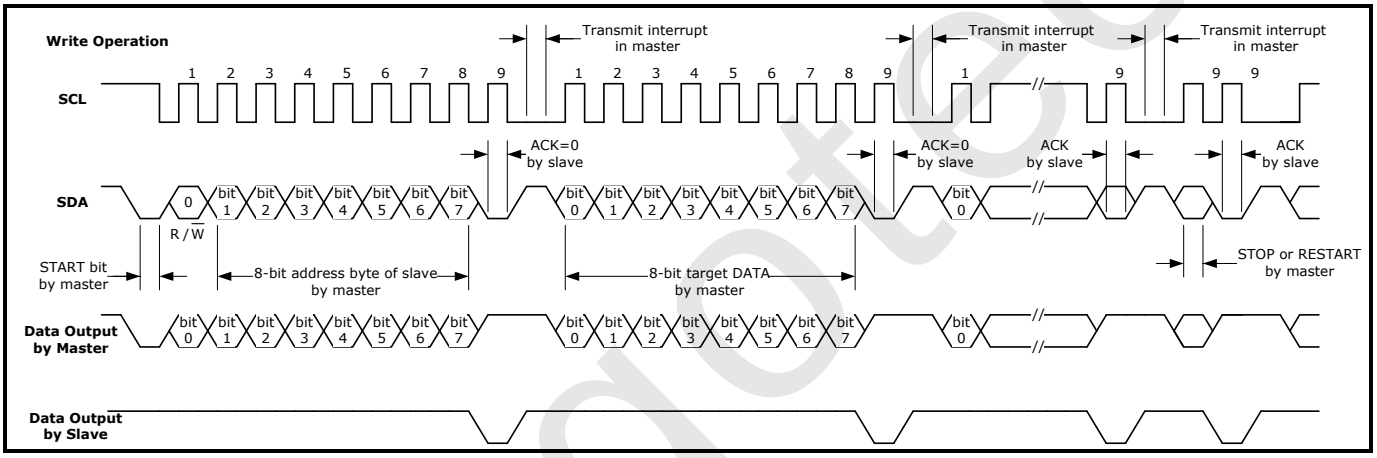


Figure 13-4 Write Operation

Figure 13-3 and Figure 13-4 depict read and write operation on I²C application when interrupt is enabled. For example, when the V98XX writes or reads a slave device connected on I²C bus via GPSI, it could be done following the procedure:

1. Write of registers SITHH/SITHL (0x2F03/0x2F02) to configure f_{SCL};
2. Write of register SICFG (0x2F01) to enable transmitting START, and clear bit Endian to 0;
3. Write anything to register SIDAT (0x2F04) to trigger to transmit START. During transmission, bit BUSY is set to 1;
4. When BUSY is cleared, write of register SICFG (0x2F01) to enable transmitting DATA and ACK; write 0x01 to register SIACK (0x2F05); and then write target slave address to bit[7:1] of register SIDAT (0x2F04) and write 1 (to read) or 0 (to write) to bit0 to trigger transmitting the slave address frame. During transmission, bit BUSY is set to 1;
5. When BUSY is cleared, read of register SIACK (0x2F05). If it is read out as 0, the target slave device is selected;
6. Write of register SICFG (0x2F01) to enable transmitting DATA and ACK; write of 0x01 to register SIACK (0x2F05); and then write the content to be transmitted to register SIDAT (0x2F04) to trigger transmitting data frame. During transmission, bit BUSY is set to 1;

7. Repeat step 5 and 6 until all data have been transmitted;
8. Write of register SICFG (0x2F01) to enable transmitting STOP or RESTART;
9. Write anything to register SIDAT (0x2F04) to trigger transmitting bit STOP or RESTART.

The bit STOP ends a serial communication.

13.6. Registers

Table 13-2 Register to Disable or Enable GPSI

0x2D00, R/W, Peripheral Control Register 0, PRCtrl0				
Bit		R/W	Default	Description
Bit7	PWMCLK	R/W	0	1: Disable the clock for PWM; 0: Enable the clock for PWM
Bit6	GPSI	R/W	0	To enable or disable GPSI. 1: enable; 0: disable.
Bit5	P10	R/W	0	1: Disabe IO P10; 0: Enable IO P10。
Bit4	P9	R/W	0	To enable or disable the fast IOs Group P9. 1: disable; 0: enable.
Bit3	P0P8	R/W	0	1: Disable all IO P0~P8; 0: Enable all IO P0~P8
Bit2	EUART2	R/W	0	1: Disable EUART2block; 0: Enable EUART2block
Bit1	EUART1	R/W	0	1: Disable EUART1block; 0: Enable EUART1block。
Bit0	TimerA	R/W	0	1: Disable TimerA; 0: Enable TimerA。

Table 13-3 GPSI Control Register (SICFG, 0x2F01)

0x2F01, R/W, GPSI Control Register, SICFG				
Bit		R/W	Default	Description
Bit[7:5]	Reserved	R/W	0	

0x2F01, R/W, GPSI Control Register, SICFG				
Bit		R/W	Default	Description
Bit4	Endian	R/W	0	To configure the DATA endian for transmission and reception. 1: LSB first; 0: MSB first.
Bit3	TXS	R/W	0	Set this bit to 1 to enable receiving or transmitting START bit.
Bit2	TXD	R/W	0	Set this bit to 1 to enable receiving or transmitting 8-bit DATA byte and 1-bit ACK.
Bit1	TXP	R/W	0	Set this bit to 1 to enable receiving or transmitting STOP bit.
Bit0	TXRS	R/W	0	Set this bit to 1 to enable receiving or transmitting RESTART bit.

Table 13-4 GPSI Timer Divider Registers (SITHH/SITHL, 0x2F03/0x2F02)

Register		Bit		R/W	Default	Description
0x2F03	SITHH	Bit[7:0]	TH[15:8]	R/W	0	Set a threshold for serial clock (SCL) generation. $f_{SCL} = \frac{f_{MCU}}{4 \times (TH[15:0]+1)}$
0x2F02	SITHL	Bit[7:0]	TH[7:0]	R/W	0	

Table 13-5 GPSI Data Register (SIDAT, 0x2F04)

0x2F04, R/W, GPSI Data Register, SIDAT								
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Endian=0	D0	D1	D2	D3	D4	D5	D6	D7
Endian=1	D7	D6	D5	D4	D3	D2	D1	D0
The content of this register is the 8-bit DATA byte received or to be transmitted. Writing of this register triggers receiving or transmitting data.								

Table 13-6 GPSI Communication Flag Register (SIFLG, 0x2F05)

0x2F05, R/W, GPSI Communication Flag Register (SIFLG)				
Bit		R/W	Default	Description
Bit[7:2]	Reserved	R/W	0	
Bit1	BUSY	R	0	When the interface is receiving or transmitting data, this bit is set to 1. In this case, writing of registers located at addresses 0x2F01~0x2F04 will trigger illegal data interrupt when this interrupt is enabled.
Bit0	ACK	R/W	0	When Master works as the receiver, writing of this bit and transmit

0x2F05, R/W, GPSI Communication Flag Register (SIFLG)				
Bit		R/W	Default	Description
				it to acknowledge the transmitter or not. When Master works as the transmitter, writing 1 to this bit to transmit it, and read this bit after the transmission to check whether the receiver acknowledge the transmitter or not. 1: not acknowledged. 0: acknowledged.

14. LCD Driver

V98XX has the LCD driver which can drive the LCD panel of 4×40 or 6×38 segments (1/3 bias) or 8×36 segments (1/3 bias or 1/4 bias). **"CLK3"**, sourced by the 32.768-kHz OSC clock, provides the LCD driver with the clock pulse. The driver is powered by the regulated voltage output from the 3.3-V LDO; the LCD bias generator composed of an internal resistor ladder generates the LCD waveform voltage; and the LCD waveform voltage level can be adjusted over the range of 2.7 V ~ 3.3 V with a resolution of 0.1 V/lsb.

When a POR/BOR, RSTn pin reset, or WDT overflow reset occurs, the LCD driver will be reset to its default state.

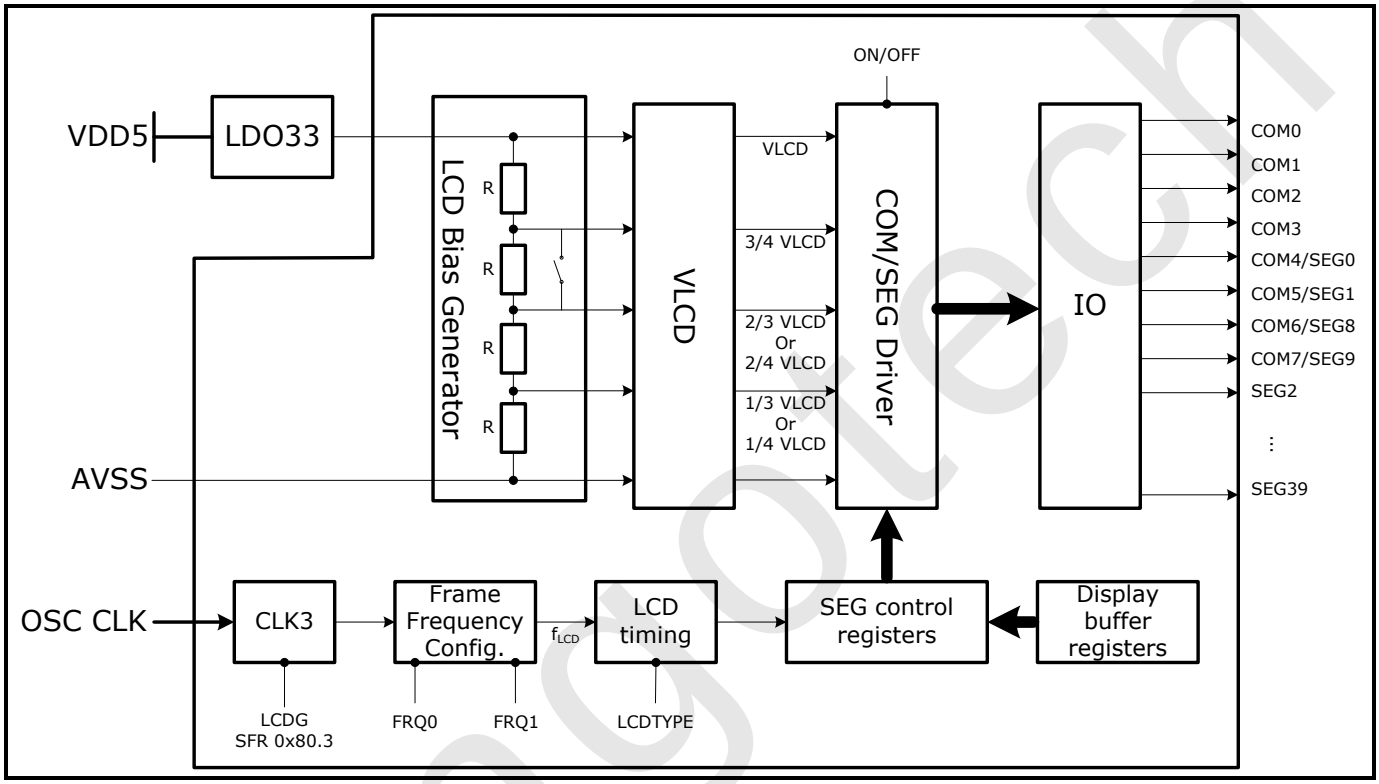


Figure 14-1 LCD Driver Block Diagram

14.1. Pins for LCD Driver

In V98XX, some pins are multiplexed by SEG/COM signal output, general-purpose input/output (GPIO), and analog input of M Channel or comparator CB.

When some bits of SEG Control Registers (R/W) are set to 1s, the corresponding pins are used for SEG output. In this condition, it is mandatory to configure the GPIO ports as **"Input disabled"** and **"Output disabled"** in the corresponding input and output enabled registers.

When the pins work as GPIO or analog input of M Channel or comparator CB, the corresponding bits of SEG Control Registers (R/W) must be cleared to disable SEG output.

14.2. LCD Timing

In the V98XX, the CLK3, sourced by the 32.768kHz OSC clock, provides the LCD driver with clock pulse

for timing generation. Generally, the crystal oscillator keeps on running until it is powered off, so the LCD driver keeps on working even in Sleep or Deep Sleep state unless CLK3 is disabled. When the crystal stops running anomaly when power is still on, the internal RC clock will become the replacement of the OSC clock to source the LCD driver until the crystal is stimulated to run again.

The CLK3 frequency is divided to generate frame frequency for the waveform. The MCU can configure bit[1:0] of LCDCtrl (0x2C1E) to select the appropriate frame frequency. By default it is 64Hz.

14.3. LCD Waveform Voltage

In the V98XX, the LCD driver is powered by the 3.3V LDO output voltage, and an internal resistor ladder is designed to generate LCD waveform voltage (VLCD). Users can adjust the waveform voltage via bits VLCD (bit2 of CtrlLCDV, 0x285E) and LDO3SEL<2:0> configurations.

$$\mathrm{VLCD} = [\mathrm{VLCD}] \times \frac{[\mathrm{LDO3SEL} < 2{:}0 >]}{3.3} \qquad \text{Equation 14-1}$$

where,

VLCD is the LCD waveform voltage;

[LDO3SEL<2:0>] is the output voltage of 3.3V LDO (LDO33). [LDO3SEL<2:0>] is equal to configuration of bits LDO3SEL<2:0> (bit[5:3] of CtrlLDO, 0x2866);

[VLCD] is the configuration of bit VLCD (bit2 of CtrlLCDV, 0x285E).

Table 14-1 VLCD to Configuration of [LDO3SEL<2:0>] and [VLCD]

[LDO3SEL<2:0>]		3.5V	3.4V	3.3V	3.2V	3.1V	3.0V
[VLCD]	3.3V	3.5V	3.4V	3.3V	3.2V	3.1V	3.0V
	3.0V	3.2V	3.1V	3.0V	2.9V	2.8V	2.7V

Users can adjust the resistance value of each resistor in the resistor ladder of the bias voltage generation circuits via bits DRV1/DRV0 (bit[3:2] of LCDCtrl, 0x2C1E) to adjust the current through the circuits to change the lightness of the display panel. By default the resistance value is 300 kΩ.

14.4. Display RAM

In the V98XX, the display RAM located at addresses of 0x2C00~0x2C1D and 0x2C28~0x2C31 stores the LCD data. When the SEG/COM driver is enabled (setting bit7 of LCDCtrl to 1), the LCD panel displays the data immediately they are updated in the RAM. When the SEG/COM driver is disabled (clearing bit7 of LCDCtrl), the LCD panel displays nothing. When POR/BOR, RSTn pin reset or WDT overflow event occurs, the SEG/COM driver will be reset and the RAM will be cleared.

The LCD driver supports LCD panel of 1/4 duty, 1/6 duty or 1/8 duty. When bits LCDTYPE (bit[5:4] of LCDCtrl, 0x2C1E) are cleared, an LCD panel of 1/4 Duty should be used. In this application, each byte of display RAM stores content of 2 LCD segments: lower 4 bits for Seg (n), and higher 4 bits for Seg (n+1).

Table 14-2 RAM Byte Allocation for Segments of LCD Panel of 1/4 Duty

Register		Segment	D7	D6	D5	D4	D3	D2	D1	D0
			COM3	COM2	COM1	COM0	COM3	COM2	COM1	COM0
0x2C00	LCDM0	S01 S00	SEG01				SEG00			
0x2C01	LCDM1	S03 S02	SEG03				SEG02			
0x2C02	LCDM2	S05 S04	SEG05				SEG04			
0x2C03	LCDM3	S07 S06	SEG07				SEG06			
0x2C04	LCDM4	S09 S08	SEG09				SEG08			
0x2C05	LCDM5	S11 S10	SEG11				SEG10			
0x2C06	LCDM6	S13 S12	SEG13				SEG12			
0x2C07	LCDM7	S15 S14	SEG15				SEG14			
0x2C08	LCDM8	S17 S16	SEG17				SEG16			
0x2C09	LCDM9	S19 S18	SEG19				SEG18			
0x2C0A	LCDM10	S21 S20	SEG21				SEG20			
0x2C0B	LCDM11	S23 S22	SEG23				SEG22			
0x2C0C	LCDM12	S25 S24	SEG25				SEG24			
0x2C0D	LCDM13	S27 S26	SEG27				SEG26			
0x2C0E	LCDM14	S29 S28	SEG29				SEG28			
0x2C0F	LCDM15	S31 S30	SEG31				SEG30			
0x2C10	LCDM16	S33 S32	SEG33				SEG32			
0x2C11	LCDM17	S35 S34	SEG35				SEG34			
0x2C12	LCDM18	S37 S36	SEG37				SEG36			
0x2C13	LCDM19	S39 S38	SEG39				SEG38			

When bits LCDTYPE (bit[5:4] of LCDCtrl, 0x2C1E) are set to 1, an LCD panel of 1/6 Duty should be used. In this application, by default every 3 bytes of display RAM store content of 4 LCD segments. But when bit 6COMTYPE (bit6 of LCDCtrl, 0x2C1E) is set to 1, each byte of display RAM stores content of one LCD segment.

Table 14-3 RAM Byte Allocation for Segments of LCD Panel of 1/6Duty When 6COMTYPE=0

Register		SEG	D7	D6	D5	D4	D3	D2	D1	D0
0x2C01	LCDM1	S02 --	SEG02							
0x2C02	LCDM2	S03 S02	SEG03						SEG02	
0x2C03	LCDM3	S05 S04	SEG05			SEG04				
0x2C04	LCDM4	S06 S05	SEG06				SEG05			

Register		SEG	D7	D6	D5	D4	D3	D2	D1	D0
0x2C05	LCDM5	S07 S06	SEG07						SEG06	
0x2C06	LCDM6	S09 S08	SEG09		SEG08					
0x2C07	LCDM7	S10 S09	SEG10				SEG09			
0x2C08	LCDM8	S11 S10	SEG11						SEG10	
0x2C09	LCDM9	S13 S12	SEG13		SEG12					
0x2C0A	LCDM10	S14 S13	SEG14				SEG13			
0x2C0B	LCDM11	S15 S14	SEG15						SEG14	
0x2C0C	LCDM12	S17 S16	SEG17		SEG16					
0x2C0D	LCDM13	S18 S17	S18				S17			
0x2C0E	LCDM14	S19 S18	SEG19						SEG18	
0x2C0F	LCDM15	S21 S20	SEG21		SEG20					
0x2C10	LCDM16	S22 S21	SEG22				SEG21			
0x2C11	LCDM17	S23 S22	SEG23						SEG22	
0x2C12	LCDM18	S25 S24	SEG25		SEG24					
0x2C13	LCDM19	S26 S25	SEG26				SEG25			
0x2C14	LCDM20	S27 S26	SEG27						SEG26	
0x2C15	LCDM21	S29 S28	SEG29		SEG28					
0x2C16	LCDM22	S30 S29	SEG30				SEG29			
0x2C17	LCDM23	S31 S30	SEG31						SEG30	
0x2C18	LCDM24	S33 S32	SEG33		SEG32					
0x2C19	LCDM25	S34 S33	SEG34				SEG33			
0x2C1A	LCDM26	S35 S34	SEG35						SEG34	
0x2C1B	LCDM27	S37 S36	SEG37		SEG36					
0x2C1C	LCDM28	S38 S37	SEG38				SEG37			
0x2C1D	LCDM29	S39 S38	SEG39						SEG38	

Table 14-4 RAM Byte Allocation for Segments of LCD Panel of 1/6 Duty When 6COMTYPE=1

Register		D7	D6	D5	D4	D3	D2	D1	D0
0x2C02	LCDM2	-	-	SEG02					
0x2C03	LCDM3	-	-	SEG03					

Register		D7	D6	D5	D4	D3	D2	D1	D0
0x2C04	LCDM4	-	-	SEG04					
0x2C05	LCDM5	-	-	SEG05					
0x2C06	LCDM6	-	-	SEG06					
0x2C07	LCDM7	-	-	SEG07					
0x2C08	LCDM8	-	-	SEG08					
0x2C09	LCDM9	-	-	SEG09					
0x2C0A	LCDM10	-	-	SEG10					
0x2C0B	LCDM11	-	-	SEG11					
0x2C0C	LCDM12	-	-	SEG12					
0x2C0D	LCDM13	-	-	SEG13					
0x2C0E	LCDM14	-	-	SEG14					
0x2C0F	LCDM15	-	-	SEG15					
0x2C10	LCDM16	-	-	SEG16					
0x2C11	LCDM17	-	-	SEG17					
0x2C12	LCDM18	-	-	SEG18					
0x2C13	LCDM19	-	-	SEG19					
0x2C14	LCDM20	-	-	SEG20					
0x2C15	LCDM21	-	-	SEG21					
0x2C16	LCDM22	-	-	SEG22					
0x2C17	LCDM23	-	-	SEG23					
0x2C18	LCDM24	-	-	SEG24					
0x2C19	LCDM25	-	-	SEG25					
0x2C1A	LCDM26	-	-	SEG26					
0x2C1B	LCDM27	-	-	SEG27					

Register		D7	D6	D5	D4	D3	D2	D1	D0
0x2C1C	LCDM28	-	-	SEG28					
0x2C1D	LCDM29	-	-	SEG29					
0x2C28	LCDM30	-	-	SEG30					
0x2C29	LCDM31	-	-	SEG31					
0x2C2A	LCDM32	-	-	SEG32					
0x2C2B	LCDM33	-	-	SEG33					
0x2C2C	LCDM34	-	-	SEG34					
0x2C2D	LCDM35	-	-	SEG35					
0x2C2E	LCDM36	-	-	SEG36					
0x2C2F	LCDM37	-	-	SEG37					
0x2C30	LCDM38	-	-	SEG38					
0x2C31	LCDM39	-	-	SEG39					

When bits LCDTYPE (bit[5:4] of LCDCtrl, 0x2C1E) are set to 2 or 3, an LCD panel of 1/8 Duty should be used. In this application, each byte of display RAM stores content of one LCD segment.

Table 14-5 RAM Byte Allocation for Segments of LCD Panel of 1/8 Duty

Register		D7	D6	D5	D4	D3	D2	D1	D0
0x2C02	LCDM2	SEG02							
0x2C03	LCDM3	SEG03							
0x2C04	LCDM4	SEG04							
0x2C05	LCDM5	SEG05							
0x2C06	LCDM6	SEG06							
0x2C07	LCDM7	SEG07							
0x2C0A	LCDM10	SEG10							
0x2C0B	LCDM11	SEG11							
0x2C0C	LCDM12	SEG12							

Register		D7	D6	D5	D4	D3	D2	D1	D0
0x2C0D	LCDM13	SEG13							
0x2C0E	LCDM14	SEG14							
0x2C0F	LCDM15	SEG15							
0x2C10	LCDM16	SEG16							
0x2C11	LCDM17	SEG17							
0x2C12	LCDM18	SEG18							
0x2C13	LCDM19	SEG19							
0x2C14	LCDM20	SEG20							
0x2C15	LCDM21	SEG21							
0x2C16	LCDM22	SEG22							
0x2C17	LCDM23	SEG23							
0x2C18	LCDM24	SEG24							
0x2C19	LCDM25	SEG25							
0x2C1A	LCDM26	SEG26							
0x2C1B	LCDM27	SEG27							
0x2C1C	LCDM28	SEG28							
0x2C1D	LCDM29	SEG29							
0x2C28	LCDM30	SEG30							
0x2C29	LCDM31	SEG31							
0x2C2A	LCDM32	SEG32							
0x2C2B	LCDM33	SEG33							
0x2C2C	LCDM34	SEG34							
0x2C2D	LCDM35	SEG35							
0x2C2E	LCDM36	SEG36							

Register		D7	D6	D5	D4	D3	D2	D1	D0
0x2C2F	LCDM37	SEG37							
0x2C30	LCDM38	SEG38							
0x2C31	LCDM39	SEG39							

14.5. LCD Drive Waveform

There are 4 resistors in series in the bias voltage generation circuit, which can be configured to work in 1/3 bias mode or 1/4 bias mode.

When an LCD panel of 1/4 or 1/6 duty is applied, only 1/3 bias mode can be used.

When an LCD panel of 1/8 duty is applied, users can configure bit LCDBMOD (bit3 of CtrlBAT, 0x285C) to disable or enable one resistor in the bias voltage generation circuit to enable the LCD driver to work in 1/3 bias mode or 1/4 bias mode.

When an LCD panel of 1/4 duty is applied, the LCD drive waveform is depicted in the following figure.

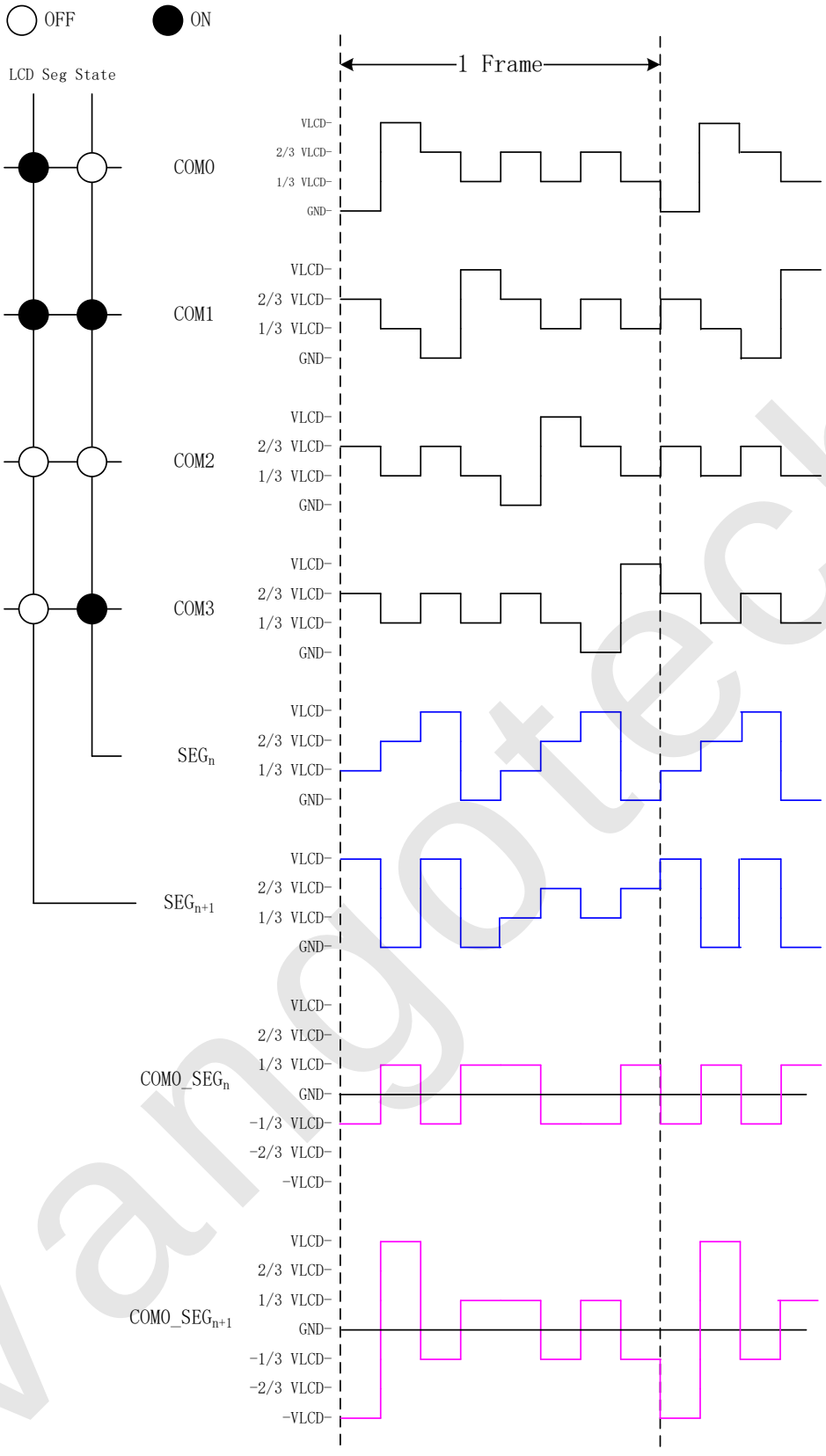


Figure 14-2 LCD Drive Waveform When an LCD Panel of 1/4 Duty and 1/3 Bias is Applied

When an LCD panel of 1/6 duty is applied, the LCD drive waveform is depicted in the following figure.

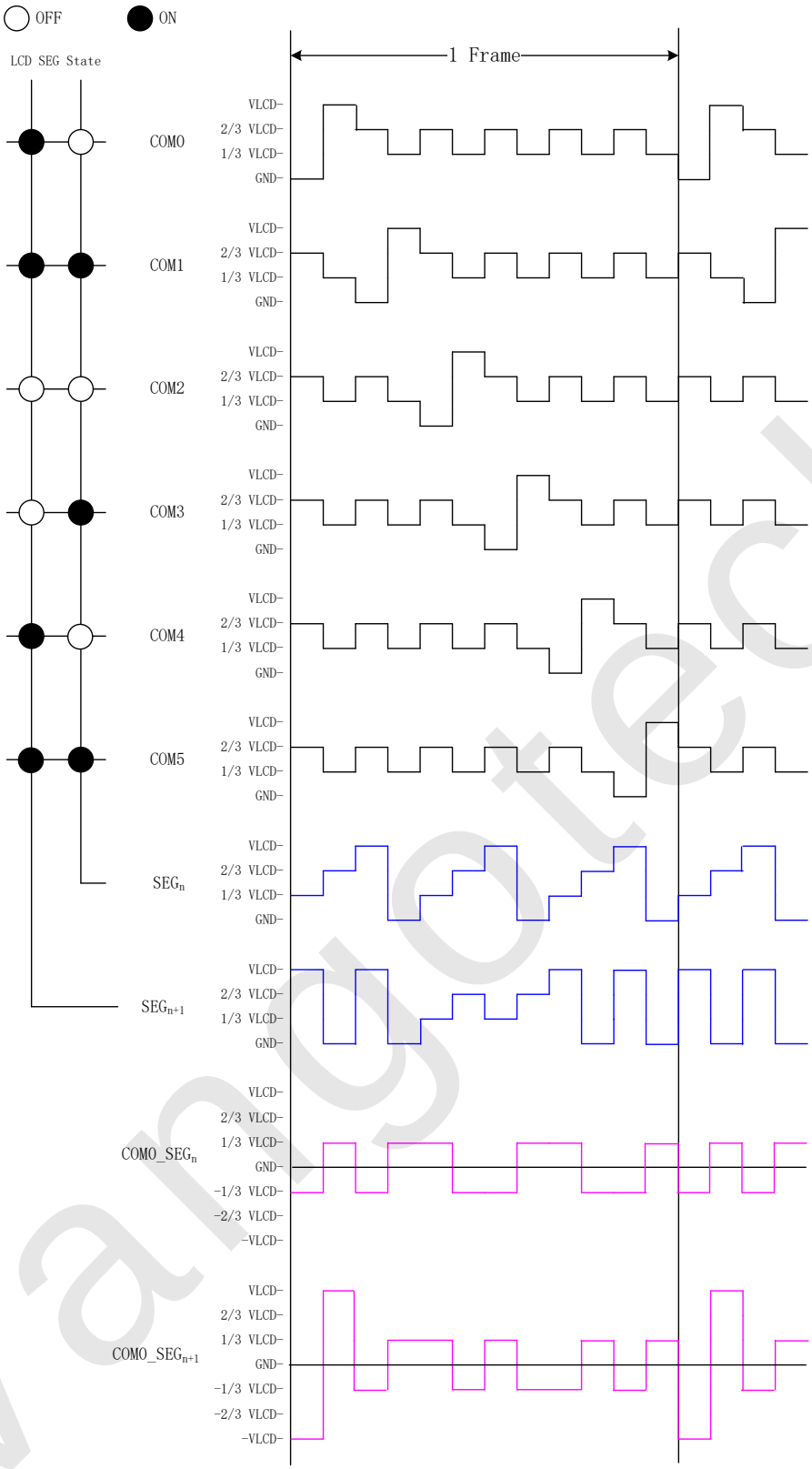


Figure 14-3 LCD Drive Waveform When an LCD Panel of 1/6 Duty and 1/3 Bias is Applied

When an LCD panel of 1/8 duty is applied, the LCD drive waveform is depicted in the following figures.

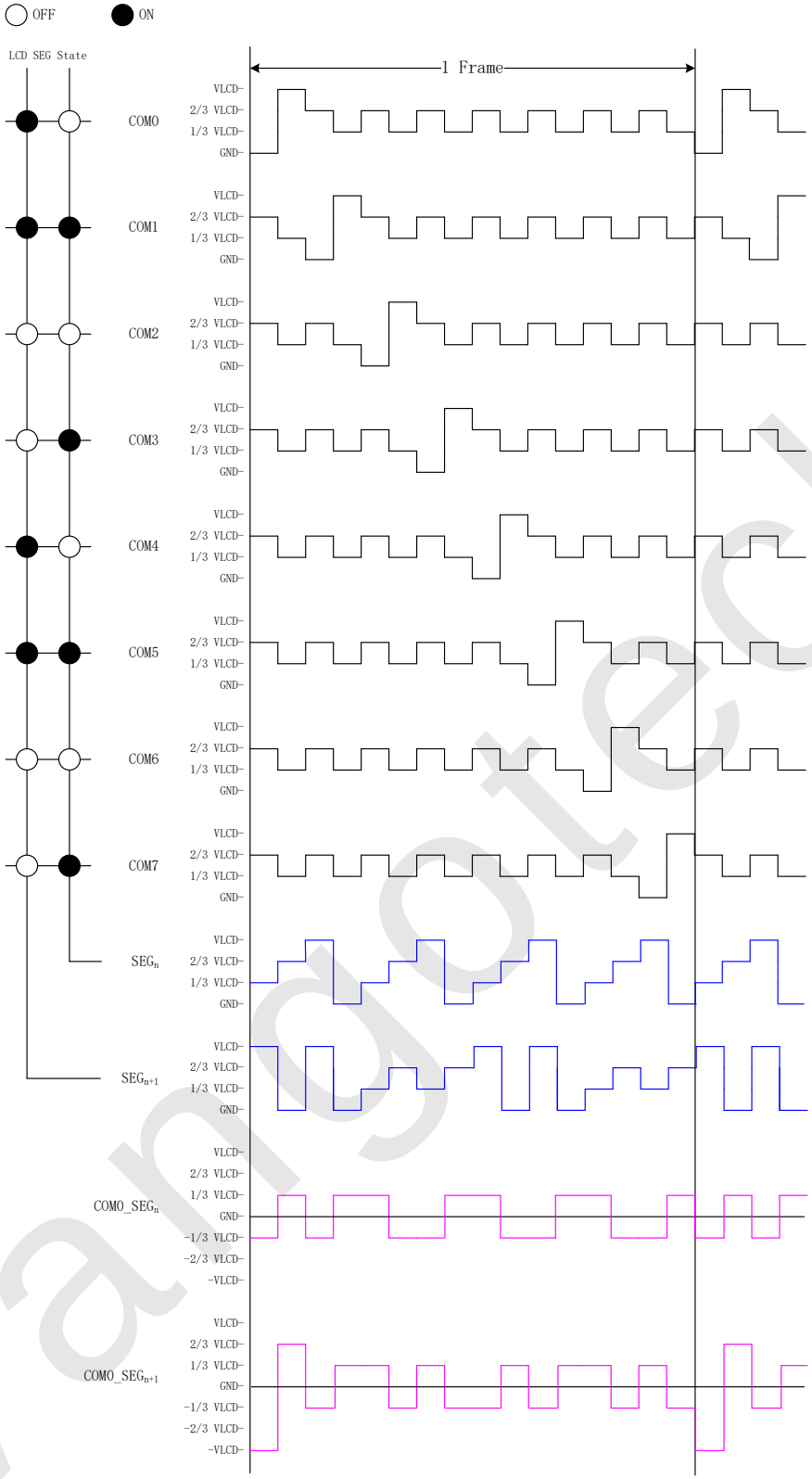


Figure 14-4 LCD Drive Waveform When an LCD Panel of 1/8 Duty and 1/3 Bias is Applied

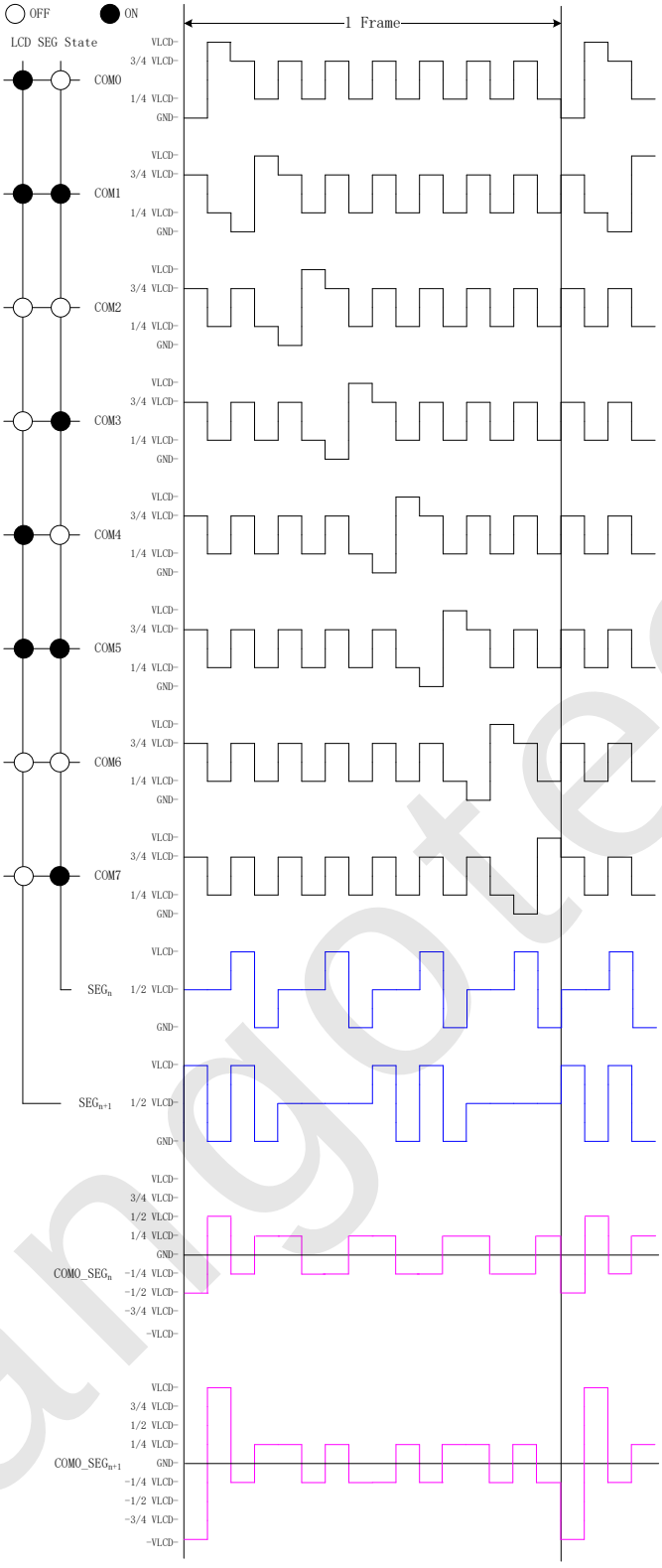


Figure 14-5 LCD Drive Waveform When an LCD Panel of 1/8 Duty and 1/4 Bias is Applied

14.6. Registers

Table 14-6 LCD Control Register (LCDCtrl, 0x2C1E)

0x2C1E, R/W, LCD Control Register, LCDCtrl		
Bit	Default	Description

0x2C1E, R/W, LCD Control Register, LCDCtrl			
Bit		Default	Description
Bit7	ON/OFF	0	To enable or disable the COM/SEG driver of the LCD driver. Set this bit to 1 to enable the COM/SEG driver to output COM and SEG signals to the LCD panel. Otherwise, this circuit outputs high impedance.
Bit6	6COMTYPE	0	When 1/6 Duty is applied, set this bit to 1 to enable each byte of display RAM to store content of one LCD segment. By default, every 6 bits of display RAM store content of 1 LCD segments in 1/6 Duty mode.
Bit[5:4]	LCDTYPE	0	To define LCD duty. 00: 1/4 Duty; 01: 1/6 Duty; 10/11: 1/8 Duty.
Bit3	DRV1	0	To set the resistance value of each resistor in the internal resistor ladder for bias voltage generation. 00: 300kΩ; 01: 600kΩ; 10: 150kΩ; 11: 200kΩ.
Bit2	DRV0	0	
Bit1	FRQ1	0	To configure the frame frequency. 11: 512Hz; 10: 256Hz; 01: 128Hz; 00: 64Hz.
Bit0	FRQ0	0	

Table 14-7 Enable/Disable CLK3

SFR 0x80, R/W, Clock Switchover Control Register, SysCtrl			
Bit		Default	Description
bit3	LCDG	0	Set this bit to 1 to stop CLK3. By default this clock is running. Only when the PLL clock is selected as the clock source for CLK1 and CLK2 can CLK3 be disabled.

Table 14-8 Register to Select Bias Mode

0x285C, R/W, Battery Discharge Control Register, CtrlBAT		
Bit	Default	Description

0x285C, R/W, Battery Discharge Control Register, CtrlBAT			
Bit		Default	Description
bit[7:4]	Reserved	0	These bits must hold their default values for proper operation.
bit3	LCDBMOD	0	When the LCD driver works in 1/8 duty mode, set this bit to select the bias ratio. 0: 1/3 Bias; 1: 1/4 Bias. When the LCD driver works in 1/4 or 1/6 duty mode, 1/3 Bias ratio is used whatever this bit is set.
bit[2:1]	IITU<1:0>	0	To adjust the bias current of the amplifier of the voltage channel ADC. 00: 0%; 01: -33%; 11:+33%; 10: 100%.
bit0	BATDISC	0	To enable discharging the battery. 1: enable; 0: disable.

Table 14-9 LCD Waveform Voltage Configuration 1

0x285E, R/W, LCD Driver Voltage Control Register, CtrlLCDV			
Bit		Default	Description
Bit7	DCENN	0	By default additional 10mV direct voltage offset is applied to the current input. Set this bit to 1 to disable this function. This bit must hold its default value for proper operation.
Bit[6:3]	Reserved	0	These bits must hold their default values for proper operation.
bit2	VLCD	0	To adjust the LCD waveform voltage. 0: 3.3V; 1: 3.0V.
bit[1:0]	Reserved	0	These bits must hold their default values for proper operation.

Table 14-10 LCD Waveform Voltage Configuration 2

0x2866, R/W, LDO Control Register, CtrlLDO		
Bit	Default	Description

0x2866, R/W, LDO Control Register, CtrlLDO			
Bit		Default	Description
Bit7	PDDET	0	Set this bit to 1 to disable the internal power detection circuit. By default this circuit is enabled. When the chip is 3.3V powered, users must set this bit to 1 to disable the power detection circuit, to prevent current leakage of the battery when a battery is connected to the device. When the chip is 5V powered, this bit must hold its default value.
Bit6	LDO3IT	0	Set this bit to 1 to increase bias current of LDO33 by 100%.
Bit[5:3]	LDO3SEL	0	To adjust output voltage of LDO33. 000: 3.3V; 001: 3.2V; 010/100/101: 3.5V; 011: 3.4V; 110: 3.1V; 111: 3.0V.
Bit[2:0]	LDOV2SEL<2:0>	0	To adjust output voltage of digital power circuit. 000: +0V; 001: -0.1V; 010: +0.2V; 011: +0.1V; 100: -0.4V; 101: -0.5V; 110: -0.2V; 111: -0.3V.

Table 14-11 SEG Control Registers (R/W)

Register		bit7	bit6	bit5	Bit4	bit3	bit2	bit1	bit0
0x2C1F	SegCtrl0	SEGON7	SEGON6	SEGON5	SEGON4	SEGON3	SEGON2	SEGON1	SEGON0
0x2C20	SegCtrl1	SEGON15	SEGON14	SEGON13	SEGON12	SEGON11	SEGON10	SEGON9	SEGON8
0x2C21	SegCtrl2	SEGON23	SEGON22	SEGON21	SEGON20	SEGON19	SEGON18	SEGON17	SEGON16
0x2C22	SegCtrl3	SEGON31	SEGON30	SEGON29	SEGON28	SEGON27	SEGON26	SEGON25	SEGON24
0x2C23	SegCtrl4	SEGON39	SEGON38	SEGON37	SEGON36	SEGON35	SEGON34	SEGON33	SEGON32
Default		0	0	0	0	0	0	0	0

0: to disable SEG signal output.

1: to enable SEG signal Output.

In the V98XX, the pins for SEG output are multiplexed by GPIO and analog input of M Channel. When these pins are configured for SEG output, they must be set to "input and output are disabled" for GPIO purpose. When the pins work as GPIO ports or for analog input of M Channel, they must be set to "disable SEG signal output" in these registers.

When bits LCDTYPE (bit[5:4] of LCDCtrl, 0x2C1E) are cleared, bit[1:0] of SegCtrl0 and SegCtrl1 are valid.

When bits LCDTYPE is set to 1, bit[1:0] of SegCtrl1 is valid, but bit[1:0] of SegCtrl0 is invalid.

When bits LCDTYPE is set to 2 or 3, bit[1:0] of SegCtrl1 and SegCtrl0 are invalid.

15. GPIO

In the V98XX there are 11 groups, P0~P10, 70 general-purpose input/output ports (GPIO) in total

of which:

- Ports of Group P0 are multiplexed by general input/output and JTAG interfaces. When the chip operates in metering mode, besides for general input/output, both P0.2 and P0.3 can be used to wake up the system from sleeping state. When the chip operates in debugging mode, these ports work as JTAG interfaces;
- Ports of Group P1 and P2 are multiplexed by general input/output and special functions. Both P1.3 and P1.4 can be used to wake up the system from sleeping state;
- Ports of Group P3 are multiplexed by general input/output and COM of the LCD driver;
- Ports of Group P4 and P5 are multiplexed by general input/output and COM or SEG output of the LCD driver;
- Ports of Group P6~P8 are multiplexed by general input/output and SEG output of the LCD driver;
- Ports of Group 9 are general-purpose input/output ports which has a communication rate of 200kbps when CLK1 frequency is 13.1072MHz. These ports are named *Fast IO* in this datasheet. These ports are multiplexed by general input/output and special functions;
- Ports of Group 10 are general-purpose input/output ports which has a communication rate of 200kbps when CLK1 frequency is 13.1072MHz. These ports are named *Fast IO* in this datasheet. These ports can be configured for transmitter data output and receiver data input of enhanced UART ports.

All the I/O ports have features:

- Ports of Group P0~P8 can be gate controlled simultaneously; Ports of Group P9 and P10 can be gate controlled independently;
- When POR/BOR, RSTn pin reset or WDT overflow event occurs, all ports will be reset to their default states: both input and output are disabled;
- In Sleep or Deep Sleep state, all ports hold their states;
- No pull-up or pull-down resistors are connected internally in all I/O ports.

15.1. P0

In Group P0 there are 4 ports, which are multiplexed by general-purpose input/output and JTAG interfaces.

When the level on the pin MODE1 is driven low, all ports of this group will work as JTAG interfaces. In this state, Port P0.0 is used for test data output (TDO); Port P0.1 is used for test data input (TDI); Port P0.2 is used for test mode select (TMS); Port P0.3 is used for test clock input (TCK).

When the level on the pin MODE1 is pulled high, all ports of this group will work as general-purpose input/output ports, and the input and output enable registers determine the state of each port. Set bit P0P8 (bit3 of PRCtrl0, 0x2D00) to 1 to gate control ports of Group P0~P8 to lower power consumption when these ports are not used. Besides, bit IOP0 (bit1 of IOWK, SFR 0xC9) determines both P0.2 and P0.3 to be used for IO wakeup inputs. See "IO Wakeup " for details.

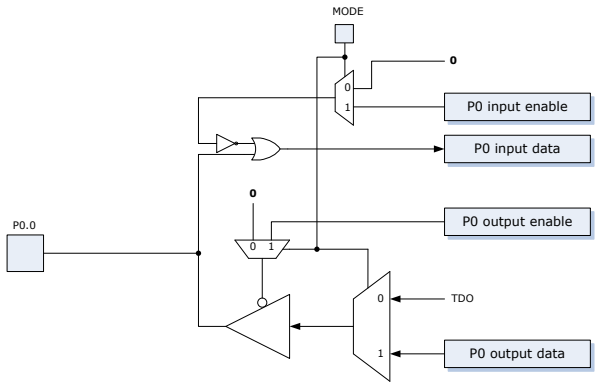


Figure 15-1 Architecture of P0.0

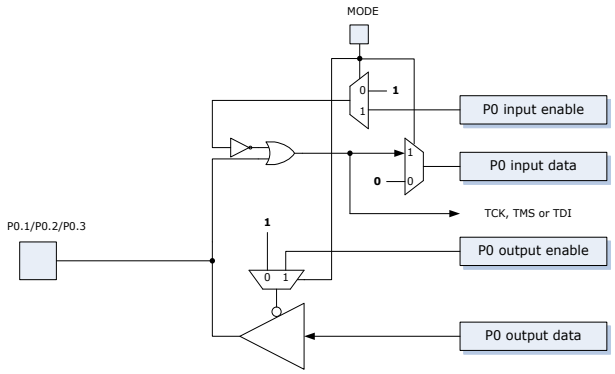


Figure 15-2 Architecture of P0.1/P0.2/P0.3

Table 15-1 P0 Output Enable Register (P0OE, 0x28A8)

0x28A8, R/W, P0 Output Enable Register, P0OE								
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
	-	-	-	-	P03OEN	P02OEN	P01OEN	P00OEN
Default	X	X	X	X	1	1	1	1
1: disable; 0: enable; X: do not care.								

Table 15-2 P0 Input Enable Register (P0IE, 0x28A9)

0x28A9, R/W, P0 Input Enable Register, P0IE								
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
	-	-	-	-	P03INEN	P02INEN	P01INEN	P00INEN
Default	X	X	X	X	0	0	0	0
1: enable; 0: disable; X: do not care.								

Table 15-3 P0 Output Data Register (P0OD, 0x28AA)

0x28AA, R/W, P0 Output Data Register, P0OD								
	bit7	Bit6	bit5	bit4	bit3	bit2	bit1	bit0
Default	X	X	X	X	1	1	1	1
X: do not care.								

Table 15-4 P0 Input Data Register (P0ID, 0x28AB)

0x28AB, R/W, P0 Input Data Register, P0ID								
	bit7	Bit6	bit5	bit4	bit3	bit2	bit1	bit0
Default	X	X	X	X	0	0	0	0

X: do not care.

the state change of an I/O port will lead to value variation of this register, which consumes more power. So to lower power consumption, it is recommended to disable data input if no need to read the input data.

15.2. P1

In Group P1 there are 5 ports, which are multiplexed by general-purpose input/output and special functions.

The function of each port can be configured via the dedicated special function register. When a port works as a general-purpose input/output port, the input and output enable registers determine its state. Set bit P0P8 (bit3 of PRCtrl0, 0x2D00) to 1 to gate control ports of Group P0~P8 to lower power consumption when these ports are not used. However, setting this bit to 1 after configuring these ports to work for special functions has no effect on its functions.

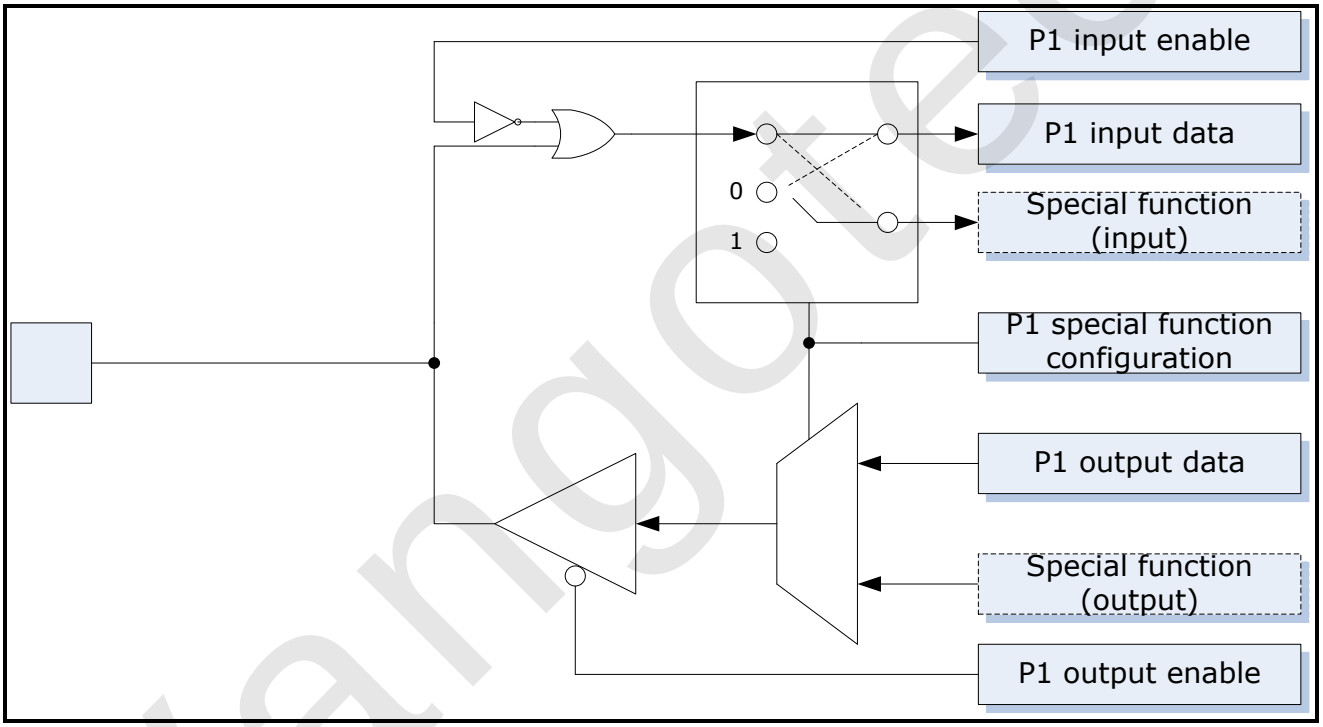


Figure 15-3 Architecture of Each Port of Group P1

If port P1.3 and/or P1.4 is set to "input enabled" before the system enters Sleep or Deep Sleep, the system will be woken up when a transition occurs to either port (either high-to-low or low-to-high, holding high and low level for at least 4 OSC clock cycles). See "IO Wakeup " for details.

Table 15-5 P1 Output Enable Register (P1OE, 0x28AC)

0x28AC, R/W, P1 Output Enable Register, P1OE								
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
	-	-	-	P14OEN	P13OEN	P12OEN	P11OEN	P10OEN
Default	X	X	X	1	1	1	1	1

1: disable; 0: enable; X: do not care.

Table 15-6 P1 Input Enable Register (P1IE, 0x28AD)

0x28AD, R/W, P1 Input Enable Register, P1IE

	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
	-	-	-	P14INEN	P13INEN	P12INEN	P11INEN	P10INEN
Default	X	X	X	0	0	0	0	0

1: enable; 0: disable; X: do not care.

Table 15-7 P1 Output Data Register (P1OD, 0x28AE)

0x28AE, R/W, P1 Output Data Register, P1OD

	bit7	Bit6	bit5	bit4	bit3	bit2	bit1	bit0
Default	X	X	X	1	1	1	1	1

X: do not care.

Table 15-8 P1 Input Data Register (P1ID, 0x28AF)

0x28AF, R/W, P1 Input Data Register, P1ID

	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Default	X	X	X	0	0	0	0	0

X: do not care.

When input is enabled, users can read the state of each I/O port via this register all the time, which is not affected by the special function of the port. But the state change of an I/O port will lead to value variation of this register, which consumes more power. So to lower power consumption, it is recommended to disable data input if no need to read the input data.

Table 15-9 P1.0 Special Function Register (P10FS, 0x28C4, R/W)

Bit		Default	Description
Bit[7:2]	Reserved.	0	
Bit[1:0]	P10FNC1 P10FNC0	0	00: GPIO, general-purpose input/output port; 01: SP, pulse per second (PPS) output from the RTC. On calibrating the RTC, every 30 seconds, from the 1st to 29th second, an un-calibrated pulse is output every second, and in the 30th second, a calibrated pulse is output that averages the period of each pulse in the 30 seconds to be 1s.

Table 15-10 P1.1 Special Function Register (P11FS, 0x28C5, R/W)

Bit		Default	Description
Bit[7:3]	Reserved.	0	

Bit		Default	Description
Bit[2:0]	P11FNC2 P11FNC1 P11FNC0	0	000: GPIO, general-purpose input/output port; 010: RXD1, receiver data input of UART1; 011: T1, Timer1 external input; 100: IO interrupt input 2.

Table 15-11 P1.2 Special Function Register (P12FS, 0x28C6, R/W)

Bit		Default	Description
Bit[7:3]	Reserved.	0	
Bit[2:0]	P12FNC2 P12FNC1 P12FNC0	0	000: GPIO, general-purpose input/output port; 001: reserved; 010: TXD1, transmitter data output of UART1; 011: T2EX, Timer2 capture or reload trigger input; 100: IO interrupt input 3.

Table 15-12 P1.3 Special Function Register (P13FS, 0x28C7, R/W)

Bit		Default	Description
Bit[7:3]	Reserved.	0	
Bit[2:0]	P13FNC2 P13FNC1 P13FNC0	0	000: GPIO, general-purpose input/output port; 001: CF2, CF pulse output of E2 path; 010: RXD5, receiver data input of UART5; 011: IO interrupt input 0; 100: CF1, CF pulse output of E1 path; 101: SP, pulse per second (PPS) output from the RTC. On calibrating the RTC, every 30 seconds, from the 1st to 29th second, an un-calibrated pulse is output every second, and in the 30th second, a calibrated pulse is output that averages the period of each pulse in the 30 seconds to be 1s. 110: PLLDIV, pulse output proportional to the divided PLL clock frequency, can be configured to output pulses of 1s width from the PLL counter.

Table 15-13 P1.4 Special Function Register (P14FS, 0x28C8)

Bit		Default	Description
Bit[7:2]	Reserved.	0	
Bit[1:0]	P14FNC1 P14FNC0	0	000: GPIO, general-purpose input/output port; 001: PLLDIV, pulse output proportional to the divided PLL clock frequency,

Bit		Default	Description
			can be configured to output pulses of 1s width from the PLL counter; 010: TXD5, transmitter data output of UART5; 011: IO interrupt input 1.

15.3. P2

In Group P2 there are 6, which are multiplexed by general-purpose input/output and special functions.

The function of each port can be configured via the dedicated special function register. When a port works as a general-purpose input/output port, the input and output enable registers determine its state. Set bit P0P8 (bit3 of PRCtrl0, 0x2D00) to 1 to gate control ports of Group P0~P8 to lower power consumption when these ports are not used. However, setting this bit to 1 after configuring these ports to work for special functions has no effect on its functions.

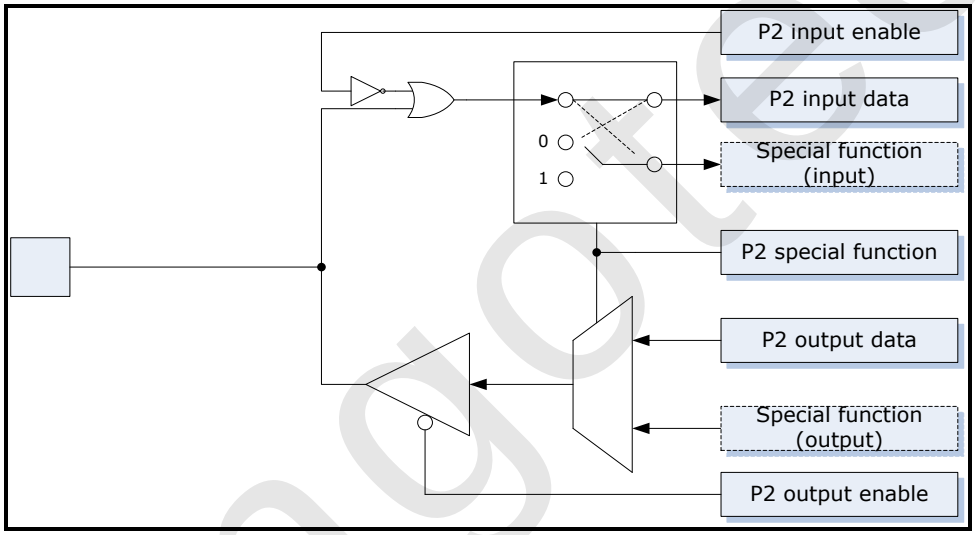


Figure 15-4 Architecture of Each Port of Group P2

Table 15-14 P2 Output Enable Register (P2OE, 0x28B0)

0x28B0, R/W, P2 Output Enable Register, P2OE								
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
	-	-	P25OEN	P24OEN	P23OEN	P22OEN	P21OEN	P20OEN
Default	X	X	1	1	1	1	1	1
1: disable; 0: enable; X: do not care.								

Table 15-15 P2 Input Enable Register (P2IE, 0x28B1)

0x28B1, R/W, P2 Input Enable Register, P2IE								
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
	-	-	P25INEN	P24INEN	P23INEN	P22INEN	P21INEN	P20INEN

Default	X	X	0	0	0	0	0	0
1: enable; 0: disable; X: do not care.								

Table 15-16 P2 Output Data Register (P2OD, 0x28B2)

0x28B2, R/W, P2 Output Data Register, P2OD								
	bit7	Bit6	bit5	bit4	bit3	bit2	bit1	bit0
Default	X	X	1	1	1	1	1	1
X: do not care.								

Table 15-17 P2 Input Data Register (P2ID, 0x28B3)

0x28B3, R/W, P2 Input Data Register, P2ID								
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Default	X	X	0	0	0	0	0	0
X: do not care. When input is enabled, users can read the state of each I/O port via this register all the time, which is not affected by the special function of the port. But the state change of an I/O port will lead to value variation of this register, which consumes more power. So to lower power consumption, it is recommended to disable data input if no need to read the input data.								

Table 15-18 P2.0 Special Function Register (P20FS, 0x28C9, R/W)

Bit		Default	Description
Bit[7:2]	Reserved.	0	
Bit[1:0]	P20FNC1 P20FNC0	0	00: GPIO, general-purpose input/output port; 01: OSC, OSC clock waveform output; 10: RXD4, receiver data input of UART4; 11: T2, Timer2 external input.

Table 15-19 P2.1 Special Function Register (P21FS, 0x28CA, R/W)

Bit		Default	Description
Bit[7:2]	Reserved.	0	
Bit[1:0]	P21FNC1 P21FNC0	0	00: GPIO, general-purpose input/output port; 01: reserved; 10: TXD4, transmitter data output of UART4; 11: T0, Timer0 external input.

Table 15-20 P2.2 Special Function Register (P22FS, 0x28CB, R/W) (V98XX)

Bit		Default	Description
Bit[7:2]	Reserved.	0	
Bit[1:0]	P22FNC1 P22FNC0	0	00: GPIO, general-purpose input/output port; 10: RXD3, receiver data input of UART3; 01/11: reserved.

Table 15-21 P2.3 Special Function Register (P23FS, 0x28CC, R/W) (V98XX)

Bit		Default	Description
Bit[7:2]	Reserved.	0	
Bit[1:0]	P23FNC1 P23FNC0	0	00: GPIO, general-purpose input/output port; 10: TXD3, transmitter data output of UART3.

Table 15-22 P2.4 Special Function Register (P24FS, 0x28CD, R/W)

Bit		Default	Description
Bit[7:2]	Reserved	0	
Bit[1:0]	P24FNC1 P24FNC0	0	00: GPIO, general-purpose input/output port; 10: RXD2, receiver data input of UART2.

Table 15-23 P2.5 Special Function Register (P25FS, 0x28CE, R/W)

Bit		Default	Description
Bit[7:2]	Reserved	0	
Bit[1:0]	P25FNC1 P25FNC0	0	00: GPIO, general-purpose input/output port; 10: TXD2, transmitter data output of UART2. This port can be configured to transmit 38kHz carrier wave.

15.4. P3

In Group P3 there are 4 ports, which are multiplexed by general-purpose input/output andCOM.

When a port works as COM, in input and output enable registers the corresponding bit must be configured "input disabled, output disabled".

When a port works as a general-purpose input/output port, the SEG/COM driver in the LCD driver must be disabled (bit7 of LCDCtrl, 0x2C1E). Set bit P0P8 (bit3 of PRCtrl0, 0x2D00) to 1 to gate control ports of Group P0~P8 to lower power consumption when these ports are not used.

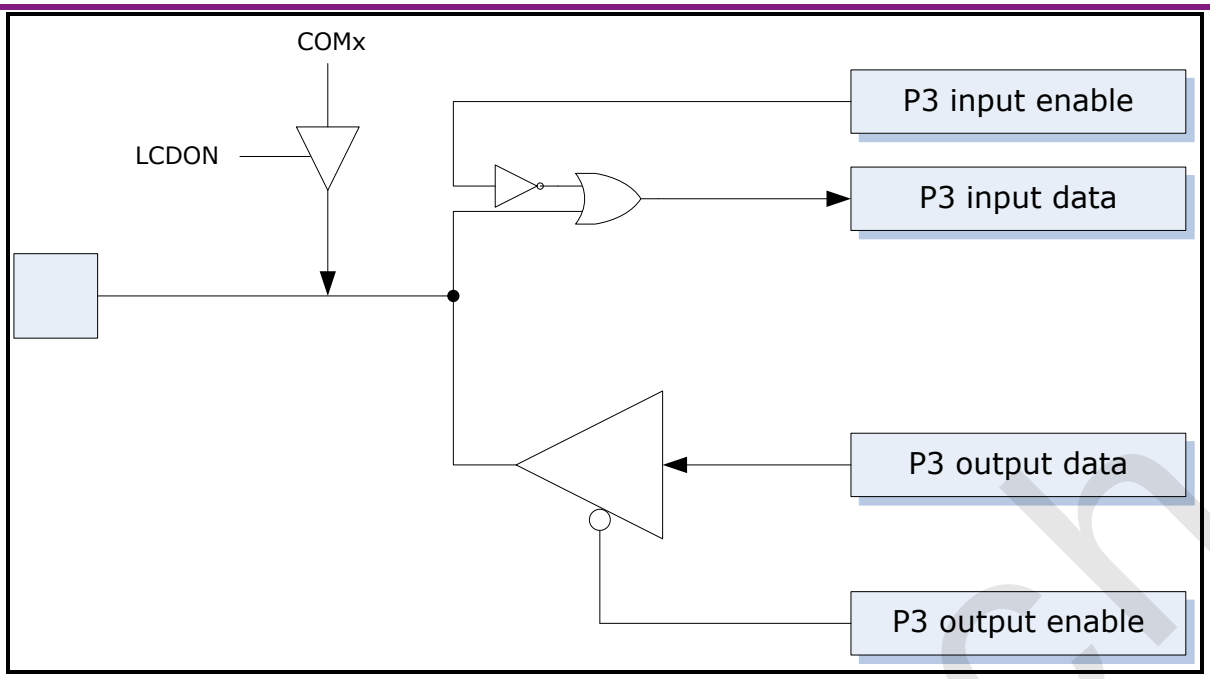


Figure 15-5 Architecture of Each Port of Group P3

Table 15-24 P3 Output Enable Register (P3OE, 0x28B4)

0x28B4, R/W, P3 Output Enable Register, P3OE								
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
	-	-	-	-	P33OEN	P32OEN	P31OEN	P30OEN
Default	X	X	X	X	1	1	1	1
1: disable; 0: enable; X: do not care.								

Table 15-25 P3 Input Enable Register (P3IE, 0x28B5)

0x28B5, R/W, P3 Input Enable Register, P3IE								
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
	-	-	-	-	P33INEN	P32INEN	P31INEN	P30INEN
Default	X	X	X	X	0	0	0	0
1: enable; 0: disable; X: do not care.								

Table 15-26 P3 Output Data Register (P3OD, 0x28B6)

0x28B6, R/W, P3 Output Data Register, P3OD								
	bit7	Bit6	bit5	bit4	bit3	bit2	bit1	bit0
Default	X	X	X	X	1	1	1	1
X: do not care.								

Table 15-27 P3 Input Data Register (P3ID, 0x28B7)

0x28B7, R/W, P3 Input Data Register, P3ID

	bit7	Bit6	bit5	bit4	bit3	bit2	bit1	bit0
Default	X	X	X	X	0	0	0	0
X: do not care.								

15.5. P4

In Group P4 there are 8 ports, which are multiplexed by General-Purpose Input/Output (GPIO) and signal output of the LCD driver.

When LCDTYPE=0 Ports P4.0~P4.7 can be configured to be multiplexed by SEG output and general-purpose input/output. When LCDTYPE=1/2/3, P4.0~ P4.7 are multiplexed by COM output and general-purpose input/output.

When a port works as backplanes or SEG output of the LCD driver, in input and output enable registers, P4OE (0x28B8) and P4IE (0x28B9), the corresponding bit must be configured "input disabled, output disabled".

When a port works as a general-purpose input/output port, the SEG output on the corresponding port must be disabled and input and output enable registers determine its state. Set bit P0P8 (bit3 of PRCtrl0, 0x2D00) to 1 to gate control ports of Group P0~P8 to lower power consumption when these ports are not used.

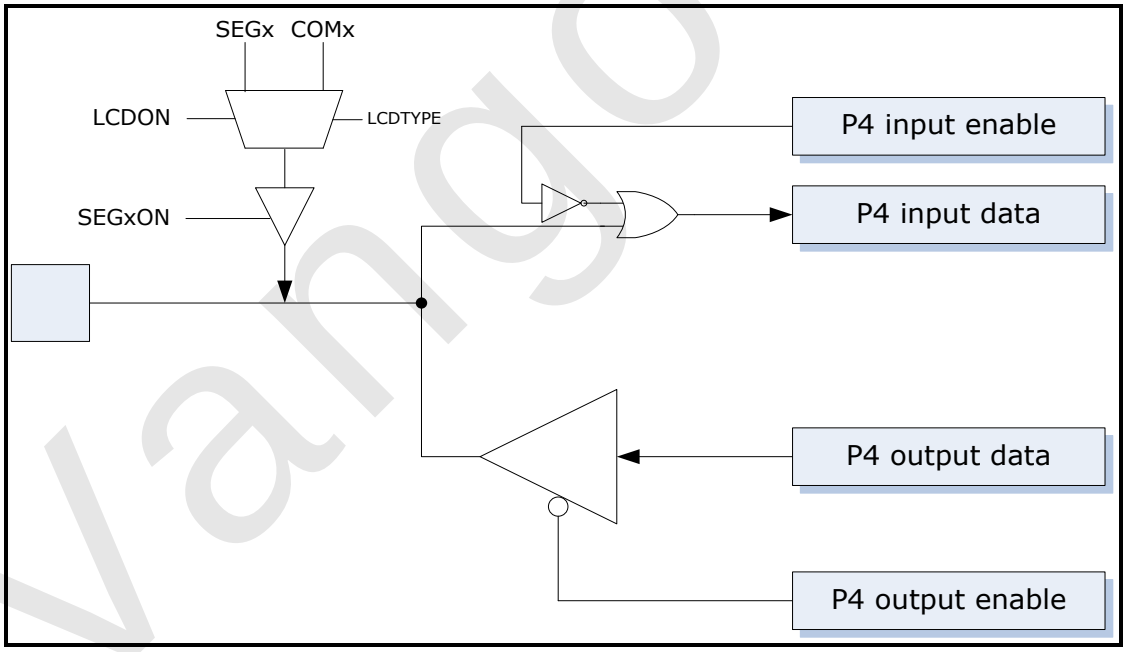


Figure 15-6 Architecture of Each Port of Group P4

Table 15-28 P4 Output Enable Register (P4OE, 0x28B8)

0x28B8, R/W, P4 Output Enable Register, P4OE								
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
	P47OEN	P46OEN	P45OEN	P44OEN	P43OEN	P42OEN	P41OEN	P40OEN
Default	1	1	1	1	1	1	1	1

1: disable; 0: enable; X: do not care.

Table 15-29 P4 Input Enable Register (P4IE, 0x28B9)

0x28B9, R/W, P4 Input Enable Register, P4IE

	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
	P47INEN	P46INEN	P45INEN	P44INEN	P43INEN	P42INEN	P41INEN	P40INEN
Default	0	0	0	0	0	0	0	0

1: enable; 0: disable; X: do not care.

Table 15-30 P4 Output Data Register (P4OD, 0x28BA)

0x28BA, R/W, P4 Output Data Register, P4OD

	bit7	Bit6	bit5	bit4	bit3	bit2	bit1	bit0
Default	1	1	1	1	1	1	1	1

X: do not care.

Table 15-31 P4 Input Data Register (P4ID, 0x28BB)

0x28BB, R/W, P4 Input Data Register, P4ID

	bit7	Bit6	bit5	bit4	bit3	bit2	bit1	bit0
Default	X	X	X	X	X	X	X	X

X: do not care.

When input is enabled, users can read the state of each I/O port via this register all the time, which is not affected by the special function of the port. But the state change of an I/O port will lead to value variation of this register, which consumes more power. So to lower power consumption, it is recommended to disable data input if no need to read the input data.

15.6. P5

In Group P5 there are 8 ports, which are multiplexed by general-purpose input/output and COM of the LCD driver.

Ports P5.0 and P5.1 can be configured to be multiplexed by SEG output and general-purpose input/output; when LCDTYPE=0 or 1, when LCDTYPE=2or3, and ports P5.2-P5.7 are multiplexed by SEG output and general-purpose input/output.

When a port works as COM or SEG output of the LCD driver, in input and output enable registers, the corresponding bit must be configured "input disabled, output disabled".

When a port works as a general-purpose input/output port, SEG or COM output on the corresponding port must be disabled, and input and output enable registers determine its state. Set bit P0P8 (bit3 of PRCtrl0, 0x2D00) to 1 to gate control ports of Group P0~P8 to lower power consumption when these ports

are not used.

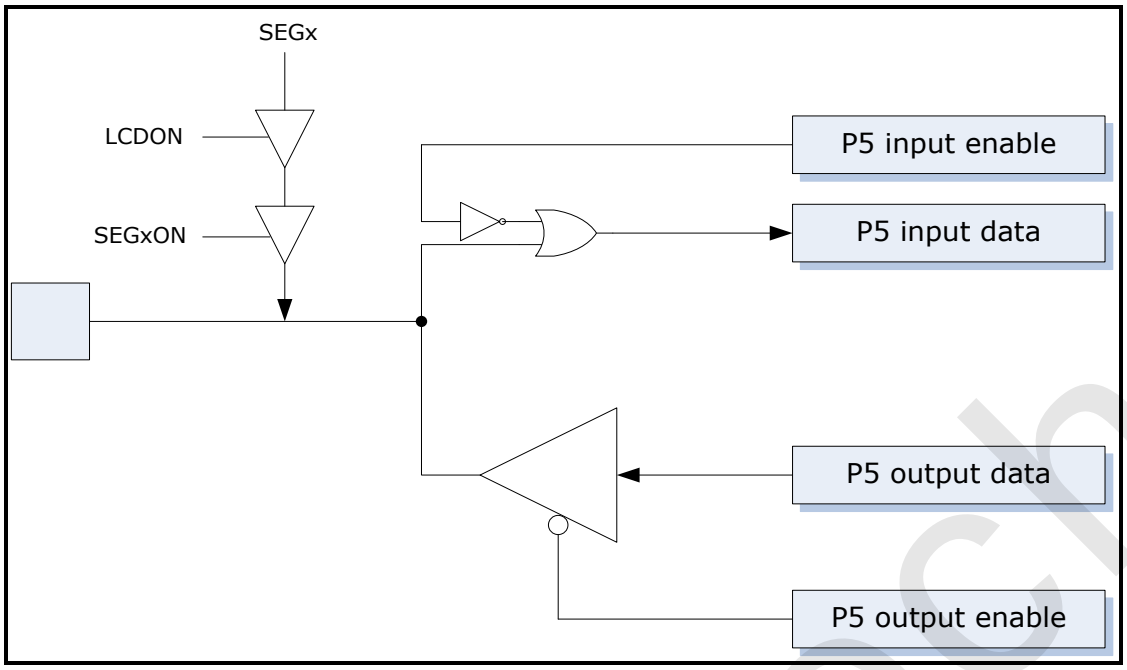


Figure 15-7 Architecture of Each Port of Group P5

Table 15-32 P5 Output Enable Register (P5OE, 0x28BC)

0x28BC, R/W, P5 Output Enable Register, P5OE								
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
	P57OEN	P56OEN	P55OEN	P54OEN	P53OEN	P52OEN	P51OEN	P50OEN
Default	1	1	1	1	1	1	1	1
1: disable; 0: enable; X: do not care.								

Table 15-33 P5 Input Enable Register (P5IE, 0x28BD)

0x28BD, R/W, P5 Input Enable Register, P5IE								
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
	P57INEN	P56INEN	P55INEN	P54INEN	P53INEN	P52INEN	P51INEN	P50INEN
Default	0	0	0	0	0	0	0	0
1: enable; 0: disable; X: do not care.								

Table 15-34 P5 Output Data Register (P5OD, 0x28BE)

0x28BE, R/W, P5 Output Data Register, P5OD								
	bit7	Bit6	bit5	bit4	bit3	bit2	bit1	bit0
Default	1	1	1	1	1	1	1	1

Table 15-35 P5 Input Data Register (P5ID, 0x28BF)

0x28BF, R/W, P5 Input Data Register, P5ID

	bit7	Bit6	bit5	bit4	bit3	bit2	bit1	bit0
Default	0	0	0	0	0	0	0	0

When input is enabled, users can read the state of each I/O port via this register all the time, which is not affected by the special function of the port. But the state change of an I/O port will lead to value variation of this register, which consumes more power. So to lower power consumption, it is recommended to disable data input if no need to read the input data.

15.7. P6

In Group P6 there are 8 ports, which are multiplexed by general-purpose input/output and SEG output of the LCD driver.

When a port works as SEG output of the LCD driver, in input and output enable registers, the corresponding bit must be configured "input disabled, output disabled".

When a port works as a general-purpose input/output port, SEG output on the corresponding port must be disabled, and input and output enable registers determine its state. Set bit P0P8 (bit3 of PRCtrl0, 0x2D00) to 1 to gate control ports of Group P0~P8 to lower power consumption when these ports are not used.

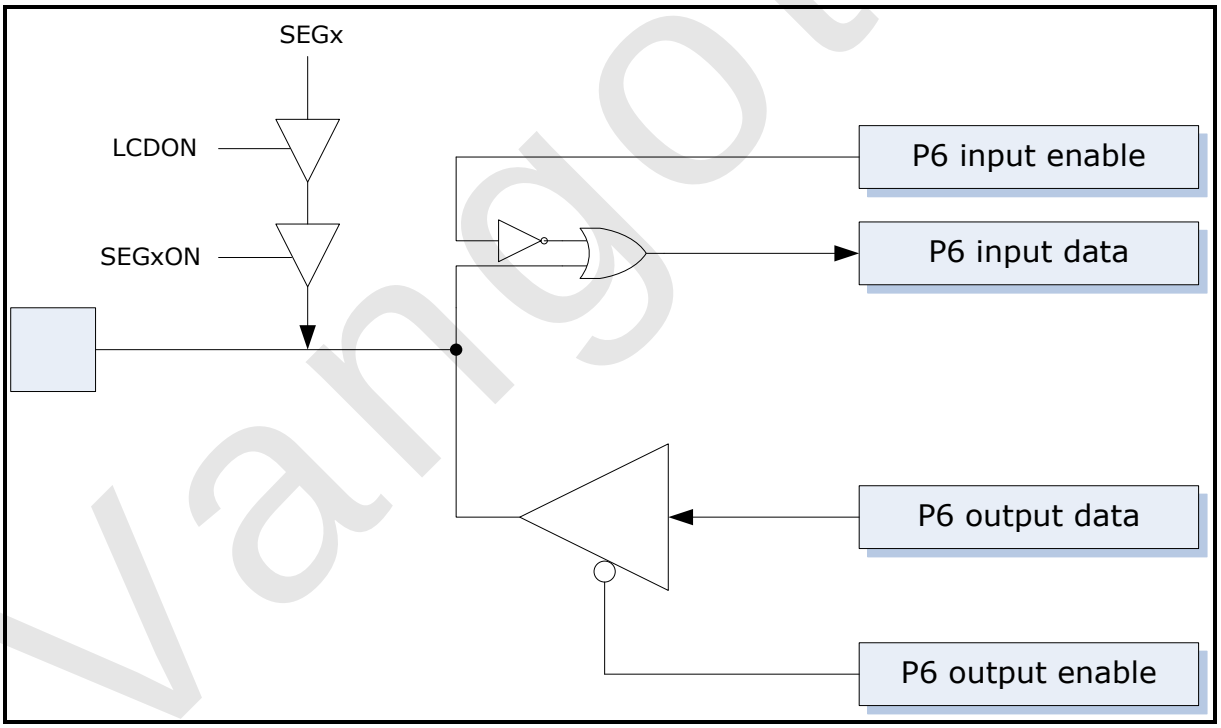


Figure 15-8 Architecture of Each Port of Group P6

Table 15-36 P6 Output Enable Register (P6OE, 0x28C0)

0x28C0, R/W, P6 Output Enable Register, P6OE								
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0

	P67OEN	P66OEN	P65OEN	P64OEN	P63OEN	P62OEN	P61OEN	P60OEN
Default	1	1	1	1	1	1	1	1

1: disable; 0: enable; X: do not care.

Table 15-37 P6 Input Enable Register (P6IE, 0x28C1)

0x28C1, R/W, P6 Input Enable Register, P6IE

	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
	P67INEN	P66INEN	P65INEN	P64INEN	P63INEN	P62INEN	P61INEN	P60INEN
Default	0	0	0	0	0	0	0	0

1: enable; 0: disable; X: do not care.

Table 15-38 P6 Output Data Register (P6OD, 0x28C2)

0x28C2, R/W, P6 Output Data Register, P6OD

	bit7	Bit6	bit5	bit4	bit3	bit2	bit1	bit0
Default	1	1	1	1	1	1	1	1

X: do not care.

Table 15-39 P6 Input Data Register (P6ID, 0x28C3)

0x28C3, R/W, P6 Input Data Register, P6ID

	bit7	Bit6	bit5	bit4	bit3	bit2	bit1	bit0
Default	0	0	0	0	0	0	0	0

X: do not care.

When input is enabled, users can read the state of each I/O port via this register all the time, which is not affected by the special function of the port. But the state change of an I/O port will lead to value variation of this register, which consumes more power. So to lower power consumption, it is recommended to disable data input if no need to read the input data.

15.8. P7

In Group P7 there are 8 ports, which are multiplexed by general-purpose input/output and SEG output of the LCD driver.

When a port works as SEG output of the LCD driver, in input and output enable registers the corresponding bit must be configured "input disabled, output disabled".

When a port works as a general-purpose input/output port, the SEG output on the corresponding ports must be disabled and input and output enable registers determine its state. Set bit P0P8 (bit3 of PRCtrl0, 0x2D00) to 1 to gate control ports of Group P0~P8 to lower power consumption when these ports are not

used.

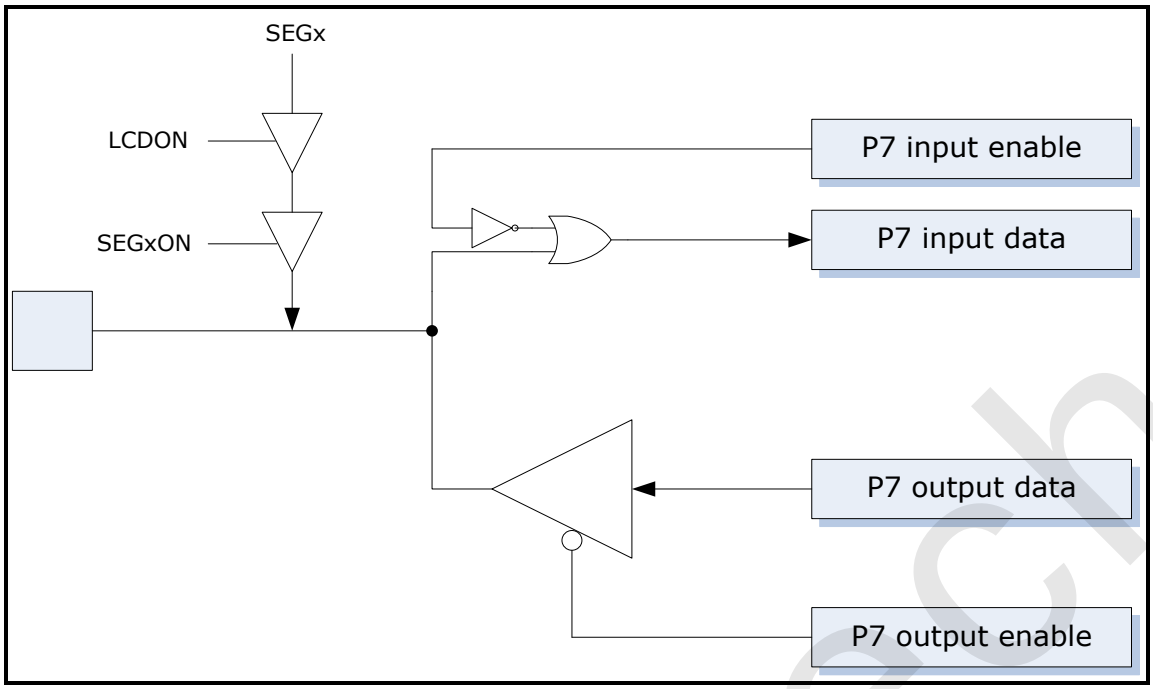


Figure 15-9 Architecture of Each Port of Group P7

Table 15-40 P7 Output Enable Register (P7OE, 0x28D5)

0x28D5, R/W, P7 Output Enable Register, P7OE								
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
	P77OEN	P76OEN	P75OEN	P74OEN	P73OEN	P72OEN	P71OEN	P70OEN
Default	1	1	1	1	1	1	1	1
1: disable; 0: enable; X: do not care.								

Table 15-41 P7 Input Enable Register (P7IE, 0x28D6)

0x28D6, R/W, P7 Input Enable Register, P7IE								
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
	P77INEN	P76INEN	P75INEN	P74INEN	P73INEN	P72INEN	P71INEN	P70INEN
Default	0	0	0	0	0	0	0	0
1: enable; 0: disable; X: do not care.								

Table 15-42 P7 Output Data Register (P7OD, 0x28D7)

0x28D7, R/W, P7 Output Data Register, P7OD								
	bit7	Bit6	bit5	bit4	bit3	bit2	bit1	bit0
Default	1	1	1	1	1	1	1	1

Table 15-43 P7 Input Data Register (P7ID, 0x28D8)

0x28D8, R/W, P7 Input Data Register, P7ID								
	bit7	Bit6	bit5	bit4	bit3	bit2	bit1	bit0
Default	0	0	0	0	0	0	0	0
When input is enabled, users can read the state of each I/O port via this register all the time, which is not affected by the special function of the port. But the state change of an I/O port will lead to value variation of this register, which consumes more power. So to lower power consumption, it is recommended to disable data input if no need to read the input data.								

15.9. P8

In Group P8 there are 3 ports, which are multiplexed by general-purpose input/output and SEG output of the LCD driver.

When a port works as SEG output of the LCD driver, in input and output enable registers, the corresponding bit must be configured "input disabled, output disabled".

When a port works as a general-purpose input/output port, the SEG output on the corresponding port must be disabled, and input/output enable registers determine its state. Set bit P0P8 (bit3 of PRCtrl0, 0x2D00) to 1 to gate control ports of Group P0~P8 to lower power consumption when these ports are not used.

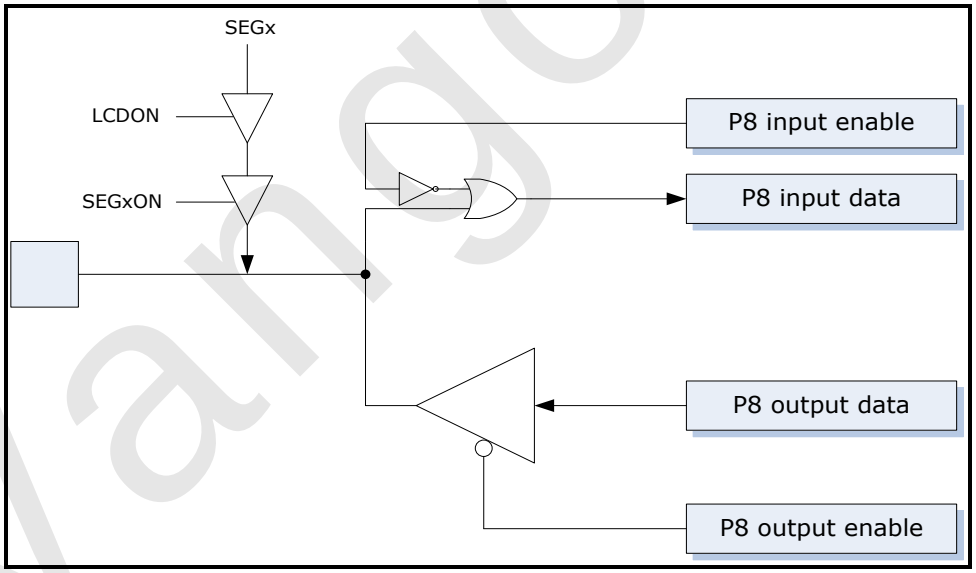


Figure 15-10 Architecture of Each Port of Group P8

Table 15-44 P8 Output Enable Register (P8OE, 0x28D9)

0x28D9, R/W, P8 Output Enable Register, P8OE								
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
	-	-	-	-	-	P82OEN	P81OEN	P80OEN
Default	X	X	X	X	X	1	1	1

1: disable; 0: enable; X: do not care.

Table 15-45 P8 Input Enable Register (P8IE, 0x28DA)

0x28DA, R/W, P8 Input Enable Register, P8IE								
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
	-	-	-	-	-	P82INEN	P81INEN	P80INEN
Default	X	X	X	X	X	0	0	0
1: enable; 0: disable; X: do not care.								

Table 15-46 P8 Output Data Register (P8OD, 0x28DB)

0x28DB, R/W, P8 Output Data Register, P8OD								
	bit7	Bit6	bit5	bit4	bit3	bit2	bit1	bit0
Default	X	X	X	X	X	1	1	1
X: do not care.								

Table 15-47 P8 Input Data Register (P8ID, 0x28DC)

0x28DC, R/W, P8 Input Data Register, P8ID								
	bit7	Bit6	bit5	bit4	bit3	bit2	bit1	bit0
Default	X	X	X	X	X	0	0	0
X: do not care. When input is enabled, users can read the state of each I/O port via this register all the time, which is not affected by the special function of the port. But the state change of an I/O port will lead to value variation of this register, which consumes more power. So to lower power consumption, it is recommended to disable data input if no need to read the input data.								

15.10. P9

In Group P9 there are 8 ports, which are multiplexed by general-purpose input/output, special functions and, P1.2 and P1.3 can be used GPSI.

When the ports work as general-purpose input/output ports, When CLK1 frequency is 13.1072MHz, the communication rate of these ports is 200kbps; input and output enable registers determine their states. But when a reference pulse of exact one second width is input to the port P9.1, the input of this port is enabled automatically.

The function of each port can be configured via the register P9FS (SFR 0xAD).

When bit GPSI (bit6 of PRCtrl0, 0x2D00) is set to 1, port P9.1 and P9.2 are used for serial data and clock delivery for general-purpose serial interface (GPSI). In this condition, P9.1 must be set to "input enabled" The P9.1 output is determined by the data on SDA; and P9.2 is set to "output enabled" automatically，Don't

need to configure P9.1 and P9.2 output register.

The port P9.0 can be used for SEG output of the LCD driver. When the port works as SEG output of the LCD driver, in input and output enable registers, the corresponding bit must be configured "input disabled, output disabled".

Set bit P9 (bit4 of PRCtrl0, 0x2D00) to 1 to gate control ports of Group P9 to lower power consumption.

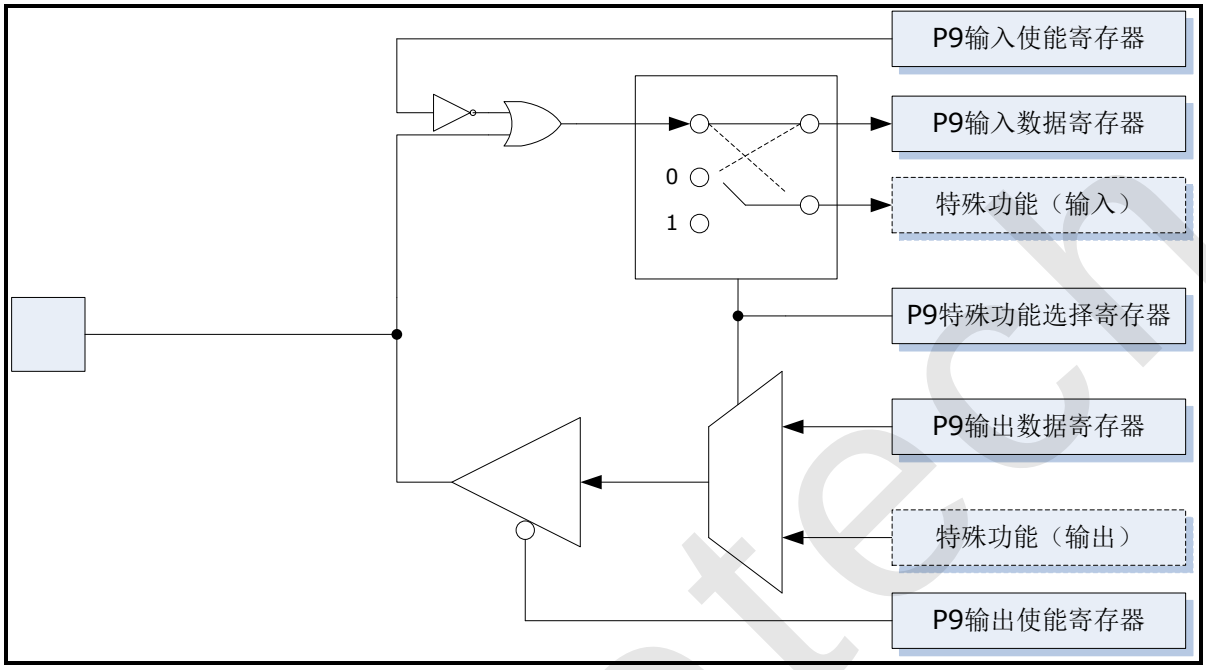


Figure 15-11 Architecture of Each Port of Group P9

Table 15-48 P9 Output Enable Register (P9OE, SFR 0xA4)

SFR 0xA4, R/W, P9 Output Enable Register, P9OE								
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
	P97OEN	P96OEN	P95OEN	P94OEN	P93OEN	P92OEN	P91OEN	P90OEN
Default	1	1	1	1	1	1	1	1
1: disable; 0: enable; X: do not care.								

Table 15-49 P9 Input Enable Register (P9IE, SFR 0xA5)

SFR 0xA5, R/W, P9 Input Enable Register, P9IE								
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
	P97INEN	P96INEN	P95INEN	P94INEN	P93INEN	P92INEN	P91INEN	P90INEN
Default	0	0	0	0	0	0	0	0
1: enable; 0: disable; X: do not care.								

Table 15-50 P9 Output Data Register (P9OD, SFR 0xA6)

SFR 0xA6, R/W, P9 Output Data Register, P9OD

	bit7	Bit6	bit5	bit4	bit3	bit2	bit1	bit0
Default	1	1	1	1	1	1	1	1

Table 15-51 P9 Input Data Register (P9ID, SFR 0xA7)

SFR 0xA7, R/W, P9 Input Data Register, P9ID

	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Default	0	0	0	0	0	0	0	0

When input is enabled, users can read the state of each I/O port via this register all the time, which is not affected by the special function of the port. But the state change of an I/O port will lead to value variation of this register, which consumes more power. So to lower power consumption, it is recommended to disable data input if no need to read the input data.

Table 15-52 P9 Special Function Register (P9FS, SFR 0xAD)

SFR 0xAD, R/W, P9 Special Function Register, P9FS

Bit		Description
Bit7	P97FNC	To configure the function of the port P9.7. 1: PWMCLK, PWM pulse output; 0: general-purpose input/output port in fast mode.
Bit6	P96FNC	To configure the function of the port P9.6. 1: CF1, CF pulse output of E1 path; 0: general-purpose input/output port in fast mode.
Bit5	P95FNC	To configure the function of the port P9.5. 1: CF2, CF pulse output of E2 path; 0: general-purpose input/output port in fast mode.
Bit4	P94FNC	To configure the function of the port P9.4. 1: SP, Pulse per second (PPS) output from the RTC. On calibrating the RTC, every 30 seconds, from the 1st to 29th second, an un-calibrated pulse is output every second, and in the 30th second, a calibrated pulse is output that averages the period of each pulse in the 30 seconds to be 1s; 0: general-purpose input/output port in fast mode.
Bit3	P93FNC	To configure the function of the port P9.3. 1: PLLDIV, pulse output proportional to the divided PLL clock frequency, can be configured to output pulses of 1s width from the PLL counter; 0: general-purpose input/output port in fast mode.
Bit2	P92FNC	To configure the function of the port P9.2.

Bit		Description
		1: TA2, to input/output the signals for Timer A Compare/Capture Module 2;
		0: general-purpose input/output port in fast mode.
Bit1	P91FNC	To configure the function of the port P9.1.
		1: TA1, to input/output the signals for Timer A Compare/Capture Module 1;
		0: general-purpose input/output port in fast mode.
Bit0	P90FNC	To configure the function of the port P9.0.
		1: TA0, to input/output the signals for Timer A Compare/Capture Module 0;
		0: general-purpose input/output port in fast mode.

15.11. P10

In Group P10 there are 8 ports, which are multiplexed by general-purpose input/output and enhanced UART interfaces. the port P10.0 is used for data input and output of EUART1. the port P10.1 is used for data output of EUART2, and the port P10.2 is used for data input of EUART2.

When the ports work as general-purpose input/output ports, the ports of Group P10 have the same feature with those of Group P9. They are accessed in a fast mode. When CLK1 frequency is 13.1072MHz, the communication rate of these ports is 200kbps. Input and output enable registers determine their states.

When the bit ENABLE (bit0 of CFGA, 0x2A05) is set to 1, the port P10.0 is used for data input and output of EUART1. In this condition, the output of this port is enabled automatically, and the input of this port is determined by the register P10IE (SFR 0xAA). When the bit ENABLE (bit0 of CFGB, 0x2B05) is set to 1, the port P10.1 is used for data output of EUART2, and the port P10.2 is used for data input of EUART2.In this condition, the output or input of the ports are determined by registers P10OE (SFR 0xA9) and P10IE (SFR 0xAA).

Set bit P10 (bit5 of PRCtrl0, 0x2D00) to 1 to gate control ports of Group P10 to lower power consumption when these ports are not used.

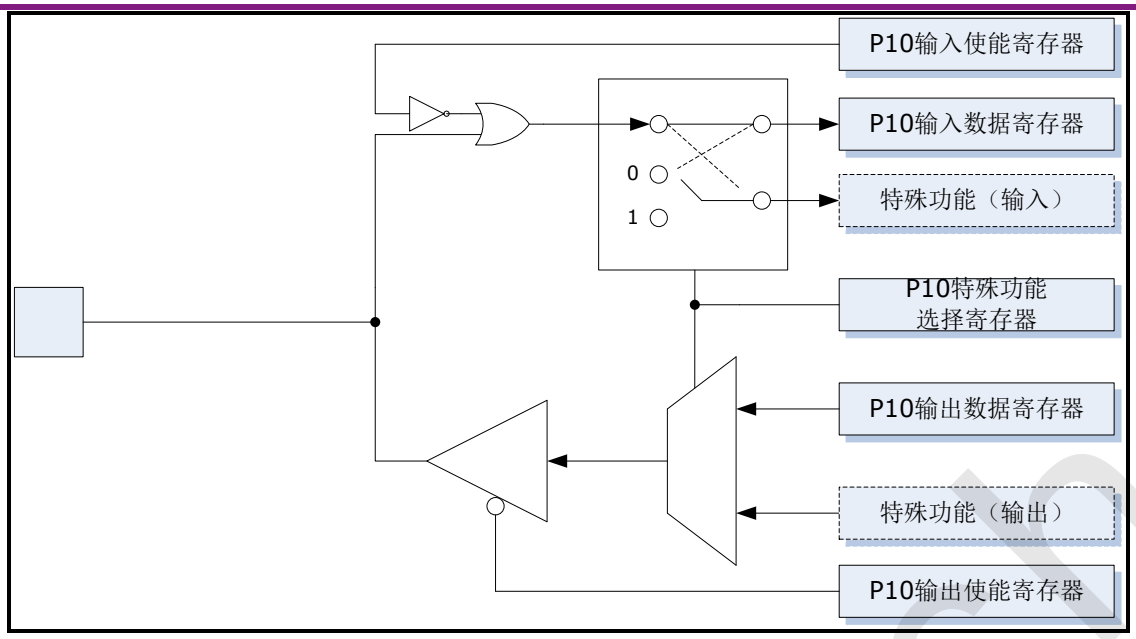


Figure 15-12 Architecture of Each Port of Group P10

Table 15-53 P10 Output Enable Register (P10OE, SFR 0xA9)

SFR 0xA9, R/W, P10 Output Enable Register, P10OE								
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
	P107OEN	P106OEN	P105OEN	P104OEN	P103OEN	P102OEN	P101OEN	P100OEN
Default	1	1	1	1	1	1	1	1
1: disable; 0: enable; X: do not care.								

Table 15-54 P10 Input Enable Register (P10IE, SFR 0xAA)

SFR 0xAA, R/W, P10 Input Enable Register, P10IE								
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
	P107INEN	P106INEN	P105INEN	P104INEN	P103INEN	P102INEN	P101INEN	P100INEN
Default	0	0	0	0	0	0	0	0
1: enable; 0: disable; X: do not care.								

Table 15-55 P10 Output Data Register (P10OD, SFR 0xAB)

SFR 0xAB, R/W, P10 Output Data Register, P10OD								
	bit7	Bit6	bit5	bit4	bit3	bit2	bit1	bit0
Default	1	1	1	1	1	1	1	1

Table 15-56 P10 Input Data Register (P10ID, SFR 0xAC)

SFR 0xAC, R/W, P10 Input Data Register, P10ID

	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Default	0	0	0	0	0	0	0	0

When input is enabled, users can read the state of each I/O port via this register all the time, which is not affected by the special function of the port. But the state change of an I/O port will lead to value variation of this register, which consumes more power. So to lower power consumption, it is recommended to disable data input if no need to read the input data.

Table 15-57 Configuration for EUART Communication

	0x2A05/0x2B05, R/W, EUART1/2 Configuration Register, CFGA/CFGB		
Bit		Default	Description
Bit7	OVIE	0	1, Enable the interrupt for Rx overflow。
Bit6	SDIE	0	1, Ebable the Tx interrupt； 0, Disable the Tx interrupt。
Bit5	RCIE	0	1, Enable the Rx interrupt； 0, Disbale the Rx interrupt。
Bit4	ACKLEN	0	When working in slave mode, ACKLEN means the duration of CKACK=0 when data receiving error happened. 0, 1byte；1, 2bytes。
Bit3	AUTOSD	0	When working in Master mode, Auto re-transmiting mechnaims will be enabled if AUTOSD=1. When CKACK is low, the UART will resend the data automatically.
Bit2	AUTORC	0	When working in slave mode, Auto re-receving mechanism will be enabled if AUTORC=1. When error data is received, CKACK will be set as low acked to the transmitter to request the data be resend.
Bit1	CHKP	0	0, Even Parity Check；1, Odd Parity Check。
bit0	ENABLE	0	ENABLE=0，Stay in IDLE state always. WhenENABLE bit of CFGA =1，P10.0 is used as EUART1data transmitter and receiver； When ENABLE bit of CFGB =1，P10.1is used as EUART2data transmitter，P10.2is used as EUART2data recevier。

	0x2A05/0x2B05, R/W, EUART1/2 Configuration Register, CFGA/CFGB	
Bit	Default	Description
In ISO/IEC 7816-3protocol，the resend tries should not be greated than 3，For example, if the transmitting failed twice，the resend mechanism will be stopped.User could use the software implementation to fulfill this requirement.		

16. Watchdog Timer (WDT)

In the V98XX the embedded 16-bit watchdog timer (WDT) counting pulses of the 32kHz RC clock. When the program gets stuck somewhere, the timer overflows and reset the system to cause the program restart from the beginning.

16.1. Clock for WDT

In the V98XX, CLK4, sourced by the 32kHz RC clock, provides clock pulse for the WDT. RC clock cannot be disabled until the chip is powered off, but CLK4 is enabled or disabled together with CLK1. When CLK4 (together with CLK1) is disabled, which means the system enters Sleep or Deep Sleep state, the WDT stops running. When the system is woken up by IO/RTC wakeup event or power recovery, the WDT restarts counting from zero.

Table 16-1 Enable/Disable CLK4

SFR 0x80, R/W, Clock Switchover Control Register, SysCtrl SFR		
Bit	Default	Description
Bit2 SLEEP1 Bit1 SLEEP0	0	When the bit PWRUP is read out as 0, write 0 to the bit MCUFRQ, and then: – set SLEEP1 and SLEEP0 to 0b11 or 0b01 to stop CLK1 (together with CLK4) and force the system entering the Sleep state. – set SLEEP1 and SLEEP0 to 0b10 to stop CLK1 (together with CLK4) and force the system entering the Deep Sleep state.

16.2. Clearing WDT

When IO/RTC wakeup event, power recovery event, POR/BOR or RSTn pin reset occurs, the WDT is reset, and its counts are cleared. When the reset signal is released, the WDT starts counting from zero again.

Users can write a program to clear the WDT counts to prevent the WDT from resetting the system when its counts overflow: write 0xA5 to the register WDTEN (SFR 0xCE) and then 0x5A to the register WDTCLR (SFR 0xCF) continuously to clear the WDT counts. Immediately the WDT is cleared, it will restart counting pulses from zero.

SFR 0xCE, W, WDTEN SFR	0xA5
SFR 0xCF, W, WDTCLR SFR	0x5A

16.3. WDT Overflow Reset

Initially, the WDT starts counting pulses from 0. If the counts are not cleared when the WDT counts to

(3×2^{14}), that is about 1.5s, the WDT overflows, a reset pulse of 8 RC clock periods ($8/f_{RC}$) width is output, and the system is reset to default state. After the reset, the WDT starts counting from (-2^{14}), and then, if the WDT is still not cleared, the WDT will overflow again when it counts to (3×2^{14}), that is about 2s.

When the WDT overflow reset occurs, the flag bit POR (bit5 of Systate, SFR 0xA1) is set to 1. When other reset events, not POR/BOR or RSTn pin reset, occurs, this bit will be cleared. In debugging mode, this reset event is masked.

A WDT overflow event can reset all circuits except the RTC calibration registers, RTC timing registers, IRAM and XRAM.

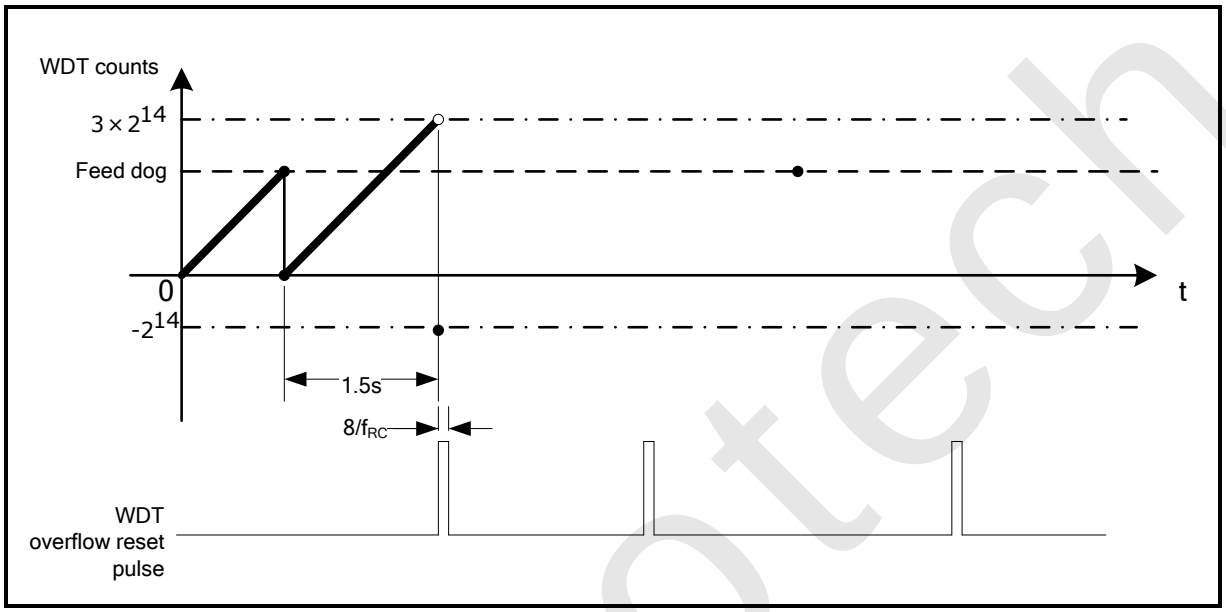


Figure 16-1 WDT Overflow Reset

17. Real-Time Clock (RTC)

In the V98XX, the RTC has features as follows:

- counting the pulses of the 32.768kHz OSC clock;
- calibrating crystal frequency over temperature variation;
- calibrated pulse output every exact one second;
- timing error less than 5ppm over operating temperature range;
- providing real-time clock and calendar, and adjusting the date for leap year automatically.

In the RTC, the registers for calibration and timing cannot be reset by any reset event; and the other registers will be reset to their default states when POR/BOR, RSTn pin reset or WDT overflow event occurs.

In Sleep state, the RTC keeps running and can be configured to wake up the system at an programmable interval of 1 day, 1 hour, 1 minute, 1~64 seconds, 500ms, 250ms, 125ms or 62.5ms. The wakeup signal will hold 8 OSC clock periods.

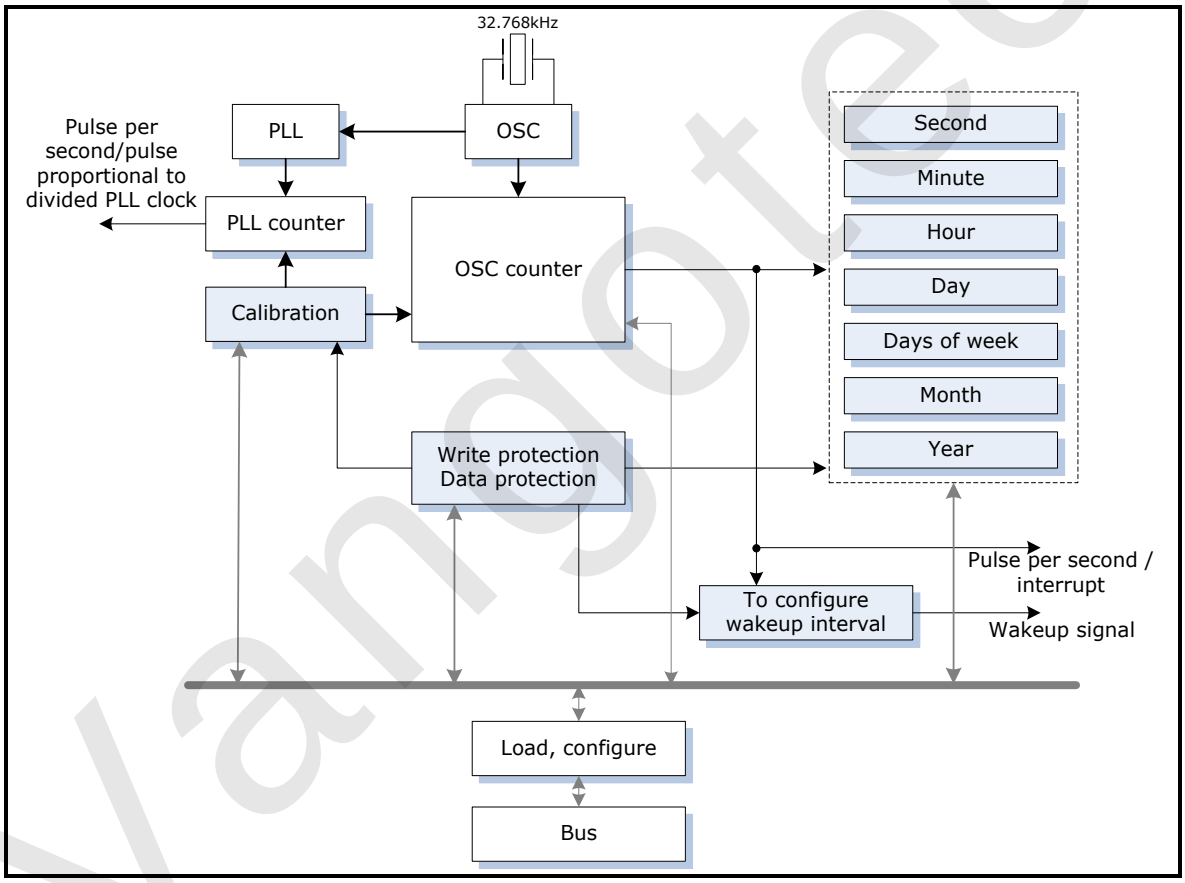


Figure 17-1 Architecture of RTC

17.1. Reading and Writing of RTC Registers

17.1.1. Writing of RTC

In the V98XX, the registers INTRTC (SFR 0x96), RTC calibration registers and RTC timing registers are

protected from writing.

The MCU must write of these registers following exact steps as:

1. writing 0x96 to the register RTCPEN to enable writing of the register RTCPWD;
2. writing 0x57 to the register RTCPWD to enable writing of INTRTC (SFR 0x96), RTC calibration registers and RTC timing registers;
3. After 5 OSC clock cycles, configuring the registers INTRTC (SFR 0x96), RTC calibration registers and RTC timing registers;
4. After 5 OSC clock cycles, writing 0x96 to the register RTCPEN to enable writing of the register RTCPWD;
5. Writing 0x56 to the register RTCPWD to disable writing of the registers INTRTC (SFR 0x96), RTC calibration registers and RTC timing registers. 5 OSC clock cycles later, the contents of the registers are activated. A second write operation can be done to these registers only when the last configuration is completed.

17.1.2. Reading of RTC

To read the timing registers, the MCU must read the register RDRTC (SFR 0xDA) firstly, waits no less than 5 OSC clock cycles till the contents of the RTC timing registers are latched, and then read the timing registers for the time information.

But the MCU can read the calibration registers directly.

17.2. Timing

When the chip is powered on, the RTC starts to run, and it keeps on running until the system is powered off.

If the timing registers are not configured, the RTC runs from a random time; otherwise, the RTC runs from the preset time.

17.3. RTC Interrupts

In the V98XX, the RTC can trigger two interrupt events if they are enabled: illegal data interrupt and pulse output interrupt per second.

17.3.1. RTC Illegal Data Interrupt

When the RTC illegal data interrupt is enabled (EA=1, EIE.2=1 and ExInt4IE.0=1), an illegal data interrupt will be triggered when:

- The MCU writes of the registers INTRTC (SFR 0x96), RTC calibration registers and RTC timing registers when they are still being protected from writing;
- The MCU writes the contents in an illegal format into the registers INTRTC (SFR 0x96), RTC calibration registers and RTC timing registers when the writing operation is enabled;

The contents of the timing registers are in binary-coded decimal (BCD) format, so 0xF is not considered as an illegal data.

In both circumstances, the RTC timing registers will hold the contents.

- Data error caused by the system error occurs during the operation. In this circumstance, the MCU must configure all RTC timing registers **consecutively** immediately the writing operation is enabled, and then disable the writing operation to activate the correction.

17.3.2. Pulse Output Interrupt per Second

When EA=1, EIE.1=1 and ExInt3IE.6=1, the pulse output interrupt per second is enabled, and the RTC will output pulses of 1 second width to the MCU to trigger interrupts.

17.4. PLL Counter

There is a 24-bit PLL counter in the V98XX. It can work as a PLL clock divider or a counter, which is determined by the register PLLCNTST (SFR 0xDE).

When the register PLLCNTST (SFR 0xDE) is set to 0x00, the PLL counter works as a divider. In this mode, the PLL counter counts from 0 and increments by 1 every OSC clock cycle. When it counts to the pre-set value of the PLL clock divider registers, this counter will be cleared, output pulses at a frequency proportional to the divided PLL clock frequency from Pin31/Pin30/Pin43, and then the counter will start recounting. The frequency of the pulse can be calculated as follows:

$$f_{DIV} = \frac{f_{MCU}}{2 \times (TH + 1)} \qquad \text{Equation 17-1}$$

where,

- f_{DIV}, the frequency of the pulse, Hz;
- f_{MCU}, the MCU clock frequency (Hz), which has a relationship with the OSC clock frequency (f_{OSC})as follows:

$$f_{MCU} = K \times f_{OSC} \qquad \text{Equation 17-2}$$

where, *K* is a coefficient, equal to 100/200/400; when the theoretical f_{MCU} is 13.1072MHz, *K* is 400.

- TH, the preset value of the PLL divider registers (DIVTHH/DIVTHM/DIVTHL). In the default state, the value of *TH* is 0, so the MCU clock frequency is divided by 2. The MCU clock frequency can be divided by up to 2^{25}.

When the register PLLCNTST (SFR 0xDE) is configured to 0x01, the PLL counter works as a counter. When the first low-to-high transition of a reference pulse of exact 1 second width input on Pin89 (SDSP) is detected, which will configure the register to 0x02 automatically, the counter starts counting from zero. And then, when the second low-to-high transition of the reference pulse input is detected, the register PLLCNTST (SFR 0xDE) is configured to 0x03 automatically, the PLL counter stops running, and the current counts is transferred to the PLL clock divider registers to calculate the actual frequency of the pulse.

17.5. Calibrating RTC

In the V98XX, the MCU can use the PLL counter or the internal counter of the RTC to calibrate the RTC.

17.5.1. Calibrating Pulse Frequency of PLL Counter

The internal counter of the RTC counts the clock pulse provided by the OSC clock. From the 1st to 29th second, the RTC outputs pulses every 32768 counts; in the 30th second, the RTC outputs a pulse when the counts are [32768-(C-1)] (C is the value of the calibration register in decimal) to average the width of pulses in 30 seconds to be 1 second each. So the RTC cannot calibrate timing error in real time by itself. But when the PLLCNTST is used to output a pulse of exact 1 second width (PPS) every second, the error of the pulse width can be corrected in real time. Because both RTC and PLLCNTST are pulsed by the OSC clock, so users can calibrate the RTC timing via correcting the PPS width error.

The relationship of the value of *C* (in decimal) and actual OSC clock frequency (f_{OSC}) is as follows:

$$C-1=30\times(32768-f_{OSC}) \qquad \text{Equation 17-3}$$

According to Equation 17-1 and Equation 17-2, to calibrate the pulse frequency of the PLL counter (f_{DIV}) to be 1Hz, the nominal *TH* and actual *TH'* has a relationship as follows:

$$TH-TH'=\Delta TH=\frac{K}{2}\times(32768-f_{OSC})=200\times(32768-f_{OSC}) \qquad \text{Equation 17-4}$$

where, *TH* is the value for nominal f_{OSC}, namely 32768Hz; *TH'* is the value for actual f_{OSC}.

According to Equation 17-3 and Equation 17-4, a relationship between *ΔTH* and *C* is obtained:

$$\frac{\Delta TH}{C-1}=\frac{200}{30} \qquad \text{Equation 17-5}$$

According to Equation 17-5, users can calibrate the RTC timing via correcting the PPS width error.

17.5.2. Calibrating Divided Pulse Frequency of PLL Counter

When Pin89 is used to input a reference pulse of exact 1 second width, the PLL counter is used to capture and measure the width of this input signal, which can be used to calibrate the RTC. The calibration steps are as follows:

1. The MCU writes 0x01 to the register PLLCNTST (SFR 0xDE) to clear the PLL counter, and the PLL counter works as a counter;
2. When the first high-to-low transition of the reference pulse of exact 1 second width is detected, which will configure the register to 0x02 automatically, the counter starts counting from zero.
3. When the second low-to-high transition of the reference pulse is detected, the register PLLCNTST (SFR 0xDE) is configured to 0x03 automatically, the PLL counter stops running, and the current counts are transferred to the PLL clock divider registers as the value of *TH* to generate pulses of exact 1 second width to calibrate the crystal frequency using the following equation:

$$f_{OSC} = \frac{2}{K} \times (TH + 1)$$ Equation 17-6

When the theoretical frequency of the MCU (f_{MCU}) is 13.1072MHz, the relationship of *C*, the value to be written to the calibration register, and *TH* in the preceding equation is as follows:

$$C - 1 = \frac{30}{200} \times (TH + 1) - 32768 \times 30$$ Equation 17-7

17.5.3. Crystal Frequency-Temperature Curve

The crystal frequency is affected by the ambient temperature. In the V98XX there is a temperature measurement circuit. Users can measure the crystal frequency in different ambient temperatures and calculate the values to be written to the calibration register (C) according to the following steps to calibrate the crystal frequency to be exact 32768Hz at different temperatures, and then tabulate them according to the relationship for table look-at:

4. Set the reference crystal frequencies in different ambient temperature, such as 32768Hz;
5. Write 0x01 to the calibration registers and measure the actual crystal frequency (f_{OSC}) using a frequency meter via Pin96 in different ambient temperature, and calculate the value of *C′* (*C′=C-1*) using the following equation:

$$C' = \frac{f_{OSC} - 32768}{32768} \times 1000000 / (\frac{1}{32768} \times \frac{1}{30} \times 1000000) = 30 \times (f_{OSC} - 32768)$$ Equation 17-8

Where, $\frac{1}{32768} \times \frac{1}{30} \times 1000000$, equal to 1.02ppm, represents the calibration accuracy of the RTC of average one second in the 30 seconds; and $\frac{f_{OSC} - 32768}{32768} \times 1000000$ represents the quantity of the crystal frequency to be calibrated in unit of ppm.

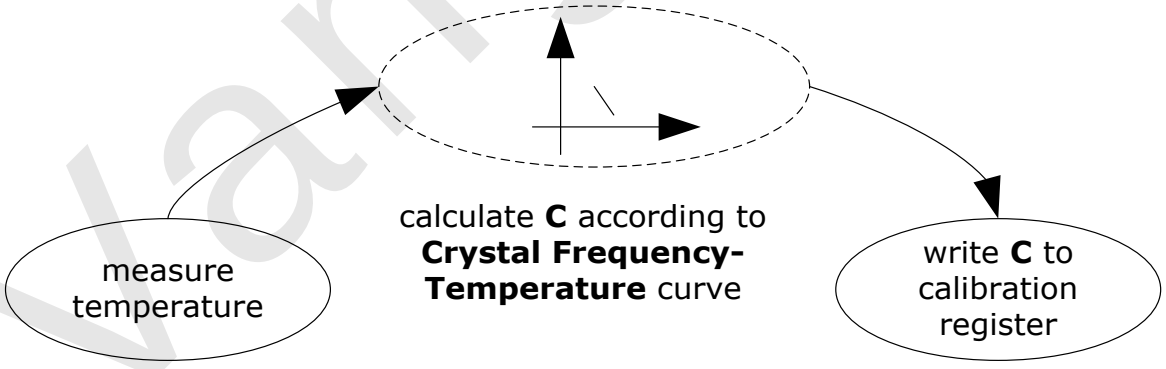


Figure 17-2 Schematics of Calibrating Crystal Frequency over Temperature Variation

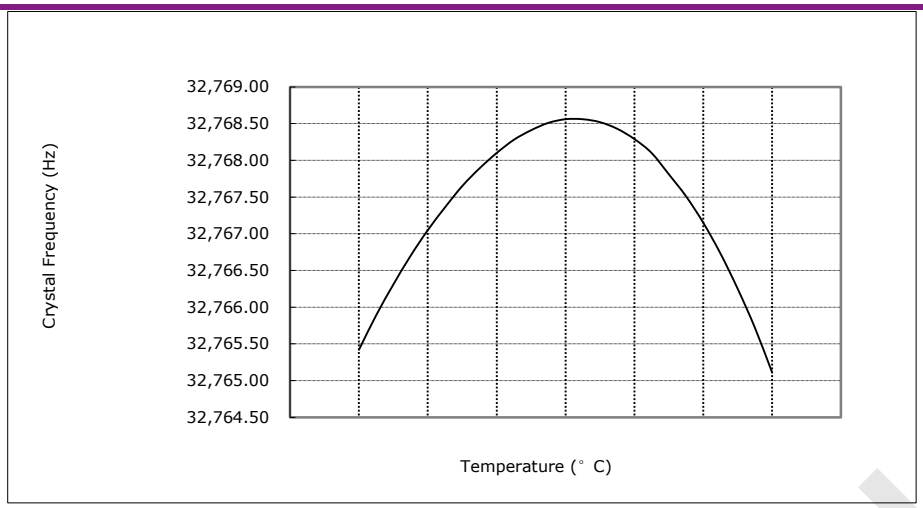


Figure 17-3 Crystal Frequency-Temperature Curve

17.6. Registers

In the RTC, the registers for calibration and timing cannot be reset by any reset event; and the other registers will be reset when POR/BOR, RSTn pin reset or WDT overflow event occurs.

Table 17-1 RTC Password Enable Register (RTCPEN, SFR 0x90)

SFR 0x90, RTC Password Enable Register, RTCPEN			
Bit	Default	R/W	Description
bit[7:0]	0	W	Only 0x96 is the valid value. Only when this register is configured to 0x96 can the register RTCPWD (SFR 0x97) be configured validly. The write operation of both registers must be consecutive without interruption.

Table 17-2 RTC Password Register (RTCPWD, SFR 0x97)

SFR 0x97, RTC Password Register, RTCPWD				
Bit		Default	R/W	Description
bit[7:1]		0	W	Bit[7:1] are writable only, but bit0 is writable and readable. Only 0x57 and 0x56 are valid for this register.
bit0	WE	0	R/W	Write 0x57 to this register to enable write operation on the registers INTRTC (SFR 0x96), RTC calibration registers and RTC timing registers. Write 0x56 to this register to disable the write operation.

Table 17-3 RTC Wakeup Interval Register (INTRTC, SFR 0x96)

SFR 0x96, RTC Wakeup Interval Register, INTRTC				
Bit		Default	R/W	Description
bit[7:3]		0	R/W	

SFR 0x96, RTC Wakeup Interval Register, INTRTC				
Bit		Default	R/W	Description
bit[2:0]	RTC<2:0>	0	R/W	000: 1 second; 001: 1 minute; 010: 1 hour; 011: 1 day; 100: 500ms; 101: 250ms; 110: 125ms; 111: 62.5ms.
Configure this register for the interval at which the RTC will wake up the system from Sleep state. The wakeup signal holds 8 OSC clock periods.				

Table 17-4 RTC Seconds Wake-up Interval Configuration Register (SECINT, SFR 0xDF)

SFR 0xDF, R/W, RTC Seconds Wake-up Interval Configuration Register, SECINT			
Bit	R/W	Default	Description
Bit7	R/W	0	Reserved
Bit6	R/W	0	It is mandatory to set register INTRTC (SFR 0x96) to 0x07, and then set this bit to 1 to enable writing of bit[5:0] of this register.
Bit[5:0]	R/W	0	To set interval in unit of second for RTC to wake up the system from Sleep. The actual wakeup interval is equal to (bit[5:0]+1) seconds, of which bit[5:0] can be set to 1~63 (decimal). Setting these bits to 0 (decimal) forces the interval to be 62.5ms.

Table 17-5 Flag Bit of RTC Wakeup Event

SFR 0xA1, R, System State Register, Systate		
Bit	Default	Description
Bit2 RTC/CF	0	When this bit is read out as 1, but bit CFWK (bit3 of IOWKDET, SFR 0xAF) is cleared, it indicates the system was woken up from Sleep by RTC wakeup event. If both this bit and bit CFWK are set to 1s, it indicates the system was woken up from Sleep by CF pulse wakeup event.

Table 17-6 RTC Calibration Registers (RTCCH/RTCCL, SFR 0x94/0x95)

Register	Bit	R/W	Description
SFR 0x94 RTCCH	bit[7:6]	R/W	Reserved.
	bit[5:0] C<13:8>	R/W	To set a value (C) to calibrate the crystal frequency. The register is in the format of 2'-complement. The internal counter of the RTC counts the clock pulse provided by the OSC clock. From the 1st to 29th second, the RTC outputs a pulse every 32768 counts; in the 30th second, the RTC outputs a pulse when the counts is up to [32768-(C-1)) to average each pulse width in the 30 seconds to be 1s. The average calibration resolution is 1.02ppm, and the adjustment range is over ±8332.3ppm (±12 min/day).
SFR 0x95 RTCCL	bit[7:0] C<7:0>	R/W	

Table 17-7 RTC Data Reading Enable Register (RDRTC, SFR 0xDA)

SFR 0xDA, RTC Data Reading Enable Register, RDRTC			
Bit	Default	R/W	Description
bit[7:0]	0	R	The MCU must read this register to enable read operation on the RTC timing registers. This register is read out as 0x00.

Table 17-8 PLL Clock Divider Registers (DIVTHH/DIVTHM/DIVTHL, SFR 0xDB/0xDC/0xDD)

Register	Bit		Default	R/W	Description
SFR 0xDB, DIVTHH	bit[7:0]	DIV<23:16>	0	R/W	High byte of the PLL clock divider.
SFR 0xDC, DIVTHM	bit[7:0]	DIV<15:8>	0	R/W	Middle byte of the PLL clock divider.
SFR 0xDD, DIVTHL	bit[7:0]	DIV<7:0>	0	R/W	Low byte of the PLL clock divider.

Table 17-9 PLL Counter State Register (PLLCNTST, SFR 0xDE)

SFR 0xDE, PLL Counter State Register, PLLCNTST, R/W			
Bit	Default	R/W	Description
bit[7:2]	0	R/W	When this register is cleared to 0x00, the PLL counter works as a divider. When the PLL counter increments from 0 to the value of the PLL clock divider registers, this counter is cleared, outputs a pulse at a frequency proportional to the divided PLL clock frequency, and then starts recounting. When this register is set to 0x01, the PLL counter works as a counter. When the first low-to-high transition of the reference pulse of exact 1 second width input on Pin89 (SDSP) is detected, which will set this register to 0x02 automatically, the counter starts counting from zero. And then, when the second low-to-high transition of the reference pulse input is detected, the register is configured to 0x03 automatically, the PLL counter stops running, and the current counts is transferred to the PLL clock divider registers to calculate the actual frequency of the pulse per second.
bit[1:0] STT<1:0>	0	R/W	

The time and calendar information is obtained by reading the appropriate register bytes. The contents of the timing registers, except the register for day of week configuration, are in binary-coded decimal (BCD) format, of which bit7~bit4 represents the tens digit of the time and calendar, and bit3~bit0 represents the units digit of the time and calendar; for example, 0b1000011 in the register RTCSC represents 43 seconds. The RTC can provide second, hour, day, week, month and year information. As such, both RTCSC (seconds) and RTCMiC (minutes) range 0~59, RTCHC (hour) ranges 00~24, RTCDC (day) ranges 1~31, RTCMoC (month) ranges 1~12 and RTCYC (year) ranges 0~99.

Table 17-10 RTC Timing Registers

Register		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SFR 0x9A	RTCSC, to set the second information, 0~59.	-	S40	S20	S10	S8	S4	S2	S1
SFR 0x9B	RTCMiC, to set the minute information, 0~59.	-	M40	M20	M10	M8	M4	M2	M1

Register		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SFR 0x9C	RTCHC, to set the hour information, 0~23.	-	-	H20	H10	H8	H4	H2	H1
SFR 0x9D	RTCDC, to set the day information, 1~31.	-	-	D20	D10	D8	D4	D2	D1
SFR 0x9E	RTCWC, to set the day of week information.	-	-	-	-	-	W4	W2	W1
SFR 0x9F	RTCMoC, to set the month information, 1~12.	-	-	-	Mo10	Mo8	Mo4	Mo2	Mo1
SFR 0x93	RTCYC, to set the year information, 00~99.	Y80	Y40	Y20	Y10	Y8	Y4	Y2	Y1
Default		X	X	X	X	X	X	X	X

Users must set the day of week information for one date; for example, set the date 1st Jan. 2010 to be Friday, and the RTC will determine the date 2nd, Jan., 2010 to be Saturday automatically. 0b000: Sunday; 0b001: Monday; 0b010: Tuesday; 0b011: Wednesday; 0b100: Thursday; 0b101: Friday; 0b110: Saturday; 0b111: Invalid data.

For the year information, only the tens and units digits of the year need to be configured in the register RTCYC; for example, 0b00010000 represents the year 2010.

Users should set the information of year, month, day, hour, minute, second, and week according to certain sequence at one time. It will fail if set up separately.

18. Registers

18.1. Analog Control Registers

In the V98XX, analog control registers are located at addresses 0x2858~0x2868. The registers are readable and writable. When POR/BOR, RSTn pin reset or WDT overflow reset occurs, the analog control registers will be reset to their default states. In this section, the default values are in decimal form unless otherwise noted.

The register located at address 0x285F must be configured to its default values for proper operation.

Users can read of bytes located at addresses 0x300C~0x3059 to obtain the recommended configuration of the analog registers, and write them to the analog registers.

Table 18-1 ADC Control Register 0 (CtrlADC0, 0x2858)

0x2858, R/W, ADC Control Register 0, CtrlADC0			
Bit		Default	Description
Bit7	Reserved	0	This bit must hold its default value for proper operation.
Bit6	ADCGU	0	To set analog PGA gain for voltage input to Voltage Channel (U) ADC. This bit must hold its default value for proper operation（×1 倍）. 0: ×1; 1: ×2.
Bit[5:3]	ADCGB<2:0>	0	To set analog PGA gain for current input to Current Channel B (IB) ADC. 000: ×1; 001: ×4; 010: ×8; 011: ×16; 100/101/110/111: ×32. To match the output signal from the sensor to the measurement scale of the ADC, the default value should not be used.
Bit[2:0]	ADCGA<2:0>	0	To set analog PGA gain for current input to Current Channel A (IA) ADC. 000: ×1; 001: ×4; 010: ×8; 011: ×16; 100/101/110/111: ×32. To match the output signal from the sensor to the measurement scale of the ADC, the default value should not be used.

Table 18-2 ADC Control Register 1 (CtrlADC1, 0x2859)

0x2859, R/W, ADC Control Register 1, CtrlADC1			
Bit		Default	Description
Bit[7:4]	Reserved	0	These bits must hold their default values for proper operation.
bit[3:2]	ADIT2<1:0>	0	To adjust the 2nd order bias current of the ADCs. 00: ×1 (recommended); 01: ×1.33; 10: ×2; 11: ×2.67.

0x2859, R/W, ADC Control Register 1, CtrlADC1			
Bit		Default	Description
bit[1:0]	ADIT1<1:0>	0	To adjust the 1st order bias current of the ADCs. 00: ×1 (recommended); 01: ×1.33; 10: ×2; 11: ×2.67.

Table 18-3 ADC Control Register 2 (CtrlADC2, 0x285A)

0x285A, R/W, ADC Control Register 2, CtrlADC2			
Bit		Default	Description
bit[7:5]	Reserved	0	These bits must hold their default values for proper operation.
bit4	DITAMP	0	To adjust the bias current of the amplifier of voltage channel. It is recommended to hold its default value for proper operation. 0: ×1; 1: ×0.67.
bit3	ADRSTM	0	To reset the integrator in the modulator in the ADC of Channel M. When some errors occur to the data output from the ADC, set this bit to 1 to reset the integrator.
bit2	ADRSTU	0	To reset the integrator in the modulator in the ADC of Channel U. When some errors occur to the data output from the ADC, set this bit to 1 to reset the integrator.
bit1	ADRSTB	0	To reset the integrator in the modulator in the ADC of Channel IB. When some errors occur to the data output from the ADC, set this bit to 1 to reset the integrator.
bit0	ADRSTA	0	To reset the integrator in the modulator in the ADC of Channel IA. When some errors occur to the data output from the ADC, set this bit to 1 to reset the integrator.

Table 18-4 ADC Control Register 3 (CtrlADC3, 0x285B)

0x285B, R/W, ADC Control Register 3, CtrlADC3			
Bit		Default	Description
bit[7:5]	Reserved	0	These bits must hold their default values for proper operation.
bit4	ADQIT	0	Set this bit to 1 to increment the bias current in the comparator by 50%. By default this function is disabled.
bit3	SHORTV2	0	Set this bit to 1 to short the voltage channel ADC 2internally. By default this function is disabled.
bit2	Reserved	0	This bit must hold its default value for proper operation.
bit1	SHORTI2	0	Set this bit to 1 to short the current channel ADCs2internally. By default this function is disabled.

0x285B, R/W, ADC Control Register 3, CtrlADC3			
Bit		Default	Description
bit0	Reserved	0	This bit must hold its default value for proper operation.

Table 18-5 Battery Discharge Control Register (CtrlBAT, 0x285C)

0x285C, R/W, Battery Discharge Control Register, CtrlBAT			
Bit		Default	Description
bit[7:4]	Reserved	0	These bits must hold their default values for proper operation.
bit3	LCDBMOD	0	When the LCD driver works in 1/8 duty mode, set this bit to select the bias ratio. 0: 1/3 Bias; 1: 1/4 Bias. When the LCD driver works in 1/4 or 1/6 duty mode, 1/3 Bias ratio is used whatever this bit is set.
bit[2:1]	IITU<1:0>	0	To adjust the bias current of the amplifier of the voltage channel ADC. 00: 0%; 01: -33%; 11:+33%; 10: 100%.
bit0	BATDISC	0	To enable discharging the battery. 1: enable; 0: disable.

Table 18-6 ADC Control Register 4 (CtrlADC4, 0x285D)

0x285D, R/W, ADC Control Register 4, CtrlADC4			
Bit		Default	Description
Bit[7:6]	Reserved	0	These bits must hold their default values for proper operation.
bit5	IAMPITB	0	Set this bit to 1 to increase operating current to the Channel IB ADC by 50%.
bit4	IAMPITA	0	Set this bit to 1 to increase operating current to the Channel IA ADC by 50%.
Bit[3:0]	Reserved	0	These bits must hold their default values for proper operation.

Table 18-7 LCD Driver Voltage Control Register (CtrlLCDV, 0x285E)

0x285E, R/W, LCD Driver Voltage Control Register, CtrlLCDV			
Bit		Default	Description
Bit7	DCENN		
Bit[6:3]	Reserved	0	These bits must hold their default values for proper operation.
bit2	VLCD	0	To adjust the LCD waveform voltage. 0: 3.3V; 1: 3.0V.
bit[1:0]	Reserved	0	These bits must hold their default values for proper operation.

Table 18-8 Crystal Control Register 1 (CtrlCry1, 0x2860)

0x2860, R/W, Crystal Control Register 1, CtrlCry1			
Bit		Default	Description
Bit[7:5]	Reserved	0	These bits must hold their default values for proper operation.
Bit4	CSEL	0	The fixed capacitance in the crystal oscillator circuit is 12.5pF. Set this bit to 1 to decrease the capacitance by 2.35pF.
Bit3	Reserved	0	These bits must hold their default values for proper operation.
Bit[2:0]	XTRSEL<2:0>	0	To adjust the resistance of the resistors in the internal crystal oscillator circuit. When the RTC is used, these bits must be set to 0b011, and the oscillation monitoring circuit must be enabled. Set bit XTRSEL<2> to 1 to increment the resistance to P end by 400kΩ. XTRSEL<1:0> to adjust the resistance to N end: 00/01: hold the resistance to N end. 10: increment by 128kΩ. 11: increment by 64kΩ.

Table 18-9 Crystal Control Register 2 (CtrlCry2, 0x2861)

0x2861, R/W, Crystal Control Register 2, CtrlCry2			
Bit		Default	Description
Bit7	REFLKEN	0	Set this bit to 1 to enable current leakage detection on BandGap circuit. When this bit is set to 1, an interrupt will be triggered when reference voltage is lowered by more than 3%.
Bit6	Reserved	0	This bit must hold its default value for proper operation. By default this function is disabled.
bit5	XRESETEN	0	Set this bit to 1 to enable the oscillation monitor.
Bit4	CMPIT	0	To select the bias current input to the comparator CB. 0: 20nA; 1: 200nA.
bit[3:2]	CMPSSELB<1:0>	0	To select the analog input to the comparator CB. 00: M2 for positive input; REF_LP for negative input; 01: M1 for positive input; REF_LP for negative input; 10/11: M2 for positive input; M1 for negative input.
Bit[1:0]	Reserved	0	These bits must hold their default values for proper operation.

Table 18-10 BandGap Control Register (CtrlBGP, 0x2862)

0x2862, R/W, BandGap Control Register, CtrlBGP		
Bit	Default	Description

0x2862, R/W, BandGap Control Register, CtrlBGP			
Bit		Default	Description
bit[7:6]	CURRIT<1:0>	0	To adjust the global bias current of the ADC. 00: -33%; 01: 1; 10: -75%; 11: -66%. It is recommended to set these bits to 0b00 for full operation, and to 0b11 for metering energy at a lower frequency.
Bit[5:4]	RESTL<1:0>	0	To roughly adjust the temperature coefficient of the BandGap circuit. 00: 0ppm; 01: -70ppm; 10: +140ppm; 11: +70ppm.
Bit[3:1]	REST<2:0>	0	To finely adjust the temperature coefficient of the BandGap circuit. The recommended configuration for 0b001, but the user should correct according to actual measured temperature coefficient of the whole table. 000: 0ppm; 001: +10ppm; 010: +20ppm; 011: +30ppm; 100: -40ppm; 101: -30ppm; 110: -20ppm; 111: -10ppm.
bit0	BGPCHOPN	0	By default the chopper in the BandGap circuit is enabled to remove the DC offset. Set this bit to '0' to disable this function In order to improve the temperature performance.

Table 18-11 ADC Control Register 5 (CtrlADC5, 0x2863)

0x2863, R/W, ADC Control Register 5, CtrlADC5			
Bit		Default	Description
Bit[7]	Reserved	0	These bits must hold value1for proper operation.
Bit[6]	Reserved	0	These bits must hold their default values for proper operation.
Bit5	GDE4	0	To set analog PGA gain for signal input to various Measurement Channel (M) ADC. 0: ×1; 1: ×1/4.
bit4	RESDIV	0	To set bit1 and the division coefficient1/4 of the resistor divider network in M Channel. The circuit is turned off by default
Bit3	Reserved	0	This bit must hold its default value for proper operation.

0x2863, R/W, ADC Control Register 5, CtrlADC5			
Bit		Default	Description
Bit[2:0]	MEAS<2:0>	0	To select the analog input to be measured in Channel M. 000: ground; 001: temperature; 010: battery voltage or other external DC voltage via pin BAT. 011: reserved; 100: external DC voltage via pin UM; 101: external DC voltage via pin M0; 110: external DC voltage via pin M1; 111: external DC voltage via pin M2.
Note: When the pins M0, M1 and M2 are used for analog input for Channel M, bit[7:5] of the register SegCtrl4 (0x2C23) must be cleared to disable the SEG output on the pins.			

Table 18-12 ADC Control Register 6 (CtrlADC6, 0x2864)

0x2864, R/W, ADC Control Register 6, CtrlADC6			
Bit		Default	Description
bit[7:6]	Reserved	0	These bits must hold their default values for proper operation.
bit5	CMPPDNB	0	To enable the comparator CB. 0: disable; 1: enable.
bit4	Reserved	0	This bit must hold its default value for proper operation.
bit3	ADCMPDN	0	To enable Channel M ADC. 0: disable; 1: enable.
bit2	ADCUPDN	0	To enable Channel U ADC. 0: disable. 1: enable.
bit1	ADCBPDN	0	To enable Channel IB ADC. 0: disable; 1: enable.
bit0	ADCAPDN	0	To enable Channel IA ADC. 0: disable; 1: enable.

Table 18-13 Channel M Control Register (CtrlM, 0x2865)

0x2865, R/W, Channel M Control Register, CtrlM			
Bit		Default	Description
bit[7:1]	Reserved	0	These bits must hold their default values for proper operation.
bit0	MADCHOPN	0	the DC offset of the input signal into the M Channel By default this circuit is enabled. When M Channel is used to measure temperature, it is recommended to set this bit to 1 to disable this function to improve the measurement accuracy.

Table 18-14 LDO Control Register (CtrlLDO, 0x2866)

0x2866, R/W, LDO Control Register, CtrlLDO			
Bit		Default	Description
Bit7	PDDET	0	Set this bit to 1 to disable the internal power detection circuit. By default this circuit is enabled. When the chip is 3.3V powered, users must set this bit to 1 to disable the power detection circuit, to prevent current leakage of the battery when a battery is connected to the device. When the chip is 5V powered, this bit must hold its default value.
Bit6	LDO3IT	0	Set this bit to 1 to increase bias current of LDO33 by 100%.
Bit[5:3]	LDO3SEL	0	To adjust output voltage of LDO33. 000: 3.3V; 001: 3.2V; 010/100/101: 3.5V; 011: 3.4V; 110: 3.1V; 111: 3.0V.
Bit[2:0]	LDOV2SEL<2:0>	0	To adjust output voltage of digital power circuit. 000: +0V; 001: -0.1V; 010: +0.2V; 011: +0.1V; 100: -0.4V; 101: -0.5V; 110: -0.2V; 111: -0.3V.

Table 18-15 Clock Control Register (CtrlCLK, 0x2867)

0x2867, R/W, Clock Control Register, CtrlCLK			
Bit		Default	Description
bit7	PLLPDN	0	To enable the PLL circuit. 0: disable; 1: enable. Enable the BandGap circuit, and then enable the PLL circuit.
bit6	BGPPDN	0	To enable the BandGap circuit. 0: disable; 1: enable. Enable the BandGap circuit, and then enable the PLL circuit.
bit[5:4]	ADCLKSEL<1:0>	0	To configure the sampling frequency of the oversampling ADCs (ADCCLK). Base: 204.8kHz. 00: ×1; 01: ×2; 10: ×4.
bit[3:2]	MEACLKSEL<1:0>	0	To configure the clock frequency for the energy metering architecture (MTCLK). Base: 819.2kHz. 00: ×1; 01: ×2; 10: ×4.
bit[1:0]	MCUCLKSEL<1:0>	0	To adjust the clock frequency for the MCU (MCUCLK). Base: 819.2kHz. 00: ×1; 01: ×2; 10: ×4; 11: ×8.

Table 18-16 PLL Control Register (CtrlPLL, 0x2868)

0x2868, R/W, PLL Control Register, CtrlPLL

Bit		Default	Description
bit7	MCU26M	0	When the bit MCU13M is set to 1, set this bit to 1 to double MCUCLK frequency further.
bit6	MCU13M	0	Set this bit to 1 to double MCUCLK frequency.
bit5	PLLSEL	0	To apply the chip to 50Hz or 60Hz power grid. 0: 50Hz; 1: 60Hz.
bit[4:0]	Reserved	0	These bits must hold their default values for proper operation.

Table 18-17 Analog Circuits State Register (ANState, 0x286B)

0x286B, R, Analog Circuits State Register, ANState			
Bit		Default	Description
bit7	OSC	0	To indicate the state of the OSC clock. 0: the crystal is working. 1: the crystal stops running, and all the circuits, including PLL circuit, sourced by the OSC clock now is being sourced by the internal RC clock.
Bit6	Reserved	-	
bit5	COMPB	0	To indicate the output of the comparator CB. 1: the positive input is higher than the negative input; 0: the negative input is higher than the positive input.
bit[4:2]	Reserved	5	It is read out as 0x5.
bit[1:0]	Reserved	-	

18.2. Metering Control Registers

When POR/BOR, RSTn pin reset or WDT overflow reset occurs, all metering control registers are reset to their default states.

All the default values in this section are in decimal form if not specifically noted.

Table 18-18 PM Control Register 1 (PMCtrl1, 0x2878)

0x2878, R/W, PM Control Register 1, PMCtrl1			
Bit		Default	Description
bit7	PVA	0	Only for test. To disable the power/RMS calculation circuits to access to the energy metering data registers. 0: enable; 1: disable.

0x2878, R/W, PM Control Register 1, PMCtrl1			
Bit		Default	Description
bit6	PHCEN	0	To enable phase compensation. 0: disable; 1: enable. When phase compensation is enabled, the phase angle errors between U and IA, and U and IB, are corrected respectively.
bit5	SELI	0	To exchange the current channels. 0: current IA is sent to Current I1 Channel for signal processing, and current IB is sent to Current I2 Channel for signal processing; 1: current IA is sent to Current I2 Channel for signal processing, and current IB is sent to Current I1 Channel for signal processing.
bit4	PREN	0	To enable power and RMS calculation, and digital signal processing in M Channel. 0: disable; 1: enable.
bit3	ONM	0	To enable digital signal input to M channel. 0: disable; 0 is input to M channel. 1: enable.
Bit2	ONI2	0	To enable digital signal input to the I2 channel. 0: disable; 0s are input to I2 channel. 1: enable.
Bit1	ONI1	0	To enable digital signal input to the I1 channel. 0: disable; 0s are input to I1 channel. 1: enable.
Bit0	ONU	0	To enable digital signal input to the U channel. 0: disable; 0s are input to U channel. 1: enable.

Table 18-19 PM Control Register 2 (PMCtrl2, 0x2879)

0x2879, R/W, PM Control Register 2, PMCtrl2			
Bit		Default	Description
bit7	PGACS	0	To set sign of the digital PGA gain for I1 signal. 0: positive; 1: negative.
bit[6:4]	PGAC2~PGAC0	0	To set the digital PGA gain for I1 signal. Gain=2^{PGACx}. PGACx is over the range of 0~5.
bit3	PGAUS	0	To set sign of the digital PGA for U signal. 0: positive; 1: negative.
bit[2:0]	PGAU2~PGAU0	0	To set the digital PGA gain for U signal. Gain=2^{PGAUx}. PGAUx is over the range of 0~5. When bit LPFEN (bit5 of PMCtrl3, 0x287A) is set to 1, the digital PGA gain for U signal is lowered to 1/4 of its configuration. When bit LPFEN is cleared, the digital PGA gain for U signal is what it is configured.

Table 18-20 PM Control Register 3 (PMCtrl3, 0x287A)

0x287A, R/W, PM Control Register 3, PMCtrl3			
Bit		Default	Description
bit7	X0EN	0	Set this bit to 1 to enable zero-crossing interrupt to CPU. By default this interrupt is masked.
bit6	BPFEN	0	To enable the band-pass filter in the voltage/current RMS calculation circuits. 0: disable; 1: enable. This filter can improve the RMS calculation accuracy, but it will lead to harmonics loss. When a low signal is input, this filter will introduce greater truncation noise and prolong the period for the system to be settled.
bit5	LPFEN	0	When this bit is set to 1, the digital PGA gain for U signal is lowered to 1/4 of its configuration. When this bit is cleared, the digital PGA gain for U signal is what it is configured.
bit4	DBLEN	0	To select the function of E2 path. 0: for reactive power calculation and energy metering based on current I1. If positive current I1 is input to the path, the reactive power is negative, and it is accumulated to the negative energy accumulators; if negative current I1 is input to the path, the reactive power is positive, and it is accumulated to the positive energy accumulators. 1: for active power calculation and energy metering based on current I2.
bit3	PGANS	0	To set sign of the digital PGA gain for I2 signal. 0: positive; 1: negative.
bit[2:0]	PGAN2~PGAN0	0	To set the digital PGA gain for I2 signal. Gain=2^{PGANx}. PGANx is over the range of 0~5.

Table 18-21 Phase Compensation Control Register 1 (PHCCtrl1, 0x287B)

0x287B, R/W, Phase Compensation Control Register 1, PHCCtrl1			
Bit		Default	Description
bit7	PHCA7	0	To select the signal to be delayed. 1: to delay voltage; 0: to delay current I1.
bit6	PHCA6	0	Not used.
Bit[5:0]	PHCA<5:0>	0	Together with bit IAPHC (bit[1:0] of CRPST, 0x287F) as the right 2 bits, these 8 bits are to set the time to be delayed. When the sampling frequency of phase compensation circuit (f_{smpl}) is 3.2768MHz, the resolution of the phase compensation is 0.0055°/lsb, and 1.4° in total of the phase angle error can be calibrated.

Table 18-22 Phase Compensation Control Register 2 (PHCCtrl2, 0x287C)

0x287C, R/W, Phase Compensation Control Register 2, PHCCtrl2			
Bit		Default	Description
bit7	PHCB7	0	To select the signal to be delayed. 1: to delay voltage; 0: to delay current I2.
bit6	PHCB6	0	Not used.
Bit[5:0]	PHCB<5:0>	0	Together with bit IBPHC (bit[3:2] of CRPST, 0x287F) as the right 2 bits, these 8 bits are to set the time to be delayed. When the sampling frequency of phase compensation circuit (f_{smpl}) is 3.2768MHz, the resolution of the phase compensation is 0.0055°/lsb, and 1.4° in total of the phase angle error can be calibrated.

Table 18-23 PM Control Register 4 (PMCtrl4, 0x287D)

0x287D, R/W, PM Control Register 4, PMCtrl4			
Bit		Default	Description
bit7	CRPENR	0	To enable no-load detection of E2 path. 0: disable; 1: enable.
bit6	CRPEN	0	To enable no-load detection of E1 path. 0: disable; 1: enable.
bit5	CFENR	0	To enable CF pulse output of E2 path. 0: disable; 1: enable.
bit4	CFEN	0	To enable CF pulse output of E1 path. 0: disable; 1: enable.
bit3	EGYEN	0	To enable energy accumulation and energy-to-pulse conversion. 0: disable; 1: enable.
bit2	CFXCG	0	To select the pins for CF pulse output. 0: CF1 pin for E1 path, CF2 pin for E2 path; 1: CF2 pin for E1 path, CF1 pin for E2 path.
bit[1:0]	PSEL1/PSEL0	0	To select the source for positive active energy accumulation in E1 path. 00/11: active power calculated based on current I1; 01: I1 current RMS; 10: a constant preset in the register DATACP (0x10FC).

Table 18-24 CF Pulse Output Control Register (CFCtrl, 0x287E)

0x287E, R/W, CF Pulse Output Control Register, CFCtrl			
Bit		Default	Description
bit[7:6]	CFQR1/CFQR0	0	To adjust the energy pulse generation rate in E2 path. 00: ×1; 01: ×4; 10: ×8; 11: ×16. When low current signal is applied, configure these bits to accelerate meter calibration.

0x287E, R/W, CF Pulse Output Control Register, CFCtrl			
Bit		Default	Description
bit[5:4]	CFQ1/CFQ0	0	To adjust the energy pulse generation rate in E1 path. 00: ×1; 01: ×4; 10: ×8; 11: ×16. When low current signal is applied, configure these bits to accelerate meter calibration.
bit[3:2]	CFSELR1/CFSELR0	0	To select the energy in E2 path to be converted into pulse. 01: positive active or reactive energy in E2 path; 10: negative active or reactive energy in E2 path; 00/11: the sum of the absolute values of the positive and negative active or reactive energy in E2 path.
bit[1:0]	CFSEL1/CFSEL0	0	To select the energy in E1 path to be converted into pulse. 01: positive active energy in E1 path; 10: negative active energy in E1 path; 00/11: the sum of the absolute values of the positive and negative active energy in E1 path.

Table 18-25 No-Load Detection Indication Register (CRPST, 0x287F)

0x287F, No-Load Detection Indication Register, CRPST				
Bit		R/W	Default	Description
Bit7	CRPST	R	0	To indicate the state of E1 path. 0: metering energy; 1: creeping.
Bit6	CRPSTR	R	0	To indicate the state of E2 path. 0: metering energy; 1: creeping.
Bit[5:4]	CFWD		0	To adjust the CF pulse width. 00: 80ms; 01: 40ms; 10: 20ms; 11: 10ms.
Bit[3:2]	IBPHC	R/W	0	Together with bits PHCB<5:0> (bit[5:0] of PHCCtrl2, 0x287C) as the left 6 bits, these 8 bits are to set the time to be delayed. When the sampling frequency of phase compensation circuit (f_{smpl}) is 3.2768MHz, the resolution of the phase compensation is 0.0055°/lsb, and 1.4° in total of the phase angle error can be calibrated.
Bit[1:0]	IAPHC	R/W	0	Together with bits PHCA<5:0> (bit[5:0] of PHCCtrl1, 0x287B) as the left 6 bits, these 8 bits are to set the time to be delayed. When the sampling frequency of phase compensation circuit (f_{smpl}) is 3.2768MHz, the resolution of the phase compensation is 0.0055°/lsb, and 1.4° in total of the phase angle error can be calibrated.

Table 18-26 Current Detection Control Register (IDET, 0x2886)

0x2886, R/W, Current Detection Control Register, IDET

Bit		R/W	Default	Description
Bit7	GT	R/W	0	Set this bit to 1 to disable the sampling circuits and power/RMS calculation circuits. In this case, the energy accumulation circuit keeps on working. So, in an application to accumulate a constant for energy accumulation, it is recommended to set this bit to 1 to lower power consumption further. But please note the threshold for energy-to-pulse conversion must be set before setting this bit to 1.
Bit6	CST	R	0	When current signal is detected, this bit is set to 1 and holds until bit CLR is set to 1 or DETON is cleared.
Bit5	CLR	R/W	0	After a cycle of current detection, set this bit to 1 and then clear it to clear bit CST.
Bit4	DETON	R/W	0	1: enable current detection; 0: disable current detection.
Bit[3:0]	IDLEN	R/W	0	To set the number of current samples for current detection. If continuous ([IDLEN]+1) samples of the AC component of instantaneous I1 current are higher than the threshold for current detection (IDETTH, 0x1002), it indicates a current signal is caught. [IDLEN] is over the range of 0~15. See "Current Detection" for the relationship between IDLEN configuration and the period for current detection.

18.3. Metering Data Registers

When POR/BOR, RSTn pin reset or WDT overflow reset occurs, all metering data registers are reset to their default states.

All metering data registers are readable and writable (R/W). But users must not write of these registers to avoid unexpected results.

All the default values in this section are in decimal form if not specifically noted. All the time for updating and settling listed in the tables is appropriate for 50Hz power grid and f_{MTCLK}=3.2768MHz. When the frequency for metering architecture (f_{MTCLK}) is divided by K, the time for updating and settling must be K times of that for 3.2768MHz. In 60Hz power grid, the time for updating and settling is 1.2 times of that for 50Hz power grid.

Table 18-27 Signal Waveform Registers (R/W)

Address	Register		R/W	Default	Format	Update in	Settle in
0x1005	DATAOIU	Raw waveform of voltage.	R/W	0	32-bit 2' complement	0.3ms	10ms

Address	Register		R/W	Default	Format	Update in	Settle in
0x100A	DATAOII1	Raw waveform of Current I1.	R/W	0	32-bit 2' complement	0.3ms	10ms
0x100F	DATAOII2	Raw waveform of Current I2.	R/W	0	32-bit 2' complement	0.3ms	10ms
0x103A	DATAIDU	DC component of instantaneous voltage.	R/W	0	32-bit 2' complement	20ms	70ms
0x1041	DATAIDI1	DC component of instantaneous Current I1.	R/W	0	32-bit 2' complement	20ms	70ms
0x1048	DATAIDI2	DC component of instantaneous Current I2.	R/W	0	32-bit 2' complement	20ms	70ms
0x1051	DATAIAU	AC component of instantaneous voltage.	R/W	0	32-bit 2' complement	0.3ms	70ms
0x1052	DATAIAI1	AC component of instantaneous Current I1.	R/W	0	32-bit 2' complement	0.3ms	70ms
0x1053	DATAIAI2	AC component of instantaneous Current I2.	R/W	0	32-bit 2' complement	0.3ms	70ms

Table 18-28 Power and RMS Registers (R/W)

Address	Register		R/W	Default	Format	Update in	Settle in
0x10D1	DATAIP	Instantaneous active power in E1 path.	R/W	0	32-bit 2' complement	80ms	250ms
0x10D2	DATAIQ	Instantaneous active/reactive power in E2 path.	R/W	0	32-bit 2' complement	80ms	250ms
0x10D3	RMSIU	Instantaneous voltage RMS.	R/W	0	32-bit 2' complement	10ms	100ms
0x10D4	RMSII1	Instantaneous current I1 RMS.	R/W	0	32-bit 2' complement	10ms	100ms
0x10D5	RMSII2	Instantaneous current I2 RMS.	R/W	0	32-bit 2' complement	10ms	100ms
0x10D6	DATAP	Average active power in E1 path.	R/W	0	32-bit 2' complement	1.28s	3s
0x10D7	DATAQ	Average active/reactive power in E2 path.	R/W	0	32-bit 2' complement	1.28s	3s
0x10D8	RMSU	Average voltage RMS.	R/W	0	32-bit 2' complement	1.28s	3s

Address	Register		R/W	Default	Format	Update in	Settle in
0x10D9	RMSI1	Average current I1 RMS.	R/W	0	32-bit 2' complement	1.28s	3s
0x10DA	RMSI2	Average current I2 RMS.	R/W	0	32-bit 2' complement	1.28s	3s
0x10DB	DATAAP1	Average apparent power calculated based on average current I1 and voltage RMS.	R/W	0	32-bit 2' complement	1.28s	3s
0x10DC	DATAAP2	Average apparent power calculated based on average current I2 and voltage RMS.	R/W	0	32-bit 2' complement	1.28s	3s

Table 18-29 Energy Accumulators and Energy Pulse Counters (R/W)

Address	Register		R/W	Default	Format
0x10F0	PPCNT	Positive active energy accumulator in E1 path.	R/W	0	32-bit, unsigned
0x10F1	NPCNT	Negative active energy accumulator in E1 path.	R/W	0	32-bit, unsigned
0x10F2	PPCFCNT	Positive active energy pulse counter in E1 path.	R/W	0	32-bit, unsigned
0x10F3	NPCFCNT	Negative active energy pulse counter in E1 path.	R/W	0	32-bit, unsigned
0x10F6	PQCNT	Positive active/reactive energy accumulator in E2 path.	R/W	0	32-bit, unsigned
0x10F7	NQCNT	Negative active/reactive energy accumulator in E2 path.	R/W	0	32-bit, unsigned
0x10F8	PQCFCNT	Positive active/reactive energy pulse counter in E2 path.	R/W	0	32-bit, unsigned
0x10F9	NQCFCNT	Negative active/reactive energy pulse counter in E2 path.	R/W	0	32-bit, unsigned

Address	Register	R/W	Default	Format
The energy accumulators are of actual 42-bit length. But only the higher 32 bits are readable; and only the higher 32 bits are valid for write operation and the 10 least significant bits are padded with 0s in write operation. When MTCLK frequency is 3.2768MHz, 1.6384MHz or 819.2kHz, the energy accumulation frequency is 12800Hz; when MTCLK frequency is 32768Hz, the energy accumulation frequency is 2979Hz. When CF pulse output is enabled, the overflow frequency of the energy accumulators is twice of CF pulse output frequency. The reading of the energy pulse counter is twice of the number of the output CF pulses.				

Table 18-30 Line Frequency Register (DATAFREQ, 0x10FD)

0x10FD, R, Line Frequency Register, DATAFREQ							
	Value	bit15	bit14	……	……	bit1	bit0
Default	0x0000	0	0	0	0	0	0
This register is in the form of 16-bit unsigned. When MTCLK frequency is 3.2768MHz, the content is updated in 320ms and settled in 500ms. The frequency measurement resolution is up to 0.05Hz/lsb, and the measurement scale is over the range of 35~75Hz.							

Table 18-31 Data Registers for Channel M

Address	Register		R/W	Default	Format	Update in	Settle in
0x10CE	DATAOM	Raw waveform of Channel M.	R/W	0	32-bit 2’ complement	0.3ms	10ms
0x10CF	DATADM	DC component of the measurement of Channel M.	R/W	0	32-bit 2’ complement	20ms	70ms
0x10D0	DATAADM	Average DC component of the measurement of Channel M.	R/W	0	32-bit 2’ complement	1.28s	3s

18.4. Calibration Registers

When POR/BOR, RSTn pin reset or WDT overflow reset occurs, all calibration registers are reset to their default states.

All the default values in this section are in decimal form if not specifically noted.

Table 18-32 Registers for Gain Calibration (R/W)

Address	Register		R/W	Format	Default	Description
0x10E8	SCP	To set a value to gain calibrate active power in E1 path.	R/W	32-bit 2’ complement	0	The gain calibration range

Address	Register		R/W	Format	Default	Description
0x10EB	SCI1	To set a value to gain calibrate current I1 RMS.	R/W	32-bit 2′ complement	0	is from -∞ to +49.9%.
0x10E9	SCQ	To set a value to gain calibrate active/reactive power in E2 path.	R/W	32-bit 2′ complement	0	
0x10EC	SCI2	To set a value to gain calibrate current I2 RMS.	R/W	32-bit 2′ complement	0	
0x10EA	SCU	To set a value to gain calibrate voltage RMS.	R/W	32-bit 2′ complement	0	

Table 18-33 Registers for Power Offset Calibration (R/W)

Address	Register		R/W	Format	Default	Description
0x10ED	PARAPC	To set a value to offset calibrate active power in E1 path.	R/W	32-bit 2′ complement	0	The gain calibration range is from -50% to +50%.
0x10EE	PARAQC	To set a value to offset calibrate active/reactive power in E2 path.	R/W	32-bit 2′ complement	0	

Table 18-34 Band-pass Filter Coefficient Register (0x10EF, R/W)

Address	Register		R/W	Format	Default
0x10EF	PARABPF	To set the coefficient for the band-pass filter in the RMS calculation circuits.	R/W	32-bit 2′ complement	0x889374BC

When MTCLK frequency is lowered to 819.2kHz, the sampling frequency of the enabled band-pass filter in the RMS calculation circuit is changed to 800Hz and the center frequency is changed to 12.5Hz, which has a greater attenuation on 50Hz signals and will reduce the accuracy of the RMS calculation and line frequency measurement. So, if MTCLK frequency is reduced to 819.2kHz, users must disable energy accumulation, CF pulse output and no-load detection, and then configure this register to 0x911D3C9C. When MTCLK frequency is reinstated to 3.2768MHz, this register must be set to its default value.

Table 18-35 Energy Threshold Registers and Constant Power Register (R/W)

Address	Register		R/W	Format	Default
0x10F4	GATEP	To set a threshold for active energy-to-pulse conversion in E1 path.	R/W	32-bit, unsigned	0
0x10F5	GATECP	To set a threshold for no-load detection in E1 path.	R/W	32-bit, unsigned	0
0x10FA	GATEQ	To set a threshold for active or reactive energy-to-pulse conversion in E2 path.	R/W	32-bit, unsigned	0

Address	Register		R/W	Format	Default
0x10FB	GATECQ	To set a threshold for no-load detection in E2 path.	R/W	32-bit, unsigned	0
0x10FC	DATACP	To set a constant for active energy accumulation in E1 path.	R/W	32-bit 2' complement	0

The energy accumulators are of actual 42-bit length, but the threshold registers for energy-to-pulse conversion are of 32-bit length. So, the threshold registers will be padded with a string of 10 0s on the right to work as 42-bit registers for computation.

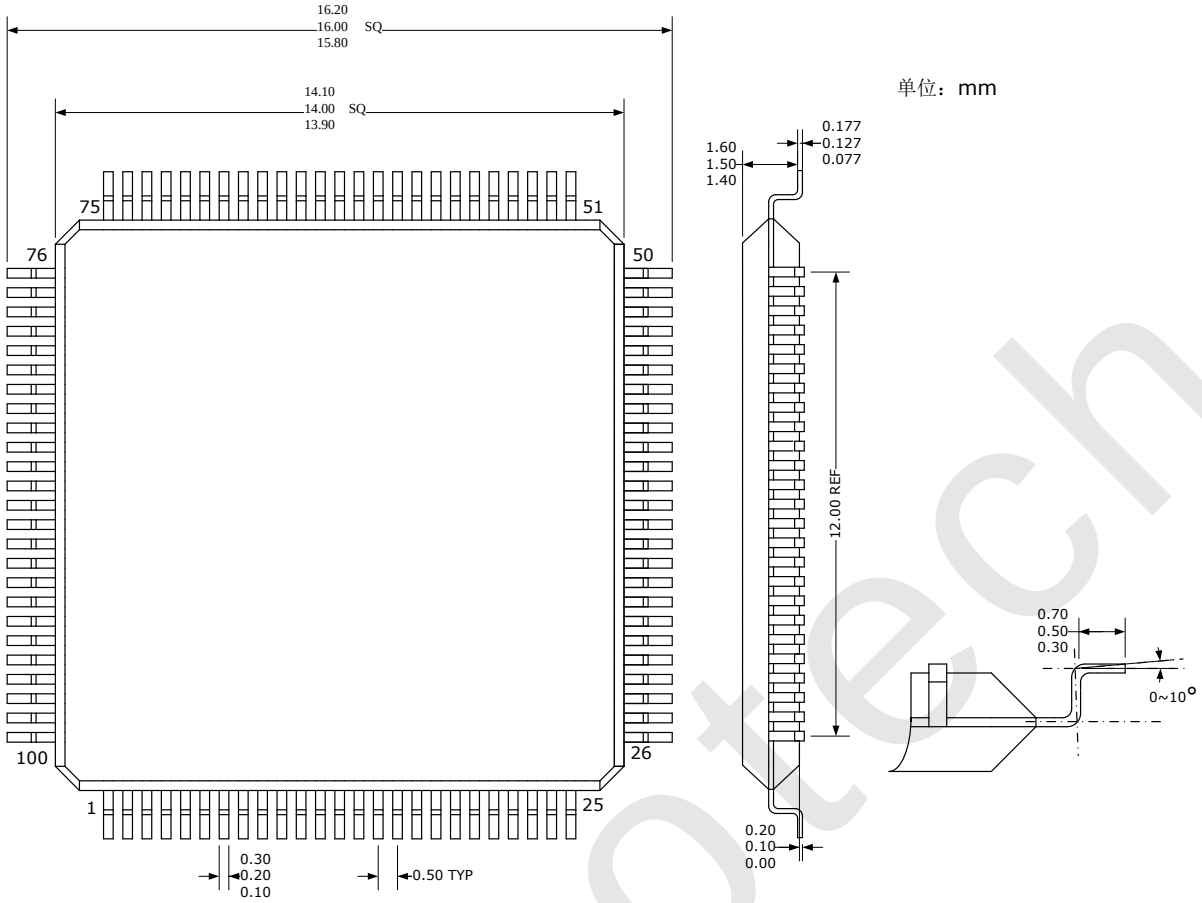
There is an anti-creeping accumulator in the no-load detection circuit. When no-load detection is enabled, 1s are accumulated in this register constantly. When MTCLK frequency is 3.2768MHz, 1.6384MHz or 819.2kHz, the accumulation frequency is 12800Hz; and when MTCLK frequency is 32768Hz, the accumulation frequency is 2979Hz.

When no-load detection is enabled, the circuit compares the rate at which the anti-creeping accumulator increments by 1s to that at which the energy accumulators accumulate E1/E2 power or the preset constant. If the energy accumulator overflows sooner, the anti-creeping accumulator is cleared, and E1 or E2 path starts to metering energy. Otherwise, the energy accumulator in E1 or E2 path is cleared, and the path enters creeping state. Users can read bit7 or bit6 of register CRPST (0x287F) to detect the state of the path.

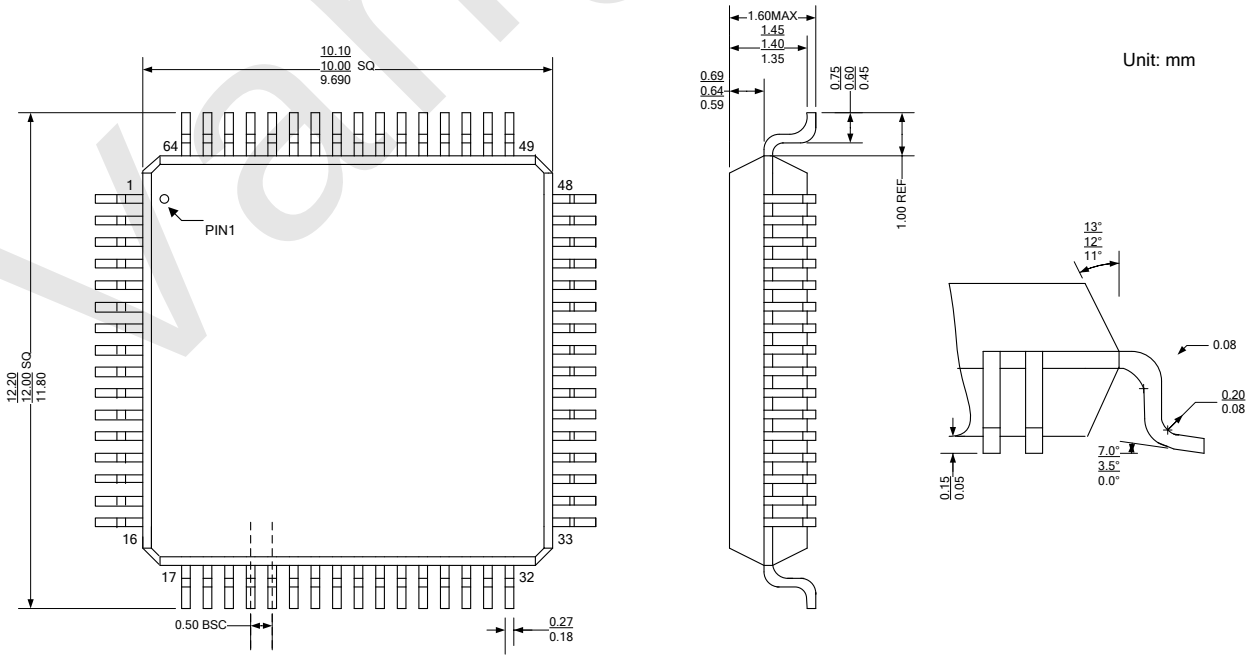
Table 18-36 Threshold Register for Current Detection (R/W)

Address	Register		R/W	Format	Default
0x1002	IDETTH	To set a threshold for current detection.	R/W	32-bit 2' complement, both bit31 and bit30 are sign bits.	0

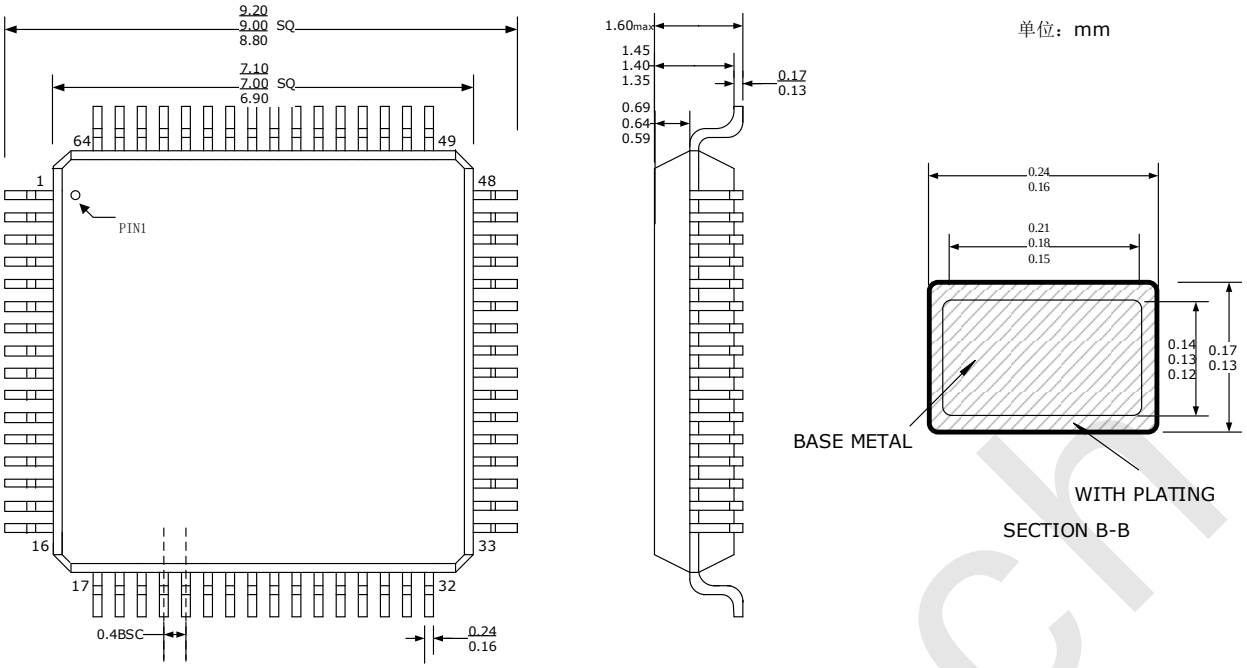
19. Outline Dimensions



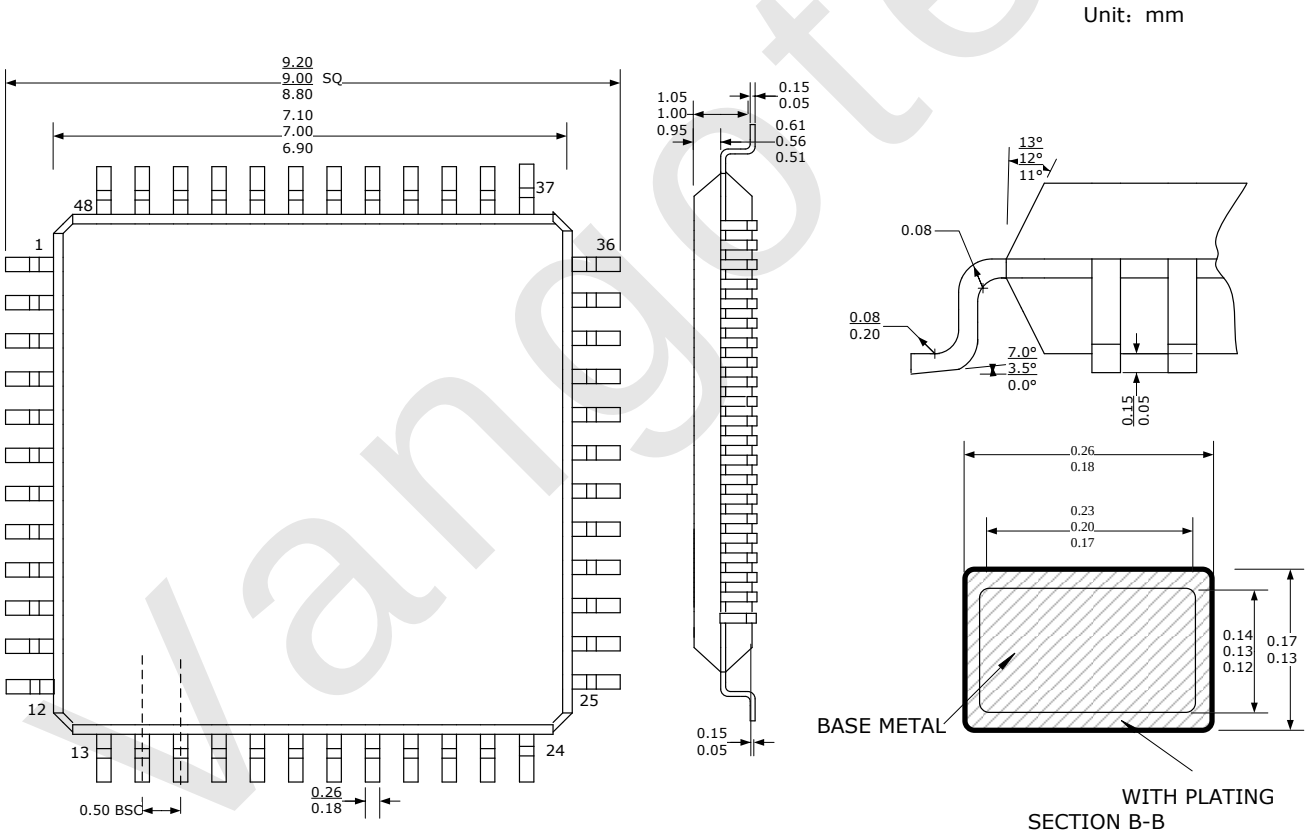
V9801S



V9811S/V9811A

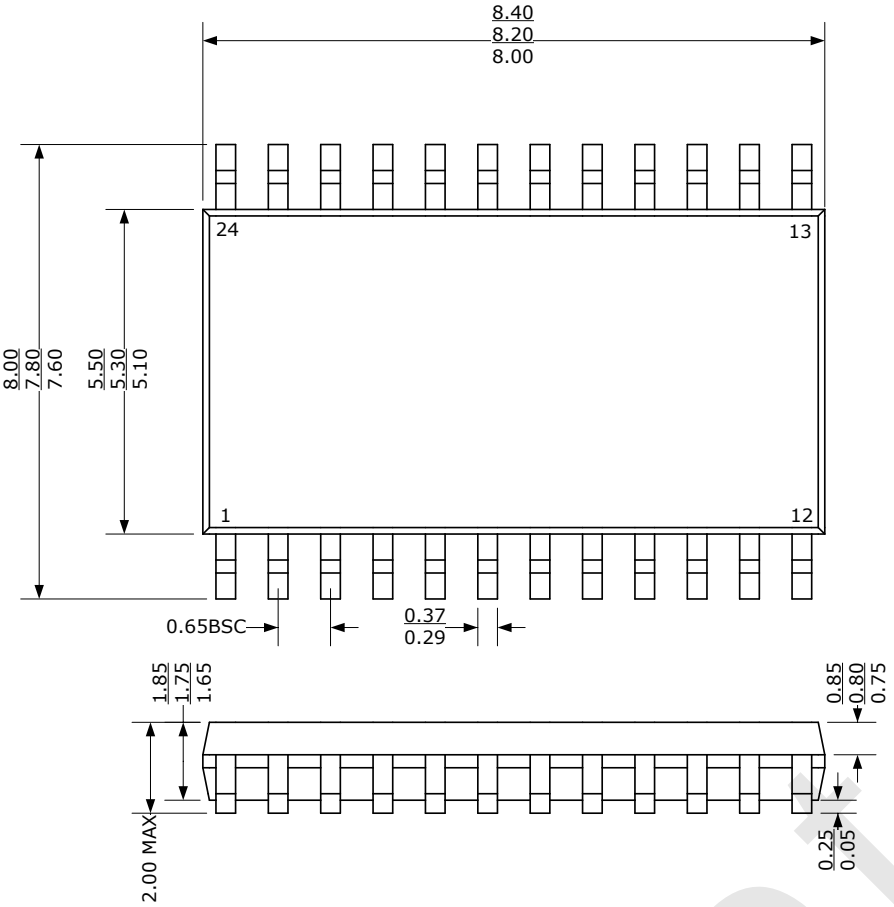


V9811B



V9821/V9821S

单位：mm



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