V8133L

Reference Manual Brief

Specifications are subject to change without notice.

Declaration

Revision History

Revision	Date	Description
1.0	Oct.12,2021	Initial Version

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1.About This Documentation

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1.1. Purpose

This document provides an overall description of the Vango's V8133L application processor, which describes the overview, features, logical structures, functions and register listings of each module. The document also describes the interface timings and related parameters in diagrams. In addition, the document describes the pins, pin usages, performance parameters, and package dimension of V8133L in detail.

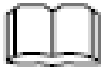
1.2. Intended Audience

The document is intended for:

- Design and maintenance personnel for electronics
- Sales personnel for electronic parts and components

1.3. Symbol Conventions

The symbols that may be found in this document are defined as follows.

Symbol	Description
 **WARNING**	A warning means that injury or death is possible if the instructions are not obeyed.
 **CAUTION**	A caution means that damage to equipment is possible.
 **NOTE**	Provides additional information to emphasize or supplement important points of the main text.

1.4. Acronyms and Abbreviations

The table below contains acronyms and abbreviations used in this documentation.

AES	Advanced Encryption Standard
ADC	Analog-to-Digital Converter
AHB	AMBA High-speed Bus
APB	Advanced Peripheral Bus
ARM	Advanced RISC Machine
CPU	Central Processing Unit
CRC	Cyclic Redundancy Check
DES	Data Encryption Standard
DLL	Delay-Locked Loop
DMA	Direct Memory Access
ECC	Error Correction Code
eFuse	Electrical Fuse, A one-time programmable memory
EHCI	Enhanced Host Controller Interface
eMMC	Embedded Multi-Media Card
ESD	Electrostatic Discharge
FBGA	Fine Ball Grid Array
FIFO	First In First Out
GIC	Generic Interrupt Controller
GMII	Gigabit Media Independent Interface
GPIO	General Purpose Input Output
GPU	Graphics Processing Unit
I2C	Inter Integrated Circuit
I2S	Inter IC Sound
JEDEC	Joint Electron Device Engineering Council
JTAG	Joint Test Action Group
LCD	Liquid-Crystal Display
LSB	Least Significant Bit
MAC	Media Access Control
MII	Media Independent Interface
MMC	Multimedia Card
MSB	Most Significant Bit
N/A	Not Application
NMI	Non Maskable Interrupt
PAL	Phase Alternating Line
PCM	Pulse Code Modulation
PHY	Physical Layer Controller

PID	Packet Identifier
PLL	Phase-Locked Loop
PWM	Pulse Width Modulation
R	Read only/non-Write
RGB	Read Green Blue
RMII	Reduced Media Independent Interface
ROM	Read Only Memory
RTC	Real Time Clock
RW	Read/Write
RWAC	Read/Write-Automatic-Clear,clear the bit automatically when the operation of complete.Write 0 has no effect
RWC	Read/Write-Clear
RW1C	Read/Write 1 to Clear, Writing 0 has non-effect
RW1S	Read/Write 1 to Set, Writing 0 has non-effect
Rsvd	Reserved: Reserved for future RO implementations. Software shall ignore the value read from these bits.
SDIO	Secure Digital Input Output
SDRAM	Sychronous Dynamic Random Access Memory
SOC	System On Chip
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
UART	Universal Asynchronous Receiver Transmitter
UDF	Undefined
USB	Universal Serial Bus
UTMI	USB2.0 Transceiver Macrocell Interface

2. Overview

This part describes the overview for V8133L processor.

- Processor Overview
- Features
- Block Diagram

2.1. Processor Overview

The V8133L processor represents Vango's latest achievement in intelligent industrial control processors. The processor is ideal for applications that require advanced data processing, rich user interfaces, lower power consumption and higher system integration.

The V8133L processor has some very exciting features:

• **CPU:** V8133L is based on Cortex™-A7 CPU architecture, the most power efficient CPU core ARM's ever developed.

• **Display:** Content can be displayed on RGB panel.

• **Audio:** Supports I2S interface for connecting to an external audio codec.

• **Memory:** Supports external memory interfaces to NAND Flash, eMMC, NOR Flash and SDRAM port. SDRAM port can be configured to support LPDDR2, DDR2, DDR3, DDR3L, MDDR.

• **Peripherals:** To reduce total system cost, V8133L has a broad range of hardware peripherals to meet the flexible peripheral configuration requirements such as UART, SPI, USB2.0 OTG, CAN, I2C, MAC, etc.

2.2. Features

2.2.1. CPU Architecture

• Cortex™-A7 Processor
  - ARMv7 ISA standard ARM instruction set
  - Thumb-2 Technology
  - TrustZone
  - Jazeller RCT
  - NEON Advanced SIMD
  - VFPv4 floating point
  - Large Physical Address Extensions(LPAE)
  - 32KB L1 Instruction cache and 32KB L1 Data cache for per CPU
  - 512KB L2 cache

2.2.2. Memory

2.2.2.1. Boot ROM

- On-chip 32KB ROM boot loader
- Supports fast boot from SPI NAND Flash, eMMC, SPI NOR Flash, or those images downloaded via UART.
- Supports system code download through USB OTG, UART, and Ethernet

2.2.2.2. Embedded SRAM

- 128KB + 32KB SRAM
- 2 instances of 32KB SRAM for one port RGMII GMAC controller memory
- 2 instances of 4KB SRAM for one port RMII MAC controller memory
- 2 instances of 4KB SRAM for one port MII MAC controller memory

2.2.2.3. SDRAM

- Compatible with JEDEC standard DDR2/DDR3/DDR3L/LPDDR2/MDDR SDRAM
- Up to 4GB address space
- 8/16/32-bit data bus width
- 8-bit for ECC that can do one-bit error correction, and two-bit error detection
- Supports clock frequency up to 1600MHz(DDR3)

2.2.2.4. eMMC

- Up to two ports, the first one is bootable
- JEDEC eMMC 5.1 mandatory part
- HS200, not support high speed DDR and HS400
- Up to 32 GB in device density

2.2.3. System Peripherals

2.2.3.1. Timer

- 8 independent 32-bit timers
- Four watchdog to generate reset signal or interrupt

• Internal or external clock source for each timer

2.2.3.2. GIC

• Supports 16 SGIs(Software Generated Interrupt), 16 PPIs(Private Peripheral Interrupt) and 101 SPIs(Shared Peripheral Interrupts)

• Supports ARM architecture security extensions

• Supports ARM architecture virtualization extensions

2.2.3.3. DMA

• 3 instances ,8 channels for each instance. Two instances in AXI, Channel arbiter with 2-level round-robin mechanism. One instance in AHB, Channel arbiter with 4-level round-robin mechanism.

• Interrupt generated for each DMA channel

• Transfers data width of 8/16/32/64-bit

• Supports linear and IO address modes

• Programs the DMA burst size

• Flexible data source and destination address generation

• Supports data transfer types with memory-to-memory, memory-to-peripheral, peripheral-to-memory

2.2.3.4. SCU

• 7 PLLs. There are total 7 PLL instances to create AXI, APB, and peripheral clocks.

• Two external oscillators. One is 25MHz oscillator, and another is 32.768kHz oscillator.

• Two internal ring oscillators for CPU fast booting purpose and RTC. One is 120MHz, and +/- 5% accuracy for CPU operation clock, and another is 32.768KHz for RTC awake module purpose.

• Supports clock configuration and clock generated for corresponding modules.

• Supports software-controlled clock gating and software-controlled reset for corresponding modules.

2.2.3.5. RTC

• Timer, Calendar, Alarm

• Supports full clock features: second/minute/hour/day/month/year(with leap year)

2.2.3.6. PWM

• 16 PWM channels outputs(4 PWM instances)

• Supports three kinds of output waveforms: continuous waveform, pulse waveform and complementarity pair
• Programmable deadzone generator and controllable dead-time
• 0% to 100% adjustable duty cycle
• Up to 15/100MHz output frequency
• Minimum resolution is 1/(65536*65536)
• Supports interrupt for PWM output

2.2.3.7. Thermal Sensor

• Temperature Accuracy：
  ±5℃ from -40℃ to 0℃
  ±3℃ from 0℃ to +100℃
  ±5℃ from 100℃ to +125℃
• Supports over-temperature protection interrupt and over-temperature alarm interrupt
• Averaging filter for thermal sensor reading

2.2.3.8. Crypto Engine

AES
• NIST FIPS 197
• Key size: 128-bit, 192-bit, and 256-bit
• Modes based on NIST SP 800-38: ECB, CTR, CBC, CFB, OFB, CBC-CS2, CMAC, CCM, GCM, and XTS
HASH
• FIPS 180-3: MD-5, SHA-1, SHA-256, SHA-224, SHA-384, and SHA-512
• FIPS 198: HMAC is supported for all algorithms except SM3
• 66 cycles per 512-bits blocks for MD5, SHA-224, and SHA-256
• 82 cycles per 512/1024-bits blocks for SHA-1, SHA-384, and SHA-512
TRNG
• FIPS 140-2 certification
• Pass NIST-800-22, NIST-800-90B, and AIS31

2.2.3.9. eFuse

• One on-chip 4Kbit eFuse

2.2.4. Display Subsystem

2.2.4.1. Video Output

- Programmable resolution of up to 2048x2048
- RGB serial output: 8-bit
- Pixel clock rate of up to 150MHz

2.2.5. External Peripherals

2.2.5.1. USB

- Up to three USB OTG interfaces
- USB 2.0 OTG, with integrated one USB 2.0 analog PHY
- Compatible with USB2.0 Specification
- Support High-Speed(HS,480Mbit/s),Full-Speed(FS,12Mbit/s),and Low-Speed(LS,1.5Mbit/s) in host mode
- Supports High-Speed (HS, 480Mbit/s), Full-Speed (FS, 12Mbit/s) in Device mode
- Up to 8 user-configurable endpoints for Bulk, Isochronous, Control and Interrupt transfer

2.2.5.2. MAC

- Up to three MAC interfaces
- Compliant with the IEEE 802.3-2002 standard
- Programmable frame length to support Standard or Jumbo Ethernet frames with size up to 9KB
- Supports 10/100/1000Mbps data transfer rates
- One RGMII port, one RMII port, and one MII port
- Supports a variety of flexible address filtering modes
- Supports full and half duplex operations

2.2.5.3. SPI

- Up to 9 independent SPI controllers
  - One port for SPI flash with XIP, and prefetch
  - One port for ESAM

- 7 ports for others, and can be master or slave

• Internally generated or externally supplied serial clock, and can be up to 100MHz
• Programmable frame/sync polarity
• Programmable serial clock polarity, phase, and frequency
• Programmable serial bit sequences (MSB or LSB first)
• Serial data length ranges from 4 bits to 128 bits
• Texas Instrument Synchronous Serial Port, Motorola Serial Peripheral Interface, National Semiconductor MICROWIRE, and LCD driver serial interface

2.2.5.4. UART

• Up to 10 UART controllers
  - Six ports(UART0/ 1/ 4/ 6/ 7/ 9) only support UART without RTS/CTS
  - Two ports(UART2/ 3) only support UART with RTS/CTS
  - Two ports(UART5/ 8) only support IrDA, and without RTS/CTS
• Compatible with industry-standard 16C550A UARTs
• Supports for word length from 5 to 8 bits,an optional parity bit,and 1,1.5 or 2 stop bits
• Programmable parity(even,odd and no parity)
• UART baud rate from 1200bps to 3686400bps
• IrDA 1.3 SIR with up to 115200bps
• IrDA 1.3 FIR 4000000bps

2.2.5.5. I2C

• Five I2C ports
• Mode: Standard, Fast, Fast+ (F/S), High-Speed (Hs)
• master-TX, master-RX, slave-TX, and slave-RX
• multi-master mode
• 7-bit, 10-bit

2.2.5.6. I2S

• Two I2S ports
• Can be reconfigured as SPI
• Can be master or slave

- Internally generated or externally supplied serial clock
- Programmable frame/sync polarity
- Programmable serial clock polarity, phase, and frequency
- Programmable serial bit sequences (MSB or LSB first)
- Serial data length ranges from 4 bits to 128 bits
- Philips I2S, Intel AC-link, SPDIF frame
- Programmable I2S format (Includes data padding bits and justification)

2.2.5.7. CAN

- Two CAN ports
- Bosch CAN 2.0 A/B and FD 1.0
- Arbitration bit rate up to 1Mbps
- Data bit rate up to 8 Mbps

2.2.5.8. Keypad

- One keypad matrix interface up to 8 rows and 16 columns
- Interrupt for key press or key release
- Internal debouncing filter to prevent switching noises

2.2.6. Package

- TFBGA 510 balls, 0.65mm ball pitch, 16mm x 16mm

2.3. Block Diagram

The follow figure shows the block diagram of the V8133L processor.

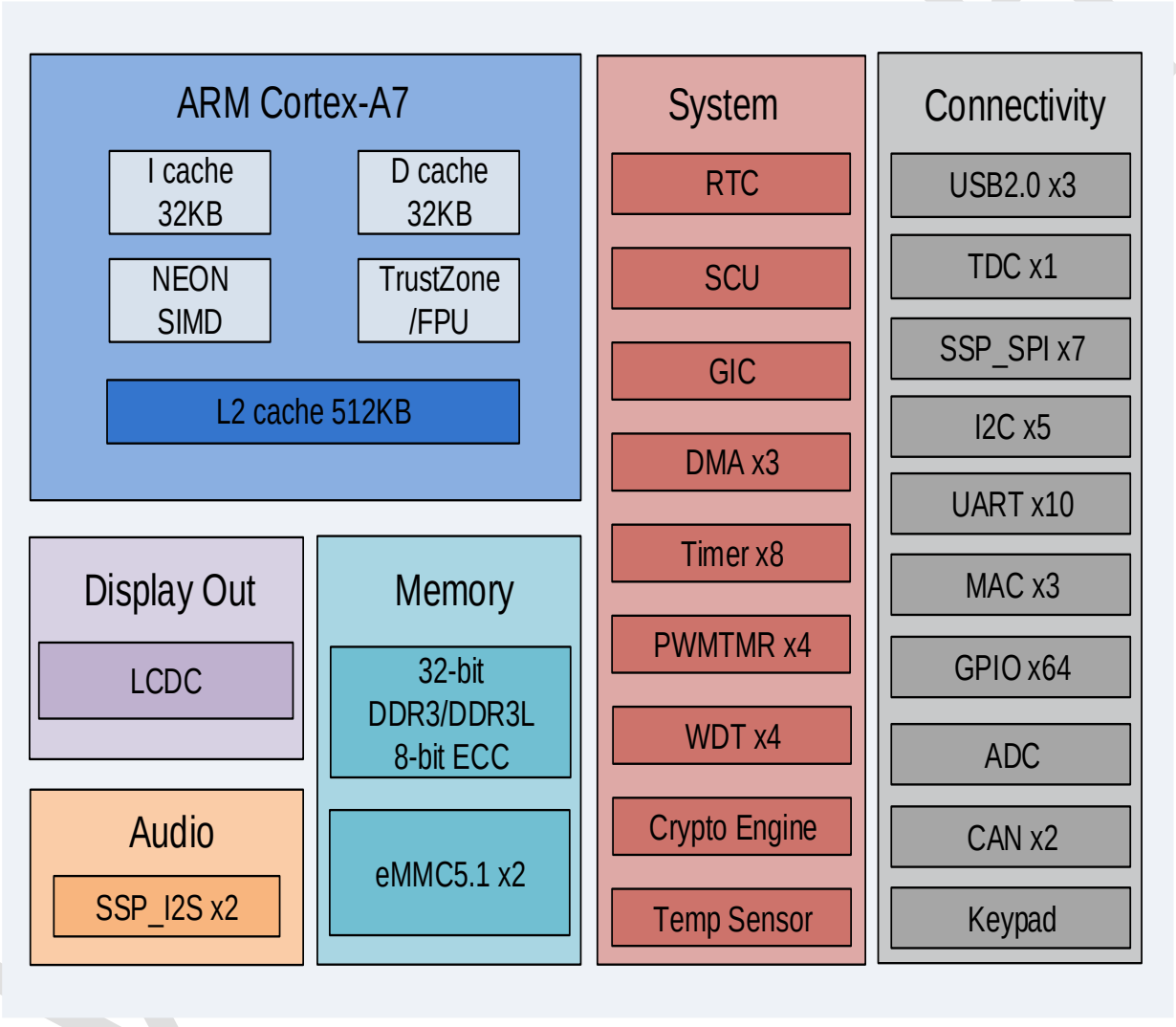


Figure 2-1. V8133L Block Diagram

3.Pin Description

This part details the V8133L pin description from the following aspects:

- Pin Characteristics
- GPIO Multiplex Function
- PWM timer output signals
- Signal Descriptions

3.1. Pin Characteristics

Table 3-1 lists the characteristics of V8133L pins.

Table 3-1. Pin Characteristics

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
A	GND	X_DDR_RDRVUP	X_DDR_DQ_1[6]	X_DDR_DQ_1[4]		X_DDR_DM_1	X_DDR_DQ_1[7]		X_DDR_DQ_3[4]	X_DDR_DQS_3		X_DDR_DQ_3[1]	X_DDR_DQ_3[5]		X_DDR_DM_4	X_DDR_DQ_4[4]		X_MII_COL	X_MII_MDIO		X_MII_RXD[0]	X_MII_RXD[1]	X_RMII_TXD[1]	GND
B	X_DDR_RASN	X_DDR_RDRVDN	X_DDR_DQ_1[2]	X_DDR_DQ_1[0]	X_DDR_DQS_1	X_DDR_DQ_1[1]	X_DDR_DQ_1[5]	X_DDR_DQ_3[2]	X_DDR_DQ_3[6]	X_DDR_DQSB_3	X_DDR_DQ_3[0]	X_DDR_DM_3	X_DDR_DQ_3[3]	X_DDR_DQ_4[5]	X_DDR_DQ_4[1]	X_DDR_DQ_4[7]	X_DDR_DQ_4[6]	GND	X_MII_MDC	X_MII_RX_DV	X_MII_RX_CK	X_MII_RXD[2]	X_RMII_RXD[1]	X_RMII_RXD[0]
C	X_DDR_CKE[0]	X_DDR_CASN	X_DDR_VREF_D0	X_DDR_VREF_D1	X_DDR_DQSB_1	X_DDR_DQSB_0	X_DDR_DQ_1[3]	GND	X_DDR_VREF_D2	X_DDR_VREF_D3	GND	X_DDR_DQSB_2	X_DDR_DQ_3[7]	X_DDR_DQ_4[3]	GND	X_DDR_DQ_4[0]	X_DDR_DQ_4[2]	GND	X_MII_TXD[0]	X_MII_RX_ER	X_MII_TXD[3]	X_RMII_REF_CLK	X_RMII_RXD[0]	X_RMII_RX_CRSDV
D	X_DDR_WEN	X_DDR_ADDR[10]	GND	X_DDR_DQ_0[7]		GND	X_DDR_DQS_0		GND	X_DDR_DQ_2[7]		GND	X_DDR_DQS_2		X_DDR_DQS_4	X_DDR_VREF_D4		X_MII_CRS	X_MII_TX_EN	X_UART0_RX	X_RMII_MDIO		

	X_RGMII_MDIO	X_RGMII_RXD[1]		X_RGMII_TXD[3]
X_RMII_MDC	X_RGMII_GTX_CK	X_RGMII_RXD[2]	X_RGMII_TXD[1]	X_RGMII_TXD[2]
X_UART0_TX	X_RGMII_RXCTL	X_RGMII_MDC	X_RGMII_TXD[0]	X_RGMII_TXCTL
X_I2C2_CLK	X_I2C2_DATA	X_RGMII_RX_CK		X_RGMII_RXD[3]
	GND	X_RGMII_RXD[0]		X_SPI1_CS
X_MII_TXD[1]	X_MII_TXD[2]	X_HSPI_DO	X_HSPI_CS	X_SPI1_DO
X_MII_TX_ER	X_MII_TX_CK	VCC3IO	VCC3IO	VCCK
	GND	VCC15O_DDR	VCC15O_DDR	GND
GND	X_MII_RXD[3]	VCC15O_DDR	VCC15O_DDR	GND
X_DDR_DQSB_4	GND	VCC15O_DDR	VCC15O_DDR	GND
	GND	VCC15O_DDR	GND	GND
X_DDR_DQ_2[6]	X_DDR_DQ_2[2]	VCC15O_DDR	VCC15O_DDR	GND
X_DDR_DQ_2[4]	X_DDR_DQ_2[1]	VCC15O_DDR	VCC15O_DDR	GND
	GND	VCC15O_DDR	VCC15O_DDR	GND
X_DDR_DQ_2[0]	X_DDR_DQ_2[3]	VCC15O_DDR	GND	GND
X_DDR_DQ_2[5]	X_DDR_DM_2	VCC15O_DDR	VCC15O_DDR	GND
	GND	VCC15O_DDR	VCC15O_DDR	GND
X_DDR_DQ_0[6]	X_DDR_DQ_0[2]	VCC15O_DDR	VCC15O_DDR	GND
X_DDR_DQ_0[4]	X_DDR_DQ_0[1]	GND	X_DDR_ODT[1]	X_DDR_ODT[0]
	GND	X_DDR_CKE[1]		X_DDR_ADDR[9]
X_DDR_DQ_0[0]	X_DDR_DQ_0[3]	X_DDR_ADDR[2]		GND
X_DDR_DQ_0[5]	X_DDR_DM_0	X_DDR_ADDR[0]	X_DDR_BA[1]	X_DDR_ADDR[13]
X_DDR_CSN[0]	X_DDR_CK	X_DDR_CSN[1]	X_DDR_ADDR[3]	X_DDR_ADDR[1]
	X_DDR_CKB	X_DDR_ADDR[15]		X_DDR_ADDR[11]
E	**F**	**G**	**H**	**J**

X_HSPI_CLK		X_SPI1_DI	X_SPI6_CLK	
X_HSPI_DI	X_SPI1_CLK	X_SPI6_DI	X_SPI5_CLK	X_SPI4_CLK
X_SPI5_DO	X_SPI5_CS	X_I2S_MCLK	X_SPI0_CLK	X_SPI0_DO
GND		X_I2S0_RXD	GND	
X_SPI6_CS		X_SPI4_CS	X_JTAG_TDO	
X_SPI6_DO	X_SPI4_DO	X_JTAG_SWDITMS	X_SPI3_DO	X_SPI3_CS
VCCK	VCC3IO	VCC3IO	VCCK	VCCK
GND	GND	GND	GND	GND
GND	GND	GND	GND	GND
VCCK	GND	GND	GND	GND
VCCK	VCCK	GND	GND	GND
GND	GND	GND	GND	GND
VCCK	VCCK	GND	GND	GND
GND	GND	GND	GND	GND
VCCK	VCCK	GND	GND	GND
GND	GND	GND	GND	GND
VCCK	VCCK	VCC11A_PLL_DDR	GND11A_PLL04	GND33A_PLL_USB2
GND	VCC15O_DDRCK	GND11A_PLL_DDR	VCC11A_PLL04	GND33A_HSRT_USB2
X_DDR_ADDR[7]	X_DDR_BA[0]	X_DDR_ADDR[12]	GND	VCC11K_RTC
X_DDR_RESETN		GND	VCC3IO_RTC	
X_DDR_ADDR[5]		VCC3IO_RTCOSC	X_SPI_DCX1	
X_DDR_BA[2]	X_DDR_ADDR[8]	GND	X_OM	X_UART9_TX
X_DDR_ADDR[14]	X_DDR_ADDR[6]	GND	X_RESET_N	X_SPI_DCX2
X_DDR_ADDR[4]		X_RTC_XTAL_IN	X_RTC_XTAL_IO	
K	**L**	**M**	**N**	**P**

X_SPI5_DI	X_SPI4_DI		X_JTAG_TRST_N
X_SPI0_DI	X_JTAG_TDI	X_SPI3_CLK	X_SPI3_DI
X_SPI0_CS	X_UART3_RX	X_JTAG_SWCLKTCK	X_UART2_NRTS
X_UART4_TX	X_I2C0_CLK		GND
X_I2C3_CLK	X_UART3_TX		X_UART2_NCTS
X_UART3_NRTS	X_SPI_HOLD_N	X_SPI_CLK	X_USB0_VBUS
VCC3IO	VCC3IO	GND11A_DLL_1	GND11A_DLL_0
GND	VCC3IO	VCC11A_DLL_1	VCC11A_DLL_0
GND	VCC3IO	GND	GND
GND	VCCK	VCC33A_PLL_USB0	VCC33A_HSRT_USB0
GND	VCCK	GND33A_HSRT_USB0	GND33A_PLL_USB0
GND	VCC3IO	VCC33IO_ADC	GND33IO_ADC
GND	VCC3IO	GND33A_ADC	VCC33A_ADC
GND	VCCK	GND11A_PLL35	VCC11A_PLL35
GND	VCCK	GND	GND
VCCK	VCCK	GND11A_PLL126	VCC11A_PLL126
VCC33A_PLL_USB2	GND33A_PLL_USB1	VCC33A_PLL_USB1	GND
VCC33A_HSRT_USB2	GND33A_HSRT_USB1	VCC33A_HSRT_USB1	VCC3IO_OSC
X_UART5_TX	X_PSW_0	GND	X_I2C1_CLK
X_UART6_RX	X_UART8_RX_H		X_I2C1_DATA
X_PSW_DDRCK	X_UART8_RX		GND
X_UART9_RX	X_UART5_RX	X_UART8_TX	GND
X_UART6_TX	X_UART7_RX	GND	X_USB2_DM
X_UART5_RX_H	X_UART7_TX		X_USB2_DP
R	T	U	V

X_I2C0_DATA		X_I2S0_FS	X_I2S0_SCLK
X_UART3_NCTS	X_SPI_WP_N	X_I2S0_TXD	GND
X_UART2_RX	X_SPI_DO	X_SPI_CS_N	X_USB0_DRVBUS
X_UART1_RX	X_SPI7_DO	X_SPI7_CS	GND
X_SPI_DI			X_EMMC0_RSTN
GND	X_EMMC1_CMD	X_EMMC1_D3	VCC3IO_EMMC0
X_EMMC1_CLK	X_EMMC1_D1	X_EMMC1_D5	X_EMMC0_CLK
X_EMMC1_D0			X_EMMC0_D1
X_EMMC1_D2	X_EMMC1_D4	X_EMMC1_D6	X_EMMC1_RSTN
GND	GND	VCC3IO_EMMC1	GND33A_HSRT_USB0
GND			X_USB0_DM
VCC33A_TDC	GND33A_TDC	VCC3IO_EFUSE	
GND33D_ADC	VCC33D_ADC	GND33A_ADC	X_ADC_XAIN[6]
GND			X_ADC_XVRT
X_USB1_DRVBUS	GND	GND33A_ADC	X_ADC_XAIN[2]
GND			GND33A_ADC
X_USB2_DRVBUS	X_LC_HS	X_LC_VS	X_LC_DE
X_USB1_VBUS	X_LC_PCLK	X_LC_DATA[23]	X_LC_DATA[16]
X_USB2_VBUS	X_LC_DATA[19]	X_LC_DATA[20]	X_LC_DATA[22]
X_LC_DATA[18]			X_LC_DATA[12]
X_SPI2_CS	X_LC_DATA[2]	X_LC_DATA[3]	X_LC_DATA[9]
GND	X_SPI2_DO	X_LC_DATA[0]	X_LC_DATA[4]
X_USB1_DM	GND	X_SPI2_DI	X_LC_DATA[5]
X_USB1_DP		X_SPI2_CLK	X_LC_DATA[1]
W	**Y**	**AA**	**AB**

X_I2C3_DATA	GND
X_UART4_RX	X_UART2_TX
X_UART1_TX	X_SPI7_CLK
GND	X_SPI7_DI
X_EMMC0_D2	
X_EMMC0_D6	X_EMMC0_D0
X_EMMC1_D7	X_EMMC0_D4
X_EMMC0_D7	
X_EMMC0_D5	X_EMMC0_D3
GND33A_HSRT_USB0	X_EMMC0_CMD
X_USB0_DP	
	X_ADC_XAIN[7]
X_ADC_XAIN[4]	X_ADC_XAIN[5]
X_ADC_XAIN[3]	
X_ADC_XAIN[1]	X_ADC_XVRB
GND33A_ADC	X_ADC_XAIN[0]
GND	
X_LC_DATA[21]	X_LC_DATA[17]
X_LC_DATA[14]	X_LC_DATA[15]
X_LC_DATA[13]	
X_LC_DATA[11]	X_LC_DATA[10]
X_LC_DATA[7]	X_LC_DATA[8]
X_SYS_XTAL_IO	X_LC_DATA[6]
X_SYS_XTAL_IN	GND
A C	**A D**

3.2. GPIO Multiplex Function

The following table provides a description of the V8133L GPIO multiplex function.

Table 3-2. GPIO Multiplex Function

PAD	Mode0	Mode1	Mode2	Mode3	Mode4	Mode5	Mode6	Mode7	ModeX
X_SPI_CS_N	SPI_CS_N								
X_SPI_CLK	SPI_CLK								
X_SPI_DO	SPI_DO								
X_SPI_DI	SPI_DI								
X_SPI_WP_N	SPI_WP_N								
X_SPI_HOLD_N	SPI_HOLD_N								
X_EMMC0_D7	SD_DAT7								
X_EMMC0_D6	SD_DAT6								
X_EMMC0_D5	SD_DAT5								
X_EMMC0_D4	SD_DAT4								
X_EMMC0_D3	SD_DAT3								
X_EMMC0_D2	SD_DAT2								
X_EMMC0_D1	SD_DAT1								
X_EMMC0_D0	SD_DAT0								
X_EMMC0_RSTN	SD_RSTn								
X_EMMC0_CMD	SD_CMD								
X_EMMC0_CLK	SD_CLK								
GNDK	GNDK								
VCC11K	VCC11K								
X_OSC_IN	X_OSC_IN								
X_OSC_IO	X_OSC_IO								
GNDIO_RTC	GNDIO_RTC								
VCC3IO_RTC	VCC3IO_RTC								
X_OSCRTC_IN	X_OSCRTC_IN								
X_OSCRTC_IO	X_OSCRTC_IO								
X_RESET_N	X_RESET_N								
X_PSW_0	X_PSW_0								
X_PSW_DDRCK	X_PSW_DDRCK								

PAD	Mode0	Mode1	Mode2	Mode3	Mode4	Mode5	Mode6	Mode7	ModeX
X_OM	X_OM								
X_USB0_DRVBUS	USB0_DRVBUS								
X_USB0_VBUS	USB0_VBUS								
X_USB1_DRVBUS	USB1_DRVBUS								
X_USB1_VBUS	USB1_VBUS								
X_USB2_DRVBUS	USB1_DRVBUS								
X_USB2_VBUS	USB1_VBUS								
X_JTAG_TRST_N	JTAG_TRST_N								
X_JTAG_TDI	JTAG_TDI								
X_JTAG_SWDITMS	JTAG_SWDITMS								
X_JTAG_SWCLKTCK	JTAG_SWCLKTCK								
X_JTAG_TDO	JTAG_TDO								
X_I2C0_CLK	I2C0_CLK								
X_I2C0_DATA	I2C0_DATA								
X_I2C1_CLK	I2C1_CLK								
X_I2C1_DATA	I2C1_DATA								
X_I2C2_CLK	I2C2_CLK								
X_I2C2_DATA	I2C2_DATA								
X_I2C3_CLK	I2C3_CLK								
X_I2C3_DATA	I2C3_DATA								
X_HSPI_CLK	HSPI_CLK								
X_HSPI_CS	HSPI_CS								
X_HSPI_DI	HSPI_DI								
X_HSPI_DO	HSPI_DO								
X_SPI0_CLK	SPI0_CLK								
X_SPI0_CS	SPI0_CS								
X_SPI0_DI	SPI0_DI	SPI0_DO							
X_SPI0_DO	SPI0_DO	SPI0_DI							
X_SPI1_CLK	SPI1_CLK								
X_SPI1_CS	SPI1_CS								
X_SPI1_DI	SPI1_DI	SPI1_DO							
X_SPI1_DO	SPI1_DO	SPI1_DI							
X_SPI2_CLK	SPI2_CLK								
X_SPI2_CS	SPI2_CS								

PAD	Mode0	Mode1	Mode2	Mode3	Mode4	Mode5	Mode6	Mode7	ModeX
X_SPI2_DI	SPI2_DI	SPI2_DO							
X_SPI2_DO	SPI2_DO	SPI2_DI							
X_SPI3_CLK	SPI3_CLK								
X_SPI3_CS	SPI3_CS								
X_SPI3_DI	SPI3_DI	SPI3_DO							
X_SPI3_DO	SPI3_DO	SPI3_DI							
X_SPI4_CLK	SPI4_CLK								
X_SPI4_CS	SPI4_CS								
X_SPI4_DI	SPI4_DI	SPI4_DO							
X_SPI4_DO	SPI4_DO	SPI4_DI							
X_SPI5_CLK	SPI5_CLK								
X_SPI5_CS	SPI5_CS								
X_SPI5_DI	SPI5_DI	SPI5_DO							
X_SPI5_DO	SPI5_DO	SPI5_DI							
X_SPI6_CLK	SPI6_CLK								
X_SPI6_CS	SPI6_CS								
X_SPI6_DI	SPI6_DI	SPI6_DO							
X_SPI6_DO	SPI6_DO	SPI6_DI							
X_SPI7_CLK	SPI7_CLK								
X_SPI7_CS	SPI7_CS								
X_SPI7_DI	SPI7_DI	SPI7_DO							
X_SPI7_DO	SPI7_DO	SPI7_DI							
X_UART0_TX	UART0_SOUT								
X_UART0_RX	UART0_SIN								
X_UART1_TX	UART1_SOUT								
X_UART1_RX	UART1_SIN								
X_UART2_TX	UART2_SOUT								
X_UART2_RX	UART2_SIN								
X_UART2_NRTS	UART2_NRTS								GPIO0_19
X_UART2_NCTS	UART2_NCTS								GPIO0_20
X_UART3_TX	UART3_SOUT								
X_UART3_RX	UART3_SIN								

PAD	Mode0	Mode1	Mode2	Mode3	Mode4	Mode5	Mode6	Mode7	ModeX
X_UART3_NRTS	UART3_NRTS								
X_UART3_NCTS	UART3_NCTS								
X_UART4_TX	UART4_SOUT								
X_UART4_RX	UART4_SIN								
X_I2S0_FS	I2S0_FS	I2S0_FS	GPIO1_11	I2S0_FS	I2S0_FS	PWM_1	X_CODEX_0	I2S0_FS	GPIO0_25
X_I2S0_RXD	I2S0_RXD	I2S0_RXD	GPIO1_12	I2S0_RXD	I2S0_RXD	PWM_2	X_CODEX_1	I2S0_RXD	GPIO0_22
X_I2S0_SCLK	I2S0_SCLK	I2S0_SCLK	GPIO1_13	I2S0_SCLK	I2S0_SCLK	PWM_3	X_CODEX_2	I2S0_SCLK	GPIO0_23
X_I2S0_TXD	I2S0_TXD	I2S0_TXD	GPIO1_14	I2S0_TXD	I2S0_TXD	PWM_4	X_CODEX_3	I2S0_TXD	GPIO0_18
X_UART5_TX	UART5_irda_TX	UART5_irda_TX	CAN0_TX	GPIO0_0	UART5_irda_TX	UART5_irda_TX	X_CODEY_0	UART5_irda_TX	GPIO0_2
X_UART5_RX	UART5_irda_RX_I	UART5_irda_RX_I	CAN0_RX	GPIO0_1	UART5_irda_RX_I	UART5_irda_RX_I	X_CODEY_1	UART5_irda_RX_I	GPIO0_3
X_UART5_RX_h	UART5_irda_RX_h	UART5_irda_RX_h	PWM_1	GPIO0_2	UART5_irda_RX_h	UART5_irda_RX_h	X_CODEY_2	UART5_irda_RX_h	
X_UART6_TX	UART6_irda_TX	UART6_irda_TX	UART6_irda_TX	GPIO0_3	UART6_irda_TX	UART6_irda_TX	X_CODEY_3	UART6_irda_TX	
X_UART6_RX	UART6_irda_RX_I	UART6_irda_RX_I	UART6_irda_RX_I	GPIO0_4	UART6_irda_RX_I	UART6_irda_RX_I	X_CODEY_4	UART6_irda_RX_I	
X_UART9_TX	UART9_irda_TX	UART9_irda_TX	UART9_irda_TX	GPIO0_5	UART9_irda_TX	UART9_irda_TX	X_CODEY_5	UART9_irda_TX	
X_UART7_TX	UART7_irda_TX	UART7_irda_TX	UART7_irda_TX	GPIO0_6	UART7_irda_TX	UART7_irda_TX	X_CODEY_6	UART7_irda_TX	GPIO0_29
X_UART7_RX	UART7_irda_RX_I	UART7_irda_RX_I	UART7_irda_RX_I	GPIO0_7	UART7_irda_RX_I	UART7_irda_RX_I	X_CODEY_7	UART7_irda_RX_I	GPIO0_30
X_UART9_RX	UART9_irda_RX	UART9_irda_RX	UART9_	GPIO0_	UART9_	UART9	GPIO1_	UART9	

PAD	Mode0	Mode1	Mode2	Mode3	Mode4	Mode5	Mode6	Mode7	ModeX
			irda_RX	8	irda_RX	_irda_RX	11	_irda_RX	
X_UART8_TX	UART8_irda_TX	UART8_irda_TX	CAN1_TX	GPIO0_9	UART8_irda_TX	UART8_irda_TX	GPIO1_12	UART8_irda_TX	UART8_TX
X_UART8_RX	UART8_irda_RX_I	UART8_irda_RX_I	CAN1_RX	GPIO0_10	UART8_irda_RX_I	UART8_irda_RX_I	GPIO1_13	UART8_irda_RX_I	UART8_RX
X_UART8_RX_h	UART8_irda_RX_h	UART8_irda_RX_h	PWM_2	GPIO0_11	UART8_irda_RX_h	UART8_irda_RX_h	GPIO1_14	UART8_irda_RX_h	
X_RGMII_RX_CK	RGMII0_RX_CK	X_CODEX_0	X_CODEX_0	X_CODEX_0	X_CODEX_0	GPIO1_15	RGMII0_RX_CK	GPIO1_30	SPI6_MISO
X_RGMII_RXD[0]	RGMII0_RXD[0]	X_CODEX_1	X_CODEX_1	X_CODEX_1	X_CODEX_1	GPIO1_16	RGMII0_RXD[0]	GPIO1_31	UART9_RX
X_RGMII_RXD[1]	RGMII0_RXD[1]	X_CODEX_2	X_CODEX_2	X_CODEX_2	X_CODEX_2	GPIO1_17	RGMII0_RXD[1]	GPIO1_17	UART9_TX
X_RGMII_RXD[2]	RGMII0_RXD[2]	X_CODEX_3	X_CODEX_3	X_CODEX_3	X_CODEX_3	GPIO1_18	RGMII0_RXD[2]	GPIO1_18	
X_RGMII_RXD[3]	RGMII0_RXD[3]	X_CODEX_4	X_CODEX_4	X_CODEX_4	X_CODEX_4	GPIO1_19	RGMII0_RXD[3]	GPIO1_19	
X_RGMII_RXCTL	RGMII0_RXCTL	X_CODEX_5	X_CODEX_5	X_CODEX_5	X_CODEX_5	GPIO1_20	RGMII0_RXCTL	GPIO1_20	UART6_TX
X_RGMII_GTX_CK	RGMII0_GTX_CK	X_CODEX_6	X_CODEX_6	X_CODEX_6	X_CODEX_6	GPIO1_21	RGMII0_GTX_CK	GPIO1_21	
X_RGMII_TXCTL	RGMII0_TXCTL	X_CODEX_7	X_CODEX_7	X_CODEX_7	X_CODEX_7	GPIO1_22	RGMII0_TXCTL	GPIO1_22	
X_RGMII_TXD[0]	RGMII0_TXD[0]	GPIO1_19	GPIO1_19	PWM_2	GPIO1_19	PWM_2	RGMII0_TXD[0]	GPIO1_19	SPI6_MOSI
X_RGMII_TXD[1]	RGMII0_TXD[1]	GPIO1_20	GPIO1_	PWM_3	GPIO1_	PWM_3	RGMII0	PWM_	SPI6_

PAD	Mode0	Mode1	Mode2	Mode3	Mode4	Mode5	Mode6	Mode7	ModeX
			20		20		_TXD[1]	3	CLK
X_RGMII_TXD[2]	RGMII0_TXD[2]	GPIO1_21	GPIO1_21	PWM_4	GPIO1_21	PWM_4	RGMII0_TXD[2]	PWM_4	SPI6_CS
X_RGMII_TXD[3]	RGMII0_TXD[3]	GPIO1_22	GPIO1_22	PWM_5	GPIO1_22	PWM_5	RGMII0_TXD[3]	PWM_5	SPI6_CS2
X_RGMII_MDC	RGMII0_MDC	GPIO1_23	GPIO1_23	PWM_6	GPIO1_23	PWM_6	RGMII0_MDC	PWM_6	UART6_RX
X_RGMII_MDIO	RGMII0_MDIO	GPIO1_24	GPIO1_24	PWM_7	GPIO1_24	PWM_7	RGMII0_MDIO	PWM_7	
X_RMII_TXD[0]	RMII0_TXD[0]	RMII0_TXD[0]	X_CODEY_0	CAN0_TX	RMII0_TXD[0]	PWM_8	RMII0_TXD[0]	GPIO1_05	
X_RMII_TXD[1]	RMII0_TXD[1]	RMII0_TXD[1]	X_CODEY_1	CAN0_RX	RMII0_TXD[1]	PWM_9	RMII0_TXD[1]	GPIO1_06	
X_RMII_TX_EN	RMII0_TX_EN	RMII0_TX_EN	X_CODEY_2	CAN1_TX	RMII0_TX_EN	PWM_10	RMII0_TX_EN	GPIO1_07	
X_RMII_RX_CRSDV	RMII0_RX_CRS_DV	RMII0_RX_CRS_DV	X_CODEY_3	CAN1_RX	RMII0_RX_CRS_DV	PWM_11	RMII0_RX_CRS_DV	GPIO1_08	
X_RMII_RX_ER	RMII0_RX_ER	RMII0_RX_ER	X_CODEY_4	PWM_12	RMII0_RX_ER	PWM_12	RMII0_RX_ER	GPIO1_09	
X_RMII_RXD[0]	RMII0_RXD[0]	RMII0_RXD[0]	X_CODEY_5	PWM_13	RMII0_RXD[0]	PWM_13	RMII0_RXD[0]	GPIO1_10	
X_RMII_RXD[1]	RMII0_RXD[1]	RMII0_RXD[1]	X_CODEY_6	GPIO1_11	RMII0_RXD[1]	GPIO1_11	RMII0_RXD[1]	GPIO1_11	GPIO0_26
X_RMII_REF_CLK	RMII0_REF_CLK	RMII0_REF_CLK	X_CODEY_7	GPIO1_12	RMII0_REF_CLK	GPIO1_12	RMII0_REF_CLK	GPIO1_12	
X_RMII_MDC	RMII0_MDC	RMII0_MDC	GPIO1_25	GPIO1_13	RMII0_MDC	GPIO1_13	RMII0_MDC	GPIO1_13	
X_RMII_MDIO	RMII0_MDIO	RMII0_MDIO	PWM_2	GPIO1_14	RMII0_MDIO	GPIO1_14	RMII0_MDIO	GPIO1_14	
X_MII_TXD[0]	MII_TXD[0]	X_CODEY_0	MII_TXD[0]	X_CODEY_0	X_CODEY_0	MII_TXD[0]	MII_TXD[0]	GPIO1_23	
X_MII_TXD[1]	MII_TXD[1]	X_CODEY_1	MII_TX	X_COD	X_COD	MII_TX	MII_TX	GPIO1	

PAD	Mode0	Mode1	Mode2	Mode3	Mode4	Mode5	Mode6	Mode7	ModeX
			D[1]	EY_1	EY_1	D[1]	D[1]	_24	
X_MII_TX_EN	MII_TX_EN	X_CODEY_2	MII_TX_EN	X_CODEY_2	X_CODEY_2	MII_TX_EN	MII_TX_EN	GPIO1_25	GPIO0_24
X_MII_RX_DV	MII_RX_CRS_DV	X_CODEY_3	MII_RX_CRS_DV	X_CODEY_3	X_CODEY_3	MII_RX_CRS_DV	MII_RX_CRS_DV	GPIO1_26	
X_MII_RX_ER	MII_RX_ER	X_CODEY_4	MII_RX_ER	X_CODEY_4	X_CODEY_4	MII_RX_ER	MII_RX_ER	GPIO1_27	
X_MII_RXD[0]	MII_RXD[0]	X_CODEY_5	MII_RXD[0]	X_CODEY_5	X_CODEY_5	MII_RXD[0]	MII_RXD[0]	GPIO1_28	
X_MII_RXD[1]	MII_RXD[1]	X_CODEY_6	MII_RXD[1]	X_CODEY_6	X_CODEY_6	MII_RXD[1]	MII_RXD[1]	GPIO1_29	
X_MII_MDC	MII_MDC	GPIO1_25	MII_MDC	GPIO1_25	PWM_2	MII_MDC	MII_MDC	GPIO0_31	
X_MII_MDIO	MII_MDIO	GPIO1_26	MII_MDIO	GPIO1_26	PWM_3	MII_MDIO	MII_MDIO	GPIO1_0	
X_MII_RX_CK	MII_RX_CK	GPIO0_09	MII_RX_CK	GPIO0_09	GPIO0_09	MII_RX_CK	MII_RX_CK	GPIO1_1	
X_MII_RXD[2]	MII_RXD[2]	GPIO0_10	MII_RXD[2]	GPIO0_10	GPIO0_10	MII_RXD[2]	MII_RXD[2]	GPIO1_2	
X_MII_RXD[3]	MII_RXD[3]	GPIO0_11	MII_RXD[3]	GPIO0_11	GPIO0_11	MII_RXD[3]	MII_RXD[3]	GPIO1_3	
X_MII_TX_CK	MII_TX_CK	GPIO0_12	MII_TX_CK	GPIO0_12	GPIO0_12	MII_TX_CK	MII_TX_CK	GPIO1_4	
X_MII_TX_ER	MII_TX_ER	GPIO0_13	MII_TX_ER	GPIO0_13	GPIO0_13	MII_TX_ER	MII_TX_ER	GPIO1_15	
X_MII_TXD[2]	MII_TXD[2]	GPIO0_14	MII_TXD[2]	GPIO0_14	GPIO0_14	MII_TXD[2]	MII_TXD[2]	GPIO1_16	
X_MII_TXD[3]	MII_TXD[3]	GPIO0_15	MII_TXD[3]	GPIO0_15	GPIO0_15	MII_TXD[3]	MII_TXD[3]	GPIO1_17	
X_MII_CRS	MII_CRS	GPIO0_16	MII_CRS	GPIO0_16	GPIO0_16	MII_CRS	MII_CRS	GPIO1_18	
X_MII_COL	MII_COL	GPIO0_17	MII_COL	GPIO0_17	GPIO0_17	MII_COL	MII_COL	GPIO1_19	
X_EMMC1_D7	SD1_DAT7	GPIO1_0	I2S1_FS	GPIO1_0	GPIO1_0	GPIO1_0	SD1_DAT7	GPIO1_0	
X_EMMC1_D6	SD1_DAT6	GPIO1_1	I2S1_R	GPIO1_	GPIO1_	GPIO1_	SD1_D	GPIO1	

PAD	Mode0	Mode1	Mode2	Mode3	Mode4	Mode5	Mode6	Mode7	ModeX
			XD	1	1	1	AT6	_1	
X_EMMC1_D5	SD1_DAT5	GPIO1_2	I2S1_SCLK	GPIO1_2	GPIO1_2	GPIO1_2	SD1_DAT5	GPIO1_2	
X_EMMC1_D4	SD1_DAT4	GPIO1_3	I2S1_TXD	GPIO1_3	GPIO1_3	GPIO1_3	SD1_DAT4	GPIO1_3	
X_EMMC1_D3	SD1_DAT3	GPIO1_4	I2C4_CLK	GPIO1_4	GPIO1_4	GPIO1_4	SD1_DAT3	GPIO1_4	
X_EMMC1_D2	SD1_DAT2	GPIO1_5	I2C4_DATA	GPIO1_5	GPIO1_5	GPIO1_5	SD1_DAT2	GPIO1_5	
X_EMMC1_D1	SD1_DAT1	GPIO1_6	UART4_NRTS	GPIO1_6	GPIO1_6	GPIO1_6	SD1_DAT1	GPIO1_6	
X_EMMC1_D0	SD1_DAT0	GPIO1_7	UART4_NCTS	GPIO1_7	GPIO1_7	GPIO1_7	SD1_DAT0	GPIO1_7	
X_EMMC1_RSTN	SD1_RSTn	GPIO1_8	SPI6_CS2	GPIO1_8	GPIO1_8	GPIO1_8	SD1_RSTn	GPIO1_8	
X_EMMC1_CMD	SD1_CMD	GPIO1_9	SPI6_CS3	GPIO1_9	GPIO1_9	GPIO1_9	SD1_CMD	GPIO1_9	
X_EMMC1_CLK	SD1_CLK	GPIO1_10	PWM_3	GPIO1_10	GPIO1_10	GPIO1_10	SD1_CLK	GPIO1_10	
X_LC_PCLK	LC_PCLK	LC_PCLK	CAN0_TX	LC_PCLK	LC_PCLK	GPIO0_0	LC_PCLK	GPIO0_0	
X_LC_VS	LC_VS	LC_VS	CAN0_RX	LC_VS	LC_VS	GPIO0_1	LC_VS	GPIO0_1	
X_LC_HS	LC_HS	LC_HS	CAN1_TX	LC_HS	LC_HS	GPIO0_2	LC_HS	GPIO0_2	
X_LC_DE	LC_DE	LC_DE	CAN1_RX	LC_DE	LC_DE	GPIO0_3	LC_DE	GPIO0_3	
X_LC_DATA[0]	LC_DATA[0]	LC_DATA[0]	PWM_0	LC_DATA[0]	LC_DATA[0]	GPIO0_4	LC_DATA[0]	GPIO0_4	
X_LC_DATA[1]	LC_DATA[1]	LC_DATA[1]	PWM_1	LC_DATA[1]	LC_DATA[1]	GPIO0_5	LC_DATA[1]	GPIO0_5	
X_LC_DATA[2]	LC_DATA[2]	LC_DATA[2]	PWM_2	LC_DATA[2]	LC_DATA[2]	GPIO0_6	LC_DATA[2]	GPIO0_6	
X_LC_DATA[3]	LC_DATA[3]	LC_DATA[3]	PWM_3	LC_DATA[3]	LC_DATA[3]	GPIO0_7	LC_DATA[3]	GPIO0_7	
X_LC_DATA[4]	LC_DATA[4]	LC_DATA[4]	I2S1_FS	LC_DATA[4]	LC_DATA[4]	GPIO0_8	LC_DATA[4]	GPIO0_8	

PAD	Mode0	Mode1	Mode2	Mode3	Mode4	Mode5	Mode6	Mode7	ModeX
X_LC_DATA[5]	LC_DATA[5]	LC_DATA[5]	I2S1_RXD	LC_DATA[5]	LC_DATA[5]	GPIO0_9	LC_DATA[5]	GPIO0_9	GPIO0_21
X_LC_DATA[6]	LC_DATA[6]	LC_DATA[6]	I2S1_SCLK	LC_DATA[6]	LC_DATA[6]	GPIO0_10	LC_DATA[6]	GPIO0_10	GPIO0_17
X_LC_DATA[7]	LC_DATA[7]	LC_DATA[7]	I2S1_TXD	LC_DATA[7]	LC_DATA[7]	GPIO0_11	LC_DATA[7]	GPIO0_11	
X_LC_DATA[8]	LC_DATA[8]	LC_DATA[8]	I2C4_CLK	LC_DATA[8]	LC_DATA[8]	GPIO0_12	LC_DATA[8]	GPIO0_12	
X_LC_DATA[9]	LC_DATA[9]	LC_DATA[9]	I2C4_DATA	LC_DATA[9]	LC_DATA[9]	GPIO0_13	LC_DATA[9]	GPIO0_13	
X_LC_DATA[10]	LC_DATA[10]	LC_DATA[10]	UART4_NRTS	LC_DATA[10]	LC_DATA[10]	GPIO0_14	LC_DATA[10]	GPIO0_14	
X_LC_DATA[11]	LC_DATA[11]	LC_DATA[11]	UART4_NCTS	LC_DATA[11]	LC_DATA[11]	GPIO0_15	LC_DATA[11]	GPIO0_15	
X_LC_DATA[12]	LC_DATA[12]	LC_DATA[12]	SPI0_CS2	LC_DATA[12]	LC_DATA[12]	GPIO0_16	LC_DATA[12]	GPIO0_16	
X_LC_DATA[13]	LC_DATA[13]	LC_DATA[13]	SPI0_CS3	LC_DATA[13]	LC_DATA[13]	GPIO0_17	LC_DATA[13]	GPIO0_17	
X_LC_DATA[14]	LC_DATA[14]	LC_DATA[14]	SPI1_CS2	LC_DATA[14]	LC_DATA[14]	GPIO0_18	LC_DATA[14]	GPIO0_18	
X_LC_DATA[15]	LC_DATA[15]	LC_DATA[15]	SPI1_CS3	LC_DATA[15]	LC_DATA[15]	GPIO0_19	LC_DATA[15]	GPIO0_19	
X_LC_DATA[16]	LC_DATA[16]	LC_DATA[16]	SPI2_CS2	LC_DATA[16]	LC_DATA[16]	GPIO0_20	LC_DATA[16]	GPIO0_20	
X_LC_DATA[17]	LC_DATA[17]	LC_DATA[17]	SPI2_CS3	LC_DATA[17]	LC_DATA[17]	GPIO0_21	LC_DATA[17]	GPIO0_21	
X_LC_DATA[18]	LC_DATA[18]	LC_DATA[18]	SPI3_CS2	LC_DATA[18]	LC_DATA[18]	GPIO0_22	LC_DATA[18]	GPIO0_22	
X_LC_DATA[19]	LC_DATA[19]	LC_DATA[19]	SPI3_CS3	LC_DATA[19]	LC_DATA[19]	GPIO0_23	LC_DATA[19]	GPIO0_23	
X_LC_DATA[20]	LC_DATA[20]	LC_DATA[20]	SPI4_CS2	LC_DATA[20]	LC_DATA[20]	GPIO0_24	LC_DATA[20]	GPIO0_24	
X_LC_DATA[21]	LC_DATA[21]	LC_DATA[21]	SPI4_CS3	LC_DATA[21]	LC_DATA[21]	GPIO0_25	LC_DATA[21]	GPIO0_25	
X_LC_DATA[22]	LC_DATA[22]	LC_DATA[22]	SPI5_CS2	LC_DATA[22]	LC_DATA[22]	GPIO0_26	LC_DATA[22]	GPIO0_26	
X_LC_DATA[23]	LC_DATA[23]	LC_DATA[23]	SPI5_C	LC_DAT	LC_DAT	GPIO0_	LC_DAT	GPIO0	

PAD	Mode0	Mode1	Mode2	Mode3	Mode4	Mode5	Mode6	Mode7	ModeX
			S3	A[23]	A[23]	27	A[23]	_27	
X_I2S_MCLK	I2S_MCLK	I2S_MCLK	GPIO0_28	I2S_MCLK	I2S_MCLK	I2S_MCLK	GPIO0_28	GPIO0_28	
X_SPI_DCX1	GPIO0_29	SPI0_DCX	SPI2_DCX	SPI4_DCX	SPI6_DCX	GPIO0_29	GPIO0_29	GPIO0_29	
X_SPI_DCX2	GPIO0_30	SPI1_DCX	SPI3_DCX	SPI5_DCX	GPIO0_30	GPIO0_30	GPIO0_30	GPIO0_30	

The RGB output can be multiplexed to BT656 output, so the pin correspondence between LCD0 and BT656 is as follows.

Pin Name	LCD Pin	BT656 Pin
PD3	LCD0_D3	VD0
PD4	LCD0_D4	VD1
PD5	LCD0_D5	VD2
PD6	LCD0_D6	VD3
PD7	LCD0_D7	VD4
PD10	LCD0_D10	VD5
PD11	LCD0_D11	VD6
PD12	LCD0_D12	VD7

Note: Please never switch pin-mux mode for different pad to the same GPIO bit, or same functional pin.

3.3. PWM timer output signals

The PWM timer output signals can be mapped to V8133L dedicated instance by the table list as below.

	FTTMR010 instance	Timer Output Signal
PWM_0	u_FTPWMTMR010	tmr1_out
PWM_1	u_FTPWMTMR010	tmr2_out
PWM_2	u_FTPWMTMR010	tmr3_out
PWM_3	u_FTPWMTMR010	tmr4_out
PWM_4	u_FTPWMTMR010_u1	tmr1_out
PWM_5	u_FTPWMTMR010_u1	tmr2_out

PWM_6	u_FTPWMTMR010_u1	tmr3_out
PWM_7	u_FTPWMTMR010_u1	tmr4_out
PWM_8	u_FTPWMTMR010_u2	tmr1_out
PWM_9	u_FTPWMTMR010_u2	tmr2_out
PWM_10	u_FTPWMTMR010_u2	tmr3_out
PWM_11	u_FTPWMTMR010_u2	tmr4_out
PWM_12	u_FTPWMTMR010_u3	tmr1_out
PWM_13	u_FTPWMTMR010_u3	tmr2_out

3.4. Signal Descriptions

V8133L contains many peripheral interfaces. Many of the interfaces can multiplex up to eight functions. Pin-multiplexing configuration can refer to Table 3-1 and Table 3-2. Table 3-3 shows the detailed function description of every signal based on the different interface.

Table 3-3. Signal Descriptions

Pad Name	Description
SPIF	
X_SPI_CLK	SPI Clock Signal
X_SPI_CS_N	SPI Chip Select Signal (active low)
X_SPI_DI	SPI Master Data In, Slave Data Out
X_SPI_DO	SPI Master Data Out, Slave Data In
X_SPI_HOLD_N	SPI Data In/Out
X_SPI_WP_N	SPI Data In/Out
EMMC0	
X_EMMC0_CLK	EMMC Clock Signal
X_EMMC0_CMD	EMMC Command Line
X_EMMC0_RSTN	EMMC Reset signal
X_EMMC0_DATA[7:0]	EMMC Data
RTC	
X_RTC_XTAL_IN	RTC XTAL In
X_RTC_XTAL_IO	RTC XTAL OUT

Pad Name	Description
AON	
X_SYS_XTAL_IN	System XTAL In
X_SYS_XTAL_IO	System XTAL Out
X_RESET_N	Reset Signal
X_PSW_0	Power Swith Signal
X_PSW_DDRCK	Power Swith For DDR
X_OM	Entering Test Mode Signal
USB	
X_USB0_DRVBUS	USB0 Drive Vbus
X_USB0_VBUS	USB0 Voltage Bus
X_USB1_DRVBUS	USB1 Drive Vbus
X_USB1_VBUS	USB1 Voltage Bus
X_USB2_DRVBUS	USB2 Drive Vbus
X_USB2_VBUS	USB2 Voltage Bus
JTAG	
X_JTAG_TRST_N	JTAG Reset Signal
X_JTAG_TDI	JTAG Data Input
X_JTAG_SWDITMS	JTAG Mode Select Input
X_JTAG_TDO	JTAG Data Output
X_JTAG_SWCLKTCK	JTAG Clock Input
I2C	
X_I2C0_SCL	Serial Clock Line
X_I2C0_SDA	Serial Data Line
X_I2C1_SCL	Serial Clock Line
X_I2C1_SDA	Serial Data Line
X_I2C2_SCL	Serial Clock Line
X_I2C2_SDA	Serial Data Line
X_I2C3_SCL	Serial Clock Line
X_I2C3_SDA	Serial Data Line

Pad Name	Description
SPI2AHB	
X_HSPI_CLK	HSPI Clock Signal
X_HSPI_CS	HSPI Chip Select Signal
X_HSPI_DI	HSPI Data In
X_HSPI_DO	HSPI Data Out
SSP(SPI)	
X_SPI0_CLK	SPI Clock Signal
X_SPI0_CS	SPI Chip Select Signal (active low)
X_SPI0_DI	SPI Master Data In, Slave Data Out
X_SPI0_DO	SPI Master Data Out, Slave Data In
X_SPI1_CLK	SPI Clock Signal
X_SPI1_CS	SPI Chip Select Signal (active low)
X_SPI1_DI	SPI Master Data In, Slave Data Out
X_SPI1_DO	SPI Master Data Out, Slave Data In
X_SPI2_CLK	SPI Clock Signal
X_SPI2_CS	SPI Chip Select Signal (active low)
X_SPI2_DI	SPI Master Data In, Slave Data Out
X_SPI2_DO	SPI Master Data Out, Slave Data In
X_SPI3_CLK	SPI Clock Signal
X_SPI3_CS	SPI Chip Select Signal (active low)
X_SPI3_DI	SPI Master Data In, Slave Data Out
X_SPI3_DO	SPI Master Data Out, Slave Data In
X_SPI4_CLK	SPI Clock Signal
X_SPI4_CS	SPI Chip Select Signal (active low)
X_SPI4_DI	SPI Master Data In, Slave Data Out
X_SPI4_DO	SPI Master Data Out, Slave Data In
X_SPI5_CLK	SPI Clock Signal
X_SPI5_CS	SPI Chip Select Signal (active low)
X_SPI5_DI	SPI Master Data In, Slave Data Out

Pad Name	Description
X_SPI5_DO	SPI Master Data Out, Slave Data In
X_SPI6_CLK	SPI Clock Signal
X_SPI6_CS	SPI Chip Select Signal (active low)
X_SPI6_DI	SPI Master Data In, Slave Data Out
X_SPI6_DO	SPI Master Data Out, Slave Data In
SPI (ESAM)	
X_SPI7_CLK	SPI Clock Signal
X_SPI7_CS	SPI Chip Select Signal (active low)
X_SPI7_DI	SPI Master Data In, Slave Data Out
X_SPI7_DO	SPI Master Data Out, Slave Data In
SSP (I2S)	
X_I2S0_FS	I2S Frame/Sync.
X_I2S0_RXD	I2S Data Input
X_I2S0_SCLK	I2S Bit Clock
X_I2S0_TXD	I2S Data Output
X_I2S1_FS	I2S Frame/Sync
X_I2S1_RXD	I2S Data Input
X_I2S1_SCLK	I2S Bit Clock
X_I2S1_TXD	I2S Data Output
UART	
X_UART0_TX	UART Data Transmit
X_UART0_RX	UART Data Receive
X_UART1_TX	UART Data Transmit
X_UART1_RX	UART Data Receive
X_UART2_TX	UART Data Transmit
X_UART2_RX	UART Data Receive
X_UART2_NRTS	UART Data Request to Send
X_UART2_NCTS	UART Data Clear to Send
X_UART3_TX	UART Data Transmit

Pad Name	Description
X_UART3_RX	UART Data Receive
X_UART3_NRTS	UART Data Request to Send
X_UART3_NCTS	UART Data Clear to Send
X_UART4_TX	UART Data Transmit
X_UART4_RX	UART Data Receive
X_UART6_TX	UART Data Transmit
X_UART6_RX	UART Data Receive
X_UART7_TX	UART Data Transmit
X_UART7_RX	UART Data Receive
X_UART9_TX	UART Data Transmit
X_UART9_RX	UART Data Receive
IrDA	
X_UART5_TX	UART IR Data Transmit
X_UART5_RX	UART IR Data Receive
X_UART5_RX_h	Infrared Receive For FIR
X_UART8_TX	UART IR Data Transmit
X_UART8_RX	UART IR Data Receive
X_UART8_RX_h	Infrared Receive For FIR
RGMII	
X_RGMII_RX_CK	RGMII receive clock
X_RGMII_RXD[3:0]	Receive data
X_RGMII_RXCTL	Control signal for transferring other RX signals from RGMII
X_RGMII_GTX_CK	RGMII transmit clock
X_RGMII_TXCTL	Control signal for transferring other TX signals from RGMII
X_RGMII_TXD[3:0]	RGMII Transmit data
X_RGMII_MDC	Clock of PHY management
X_RGMII_MDIO	Data input/output of PHY management
RMII	
X_RMII_TXD[1:0]	RMII Transmit data

Pad Name	Description
X_RMII_TX_EN	Transmit enable
X_RMII_RX_CRSDV	Receive carrier sense/data valid
X_RMII_RX_ER	Receive error
X_RMII_RXD[1:0]	Receive data
X_RMII_REF_CLK	RMII 50-MHz REF_CLK
X_RMII_MDC	Clock of PHY management
X_RMII_MDIO	Data input/output of PHY management
MII	
X_MII_TXD[3:0]	MII Transmit data
X_MII_TX_EN	MII Transmit enable
X_MII_RX_DV	Receive data valid
X_MII_RX_ER	Receive error
X_MII_RXD[3:0]	MII Receive data
X_MII_MDC	Clock of PHY management
X_MII_MDIO	Data input/output of PHY management
X_MII_RX_CK	MII receive clock
X_MII_TX_CK	MII transmit clock
X_MII_TX_ER	Transmit error
X_MII_CRS	Carrier sense
X_MII_COL	Collision detect
EMMC1	
X_EMMC1_CLK	EMMC1 Clock Signal
X_EMMC1_CMD	EMMC1 Command Line
X_EMMC1_RSTN	EMMC1 Reset Signal
X_EMMC1_DATA[7:0]	EMMC1 Data
LCDC	
X_LC_PCLK	Pixel clock of panel
X_LC_VS	Vertical synchronization signal of panel
X_LC_HS	Horizontal synchronization signal of panel

Pad Name	Description
X_LC_DE	Data enable signal of panel
X_LC_DATA[23:0]	Pixel data of panel DATA
MISC	
X_I2S_MCLK	I2S Clock Signal
X_SPI_DCX1	SPI Data Command Flag
X_SPI_DCX2	SPI Data Command Flag
DDR	
X_DDR_RASn	Row Address Strobe
X_DDR_ADDR[15:0]	DDR Address
X_DDR_ODT[1:0]	DDR On-Die Termination
X_DDR_BA[2:0]	DDR Bank Select Signal
X_DDR_CSn[1:0]	DDR Chip Select Signal
X_DDR_RESETN	DDR Reset Signal
X_DDR_CKE[1:0]	DDR Clock Select
X_DDR_CK	DDR Clock Output Signal
X_DDR_CKB	DDR Clock Output Signal
X_DDR_WEn	DDR Writer Enable
X_DDR_CASn	DDR Column Address Strobe
X_DDR_DM_0	DDR Data Mask 0
X_DDR_DQSB_0	DDR DQS 0 # Used In the Different DQS Mode
X_DDR_DQS_0	DDR DQS 0
X_DDR_DQ_0[7:0]	DDR DQ Data Bus 0
X_DDR_VREF_D0	DDR Reference Voltage For Receivers 0
X_DDR_DM_1	DDR Data Mask 1
X_DDR_DQSB_1	DDR DQS 1 # Used In the Different DQS Mode
X_DDR_DQS_1	DDR DQS 1
X_DDR_DQ_1[7:0]	DDR DQ Data Bus 1
X_DDR_VREF_D1	DDR Reference Voltage For Receivers 1
X_DDR_DM_2	DDR Data Mask 2

Pad Name	Description
X_DDR_DQSB_2	DDR DQS 2 # Used In the Different DQS Mode
X_DDR_DQS_2	DDR DQS 2
X_DDR_DQ_2[7:0]	DDR DQ Data Bus 2
X_DDR_VREF_D2	DDR Reference Voltage For Receivers 2
X_DDR_DM_3	DDR Data Mask 3
X_DDR_DQSB_3	DDR DQS 3 # Used In the Different DQS Mode
X_DDR_DQS_3	DDR DQS 3
X_DDR_DQ_3[7:0]	DDR DQ Data Bus 3
X_DDR_VREF_D3	DDR Reference Voltage For Receivers 3
X_DDR_DM_4	DDR Data Mask 4
X_DDR_DQSB_4	DDR DQS 4 # Used In the Different DQS Mode
X_DDR_DQS_4	DDR DQS 4
X_DDR_DQ_4[7:0]	DDR DQ Data Bus 4
X_DDR_VREF_D4	DDR Reference Voltage For Receivers 4
X_DDR_RDRVUP	Pad To The Precise External Resistor For Compensating The Pull-up Driver
X_DDR_RDRVDN	Pad To The Precise Internal Resistor For Compensating The Pull-down Driver
OTG	
X_USB0_DP	USB D- Signal
X_USB0_DM	USB D+ Signal
X_USB1_DP	USB D- Signal
X_USB1_DM	USB D+ Signal
X_USB2_DP	USB D- Signal
X_USB2_DM	USB D+ Signal
ADC	
X_ADC_XAIN0	Analog Input 0
X_ADC_XAIN1	Analog Input 1
X_ADC_XAIN2	Analog Input 2
X_ADC_XAIN3	Analog Input 3
X_ADC_XAIN4	Analog Input 4

Pad Name	Description
X_ADC_XAIN5	Analog Input 5
X_ADC_XAIN6	Analog Input 6
X_ADC_XAIN7	Analog Input 7
X_ADC_XVRT	Analog Higher/Positive Reference Voltage For ADC
X_ADC_XVRB	Analog Lower/Negative Reference Voltage For ADC

4. System

This part details the V8133L system construction from following aspects.

- Memory Mapping
- Clock
- Reset
- GPV
- DDR
- SCU
- WDT
- System Boot
- PWMTMR
- GIC
- DMAC for AXI
- DMAC for AHB
- ADC
- TDC
- eFUSE
- Port Controller
- Crypto Engine
- Secure design

5. Memory

This chapter details the V8133L external memory.

- EMC
- eMMC

6. Display

This chapter provides a detailed description of the display feature of V8133L processor from following aspects.

• LCDC

7. Audio

This section details the interfaces that provided in V8133L, mainly includes:

- I2S

8. Interface

This section details the interfaces that provided in V8133L, mainly includes:

- USB2.0
- SSP
- SPIF
- SPI2AHB
- I2C
- UART
- MAC
- GPIO
- CAN
- KBC

9. Electrical Characteristics

9.1. Absolute Maximum Ratings

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Table 9-1 specifies the absolute maximum ratings.

CAUTION

Stresses beyond those listed under Table 9-1 may affect reliability or cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under Section 9.2, *Recommended Operating Conditions*, is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Table 9-1. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
Tstg	Storage Temperature	-40	125	°C
VCC11K_RTC	Core Power Supply for RTC Domain	-0.5	1.5	V
VCC3IO_RTC	I/O Power Supply for RTC Domain	-0.5	4.6	V
VCC3IO_RTCOSC	Power Supply for RTC's Xtal Pad	-0.5	4.6	V
VCCK	Core Power Supply for System Domain	-0.5	1.5	V
VCC3IO	I/O Power Supply for System Domain	-0.5	4.6	V
VCC3IO_OSC	Power Supply for System's Xtal Pad	-0.5	4.6	V
VCC3IO_EFUSE	Power Supply for Efuse's Program	-0.5	4.6	V
VCC3IO_EMMC0	I/O Power Supply for EMMC0	-0.5	4.6	V
VCC3IO_EMMC1	I/O Power Supply for EMMC1	-0.5	4.6	V
VCC11A_DLL_0	Power Supply for DLL0	-0.5	1.5	V
VCC11A_DLL_1	Power Supply for DLL1	-0.5	1.5	V
VCC11A_PLL04	Power Supply for PLL0 and PLL4	-0.5	1.5	V
VCC11A_PLL126	Power Supply for PLL1, PLL2 and PLL6	-0.5	1.5	V

VCC11A_PLL35	Power Supply for PLL3 and PLL5		-0.5	1.5	V
VCC11K_DDR	Core Power Supply for DDR PHY		-0.5	1.5	V
VCC11A_PLL_DDR	Power Supply for DDR PHY's PLL		-0.5	1.5	V
VCC15O_DDR	I/O Power Supply for DDR PHY		-0.5	2.5	V
VCC15O_DDRCK	Power Supply for DRAM's CK Pad		-0.5	2.5	V
VCC33A_HSRT_USB0	Power Supply for USB0		-0.5	4.6	V
VCC33A_HSRT_USB1	Power Supply for USB1		-0.5	4.6	V
VCC33A_HSRT_USB2	Power Supply for USB2		-0.5	4.6	V
VCC33A_PLL_USB0	Power Supply for USB0's PLL		-0.5	4.6	V
VCC33A_PLL_USB1	Power Supply for USB1's PLL		-0.5	4.6	V
VCC33A_PLL_USB2	Power Supply for USB2's PLL		-0.5	4.6	V
VCC33A_TDC	Power Supply for TDC		-0.3	3.9	V
VCC33A_ADC	Power Supply for ADC		-0.3	3.9	V
VCC33D_ADC	Power Supply for ADC		-0.3	3.9	V
VCC33IO_ADC	Power Supply for ADC		-0.3	3.9	V
V_{ESD}	Electrostatic Discharge	Human Body Model(HBM)(1)	-4000	4000	V
		Charged Device Model(CDM)(2)	-250	250	V
$I_{Latch-up}$	Latch-up I-test performance current-pulse injection on each IO pin(3)		Pass		
	Latch-up over-voltage performance voltage injection on each IO pin(4)		Pass		

(1). Test method: JEDEC JS-001-2014(Class-3A). JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

(2). Test method: JESD22-C101F(Class-C1). JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

(3). Current test performance: Pins stressed per JEDEC JESD78D(Class I, Level A) and passed with I/O pin injection current as defined in JEDEC.

(4). Over voltage performance: Supplies stressed per JEDEC JESD78D(Class I, Level A) and passed voltage injection as defined in JEDEC.

9.2. Recommended Operating Conditions

All V8133L modules are used under the operating conditions contained in Table 9-2.

NOTE

Logic functions and parameter values are not assured out of the range specified in the recommended operating conditions.

Table 9-2. Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
Ta	Ambient Operating Temperature	-40	-	85	°C
VCC11K_RTC	Core Power Supply for RTC Domain	1.045	1.1	1.21	V
VCC3IO_RTC	I/O Power Supply for RTC Domain	3.135	3.3	3.465	V
VCC3IO_RTCOSC	Power Supply for RTC's Xtal Pad	3.135	3.3	3.465	V
VCCK	Core Power Supply for System Domain	0.99	1.1	1.21	V
VCC3IO	I/O Power Supply for System Domain	2.97	3.3	3.63	V
VCC3IO_OSC	Power Supply for System's Xtal Pad	3.135	3.3	3.465	V
VCC3IO_EFUSE	Power Supply for Efuse's Program	3.135	3.3	3.465	V
VCC3IO_EMMC0	I/O Power Supply for EMMC0	3.135	3.3	3.465	V
		1.71	1.8	1.89	
VCC3IO_EMMC1	I/O Power Supply for EMMC1	3.135	3.3	3.465	V
		1.71	1.8	1.89	
VCC11A_DLL_0	Power Supply for DLL0 and PLL7	1.045	1.1	1.21	V
VCC11A_DLL_1	Power Supply for DLL1	1.045	1.1	1.21	V
VCC11A_PLL04	Power Supply for PLL0 and PLL4	1.045	1.1	1.21	V
VCC11A_PLL126	Power Supply for PLL1, PLL2 and PLL6	1.045	1.1	1.21	V
VCC11A_PLL35	Power Supply for PLL3 and PLL5	1.045	1.1	1.21	V
VCC11K_DDR	Core Power Supply for DDR PHY	1.045	1.1	1.21	V
VCC11A_PLL_DDR	Power Supply for DDR PHY's PLL	1.045	1.1	1.21	V
VCC15O_DDR	I/O Power Supply for DDR PHY	1.425	1.5	1.575	V
VCC15O_DDRCK	Power Supply for DRAM's CK Pad	1.425	1.5	1.575	V

VCC33A_HSRT_USB0	Power Supply for USB0	3.135	3.3	3.465	V
VCC33A_HSRT_USB1	Power Supply for USB1	3.135	3.3	3.465	V
VCC33A_HSRT_USB2	Power Supply for USB2	3.135	3.3	3.465	V
VCC33A_PLL_USB0	Power Supply for USB0's PLL	3.135	3.3	3.465	V
VCC33A_PLL_USB1	Power Supply for USB1's PLL	3.135	3.3	3.465	V
VCC33A_PLL_USB2	Power Supply for USB2's PLL	3.135	3.3	3.465	V
VCC33A_TDC	Power Supply for TDC	3.135	3.3	3.465	V
VCC33A_ADC	Power Supply for ADC	3.135	3.3	3.465	V
VCC33D_ADC	Power Supply for ADC	3.135	3.3	3.465	V
VCC33IO_ADC	Power Supply for ADC	3.135	3.3	3.465	V
Tj	Junction Temperature Range	-40	-	125	°C

9.3. DC Electrical Characteristics

Table 9-3 summarizes the DC electrical characteristics of V8133L.

Table 9-3. DC Electrical Characteristics

Parameter		Symbol	Condition	Min	Typ	Max	Unit
Digital GPIO	High-Level Input Voltage	V_{IH}	LVTTL	2.0	-	-	V
	Low-Level Input Voltage	V_{IL}	LVTTL	-	-	0.8	V
	Schmitt-trigger negative-to-threshold voltage	V_{T-}	LVTTL	0.8	1.1		V
	Schmitt-trigger positive-to-threshold voltage	V_{T+}	LVTTL		1.6	2.0	V
	Input Pull-up Resistance	R_{PU}	V_{in}=0V	40	75	190	kΩ
	Input Pull-down Resistance	R_{PD}	V_{in}=VCC3IO	30	75	190	kΩ
	High-Level Input Current	I_{IH}		-	-		uA
	Low-Level Input Current	I_{IL}		-	-		uA
	High-Level Output Voltage	V_{OH}	I_{oh}=4.0mA~16mA	2.4	-	-	V
	Low-Level Output Voltage	V_{OL}	I_{ol}=4.0mA~16mA	-	-	0.4	V
	Tri-State Output Leakage Current	I_{OZ}		-	1.0	10	uA
	Input Capacitance	C_{IN}		-	2.3	-	pF

	Output Capacitance	C_{OUT}		-	-		pF

9.4. SDRAM I/O DC Electrical Characteristics

The SDRAM I/O pads support DDR3,DDR3L,LPDDR2,and DDR2 operational modes. The SDRAM Controller(DRAMC) is designed to be compatible with JEDEC-compliant SDRAMs. The DRAMC supports the following memory types:

- DDR3 SDRAM compliant to JESD79-3E DDR3 JEDEC standard release July, 2010
- LPDDR2 SDRAM compliant to JESD209-2B LPDDR2 JEDEC standard release June, 2009
- DDR3L SDRAM compliant to JESD79-3-1A.01 DDR3L JEDEC standard release May, 2013

Table 9-4. DC Input Logic Level

Characteristics	Symbol	Min	Typ	Max	Unit
DC input logic high	$V_{IH(DC)}$	VREF + 100	-	-	mV
DC input logic low	$V_{IL(DC)}$	-	-	VREF – 100	mV
Input reference voltage	Vref	0.49 * VDDQ	-	0.51 * VDDQ	V
Input termination resistance(ODT) to $V_{DDQ}/2$	R_{TT}	60	120	Open	Ω

Table 9-5. Output DC Current Drive

Characteristics	Symbol	Min	Max	Unit
DC output high voltage	V_{OH}	0.9 * VDDQ	-	V
DC output low voltage	V_{OL}	-	0.1 * VDDQ	V

9.5. Oscillator Electrical Characteristics

V8133L contains two external input clocks: X25MIN and X32KIN, two output clocks: X25MOUT and X32KOUT. The 25 MHz frequency is used to generate the main source clock for PLL and the main digital blocks, the clock is provided through X25MIN. **Table 9-6** lists the 25 MHz crystal specifications.

Table 9-6. 25 MHz Crystal Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
$1/(t_{CPMAIN})$	Crystal Oscillator Frequency Range	–	25.000	–	MHz
	Frequency Tolerance at 25 °C	-20	–	+20	ppm
	Oscillation Mode	Fundamental			–

	Maximum Change Over Temperature Range	-20	–	+20	ppm
C_L	Equivalent Load Capacitance	12	18	22	pF
C_O	Shunt Capacitance	–	3	–	pF

The 32.768kHz frequency is used for low frequency operation. It supplies the wake-up domain for operation in lowest power mode. The clock is provided through X32KIN. **Table 9-7** lists the 32.768kHz crystal specifications.

Table 9-7. 32.768kHz Crystal Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
$1/(t_{CPMAIN})$	Crystal Oscillator Frequency Range	–	32.768	–	kHz
	Frequency Tolerance at 25 °C	-20	–	+20	ppm
	Oscillation Mode	Fundamental			–
	Maximum Change Over Temperature Range	-20	–	+20	ppm
C_L	Equivalent Load Capacitance	–	12.5	–	pF
C_O	Shunt Capacitance	–	1.1	–	pF

9.6. External Peripherals Electrical Characteristics

9.6.1. LCD AC Electrical Characteristics

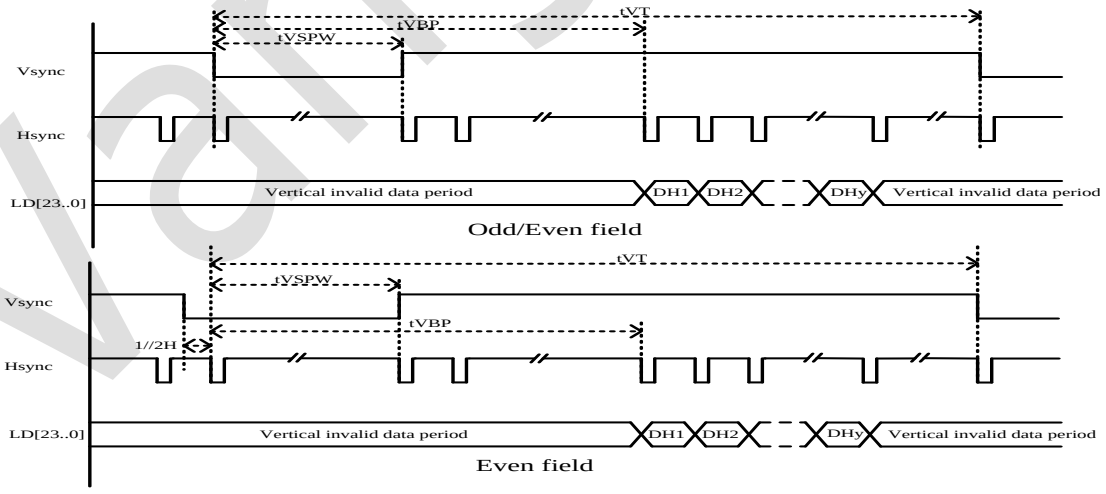


Figure 9-1. HV_IF Interface Vertical Timing

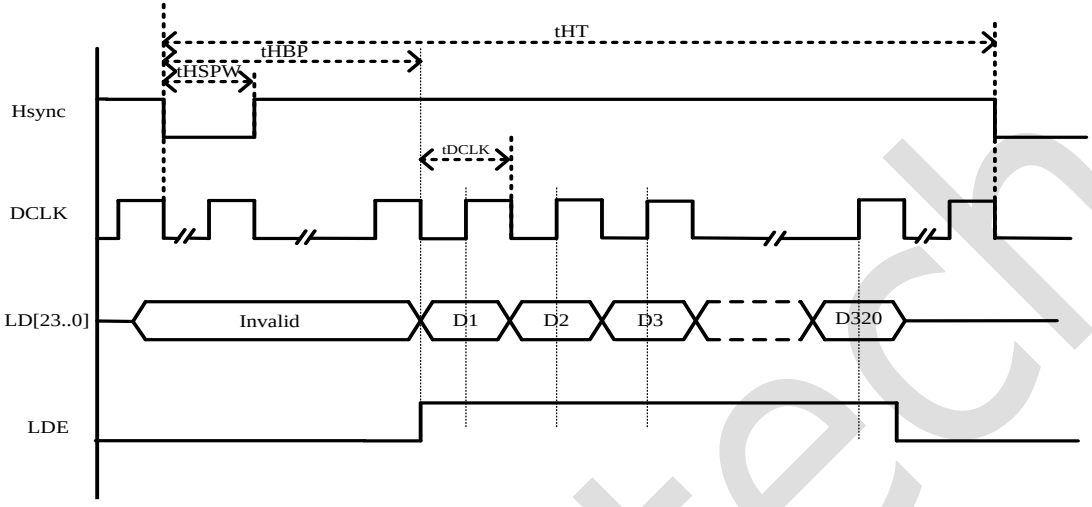


Figure 9-2. HV_IF Interface Parallel Mode Horizontal Timing

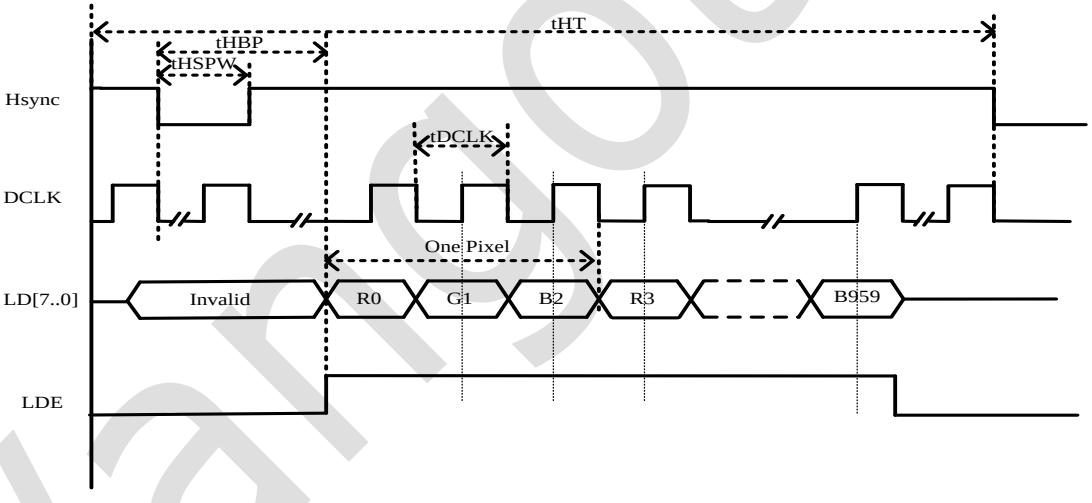


Figure 9-3. HV_IF Interface Serial Mode Horizontal Timing

Table 9-8. LCD HV_IF Interface Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
DCLK cycle time	tDCLK	5	-	-	ns
HSYNC period time	tHT	-	HT+1	-	tDCLK
HSYNC width	tHSPW	-	HSPW+1	-	tDCLK
HSYNC back porch	tHBP	-	HBP+1	-	tDCLK

VSYNC period time	tVT	-	VT/2	-	tHT
VSYNC width	tVSPW	-	VSPW+1	-	tHT
VSYNC back porch	tVBP	-	VBP+1	-	tHT

(1). Vsync: Vertical sync, indicates one new frame.

(2). Hsync: Horizontal sync, indicate one new scan line.

(3). DCLK: Dot clock, pixel data are sync by this clock.

(4). LDE: LCD data enable.

(5). LD[23..0]: 24Bit RGB/YUV output from input FIFO for panel.

9.6.2. SPI AC Electrical Characteristics

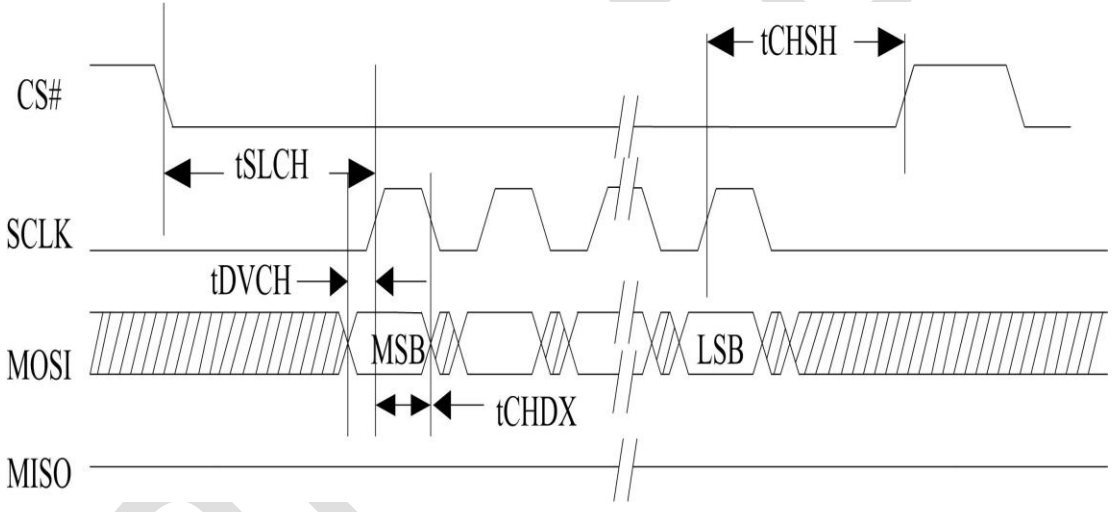


Figure 9-4. SPI MOSI Timing

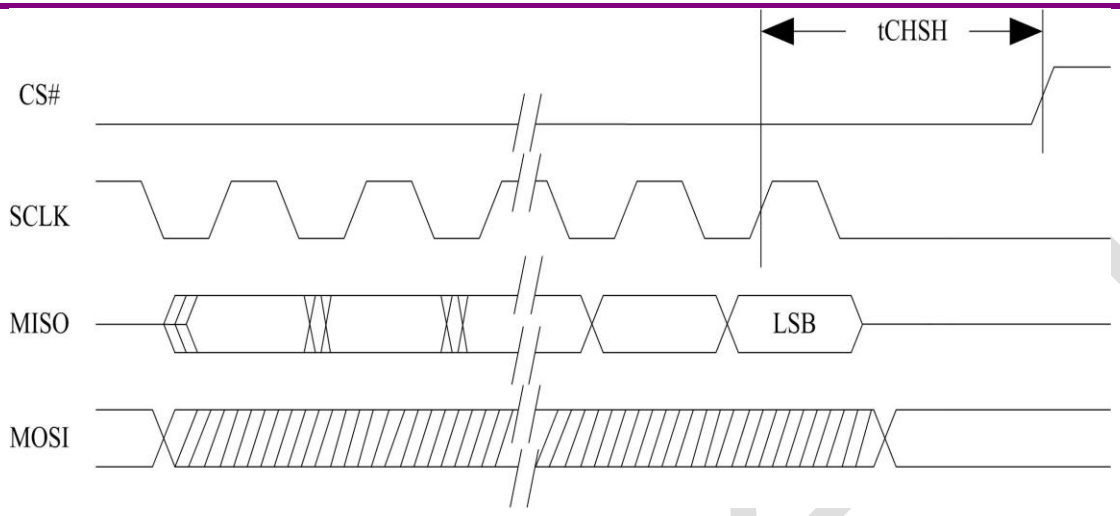


Figure 9-5. SPI MISO Timing

Table 9-9. SPI Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
CS# Active Setup Time	tSLCH	-	2T	-	ns
CS# Active Hold Time	tCHSH	-	2T(1)	-	ns
Data In Setup Time	tDVCH	-	T/2-3	-	ns
Data In Hold Time	tCHDX	-	T/2-3	-	ns

NOTE

(1):T is the cycle of clock.

9.6.3. UART AC Electrical Characteristics

Register Setting:

Data length(DLS in LCR[1:0]) = 3 (8bit)

Stop bit length(STOP in LCR[2]) = 1 (2bit)

Parity enable(PEN in LCR[3]) = 1

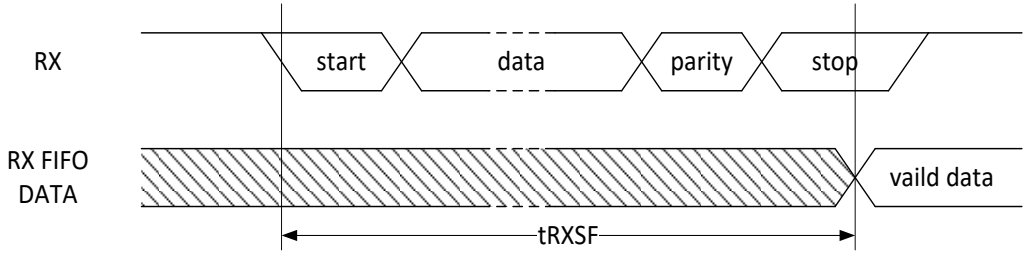


Figure 9-6. UART RX Timing

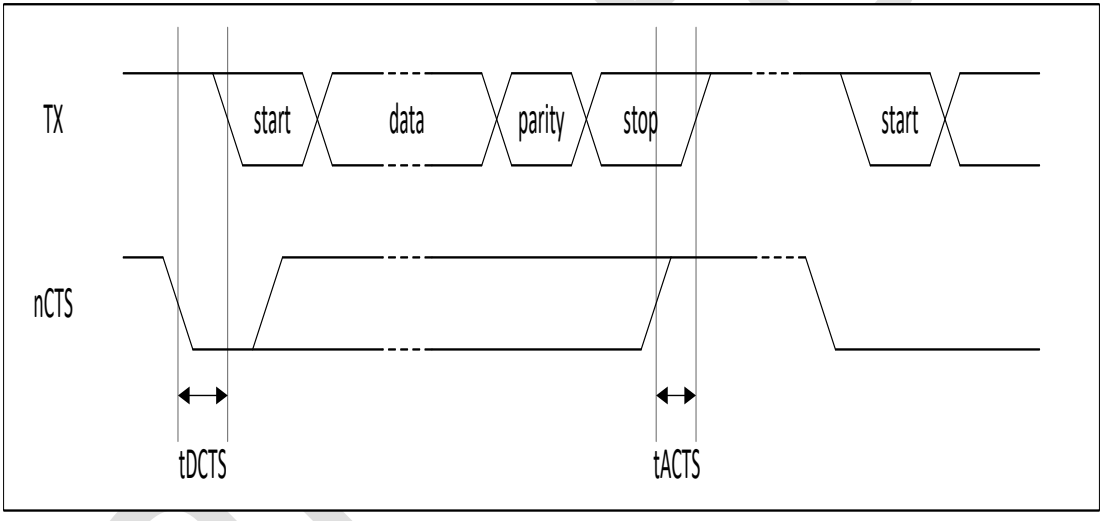
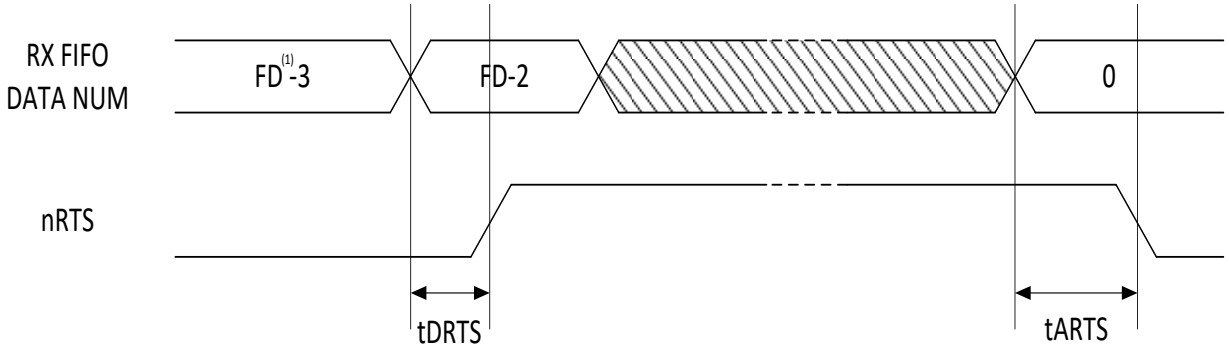


Figure 9-7. UART nCTS Timing

Register Setting:

RTS Trigger level(RT in FCR[7:6]) = 3 (De-asserted nRTS when FIFO valid data number reach FIFO depth-2)



Note (1): FD: FIFO Depth

Figure 9-8. UART nRTS Timing

Table 9-10. UART Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
RX start to RX FIFO	tRXSF	10.5× BRP(1)	-	11× BRP(1)	ns
Delay time of de-asserted nCTS to TX start	tDCTS	-	-	BRP(1)	ns
Step time of asserted nCTS to stop next transmission	tACTS	BRP(1)/4	-	-	ns
Delay time of de-asserted nRTS	tDRTS	-	-	BRP(1)	ns
Delay time of asserted nRTS	tARTS	-	-	BRP(1)	ns

NOTE

(1): BRP(Baud-Rate Period).

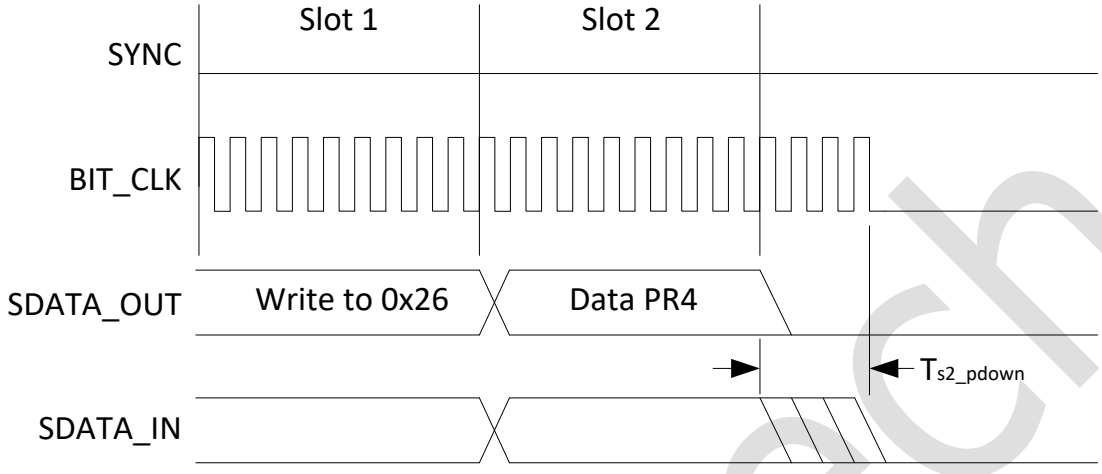


Figure 9-9. AC-link Low Power Mode Timing

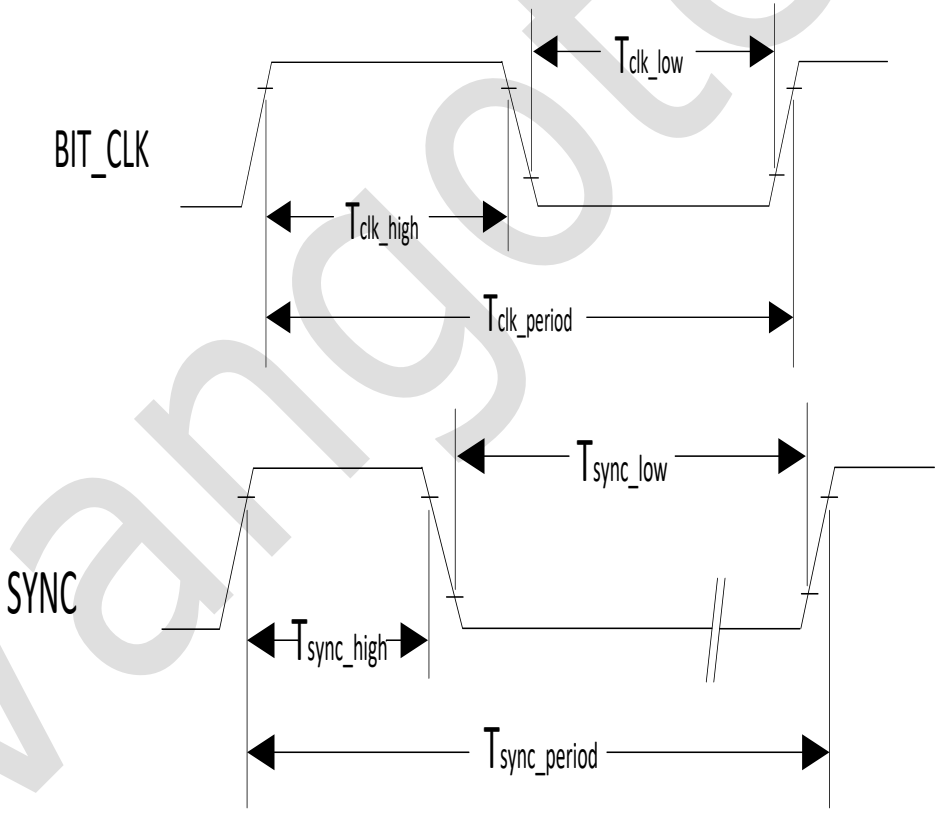


Figure 9-10. BIT_CLK and SYNC Timing

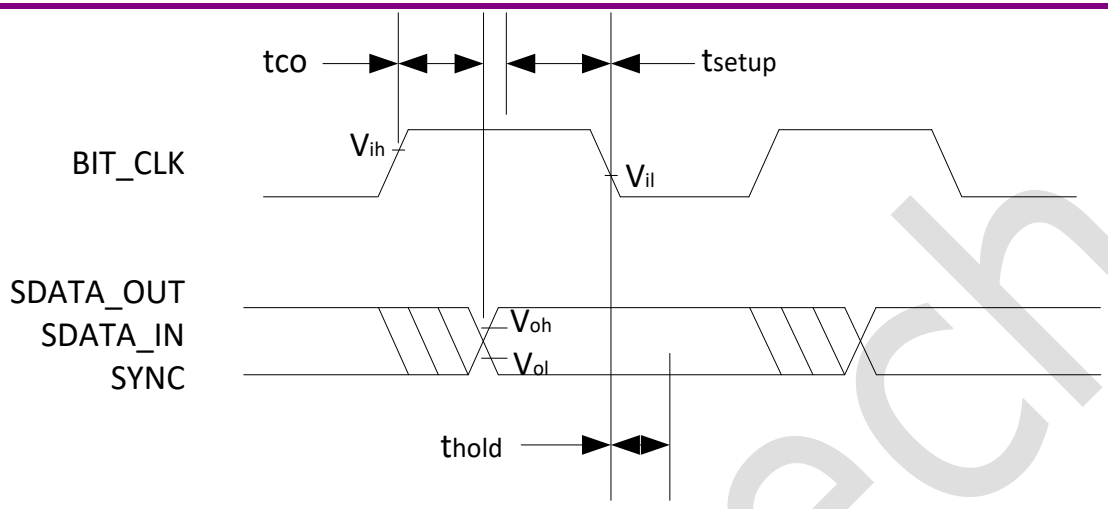


Figure 9-11. AC-link Data Transmission Output and Input Timing

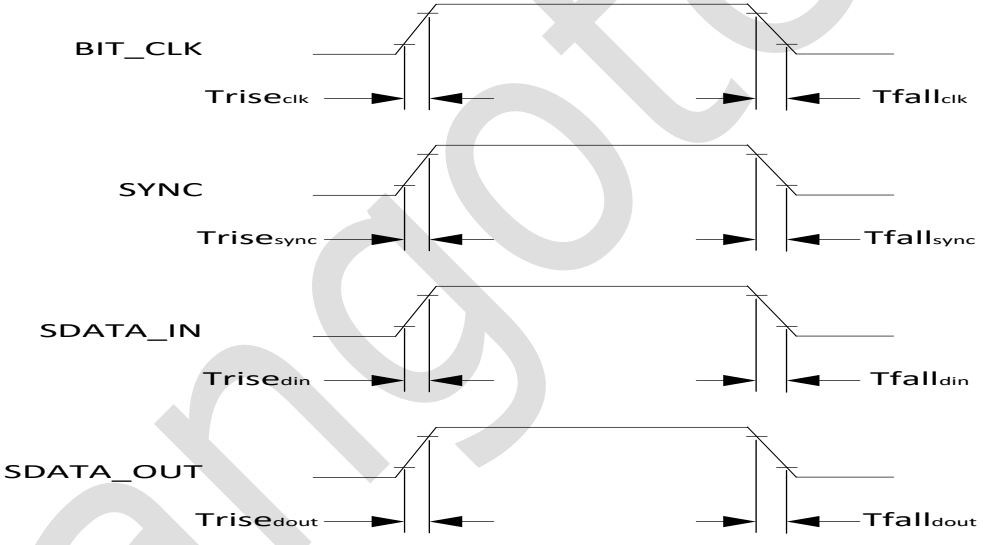


Figure 9-12. Signal Rise and Fall Timing

Table 9-11. AC97 Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
RESET# active low pulse width	T_{rst_low}	1.0	-	-	us
RESET# inactive to SDATA_IN Or BIT_CLK active delay	$T_{tri2actv}$	-	-	25	ns
RESET# inactive to BIT_CLK Startup delay	$T_{rst2clk}$	162.8	-	-	ns

SYNC active high pulse width	T_{sync_high}	1.0	-	-	us
SYNC inactive to BIT_CLK startup delay	$T_{sync2clk}$	162.8	-	-	ns
End of Slot 2 to BIT_CLK, SDATA_IN low	T_{s2_pdown}	-	-	1.0	us
BIT_CLK frequency		-	12.288	-	MHz
BIT_CLK period	Tclk_period	-	81.4	-	ns
BIT_CLK output jitter		-	-	750	ps
BIT_CLK high pulse width	Tclk_high	36	40.7	45	ns
BIT_CLK low pulse width	Tclk_low	36	40.7	45	ns
SYNC frequency		-	48.0	-	kHz
SYNC period	Tsync_period	-	20.8	-	us
SYNC high pulse width	Tsync_high	-	1.3	-	us
SYNC low pulse width	Tsync_low	-	19.5	-	us
Output Valid Delay from rising edge of BIT_CLK	tco	-	-	15	ns
Input Setup to falling edge of BIT_CLK	tsetup	10	-	-	ns
Input Hold from falling edge of BIT_CLK	thold	10	-	-	ns
BIT_CLK combined rise or fall plus flight time (Primary Codec to Controller or Secondary)		-	-	7	ns
SDATA combined rise or fall plus flight time (Output to Input)		-	-	7	ns
BIT_CLK rise time	Triseclk	-	-	6	ns
BIT_CLK fall time	Tfallclk	-	-	6	ns
SYNC rise time	Trisesync	-	-	6	ns
SYNC fall time	Tfallsync	-	-	6	ns

SDATA_IN rise time	Trisedin	-	-	6	ns
SDATA_IN fall time	Tfalldin	-	-	6	ns
SDATA_OUT rise time	Trisedout	-	-	6	ns
SDATA_OUT fall time	Tfalldout	-	-	6	ns

(1). Worst case duty cycle restricted to 45/55.

(2). Combined rise or fall plus flight times are provided for worst case scenario modeling purpose.

(3). BIT_CLK rise/fall times with an external load of 75 pF.

(4). SYNC and SDATA_OUT rise/fall times with a external load of 75 pF.

(5). SDATA_IN rise/fall times with an external load of 60 pF.

(6). Rise is from 10% to 90% of Vdd (Vol to Voh).

(7). Fall is from 90% to 10% of Vdd (Voh to Vol).

9.6.4. SCR AC Electrical Characteristics

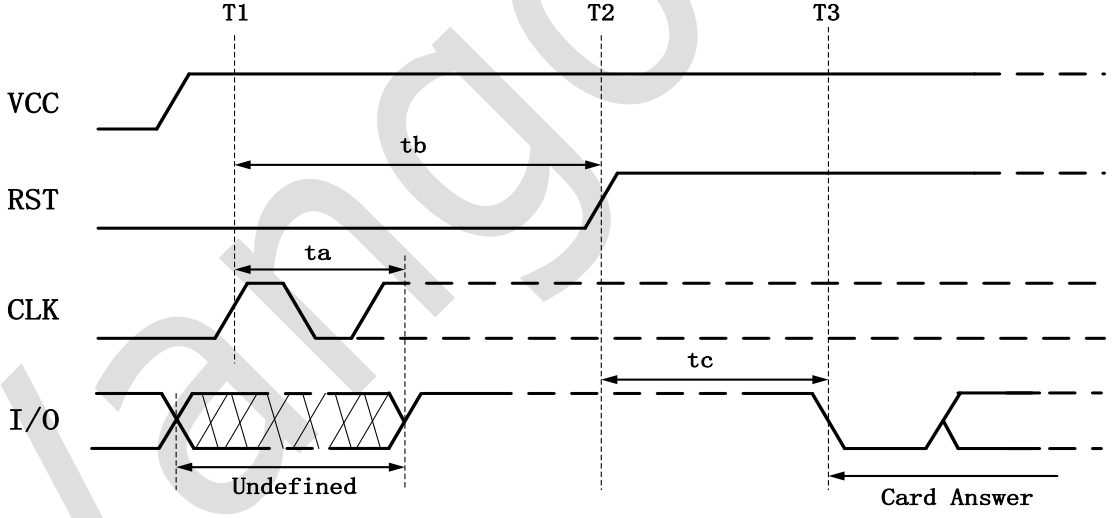


Figure 9-13. SCR Activation and Cold Reset Timing

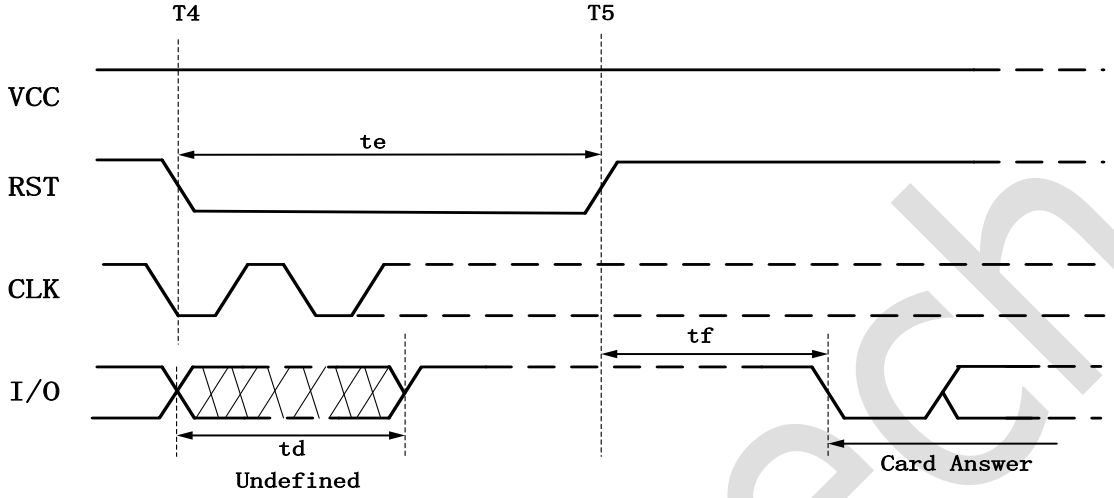


Figure 9-14. SCR Warm Reset Timing

Table 9-12. SCR Timing Constants

Symbol	Min	Typ	Max	Unit
ta	-	-	200/f	us
tb	400/f	-	-	us
tc	400/f	-	40000/f	us
td	-	-	200/f	us
te	400/f	-	-	us
tf	400/f	-	40000/f	us

(1). Activation: Before time T1

(2). Cold Reset: After time T1

(3). T1: The clock signal is applied to CLK at time T1.

(4). T2: The RST is put to state H.

(5). T3: The card begin answer at time T3

(6). ta: The card shall set I/O to state H within 200 clock cycles (delay ta) after the clock signal is applied to CLK (at time T1+ta).

(7). tb: The cold reset results from maintaining RST at state L for at least 400 clock cycles (delay tb) after the clock signal is applied to CLK (at time T1+tb).

(8). tc: The answer on I/O shall begin between 400 and 40000 clock cycles (delay tc) after the rising edge of the signal on RST (at time T2+tc).

(9). td: The card shall set I/O to state H within 200 clock cycles (delay td) after state L is applied to RST (at time T4+td).
(10). te: The controller initiates a warm reset (at time T4) by putting RST to state L for at least 400 clock cycles (delay te) while VCC remains powered and CLK provided with a suitable and stabled clock signal.
(11). tf: The card answer on I/O shall begin between 400 and 40000 clock cycles (delay tf) after the rising edge of the signal on RST (at time T5+tf).
(12). f is the frequency of clock.

9.7. Power-up and Power-down Sequence

Figure 9-15 shows the power-up sequence for V8133L. It's recommended for 1.1V core power(VCCK) to be stable before 3.3V PAD power (VCC3IO) is. After 3.3V is stable, X_RESET_N should be low level for at least 1ms. 1.8V/3.3V power for eMMC IO, VCC3IO_EMMC0 and VCC3IO_EMMC1, needs to be stable within 6.76ms after X_RESET de-asserted. 1.5V power for DDR IO, VCC15O_DDR and VCC15O_DDRCK, needs to be stable within 10.16ms after X_RESET_N de-asserted.

All power supplies can ramp down except VCC_RTC. The ramping down rate is determined by the load on the power source.

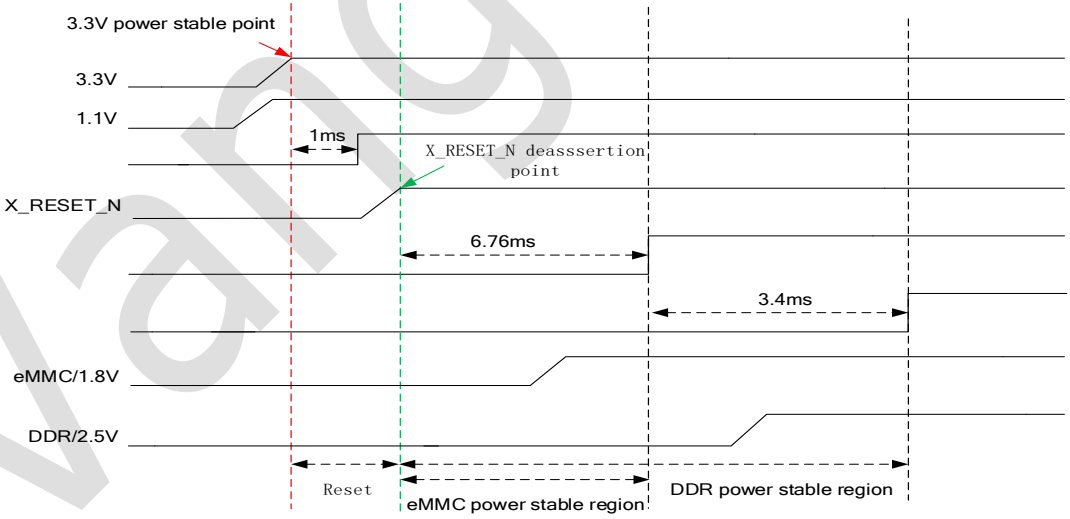


Figure 9-15. V8133L Power Up Sequence

10. Package Thermal Characteristics

The testing PCB is based on 4 layers. The following thermal resistance characteristics in Table 10-1 is based on JEDEC JESD51 standard, because the system design and temperature could be different with JEDEC JESD51, the simulating resulting data is a reference only, please prevail in the actual application condition test.

Table 10-1. V8133L Thermal Resistance Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
θ_{JA}	Junction-to-Ambient Thermal Resistance	-	17	-	°C/W
θ_{JB}（TBD）	Junction-to-Board Thermal Resistance	-	5.648	-	°C/W
θ_{JC}	Junction-to-Case Thermal Resistance	-	4.98	-	°C/W

(1). These values are based on a JEDEC-defined 2S2P system and will change based on environment as well as application.

(2). °C/W：degrees Celsius per watt.

11. Pin Assignment

11.1. Pin Map

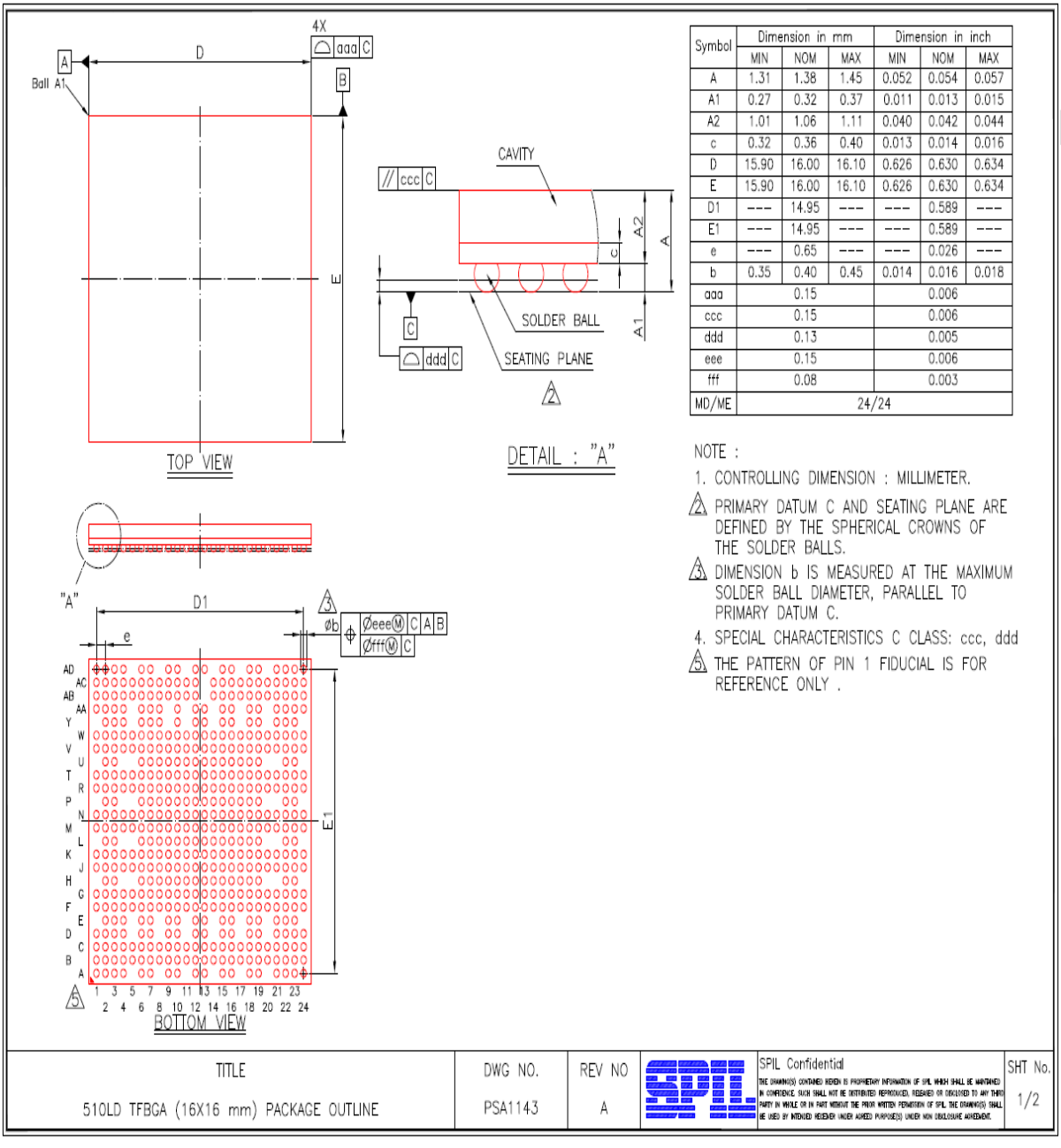
For V8133L, TFBGA 510 balls, 16 mm x 16 mm, 0.65 mm pitch package is offered. The pin maps are illustrated in Figure 11-1 for this package.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
A	GND	X_DDR_RDRVUP	X_DDR_DQ_1[6]	X_DDR_DQ_1[4]		X_DDR_DM_1	X_DDR_DQ_1[7]		X_DDR_DQ_3[4]	X_DDR_DQS_3		X_DDR_DQ_3[1]	X_DDR_DQ_3[5]		X_DDR_DM_4	X_DDR_DQ_4[4]		X_MII_COL	X_MII_MDIO		X_MII_RXD[0]	X_MII_RXD[1]	X_RMII_TXD[1]	GND
B	X_DDR_RASN	X_DDR_RDRVDN	X_DDR_DQ_1[2]	X_DDR_DQ_1[0]	X_DDR_DQS_1	X_DDR_DQ_1[1]	X_DDR_DQ_1[5]	X_DDR_DQ_3[2]	X_DDR_DQ_3[6]	X_DDR_DQSB_3	X_DDR_DQ_3[0]	X_DDR_DM_3	X_DDR_DQ_3[3]	X_DDR_DQ_4[5]	X_DDR_DQ_4[1]	X_DDR_DQ_4[7]	X_DDR_DQ_4[6]	GND	X_MII_MDC	X_MII_RX_DV	X_MII_RX_CK	X_MII_RXD[2]	X_RMII_RXD[1]	X_RMII_TXD[0]
C	X_DDR_CKE[0]	X_DDR_CASN	X_DDR_VREF_D0	X_DDR_VREF_D1	X_DDR_DQSB_1	X_DDR_DQSB_0	X_DDR_DQ_1[3]	GND	X_DDR_VREF_D2	X_DDR_VREF_D3	GND	X_DDR_DQSB_2	X_DDR_DQ_3[7]	X_DDR_DQ_4[3]	GND	X_DDR_DQ_4[0]	X_DDR_DQ_4[2]	GND	X_MII_TXD[0]	X_MII_RX_ER	X_MII_TXD[3]	X_RMII_RX_ER	X_RMII_RXD[0]	X_RMII_TX_EN
D	X_DDR_WEN	X_DDR_ADDR[10]	GND	X_DDR_DQ_0[7]		GND	X_DDR_DQS_0		GND	X_DDR_DQ_2[7]		GND	X_DDR_DQS_2		X_DDR_DQS_4	X_DDR_VREF_D4		X_MII_CRS	X_MII_TX_EN		X_UART0_RX	X_RMII_REF_CLK	X_RMII_MDIO	X_RMII_RX_CRS_DV
E		X_DDR_CSN[0]	X_DDR_DQ_0[5]	X_DDR_DQ_0[0]		X_DDR_DQ_0[4]	X_DDR_DQ_0[6]		X_DDR_DQ_2[5]	X_DDR_DQ_2[0]		X_DDR_DQ_2[4]	X_DDR_DQ_2[6]		X_DDR_DQSB_4	GND		X_MII_TX_ER	X_MII_TXD[1]		X_I2C2_CLK	X_UART0_TX	X_RMII_MDC	
F	X_DDR_CKB	X_DDR_CK	X_DDR_DM_0	X_DDR_DQ_0[3]	GND	X_DDR_DQ_0[1]	X_DDR_DQ_0[2]	GND	X_DDR_DM_2	X_DDR_DQ_2[3]	GND	X_DDR_DQ_2[1]	X_DDR_DQ_2[2]	GND	GND	X_MII_RXD[3]	GND	X_MII_TX_CK	X_MII_TXD[2]	GND	X_I2C2_DATA	X_RGMII_RXCTL	X_RGMII_GTX_CK	X_RGMII_MDIO
G	X_DDR_ADDR[15]	X_DDR_CSN[1]	X_DDR_ADDR[0]	X_DDR_ADDR[2]	X_DDR_CKE[1]	GND	VCC15O_DDR	VCC15O_DDR	VCC15O_DDR	VCC15O_DDR	VCC15O_DDR	VCC15O_DDR	VCC15O_DDR	VCC15O_DDR	VCC15O_DDR	VCC15O_DDR	VCC15O_DDR	VCC3IO	X_HSPI_DO	X_RGMII_RXD[0]	X_RGMII_RX_CK	X_RGMII_MDC	X_RGMII_RXD[2]	X_RGMII_RXD[1]
H		X_DDR_ADDR[3]	X_DDR_BA[1]			X_DDR_ODT[1]	VCC15O_DDR	VCC15O_DDR	VCC15O_DDR	GND	VCC15O_DDR	VCC15O_DDR	VCC15O_DDR	GND	VCC15O_DDR	VCC15O_DDR	VCC15O_DDR	VCC3IO	X_HSPI_CS			X_RGMII_TXD[0]	X_RGMII_TXD[1]	
J	X_DDR_ADDR[11]	X_DDR_ADDR[1]	X_DDR_ADDR[13]	GND	X_DDR_ADDR[9]	X_DDR_ODT[0]	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	VCCK	X_SPI1_DO	X_SPI1_CS	X_RGMII_RXD[3]	X_RGMII_TXCTL	X_RGMII_TXD[2]	X_RGMII_TXD[3]
K	X_DDR_ADDR[4]	X_DDR_ADDR[14]	X_DDR_BA[2]	X_DDR_ADDR[5]	X_DDR_RESETN	X_DDR_ADDR[7]	GND	VCCK	GND	VCCK	GND	VCCK	GND	VCCK	VCCK	GND	GND	VCCK	X_SPI6_DO	X_SPI6_CS	GND	X_SPI5_DO	X_HSPI_DI	X_HSPI_CLK
L		X_DDR_ADDR[6]	X_DDR_ADDR[8]			X_DDR_BA[0]	VCC15O_DDRCK	VCCK	GND	VCCK	GND	VCCK	GND	VCCK	GND	GND	GND	VCC3IO	X_SPI4_DO			X_SPI5_CS	X_SPI1_CLK	
M	X_RTC_XTAL_IN	GND	GND	VCC3IO_RTCOSC	GND	X_DDR_ADDR[12]	GND11A_PLL_DDR	VCC11A_PLL_DDR	GND	GND	GND	GND	GND	GND	GND	GND	GND	VCC3IO	X_JTAG_SWDITMS	X_SPI4_CS	X_I2S0_RXD	X_I2S_MCLK	X_SPI6_DI	X_SPI1_DI
N	X_RTC_XTAL_IO	X_RESET_N	X_OM	X_SPI_DCX1	VCC3IO_RTC	GND	VCC11A_PLL04	GND11A_PLL04	GND	GND	GND	GND	GND	GND	GND	GND	GND	VCCK	X_SPI3_DO	X_JTAG_TDO	GND	X_SPI0_CLK	X_SPI5_CLK	X_SPI6_CLK
P		X_SPI_DCX2	X_UART9_TX			VCC11K_RTC	GND33A_HSRT_USB2	GND33A_PLL_USB2	GND	GND	GND	GND	GND	GND	GND	GND	GND	VCCK	X_SPI3_CS			X_SPI0_DO	X_SPI4_CLK	
R	X_UART5_RX_H	X_UART6_TX	X_UART9_RX	X_PSW_DDRCK	X_UART6_RX	X_UART5_TX	VCC33A_HSRT_USB2	VCC33A_PLL_USB2	VCCK	GND	GND	GND	GND	GND	GND	GND	GND	VCC3IO	X_UART3_NRTS	X_I2C3_CLK	X_UART4_TX	X_SPI0_CS	X_SPI0_DI	X_SPI5_DI
T	X_UART7_TX	X_UART7_RX	X_UART5_RX	X_UART8_RX	X_UART8_RX_H	X_PSW_0	GND33A_HSRT_USB1	GND33A_PLL_USB1	VCCK	VCCK	VCCK	VCC3IO	VCC3IO	VCCK	VCCK	VCC3IO	VCC3IO	VCC3IO	X_SPI_HOLD_N	X_UART3_TX	X_I2C0_CLK	X_UART3_RX	X_JTAG_TDI	X_SPI4_DI
U		GND	X_UART8_TX			GND	VCC33A_HSRT_USB1	VCC33A_PLL_USB1	GND11A_PLL126	GND	GND11A_PLL35	GND33A_ADC	VCC33IO_ADC	GND33A_HSRT_USB0	VCC33A_PLL_USB0	GND	VCC11A_DLL_1	GND11A_DLL_1	X_SPI_CLK			X_JTAG_SWCLKTCK	X_SPI3_CLK	
V	X_USB2_DP	X_USB2_DM	GND	GND	X_I2C1_DATA	X_I2C1_CLK	VCC3IO_OSC	GND	VCC11A_PLL126	GND	VCC11A_PLL35	VCC33A_ADC	GND33IO_ADC	GND33A_PLL_USB0	VCC33A_HSRT_USB0	GND	VCC11A_DLL_0	GND11A_DLL_0	X_USB0_VBUS	X_UART2_NCTS	GND	X_UART2_NRTS	X_SPI3_DI	X_JTAG_TRST_N
W	X_USB1_DP	X_USB1_DM	GND	X_SPI2_CS	X_LC_DATA[18]	X_USB2_VBUS	X_USB1_VBUS	X_USB2_DRVBUS	GND	X_USB1_DRVBUS	GND	GND33D_ADC	VCC33A_TDC	GND	GND	X_EMMC1_D2	X_EMMC1_D0	X_EMMC1_CLK	GND	X_SPI_DI	X_UART1_RX	X_UART2_RX	X_UART3_NCTS	X_I2C0_DATA
Y		GND	X_SPI2_DO	X_LC_DATA[2]		X_LC_DATA[19]	X_LC_FCLK	X_LC_HS		GND		VCC33D_ADC	GND11A_TDC		GND	X_EMMC1_D4		X_EMMC1_D1	X_EMMC1_CMD		X_SPI7_DO	X_SPI_DO	X_SPI_WP_N	
AA	X_SPI2_CLK	X_SPI2_DI	X_LC_DATA[0]	X_LC_DATA[1]		X_LC_DATA[20]	X_LC_DATA[23]	X_LC_VS		GND33A_ADC		GND33A_ADC	VCC3IO_EFUSE		VCC3IO_EMMC1	X_EMMC1_D6		X_EMMC1_D5	X_EMMC1_D3		X_SPI7_CS	X_SPI_CS_N	X_I2S0_TXD	X_I2S0_FS
AB	X_LC_DATA[1]	X_LC_DATA[5]	X_LC_DATA[4]	X_LC_DATA[9]	X_LC_DATA[12]	X_LC_DATA[22]	X_LC_DATA[16]	X_LC_DE	GND33A_ADC	X_ADC_XAIN[2]	X_ADC_XVRT	X_ADC_XAIN[6]		X_USB0_DM	GND33A_HSRT_USB0	X_EMMC1_RSTN	X_EMMC0_D1	X_EMMC0_CLK	VCC3IO_EMMC0	X_EMMC0_RSTN	GND	X_USB0_DRVBUS	GND	X_I2S0_SCLK
AC	X_SYS_XTAL_IN	X_SYS_XTAL_IO	X_LC_DATA[7]	X_LC_DATA[11]	X_LC_DATA[13]	X_LC_DATA[14]	X_LC_DATA[21]	GND	GND33A_ADC	X_ADC_XAIN[1]	X_ADC_XAIN[3]	X_ADC_XAIN[4]		X_USB0_DP	GND33A_HSRT_USB0	X_EMMC1_D5	X_EMMC0_D7	X_EMMC1_D7	X_EMMC0_D6	X_EMMC0_D2	GND	X_UART1_TX	X_UART4_RX	X_I2C3_DATA
AD	GND	X_LC_DATA[6]	X_LC_DATA[8]	X_LC_DATA[10]		X_LC_DATA[15]	X_LC_DATA[17]		X_ADC_XAIN[0]	X_ADC_XVRB		X_ADC_XAIN[5]	X_ADC_XAIN[7]		X_EMMC0_CMD	X_EMMC1_D3		X_EMMC1_D4	X_EMMC0_D0		X_SPI7_DI	X_SPI7_CLK	X_UART2_TX	GND

Figure 11-1. V8133L Pin Map

11.2. Package Dimension

Figure 11-2 shows the top, bottom, and side views of V8133L package dimension.



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.31	1.38	1.45	0.052	0.054	0.057
A1	0.27	0.32	0.37	0.011	0.013	0.015
A2	1.01	1.06	1.11	0.040	0.042	0.044
c	0.32	0.36	0.40	0.013	0.014	0.016
D	15.90	16.00	16.10	0.626	0.630	0.634
E	15.90	16.00	16.10	0.626	0.630	0.634
D1	---	14.95	---	---	0.589	---
E1	---	14.95	---	---	0.589	---
e	---	0.65	---	---	0.026	---
b	0.35	0.40	0.45	0.014	0.016	0.018
aaa		0.15			0.006	
ccc		0.15			0.006	
ddd		0.13			0.005	
eee		0.15			0.006	
fff		0.08			0.003	
MD/ME		24/24				

NOTE :

1. CONTROLLING DIMENSION : MILLIMETER.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. SPECIAL CHARACTERISTICS C CLASS: ccc, ddd
5. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY .

TITLE	DWG NO.	REV NO		SHT No.
510LD TFBGA (16X16 mm) PACKAGE OUTLINE	PSA1143	A	SPIL Confidential	1/2

Figure 11-2. V8133L Package Dimension

12. Carrier, Storage and Baking Information

12.1. Carrier

12.1.1. Matrix Tray Information

Table 12-1 shows the V8133L matrix tray carrier information.

Table 12-1. Matrix Tray Carrier Information

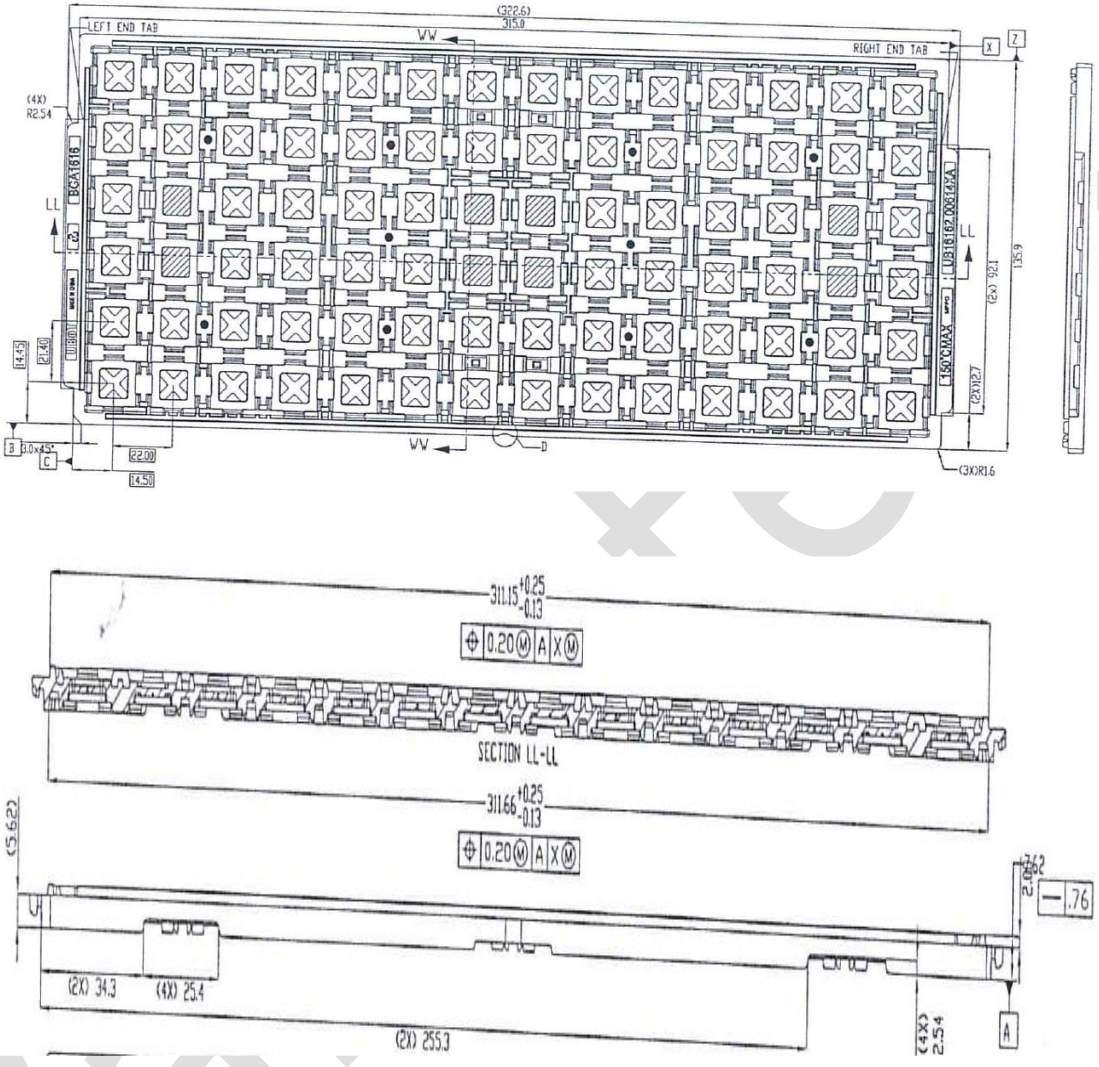
Item	Color	Size	Note
Tray	Black	315mm x 136mm x 7.62mm	84 Qty/Tray
Aluminum foil bags	Silvery white	540mm x 300mm x 0.14mm	Surface impedance:$10^9\Omega$ Vacuum packing Including HIC and desiccant Printing: RoHS symbol
Pearl cotton cushion(Vacuum bag)	White	12mm x 680mm x 185mm	
Pearl cotton cushion (The Gap between vacuum bag and inner box)	White	Left-Right:12mm x 180mm x 85mm Front-Back:12mm x 350mm x 70mm	
Inner Box	White	396mm x 196mm x 96mm	Printing: RoHS symbol 10 Tray/Inner box
Carton	White	420mm x 410mm x 320mm	6 Inner box/Carton

Table 12-2 shows the V8133L packing quantity.

Table 12-2. Packing Quantity Information

Sample	Size(mm)	Qty/Tray	Tray/Inner Box	Full Inner Box Qty	Inner Box/Carton	Full Carton Qty
V8133L	16 x 16	84	10	840	6	5040

Figure 12-1 shows tray dimension drawing of the V8133L.



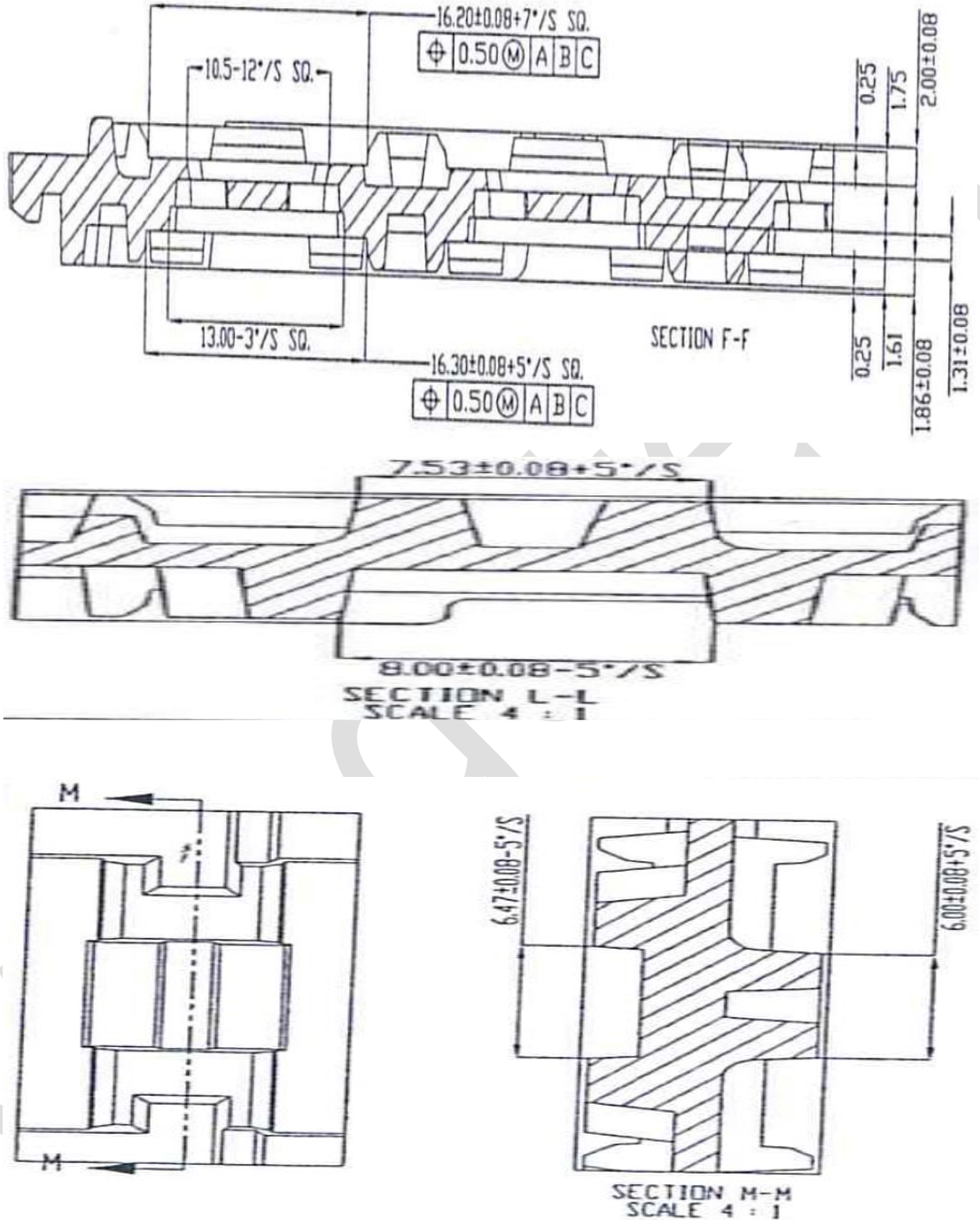


Figure 12-1. Tray Dimension Drawing

12.2. Storage

Reliability is affected if any condition specified in section 12.2.2 and section 12.2.3 has been exceeded.

12.2.1. Matrix Tray Information

A package's MSL indicates its ability to withstand exposure after it is removed from its shipment bag, a low MSL device sample can be exposed on the factory floor longer than a high MSL device sample. All MSL are defined in Table 12-3.

Table 12-3. MSL Summary

MSL	Out-of-bag floor life	Comments
1	Unlimited	≤30°C / 85%RH
2	1 year	≤30°C / 60%RH
2a	4 weeks	≤30°C / 60%RH
3	168 hours	≤30°C / 60%RH
4	72 hours	≤30°C / 60%RH
5	48 hours	≤30°C / 60%RH
5a	24 hours	≤30°C / 60%RH
6	Time on Label(TOL)	≤30°C / 60%RH

NOTE

The V8133L device samples are classified as MSL3.

12.2.2. Bagged Storage Conditions

The shelf life of the V8133L device samples is defined in Table 12-4.

Table 12-4. Bagged Storage Conditions

Packing mode	Vacuum packing
Storage temperature	20°C ~26°C
Storage humidity	40%~60%RH

Shelf life	12 months

12.2.3. Out-of-bag Duration

It is defined by the device MSL rating, the out-of-bag duration of the V8133L is as follows.

Table 12-5. Out-of-bag Duration

Storage temperature	20°C ~26°C
Storage humidity	40%~60%RH
Moisture sensitive level(MSL)	3
Floor life	168 hours

For no mention of storage rules in this document, please refer to the latest ***IPC/JEDEC J-STD-020C***.

12.3. Baking

It is not necessary to bake the V8133L if the conditions specified in section 12.2.2 and section 12.2.3 have not been exceeded. It is necessary to bake the V8133L if any condition specified in section 12.2.2 and section 12.2.3 has been exceeded.

It is necessary bake the V8133L if the storage humidity condition has been exceeded, we recommend that the device sample removed from its shipment bag more than 2 days shall be baked to guarantee production. Baking conditions: 125°C, 8 hours, nitrogen protection. Note that baking should not exceed 3 times.

13. Reflow Profile

All Vango chips provided for clients are lead-free RoHS-compliant products.

The reflow profile recommended in this document is a lead-free reflow profile that is suitable for pure lead-free technology of lead-free solder paste. If customers need to use lead solder paste, please contact with VANGO FAE.

The lead-free reflow profile conditions are given in Table 13-1. The table is for reference only.

Table 13-1. Lead-free Reflow Profile Conditions

	QTI typical SMT reflow profile conditions(for reference only)	
	Step	**Reflow condition**
Environment	N2 purge reflow usage (yes/no)	Yes, N2 purge used
	If yes, O2 ppm level	O2 < 1500 ppm
A	Preheat ramp up temperature range	25°C -> 150°C
B	Preheat ramp up rate	1.5~2.5 °C /sec
C	Soak temperature range	150°C -> 190°C
D	Soak time	80~110 sec
E	Liquidus temperature	217°C
F	Time above liquidus	60-90 sec
G	Peak temperature	240-250°C
H	Cool down temperature rate	≤4°C /sec

Figure 13-1 shows the typical lead-free reflow profile.

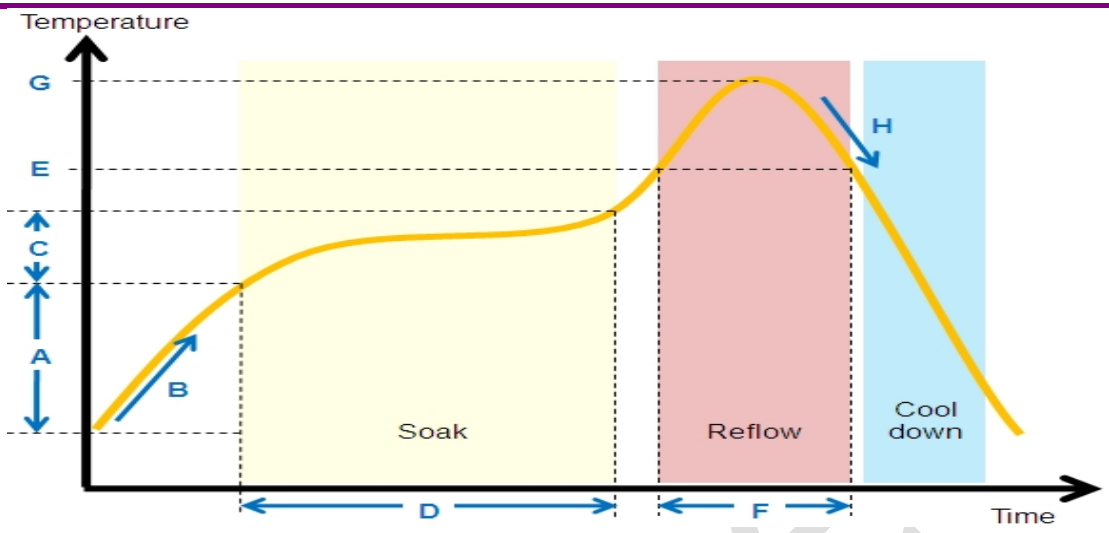


Figure 13-1. Typical Lead-free Reflow Profile

NOTE

The above reflow profile is solder joint testing result, it is for reference only, please adjust depending on actual production conditions.

The method of measuring the reflow soldering process is as follows.

Fix the thermocouple probe of the temperature measuring line at the connection point between the pin (solderable end) of the packaged device and the pad by using high-temperature solder wire or high-temperature tape, fix the packaged device at the pad by using high-temperature tape or other methods, and cover over the thermocouple probe. See Figure 13-2.

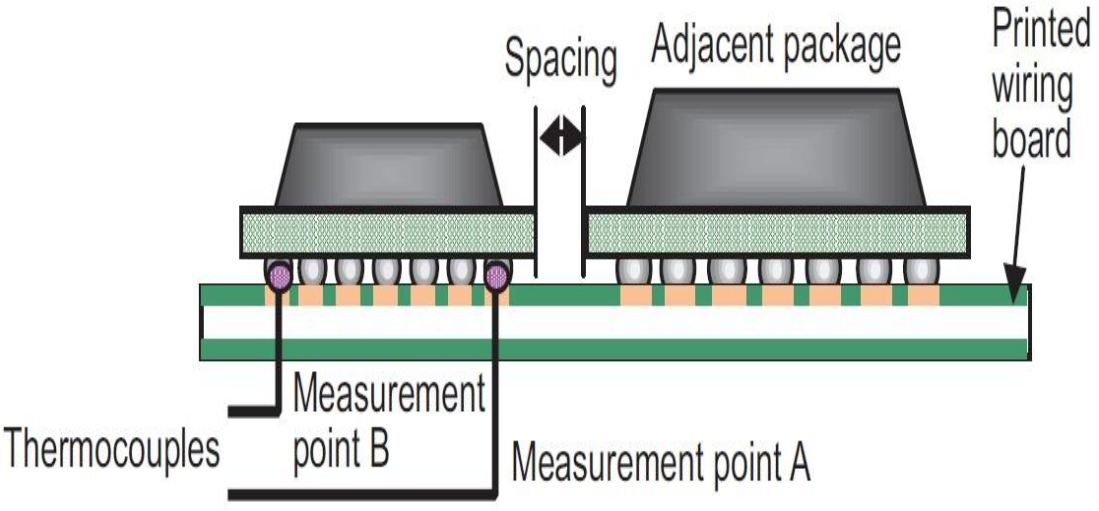


Figure 13-2. Measuring the Reflow Soldering Process

NOTE

To measure the temperature of QFP-packaged chip, place the temperature probe directly at the pin.

If possible, the more accurate measuring way is to drill the packaged device, or drill the PCB, and fix the thermocouple probe through the drilled hole at the pad.

14. Part Marking

Figure 14-1 shows the V8133L marking.

Figure 14-1. V8133L Marking

Table 14-1 describes the V8133L marking definitions.

Table 14-1. V8133L Marking Definitions

NO.	Marking	Description	Fixed/Dynamic
1	Vango	Logo	
2	V8130L	Part number	
3	XXXXX-XXX	Wafer lot ID	
4	H121YYWW	H121+Date code Date code : YYWW	